FUJITSU

NMOS 8&16-BIT I/O PROCESSOR

MBL 8089
MBL 8089-2

April 1985
Edition 3.0

NMOS 8 & 16-BIT I/O PROCESSOR

The Fujitsu MBL 8089 is a revolutionary concept in microprocessor input/output processing. Packaged in a 40-pin DIP package. MBL 8089 is a high performance processor implemented in N-channel, depletion load silicon gate technology (NMOS). The MBL 8089's instruction set and capabilities are optimized for high speed, flexible and efficient I/O handling. It allows easy interface of Fujitsu's 16-bit MBL 8086 and 8-bit MBL 8088 microprocessors with 8- and 16-bit peripherals. In the REMOTE configuration, MBL 8089 bus is user definable allowing it to be compatible with any 8/16-bit Fujitsu microprocessor, interfacing easily to the Fujitsu multiprocessor system bus standard MULTIBUS*.

The MBL 8089 performs the function of an intelligent DMA controller for the MBL 8086, 88 family and with its processing power, can remove I/O overhead from the MBL 8086 or MBL 8088. It may operate completely in parallel with a CPU, giving dramatically improved performance in I/O intensive applications. MBL 8089 provides two I/O channels, each supporting a transfer rate up to 1.25 Mbyte/sec (2.00 Mbyte/sec) at the standard clock frequency of 5 MHz (8 MHz). Memory based communication between the IOP and CPU enhances system flexibility and encourages software modularity, yielding more reliable, easier to develop systems.

- **High Speed DMA Capabilities Including I/O to Memory, Memory to I/O, Memory to Memory, and I/O to I/O**
- **MBL 8086, MBL 8088 Compatible: Removes I/O Overhead from CPU in iAPX 86/11 or 88/11 Configuration**
- **Allows Mixed Interface of 8- & 16-Bit Peripherals, to 8- & 16-Bit Processor Busses**
- **1 Mbyte Addressability**
- **Memory Based Communication with CPU**
- **Supports LOCAL or REMOTE I/O Processing**
- **Flexible, Intelligent DMA Functions Including Translation, Search, Word Assembly/Disassembly**
- **MULTIBUS* Compatible System Interface**
- **Two Clock Rates:**
  5 MHz for MBL 8089
  8 MHz for MBL 8089-2
- **40-pin Ceramic DIP (Suffix -C)**

Fig. 1 – BLOCK DIAGRAM

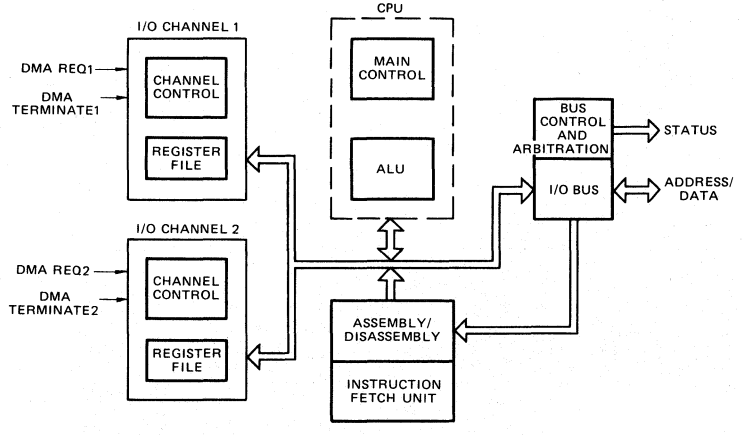
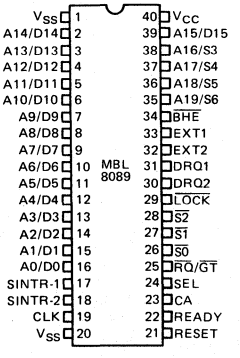


Fig. 2 – PIN CONFIGURATION



*Trade Mark of Intel Corporation, USA

Table 1 – PIN DESCRIPTION

Symbol	Type	Name and Function
A0–A15/ D0–D15	I/O	**Multiplexed Address and Data Bus:** The functions of these lines are defined by the state of $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ lines. The pins are floated after reset and when the bus is not acquired. A8–A15 are stable on transfers to a physical 8-bit data bus (same bus as MBL 8088), and are multiplexed with data on transfers to a 16-bit physical bus.
A16–A19/ S3–S6	O	**Address and Status:** Multiplexed most significant address lines and status information. The address lines are active only when addressing memory. Otherwise, the status lines are active and are encoded as shown below. The pins are floated after reset and when the bus is not acquired. S6 S5 S4 S3 1 1 0 0 DMA cycle on CH1 1 1 0 1 DMA cycle on CH2 1 1 1 0 Non-DMA cycle on CH1 1 1 1 1 Non-DMA cycle on CH2
$\overline{BHE}$	O	**Bus High Enable:** The Bus High Enable is used to enable data operations on the most significant half of the data bus (D8–D15). The signal is active low when a byte is to be transferred on the upper half of the data bus. The pin is floated after reset and when the bus is not acquired. $\overline{BHE}$ does not have to be latched.
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	O	**Status:** These are the status pins that define the IOP activity during any given cycle. They are encoded as shown below: $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ 0 0 0 Instruction fetch; I/O space 0 0 1 Data fetch; I/O space 0 1 0 Data store; I/O space 0 1 1 Not used 1 0 0 Instruction fetch; System Memory 1 0 1 Data fetch; System Memory 1 1 0 Data store; System Memory 1 1 1 Passive The status lines are utilized by the bus controller and bus arbiter to generate all memory and I/O control signals. The signals change during T4 if a new cycle is to be entered while the return to passive state in T3 or T_W indicates the end of a cycle. The pins are floated after system reset and when the bus is not acquired.
READY	I	**Ready:** The ready signal received from the addressed device indicates that the device is ready for data transfer. The signal is active high and is synchronized by the MBL 8284A clock generator.

Symbol	Type	Name and Function
$\overline{LOCK}$	O	**Lock:** The lock output signal indicates to the bus arbiter that the bus is needed for more than one continuous cycle. It is set via the channel control register, and during the TSL instruction. The pin floats after reset and when the bus is not acquired. This output is active low.
RESET	I	**Reset:** The receipt of a reset signal causes the IOP to suspend all its activities and enter an idle state until a channel attention is received. The signal must be active for at least four clock cycles.
CLK	I	**Clock:** Clock provides all timing needed for internal IOP operation.
CA	I	**Channel Attention:** Gets the attention of the IOP. Upon the falling edge of this signal, the SEL input pin is examined to determine Master/Slave or CH1/CH2 information. This input is active high.
SEL	I	**Select:** The first CA received after system reset informs the IOP via the SEL line, whether it is a Master or Slave (0/1 for Master/Slave respectively) and starts the initialization sequence. During any other CA the SEL line signifies the selection of CH1/CH2. (0/1 respectively.)
DRQ1-2	I	**Data Request:** DMA request inputs which signal the IOP that a peripheral is ready to transfer/receive data using channels 1 or 2 respectively. The signals must be held active high until the appropriate fetch/stroke is initiated.
$\overline{RQ}/\overline{GT}$	I/O	**Request Grant:** Request Grant implements the communication dialogue required to arbitrate the use of the system bus (between IOP and CPU, LOCAL mode) or I/O bus when two IOPs share the same bus (REMOTE mode). The $\overline{RQ}/\overline{GT}$ signal is active low. An internal pull-up permits $\overline{RQ}/\overline{GT}$ to be left floating if not used.
SINTR1-2	O	**Signal Interrupt:** Signal interrupt outputs from channels 1 and 2 respectively. The interrupts may be sent directly to the CPU or through the MBL 8259A interrupt controller. They are used to indicate to the system the occurrence of user defined events.
EXT1-2	I	**External Terminate:** External terminate inputs for channels 1 and 2 respectively. The EXT signals will cause the termination of the current DMA transfer operation if the channel is so programmed by the channel control register. The signal must be held active high until termination is complete.
V_{CC}		**Voltage:** +5 volt power input.
V_{SS}		**Ground.**

FUNCTIONAL DESCRIPTION

The MBL 8089 IOP has been designed to remove I/O processing, control and high speed transfers from the central processing unit. Its major capabilities include that of initializing and maintaining peripheral components and supporting versatile DMA. This DMA function boasts flexible termination conditions (such as external terminate, mask compare, single transfer and byte count expired). The DMA function of the MBL 8089 IOP uses a two cycle approach where the information actually flows through the MBL 8089 IOP. This approach to DMA vastly simplifies the bus timings and enhances compatibility with memory and peripherals, in addition to allowing operations to be performed on the data as it is transferred. Operations can include such constructs as translate, where the MBL 8089 automatically vectors through a lookup table and mask compare, both on the "fly".

The MBL 8089 is functionally compatible with Fujitsu's MBL 8086, MBL 8088 family. It supports any combination of 8/16-bit busses. In the REMOTE mode it can be used to complement other Intel processor families. Hardware and communication architecture are designed to provide simple mechanisms for system upgrade.

The only direct communication between the IOP and CPU is handled by the Channel Attention and interrupt lines. Status information, parameters and task programs are passed via blocks of shared memory, simplifying hardware interface and encouraging structured programming.

The MBL 8089 can be used in applications such as file and buffer management in hard disk or floppy disk control. It can also provide for soft error recovery routines and scan control. CRT control, such as cursor control and auto scrolling, is simplified with the MBL 8089. Keyboard control, communication control and general I/O are just a few of the typical applications for the MBL 8089.

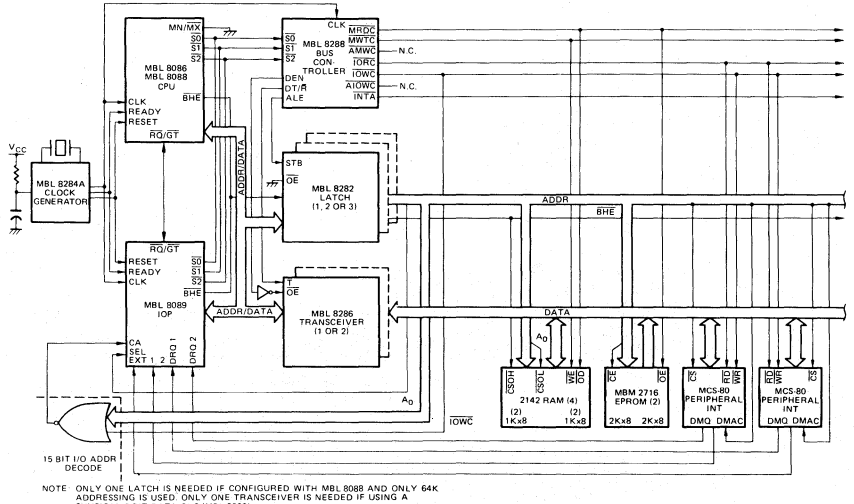
Remote and Local Modes

Shown in Figure 3 is the MBL 8089 in a LOCAL configuration. The MBL 8086 (or MBL 8088) is used in its maximum mode. The MBL 8089 and MBL 8086 reside on the same local bus, sharing the same set of system buffers. Peripheral located on the system bus can be addressed by either the MBL 8086 or the MBL 8089. The MBL 8089 requests the use of the LOCAL bus by means of the $\overline{RQ}/\overline{GT}$ line. This performs a similar function to that of HOLD and HLDA on the Intel 8085A, 8080A and MBL 8086 minimum mode but is implemented on one physical line. When the MBL 8086 relinquishes the system bus, the MBL 8089 used the same bus control, latches and transceiver components to generate the system address, control and data lines. This mode allows a more economical system configuration at the expense of reduced CPU thruput due to IOP bus utilization.

A typical REMOTE configuration is shown in Figure 4. In this mode, the IOP's bus is physically separated from the system bus by means of system buffers/latches. The IOP maintains its own local bus and can operate out of local or system memory. The system bus interface contains the following components:

- Up to three MBL 8282 buffer/latches to latch the address to the system bus.
- Up to two MBL 8286 devices bidirectionally buffer the system data bus.

Fig. 3 — TYPICAL iAPX 86/11, 88/11 CONFIGURATION WITH MBL 8089 IN LOCAL MODE, MBL 8088, MBL 8086 IN MAX MODE



NOTE ONLY ONE LATCH IS NEEDED IF CONFIGURED WITH MBL 8088 AND ONLY 64K ADDRESSING IS USED. ONLY ONE TRANSCEIVER IS NEEDED IF USING A PHYSICAL 8-BIT DATA BUS (MBL 8088).

- An MBL 8288 bus controller supplies the control signals necessary for buffer operation as well as $\overline{MRDC}$ (Memory Read) and $\overline{MWTC}$ (Memory Write) signals.
- An MBL 8289 bus arbiter performs all the functions necessary to arbitrate the use of the system bus. This is used in place of the $\overline{RQ}/\overline{GT}$ logic in the LOCAL mode. This arbiter decodes type of cycle information from the MBL 8089 status lines to determine if the IOP desires to perform a transfer over the "common" or system bus.

The peripheral device PER1 and PER2 are supported on their own data and address bus, the MBL8089 communicates with the peripherals without affecting system bus operation. Optional buffers may be used on the local bus when capacitive loading conditions so dictate. I/O programs and RAM buffers may also reside on the local bus to further reduce system bus utilization.

COMMUNICATION MECHANISM

Fundamentally, communication between the CPU and IOP is performed through messages prepared in shared memory. The CPU can cause the MBL 8089 to execute a program by placing it in the MBL 8089's memory space and/or directing the MBL 8089's attention to it by asserting a hardware Channel Attention (CA) signal to the IOP, activating the proper I/O channel. The SEL Pin indicates to the IOP which channel is being addressed. Communication from the IOP to the processor can be performed in a simillar manner via a system interrupt (SINTR-1,2), if the CPU has enabled interrupts for this purpose. Additionally, the MBL 8089 can store messages in memory regarding its status and the status of any peripherals. This communication mechanism is supported by a hierarchical data structure to provide a maximum amount of flexibility of memory use with the added capability of handling multiple IOP's.

Illustrated in Figure 5 is an overview of the communication data structure hierarchy that exists for the MBL 8089 I/O processor. Upon the first CA from RESET, if the IOP is initialized as the BUS MASTER, 5 bytes of information are read into the MBL 8089 starting at location FFFF6 (FFFF6, FFFF8-FFFFB) where the type of system bus (16-bit or 8-bit) and pointers to the system configuration block are obtained. This is the only fixed location the MBL 8089 accesses. The remaining addresses are obtained via the data structure hierarchy. The MBL 8089 determines addresses in the same manner as does the MBL 8086; i.e., a 16-bit relocation pointer is offset left 4 bits and added to the 16-bit address offset, obtaining a 20-bit address. Once these 20-bit addresses are formed, they are stored as such as all the MBL 8089 address registers are 20 bits long. After the system configuration pointer address is formed, the MBL 8089 IOP accesses the system configuration block.

Fig. 4 – TYPICAL REMOTE CONFIGURATION

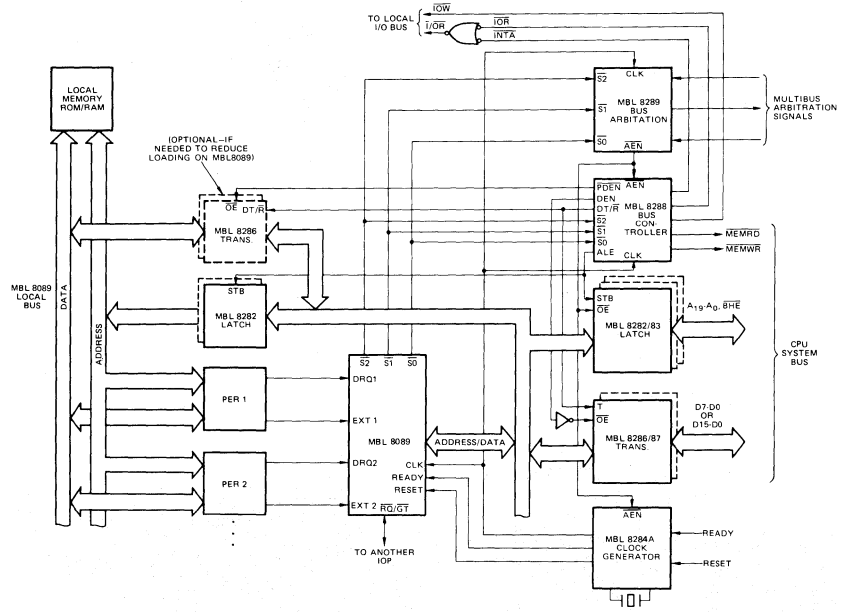
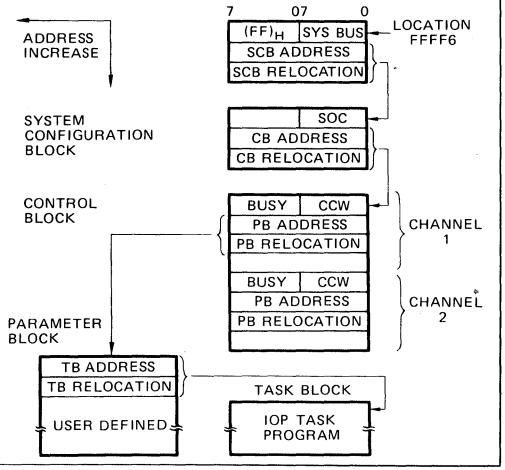


Fig. 5 – COMMUNICATION DATA STRUCTURE HIERARCHY



The System Configuration Block (SCB), used only during startup, points to the Control Block (CB) and provides IOP system configuration data via the SOC byte. The SOC byte initializes IOP I/O bus width to 8/16, and defines one of two IOP $\overline{RQ}/\overline{GT}$ operating modes. For $\overline{RQ}/\overline{GT}$ mode 0, the IOP is typically initialized as SLAVE and has its $\overline{RQ}/\overline{GT}$ line tied to a MASTER CPU (typical LOCAL configuration). In this mode, the CPU normally has control of the bus, grants control to the IOP as needed, and has the bus restored to it upon IOP task completion (IOP request–CPU grant–IOP done). For $\overline{RQ}/\overline{GT}$ mode 1, useful only in remote mode between two IOPs, MASTER/SLAVE designation is used only to initialize bus control: from then on, each IOP requests and grants as the bus is needed (IOP1 request–IOP2 grant–IOP2 request–IOP1 grant). Thus, each IOP retains bus control until the other requests it. The completion of initialization is signalled by the IOP clearing the BUSY flag in the CB. This type of startup allows the user to have the startup pointers in ROM with the SCB in RAM. Allowing the SCB to be in RAM gives the user the flexibility of being able to initialize multiple IOPs.

The Control Block furnishes bus control initialization for the IOP operation (CCW or Channel Control Word) and provides pointers to the Parameter Block or "data" memory for both channels 1 and 2. The CCW is retrieved and analyzed upon all CA's other than the first after a reset. The CCW byte is decoded to determine channel operation.

The Parameter Block contains the address of the Task Block and acts as a message center between the IOP and CPU. Parameters or variable information is passed from the CPU to its IOP in this block to customize the software interface to the peripheral device. It is also used for transferring data and status information between the IOP and CPU.

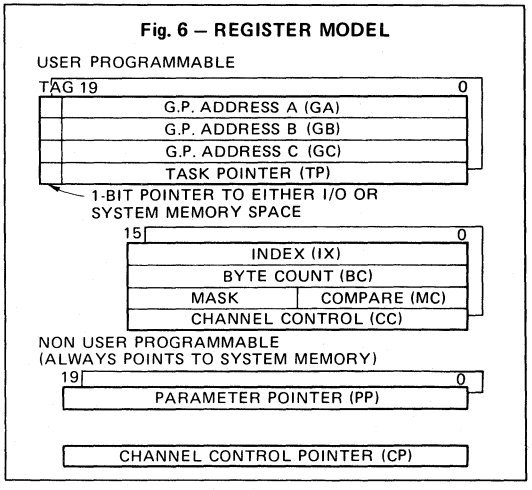
The Task Block contains the instructions for the respective channel. This block can reside on the local bus of the IOP, allowing the IOP to operate concurrently with the CPU, or reside in system memory.

The advantage of this type of communication between the processor, IOP and peripheral, is that it allows for a very clean method for the operating system to handle I/O routines. Canned programs or "Task Blocks" allow for execution of general purpose I/O routines with the status and peripheral command information being passed via the Parameter Block ("data" memory). Task Blocks (or "program" memory) can be terminated or restarted by the CPU, if need be. Clearly, the flexibility of this communication lends itself to modularity and applicability to a large number of peripheral devices and upward compatibility to future end user systems and microprocessor familes.

Register Set

The MBL 8089 maintains separate registers for its two I/O channels as well as some common registers (see Figure 6). There are sufficient registers for each channel to sustain its own DMA transfers, and process its own instruction stream. The basic DMA pointer registers (GA, GB – 20 bits each), can point either the system bus or local bus, DMA source or destination, and can be autoincremented. A third register set (GC) can be used to allow translation during the DMA process through a lookup table it points to. Additionally, registers are provided for a masked compare during the data transfer and can be set up to act as one of the termination conditions. Other registers are also provided. Many of these registers can be used as general purpose registers during program execution, when the IOP is not performing DMA cycles.

Fig. 6 – REGISTER MODEL



Bus Operation

The MBL 8089 utilizes the same bus structure as the MBL 8086, MBL 8088 in their maximum mode configurations (see Figure 7).The address is time multiplexed with the data on the first 16/8 lines. A16 through A19 are time multiplexed with four status lines S3-S6. For MBL 8089 cycles, S4 and S3 determined what type of cycle (DMA versus non-DMA) is being performed on channels 1 or 2. S5 and S6 are a unique code assigned to the MBL 8089 IOP, enabling the user to detect which processor is performing a bus cycle in a multiprocessing environment. The first three status lines, $\overline{S0}$-$\overline{S2}$, are used with an MBL 8288 bus controller to determine if an instruction fetch or data transfer is being performed in I/O or system memory space.

DMA transfers require at least two bus cycles with each bus cycle requiring a minimum of four clock cycles. Additional clock cycles are added if wait states are required. This two cycle approach simplifies considerably the bus timings in burst DMA. The MBL 8089 optimizes the transfer between two different bus widths by using three bus cycles versus four to transfer 1 word. More than one read (write) is performed when mapping an 8-bit bus onto a 16-bit bus (vice versa). For example, a data transfer from an 8-bit peripheral to a 16-bit physical location in memory is performed by first doing two reads, with word assembly within the IOP assembly register file and then one write.

As can be expected, the data bandwidth of the IOP is a function of the physical bus width of the system and I/O busses. Table 2 gives the bandwidth, latency and bus utilization of the MBL 8089. The system bus is assumed to be 16-bits wide with either an 8-bit peripheral (under byte column) or 16-bit peripheral (word column) being shown.

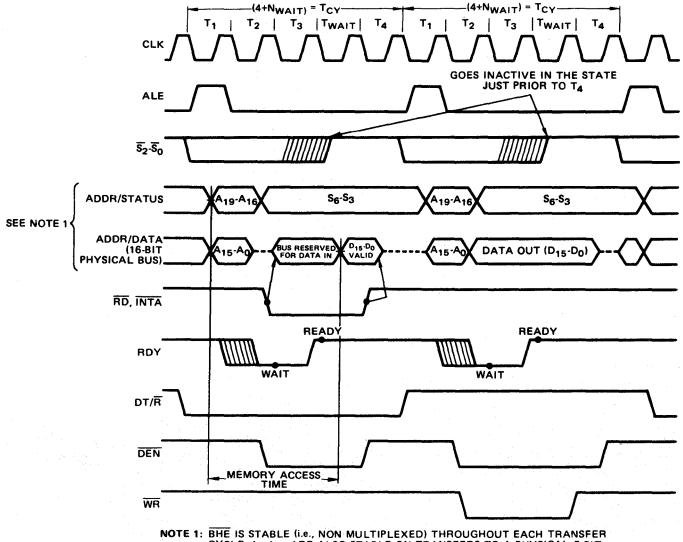
The latency refers to the worst case response time by the IOP to a DMA request, without the bus arbitration times. Notice that the word transfer allows 50% more bandwidth. This occurs since three bus cycles are required to map 8-bit data into a 16-bit location, versus two for a 16-bit to 16-bit transfer. Note that it is possible to fully saturate the system bus in the LOCAL mode whereas in the REMOTE mode this is reduced to a maximum of 50%.

Table 2 – ACHIEVABLE MBL 8089 OPERATIONS WITH 16-BIT SYSTEM BUS

	MBL 8089 (5MHz)				MBL 8089-2 (8MHz)			
	Local		Remote		Local		Remote	
	Byte	Word	Byte	Word	Byte	Word	Byte	Word
Bandwidth	830 KB/S	1250 KB/S	830 KB/S	1250 KB/S	1328 KB/S	2000 KB/S	1328 KB/S	2000 KB/S
Latency	1.0/2.4μsec*	1.0/2.4μsec*	1.0/2.4μsec*	1.0/2.4μsec*	0.625/1.5 μsec**	0.625/1.5μsec**	0.625/1.5μsec**	0.625/1.5μsec**
System Bus Utilization	2.4μsec/ Transfer	1.6μsec/ Transfer	0.8μsec/ Transfer	0.8μsec/ Transfer	1.5μsec/ Transfer	1.0μsec/ Transfer	0.5μsec/ Transfer	0.5μsec/ Transfer

* 2.4μsec if interleaving with other channel and no wait states. 1μse if channel is waiting for request.
** 1.5μsec if interleaving with other channel and no wait states. 0.625μsec if channel is waiting for request.

Fig. 7 – MBL 8089 BUS OPERATION



NOTE 1: $\overline{BHE}$ IS STABLE (i.e., NON MULTIPLEXED) THROUGHOUT EACH TRANSFER CYCLE. A_8-A_{15} ARE ALSO STABLE ON TRANSFERS TO A PHYSICAL 8-BIT BUS.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . . −0.5 to +7V
Power Dissipation . . . . . 2.5 Watt

*NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 1.0	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{CC}	Power Supply Current		350	mA	T_A = 25°C
I_{LI}	Input Leakage Current		±10	μA	$0V < V_{IN} < V_{CC}$
I_{LO}	Output Leakage Current		±10	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
V_{CL}	Clock Input Low Voltage	−0.5	+0.6	V	
V_{CH}	Clock Input High Voltage	3.9	V_{CC} + 1.0	V	
C_{IN}	Capacitance of Input Buffer (All Input except AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)		15	pF	fc = 1 MHz
C_{IO}	Capacitance of I/O Buffer (AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)		15	pF	fc = 1 MHz

A.C. CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0°C to 70°C)

MBL 8089/8086 AND MBL 8089-2/8086-2 MAX MODE SYSTEM (USING MBL 8288 BUS CONTROLLER) TIMING REQUIREMENTS

Symbol	Parameter	MBL 8089		MBL 8089-2		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	200	500	125	500	ns	
TCLCH	CLK Low Time	(2/3 TCLCL) −15		(2/3 TCLCL) −15		ns	
TCHCL	CLK High Time	(1/3 TCLCL) +2		(1/3 TCLCL) +2		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		20		ns	
TCLDX	Data in Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into MBL 8284A (See Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into MBL 8284A (See Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into MBL 8089	(2/3 TCLCL) −15		(2/3 TCLCL) −15		ns	
TCHRYX	READY Hold Time into MBL 8089	30		20		ns	
TRYLCL	READY Inactive to CLK (See Note 4)	−8		−8		ns	
TINVCH	Setup Time Recognition (DRQ 1,2, RESET, Ext 1,2) (See Note 2)	30		15		ns	
TGVCH	$\overline{RQ}/\overline{GT}$ Setup Time	30		15		ns	
TCAHCAL	CA Width	95		75		ns	
TSLVCAL	SEL Setup Time	75		55		ns	
TCALSLX	SEL Hold Time	0		0		ns	
TCHGX	$\overline{GT}$ Hold Time into MBL 8089	40		30		ns	
TILIH	Input Rise Time (Except CLK)		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12	ns	From 2.0V to 0.8V

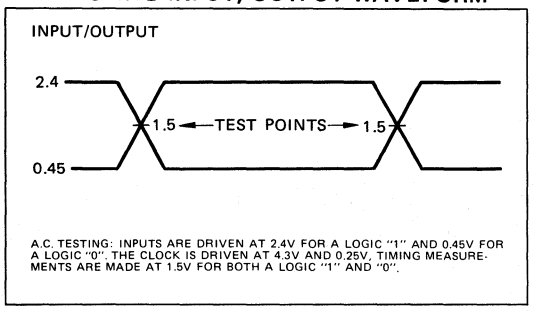
A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

Symbol	Parameter	MBL 8089		MBL 8089-2		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TCLML	Command Active Delay (See Note 1)	10	35	10	35	ns	C_L = 80pF
TCLMH	Command Inactive Delay (See Note 1)	10	35	10	35	ns	
TRYHSH	READY Active to Status Passive (See Note 3)		110		65	ns	
TCHSV	Status Active Delay	10	110	10	60	ns	
TCLSH	Status Inactive Delay	10	130	10	70	ns	
TCLAV	Address Valid Delay	10	110	10	60	ns	
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	
TSVLH	Status Valid to ALE High (See Note 1)		15		15	ns	
TCLLH	CLK Low to ALE Valid (See Note 1)		15		15	ns	C_L = 150pF
TCHLL	ALE Inactive Delay (See Note 1)		15		15	ns	
TCLDV	Data Valid Delay	10	110	10	60	ns	
TCHDX	Data Hold Time	10		10		ns	
TCVNV	Control Active Delay (See Note 1)	5	45	5	45	ns	
TCVNX	Control Inactive Delay (See Note 1)	10	45	10	45	ns	
TCHDTL	Direction Control Active Delay (See Note 1)		50		50	ns	
TCHDTH	Direction Control Inactive Delay (See Note 1)		30		30	ns	
TCLGL	$\overline{RQ}$ Active Delay	0	85	0	50	ns	C_L = 100pF
TCLGH	$\overline{RQ}$ Inactive Delay		85		50	ns	Note 5; C_L = 30pF
TCLSRV	SINTR Valid Delay		150		100	ns	C_L = 100pF
TOLOH	Output Rise Time		20		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12		12	ns	From 2.0V to 0.8V

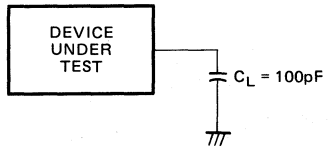
NOTES: 1. Signal at MBL 8284A or MBL 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and TW states.
4. Applies only to T2 state.
5. Applies only if $\overline{RQ}/\overline{GT}$ Mode 1 C_L = 30 pF, 2.7 kΩ pull up to V_{CC}.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". THE CLOCK IS DRIVEN AT 4.3V AND 0.25V. TIMING MEASUREMENTS ARE MADE AT 1.5V FOR BOTH A LOGIC "1" AND "0".

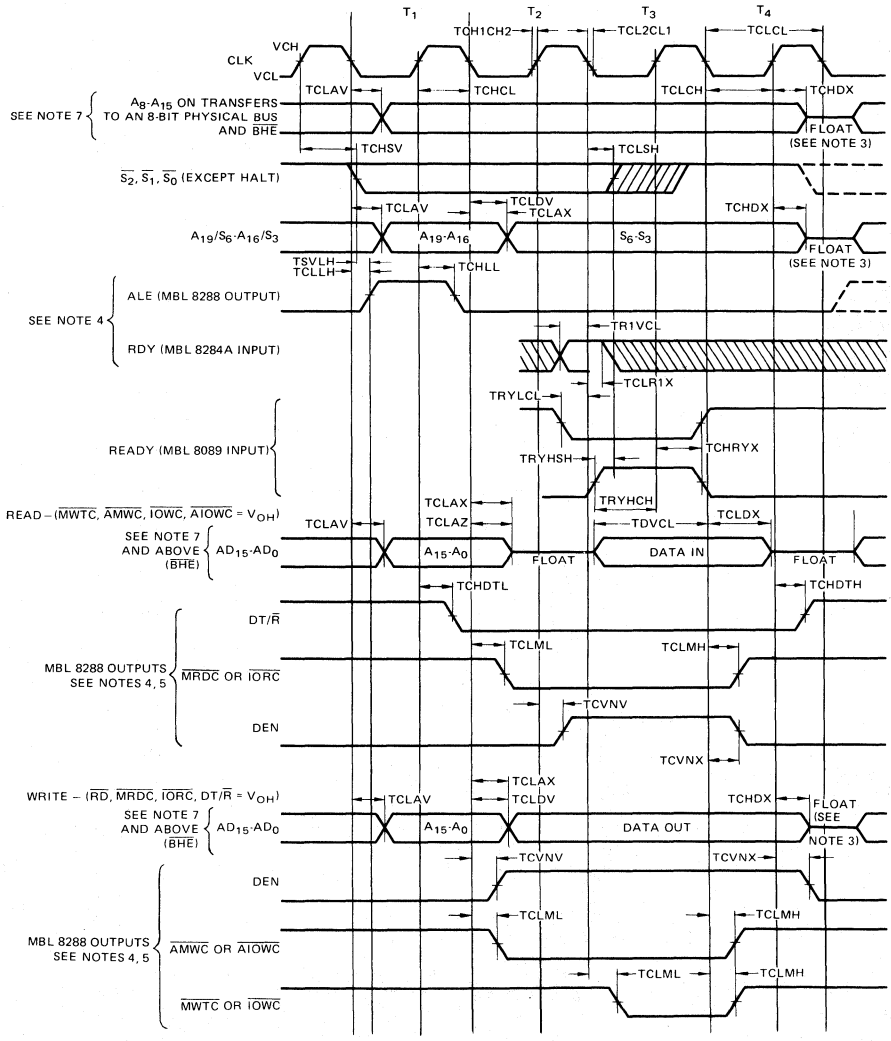
A.C. TESTING LOAD CIRCUIT



C_L = 100pF
C_L INCLUDES JIG CAPACITANCE

WAVEFORMS

MBL 8089 BUS TIMING USING MBL 8288

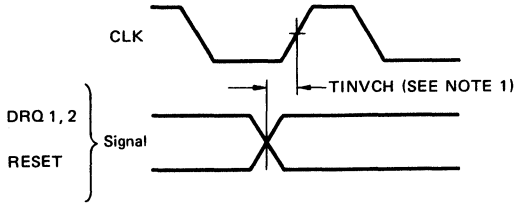


NOTES:

1. ALL SIGNALS SWITCH BETWEEN V_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED.
2. RDY IS SAMPLED NEAR THE END OF T_2, T_3, T_W TO DETERMINE IF T_W MACHINE STATES ARE TO BE INSERTED.
3. FOLLOWING A WRITE CYCLE DATA REMAINS VALID ON THE MBL 8089 LOCAL BUS UNTIL A LOCAL BUS MASTER DECIDES TO RUN ANOTHER BUS CYCLE. THE LOCAL BUS IS FLOATED BY THE MBL 8089 WHEN THE MBL 8089 ENTERS A REQUEST BUS ACKNOWLEDGE STATE.
4. SIGNALS AT MBL 8284A OR MBL 8288 ARE SHOWN FOR REFERENCE ONLY.
5. THE ISSUANCE OF THE MBL 8288 COMMAND AND CONTROL SIGNALS ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$ AND DEN) LAGS THE ACTIVE HIGH MBL 8288 CEN.
6. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.
7. A_8-A_{15} ARE STABLE ON TRANSFERS TO AN 8 BIT PHYSICAL DATA BUS, i.e. A_8-A_{15} DON'T FLOAT ON A READ FROM AN 8 BIT PHYSICAL BUS OR MULTIPLEX WITH DATA ON A WRITE TO AN 8 BIT PHYSICAL BUS $\overline{BHE}$ IS STABLE (NON MULTIPLEXD) FOR ALL TRANSFERS.

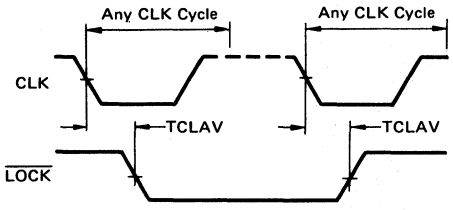
WAVEFORMS (Continued)

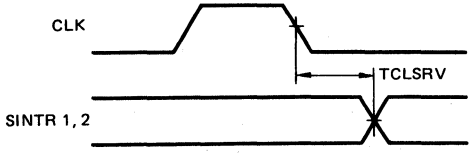
ASYNCHRONOUS SIGNAL RECOGNITION



NOTES:
1. SETUP REQUIREMENTS FOR ASYNCHRONOUS SIGNALS ONLY TO GUARANTEE RECOGNITION AT NEXT CLK.
2. ALL INPUTS EXCEPT CA ARE LATCHED ON A CLK EDGE. THE CA INPUT IS NEGATIVE EDGE TRIGGERED.
3. DRQ BECOMING ACTIVE GREATER THAN 30 ns AFTER THE RISING EDGE OF CLK WILL GUARANTEE NON-RECOGNITION UNTIL THE NEXT RISING CLOCK EDGE.

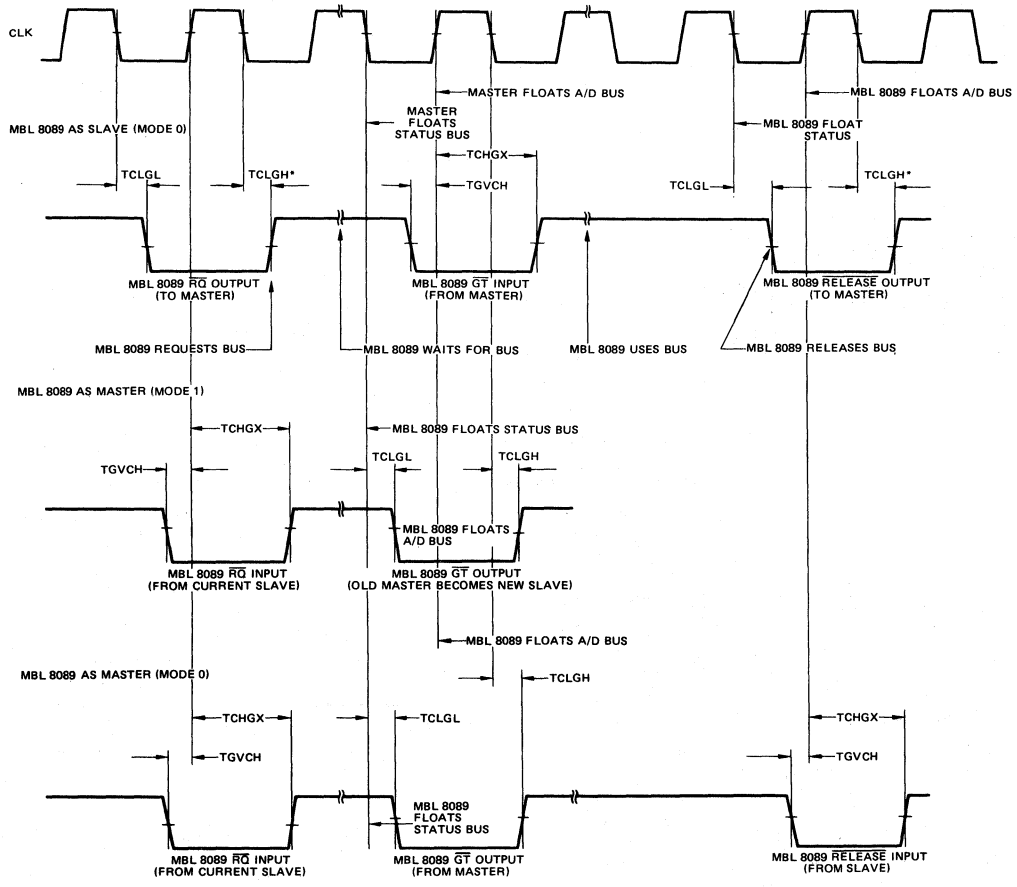
BUS LOCK SIGNAL TIMING AND SINTR TIMING





WAVEFORMS (Continued)

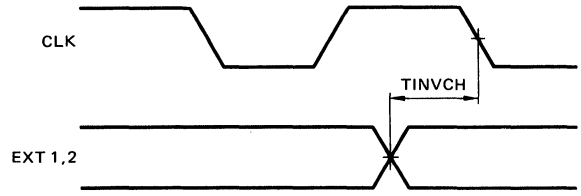
REQUEST/GRANT SEQUENCE TIMING



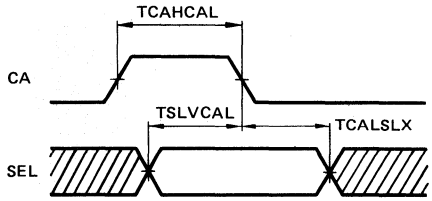
* CPU provides active pull-up.

WAVEFORMS (Continued)

EXTERNAL TERMINATE SETUP TIMING



SEL SETUP AND TIMING



1

MBL 8089 INSTRUCTION SET SUMMARY†

Data Transfers

	POINTER INSTRUCTIONS	OPCODE
		7 0 7 0
LPD P, M	Load Pointer PPP from Addressed Location	P P P 0 0 A A 1 1 0 0 0 1 0 M M
LPDI P, I	Load Pointer PPP Immediate 4 Bytes	P P P 1 0 0 0 1 0 0 0 0 1 0 0 0
MOVP M, P	Store Contents of Pointer PPP in Addressed Location	P P P 0 0 A A 1 1 0 0 1 1 0 M M
MOVP P, M	Restore Pointer	P P P 0 0 A A 1 1 0 0 0 1 1 M M

	MOVE DATA	OPCODE
MOV M, M	Move from Source to Destination — Source	0 0 0 0 0 A A W 1 0 0 1 0 0 M M
	Destination	0 0 0 0 0 A A W 1 1 0 0 1 1 M M
MOV R, M	Load Register RRR from Addressed Location	R R R 0 0 A A W 1 0 0 0 0 0 M M
MOV M, R	Store Contents of Register RRR in Addressed Location	R R R 0 0 A A W 1 0 0 0 0 1 M M
MOVI R	Load Register RRR Immediate (Byte) Sign Extend	R R R wb 0 0 W 0 0 1 1 0 0 0 0
MOVI M	Move Immediate to Addressed Location	0 0 0 wb A A W 0 1 0 0 1 1 M M

Control Transfer

	CALLS	OPCODE
		7 0 7 0
*CALL	Call Unconditional	1 0 0 dd A A W 1 0 0 1 1 1 M M

	JUMP	OPCODE
JMP	Unconditional	1 0 0 dd 0 0 W 0 0 1 0 0 0 0 0
JZ M	Jump on Zero Memory	0 0 0 dd A A W 1 1 1 0 0 1 M M
JZ R	Jump on Zero Register	R R R dd 0 0 0 0 1 0 0 0 1 0 0
JNZ M	Jump on Non-Zero Memory	0 0 0 dd A A W 1 1 1 0 0 0 M M
JNZ R	Jump on Non-Zero Register	R R R dd 0 0 0 0 1 0 0 0 0 0 0
JBT	Test Bit and Jump if True	B B B dd A A 0 1 0 1 1 1 1 M M
JNBT	Test Bit and Jump if Not True	B B B dd A A 0 1 0 1 1 1 0 M M
JMCE	Mask/Compare and Jump on Equal	0 0 0 dd A A 0 1 0 1 1 0 0 M M
JMCNE	Mask/Compare and Jump on Non-Equal	0 0 0 dd A A 0 1 0 1 1 0 1 M M

Arithmetic and Logic Instructions

	INCREMENT, DECREMENT	OPCODE
		7 0 7 0
INC M	Increment Addressed Location	0 0 0 0 0 A A W 1 1 1 0 1 0 M M
INC R	Increment Register	R R R 0 0 0 0 0 0 0 1 1 1 0 0 0
DEC M	Decrement Addressed Location	0 0 0 0 0 A A W 1 1 1 0 1 1 M M
DEC R	Decrement Register	R R R 0 0 0 0 0 0 0 1 1 1 0 0

†Mnemonics © Intel, 1980

Arithmetic and Logic Instructions

	ADD	OPCODE
		7 0 7 0
ADDI M, I	ADD Immediate to Memory	0 0 0 wb A A W 1 1 0 0 0 0 M M
ADDI R, I	ADD Immediate to Register	R R R wb 0 0 W 0 0 1 0 0 0 0 0
ADD M, R	ADD Register to Memory	R R R 0 0 A A W 1 1 0 1 0 0 M M
ADD R, M	ADD Memory to Register	R R R 0 0 A A W 1 0 1 0 0 0 M M
	AND	**OPCODE**
ANDI M, I	AND Memory with Immediate	0 0 0 wb A A W 1 1 0 0 1 0 M M
ANDI R, I	AND Register with Immediate	R R R wb 0 0 W 0 0 1 0 1 0 0 0
AND M, R	AND Memory with Register	R R R 0 0 A A W 1 1 0 1 1 0 M M
AND R, M	AND Register with Memory	R R R 0 0 A A W 1 0 1 0 1 0 M M
	OR	**OPCODE**
ORI M, I	OR Memory with Immediate	0 0 0 wb A A W 1 1 0 0 0 1 M M
ORI R, I	OR Register with Immediate	R R R wb A A W 0 0 1 0 0 1 0 0
OR M, R	OR Memory with Register	R R R 0 0 A A W 1 1 0 1 0 1 M M
OR R, M	OR Register with Memory	R R R 0 0 A A W 1 0 1 0 0 1 M M
	NOT	**OPCODE**
NOT R	Complement Register	R R R 0 0 0 0 0 0 0 1 0 1 1 0 0
NOT M	Complement Memory	0 0 0 0 0 A A W 1 1 0 1 1 1 M M
NOT R, M	Complement Memory, Place in Register	R R R 0 0 A A W 1 0 1 0 1 1 M M

BIT Manipulation and Test Instructions

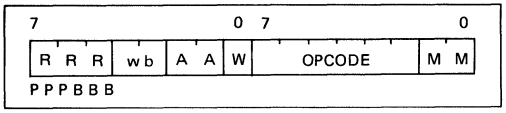
	BIT MANIPULATION	OPCODE
		7 0 7 0
SET	Set the Selected Bit	B B B 0 0 A A 0 1 1 1 1 0 1 M M
CLR	Clear the Selected Bit	B B B 0 0 A A 0 1 1 1 1 1 0 M M
	TEST	**OPCODE**
TSL	Test and Set Lock	0 0 0 1 1 A A 0 1 0 0 1 0 1 M M

Control

	CONTROL	OPCODE
		7 0 7 0
HLT	Halt Channel Execution	0 0 1 0 0 0 0 0 0 1 0 0 1 0 0 0
SINTR	Set Interrupt Service Flip Flop	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
NOP	No Operation	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
XFER	Enter DMA Transfer	0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0
WID	Set Source, Destination Bus Width; S, D 0=8, 1=16	1 S D 0 0 0 0 0 0 0 0 0 0 0 0 0

*AA Field in call instruction can be 00, 01, 10 only.
**OPCODE is second byte fetched.

All instructions consist of at least 2 bytes, while some instructions may use up to 3 additional bytes to specify literals and displacement data. The definition of the various fields within each instruction is given below:



MM Base Pointer Select	
00	GA; general purpose A
01	GB; general purpose B
10	GC; general purpose C
11	PP; parameter pointer

RRR Register Field

The RRR field specifies a 16-bit register to be used in the instruction. If GA, GB, GC or TP are referenced by the RRR field, the upper 4 bits of the registers are loaded with the sign bit (Bit 15). PPP registers are used as 20-bit address pointers.

RRR				
000	r0	GA	;	general purpose A
001	r1	GB	;	general purpose B
010	r2	GC	;	general purpose C
011	r3	BC	;	byte count
100	r4	TP	;	task block pointer
101	r5	IX	;	index register
110	r6	CC	;	channel control (mode)
111	r7	MC	;	mask/compare

See Notes 1, 2.

PPP				
000	p^0	GA	;	general purpose A
001	p^1	GB	;	general purpose B
010	p^2	GC	;	general purpose C
100	p^4	TP	;	task block pointer

Note 1. Logical and arithmetic instructions should not be used to update the CC register (i.e. – only MOV and MOVI instructions should be used.)
2. A 20-bit register (GA, GB, GC or TP) that is initialized as a 16-bit I/O space pointer must be saved at even addresses when using MOVP or CALL instructions.

Notes:

BBB Bit Select Field

The bit select field replaces the RRR field in bit manipulation instructions and is used to select a bit to be operated on by those instructions. Bit 0 is the least significant bit.

wb

01 1 byte literal
10 2 byte (word) literal

dd

01 1 byte displacement
10 2 byte (word) displacement.

AA Field

00 The selected pointer contains the operand address.
01 The operand address is formed by adding an 8-bit, unsigned, offset contained in the instruction to the selected pointer. The contents of the pointer are unchanged.
10 The operand address is formed by adding the contents of the index register to the selected pointer. Both registers remain unchanged.
11 Same as 10 except the index register is post auto-incremented (by 1 for 8-bit transfer, by 2 for 16-bit transfer)

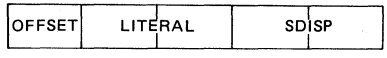
W Width Field

0 The selected operand is 1 byte long.
1 The selected operand is 2 bytes long.

Additional Bytes

OFFSET : 8-bit unsigned offset.
SDISP : 8/16-bit signed displacement.
LITERAL : 8/16-bit literal. (32 bits for LDPI).

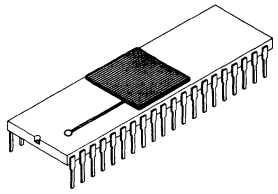
The order in which the above optional bytes appear in IOP instructions is given below:



Offsets are treated as unsigned numbers. Literals and displacements are sign extended (2's complement).

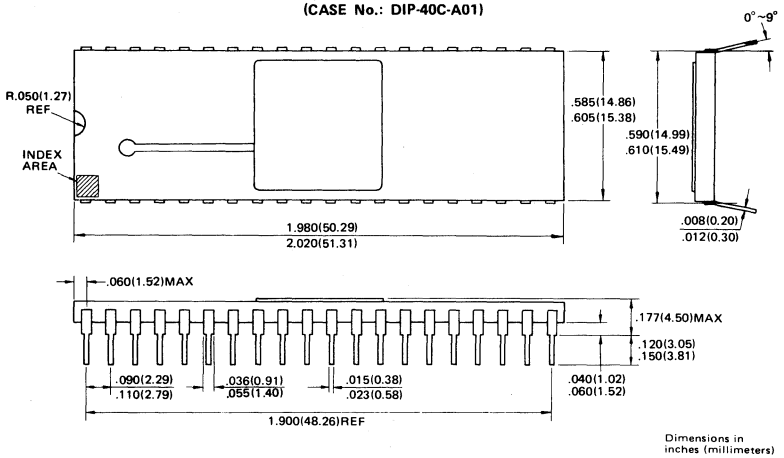
PACKAGE ILLUSTRATION

CERAMIC PACKAGE
(METAL SEAL)



PACKAGE DIMENSIONS
(Suffix : -C)

40-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-40C-A01)



Dimensions in
inches (millimeters)

1