FUJITSU

NMOS SINGLE-CHIP 8-BIT MICROCOMPUTER

MBL8749H/N

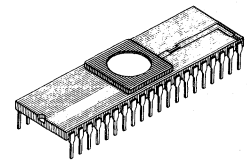
October 1986
Edition 1.0

DESCRIPTION

The Fujitsu MBL8749 is an 8-bit single-chip microcomputer that uses a 2K × 8-bit Electrically Programmable Read Only Memory (EPROM) for program memory. The EPROM can be erased by using an ultraviolet (UV) light source; thus, program memory for the MBL8749 can be changed as often as required. Also included in the MBL8749 are: 256 × 8-bit static RAM, 27 I/O lines, an 8-bit timer/counter, and a clock generator. The device can be ordered in either of two speed versions: N-version for operation at 6MHz and the H-version for operation at 11MHz. For either frequency, the operating temperature range is 0°C to 70°C.

The MBL8749 is fabricated using an N-channel, 2-layer polysilicon-gate MOS process. The MBL8749 is housed in a 40-pin ceramic windowed DIP and requires a single +5-volt supply for basic operation and a 21-volt supply for programming the EPROM.

The MBL8749 is well suited for applications such as system evaluation, system prototyping, and low-volume production work.

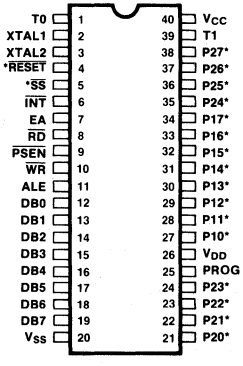


Ceramic DIP
(DIP-40C-A04)

FEATURES

- 2K × 8-bit program memory (EPROM)
- 256 × 8-bit data memory (static RAM)
- 8-level stack
- 8 pairs of working registers
- 27 I/O lines: Two 8-bit I/O ports, one 8-bit data bus, two test inputs, and one interrupt input
- 8-bit timer/counter
- On-chip clock generator (or external clock source)
- Single-level interrupt
- External program mode
- Single-step operation
- RAM retention in low-power standby mode
- ALU functions: Addition, decimal adjust addition, and logic operations
- Instruction cycle time: 1.36μs for H-version (11MHz) and 2.5μs for N-Version (6MHz)
- Powerful instruction set: 96 instructions (230 op-codes). All instructions complete in one or two instruction cycles with 70% being of the single-byte type
- Some instructions can process ROM contents as data

PIN ASSIGNMENT



*These pins have on-chip pullups.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Features (Cont)

- I/O port data can be handled directly in logic operations
- Binary coded decimal (BCD) data can be handled
- Single +5V power supply
- 0°C to 70°C operating temperature range
- N-channel, 2-layer polysilicon-gate MOS process
- 40-pin ceramic DIP package
- Compatible with Intel 8749
- Replaceable with Fujitsu MBL8049/48 and Intel 8049/8048

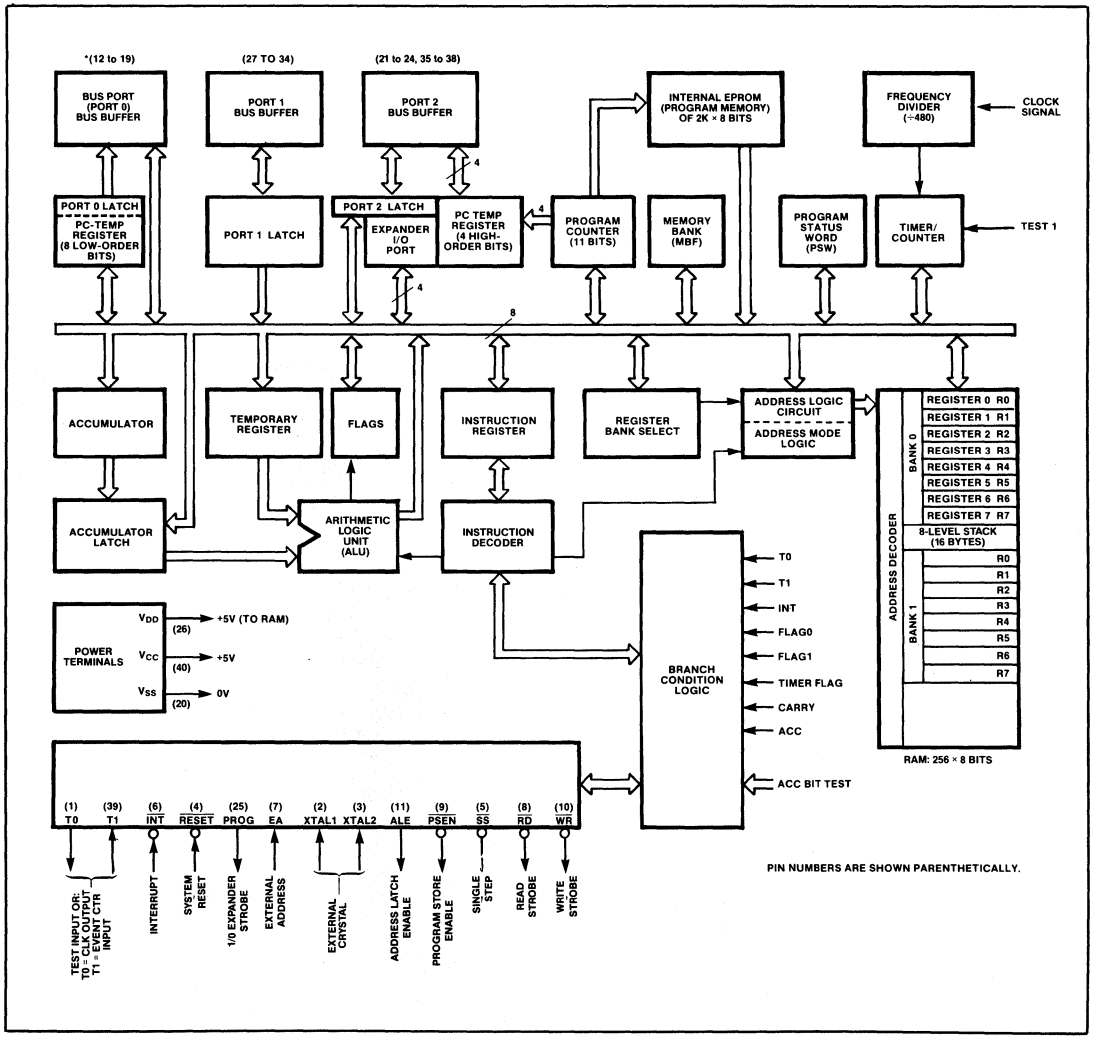
PIN DESCRIPTIONS

Pin No.	Symbol	Function
1	T0	Test Input 0: Input for conditional branch instructions JT0 and JNT0. Clock output when an ENT0 CLK instruction is executed.
2	XTAL1	Connections for external crystal. If an external TTL clock source is used, proper interface circuits are required between the clock source and XTAL1/XTAL2, since these inputs are not TTL compatible. Generally an open-collector drive and a squarewave pulse shaper will suffice.
3	XTAL2	
4	$\overline{\text{RESET}}$	When active low, resets MPU and initializes processor as follows: • Clears program counter and stack pointer. • Selects memory bank 0 and register bank 0. • Disables T0 output. • Places bus in the high-impedance state and ports 1 and 2 in the input mode. • Disables interrupts and stops the timer/counter. • Clears timer and user flags F0 and F1.
5	$\overline{\text{SS}}$	Input for single step operation. When $\overline{\text{SS}}$ is pulsed and goes low, the MPU executes the current instruction and stops. The next instruction address is fetched and placed in the four low-order bits of port 2 and the bus port. When $\overline{\text{SS}}$ is pulsed high, the single-step operation is repeated so long as $\overline{\text{SS}}$ is repetitively driven low, high, low, high, etc. When $\overline{\text{SS}}$ is permanently set to the high state, normal operation resumes.
6	$\overline{\text{INT}}$	When active low, initiates an external interrupt request. The $\overline{\text{INT}}$ input signal must remain low until the interrupt request is latched. This pin also serves as an input for a conditional branch instruction (JNI).
7	EA	All program memory accesses are directed to an external program memory when EA is high. At this time, the Program Store Enable ($\overline{\text{PSEN}}$) strobe is also output to external program memory.
8	$\overline{\text{RD}}$	The read strobe ($\overline{\text{RD}}$) is active (Low) when data is read from the bus port. This strobe output signal enables data onto the bus port from external devices including external data memory. The $\overline{\text{RD}}$ strobe is output when either an INS A,BUS or MOVX A @Rr instruction is executed.
9	$\overline{\text{PSEN}}$	The Program Store Enable ($\overline{\text{PSEN}}$) strobe is output to external program memory each time the memory is accessed. This external program memory enable signal is generated in the instruction fetch cycle and the instruction is fetched on the rising edge of this signal.

PIN DESCRIPTIONS (continued)

Pin No.	Designator	Function
10	$\overline{WR}$	When active low, the write ($\overline{WR}$) strobe enables data to pass from the data bus port to external I/O devices, including external memory. The $\overline{WR}$ strobe is active when executing an "OUTL BUS, A" or a "MOVX@Rr, A" instruction.
11	ALE	Clock signal (ALE) output generated in each instruction cycle. This signal is used for external synchronization with the MPU. The address signal to the external program memory or external data memory is latched at the falling edge of the ALE signal. This signal is output except during single-step operations.
12 to 19	DB0 to DB7	A bidirectional I/O port called the bus port (Port 0). Strobe signals $\overline{RD}$ and $\overline{WR}$ are output on data input or output. This port can also be used for latch output or as the interface to the external program memory or external data memory. When the external program memory is accessed, the address signal (the low-order 8 bits) is output synchronously with the ALE signal and the instruction is fetched from the specified address synchronously with the $\overline{PSEN}$ signal. When external data memory is accessed, the address signal is output synchronously with the ALE signal and data is read or written synchronously with the $\overline{RD}$ or $\overline{WR}$ signal. When data is not being input or output, the bus port is in a high-impedance state.
20	V_{SS}	Ground terminal (GND)
21 to 24	P20 to P23	A pseudo-bidirectional I/O port. All bits must be set to 1 before the port is used for input. The four low-order bits (P20 to P23) function as the interface to the I/O expander (MBL8243) or serve as an output for the address signal (four high-order bits) when the external program memory is used. The port data is lost on access to the I/O expander and retained when the external program memory is accessed; it is recovered when no address data is output.
35 to 38	P24 to P27	
25	PROG	Strobe signal (PROG) output to the I/O expander. This signal is also used as an input strobe to program the internal EPROM.
26	V_{DD}	Power supply to the internal RAM and EPROM.
27 to 34	P10 to P17	An 8-bit pseudo-bidirectional I/O port. All bits must be set high before the port is used for input.
39	T1	Input for conditional branch instructions JT1 and JNT1; also serves as event input when event counter mode is selected. The event counter is incremented on the falling edge of this input signal.
40	V_{CC}	+5-volt power supply.

BLOCK DIAGRAM



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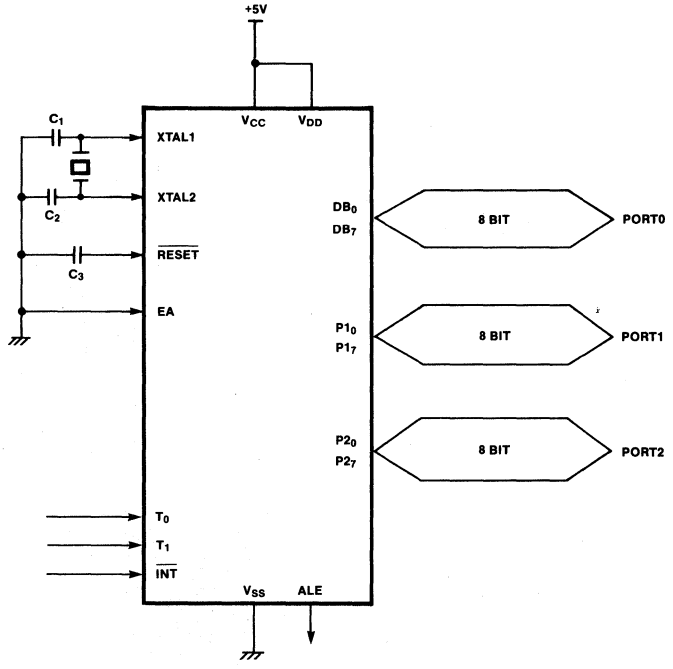
FUNCTIONAL DESCRIPTION

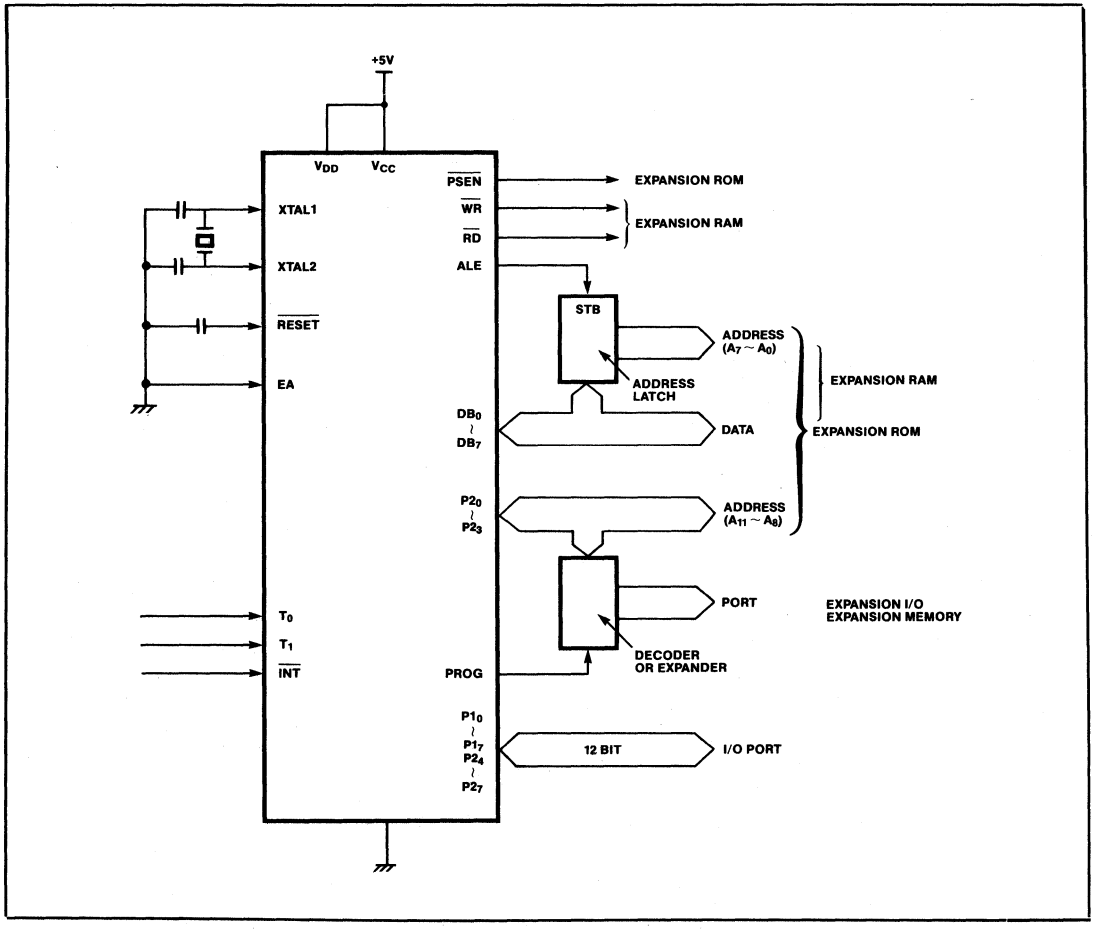
Block Name	Function
Clock Generation Circuitry	Using a capacitor, a crystal, or an external clock source, the on-chip clock generator produces a master clock within a frequency range of 1-to-6 MHz for N-version parts and 11 MHz for H-version parts. The master clock frequency is divided by three to produce a state clock signal which, in turn, is divided by five to produce a cycle clock signal. The cycle clock is used for all internal operations and is available on the ALE pin. When an ENT0 CLK instruction is executed, the state clock is output on the T0 pin.
I/O Port	Three bidirectional or quasi-bidirectional 8-bit I/O ports and three input terminals are provided for signal inputs and outputs. Port 0 (Bus Port) and the lower 4 bits of Port 2 shown in the Block Diagram are used for access to external memories or I/O expanders.
On-chip ROM and RAM	Programs are stored in the on-chip EPROM (2K bytes). Also, the contents of ROM can be used as data for some instructions. The on-chip RAM (256 bytes) is used for general-purpose registers, the 16-byte stack, and scratch-pad memory (refer to RAM memory map that follows). ROM can be expanded up to 4K bytes by memory addons and by switching memory banks; RAM can be expanded an additional 256 bytes by simple addons. A standalone system and one designed for memory addons are shown following the "Functional Description."
Program Counter	The program counter is a 12-bit register that holds the address in program memory from which the next instruction is to be fetched and is incremented by every execution of an instruction.
Instruction Register	The Instruction Register is an 8-bit register that holds the next instruction to be executed.
Instruction Decoder	The Instruction Decoder decodes the instruction stored in the Instruction Register and generates various control signals for both internal circuits and external peripherals.
Arithmetic Logic Unit (ALU)	Various operations such as addition, subtraction, comparison, etc. are executed in the ALU. Operations to be executed are determined from the instruction decoding process.
Interval Timer/ Event Counter	The Interval Timer/Event Counter is an 8-bit register under instruction control. The interval timer mode or event counter mode can be designated by instruction execution, as well. This register is not initialized by the RESET signal. In the interval timer mode, the register counts up the frequency signal which is generated by dividing the cycle clock frequency by 32. When the source frequency is 6MHz, this enables the register to count a time interval of up to 20.48ms with a resolution of 80μs. In this mode, the register generates an interrupt vector address (Address 07), if the register overflows from $(FF)_{16}$ to $(00)_{16}$. Even if an oveflow occurs, the register continues to count up. This enables the register to count a longer time interval by using proper software. In the event counter mode, the register counts on the falling edge of the T_1 input. In this mode, the features of the register other than the counting trigger are the same as those in the interval timer mode. (Note. The T_1 input pulse has a minimum width of 500-nanoseconds and, at 6MHz, a minimum cycle time of 7.5-microseconds.)
Status Register Including Stack Pointer	The Status Register is an 8-bit register which consists of four bits for flags, three bits for the Stack Pointer, and an unused bit. The flag bits indicate the status of the MPU. The Stack Pointer specifies an address in the stack to be used in the next subroutine call or interrupt.

STANDALONE SYSTEM

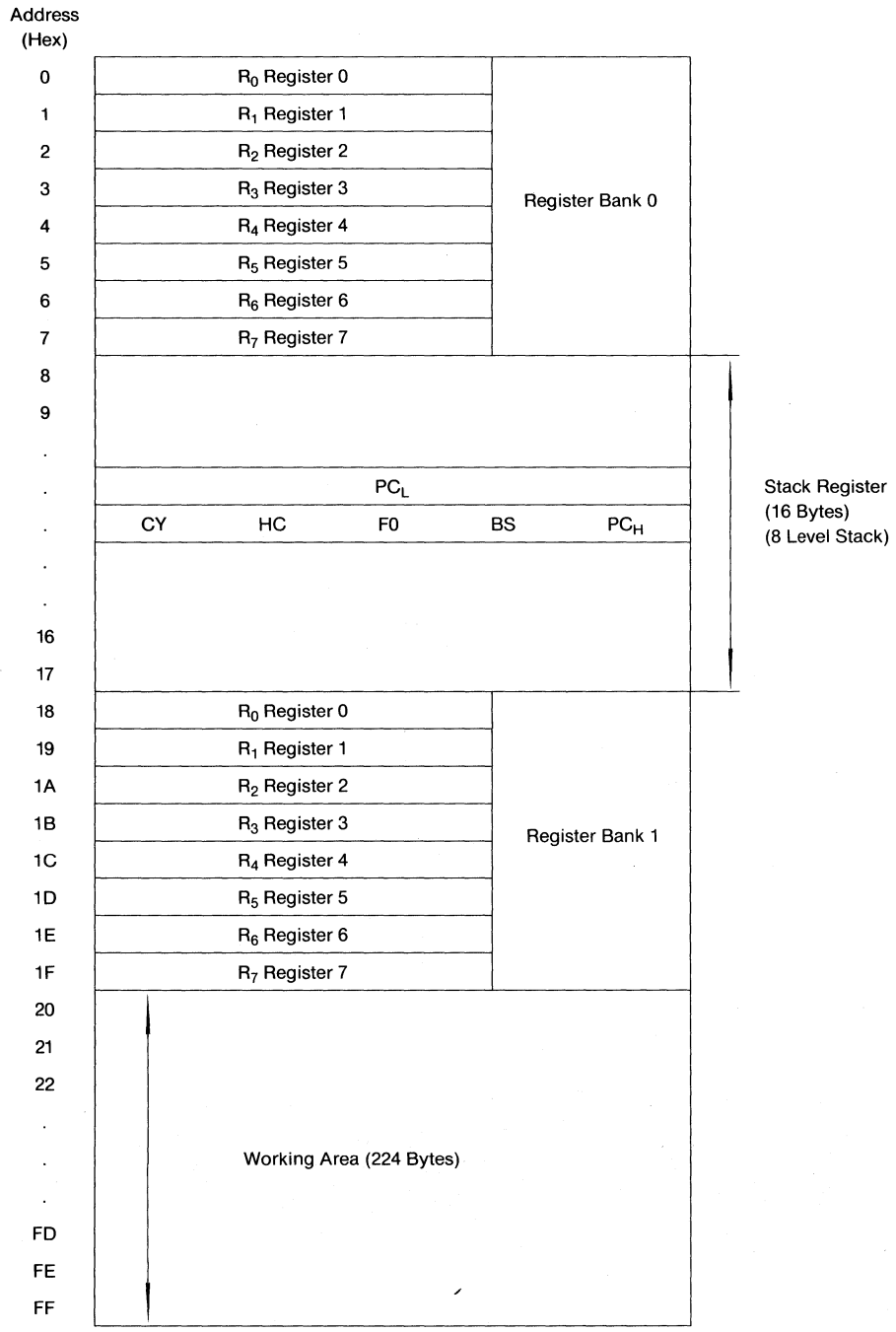


Example: OSC XTAL 1 TO 6MHz
C_1, C_2 = 20pF
RESET C_3 = 1μF

EXPANDED SYSTEM



RESIDENT DATA MEMORY MAP (RAM)



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STATUS REGISTER

The Status Register is an 8-bit register that holds the Program Status Word (PSW). The register is configured as shown. The upper four bits are used for flags to indicate the status of the MPU. When a subroutine call or an interrupt occurs, the contents of the program counter are transferred to one of the 8 register pairs of the Stack Register as determined by the lower three bits of the Status Register. The remaining bit is unused.

7	6	5	4	3	2	1	0
CY	HC	F_0	BS	Blank (Unused Bit)	SP_2	SP_1	SP_0
← Flags →					← Stack Pointer →		

FLAGS

CY (Carry): When an overflow occurs in the Accumulator during an ALU operation, this bit is set to "1".

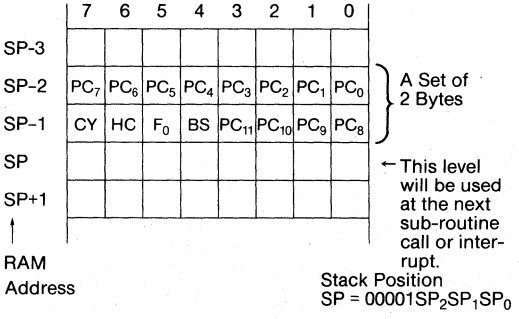
HC (Half Carry): When an overflow occurs from Bit 3 to Bit 4 in the accumulator as a result of an addition, this bit is set to "1".

F_0 (User Flag): This flag is instruction-controlled by the user.

BS (Bank Select): This flag is used for register-bank identification. When BS = 0, Register Bank 0 is selected; when BS = 1, Register Bank 1 is selected.

STACK REGISTER

The Stack Register uses 16 bytes of memory in the on-chip RAM. The Stack Register consists of eight levels, that is, a stack level consists of two bytes as shown.



SP (Stack Pointer): In the above figure, "SP" indicates an address in the stack pointer that will be used for the next subroutine call or interrupt. "SP" is given as an 8-bit code from the lower three bits of the status register as follows:

$$SP = 00001SP_2SP_1SP_0$$

↳ Status Register bits 0 to 2.

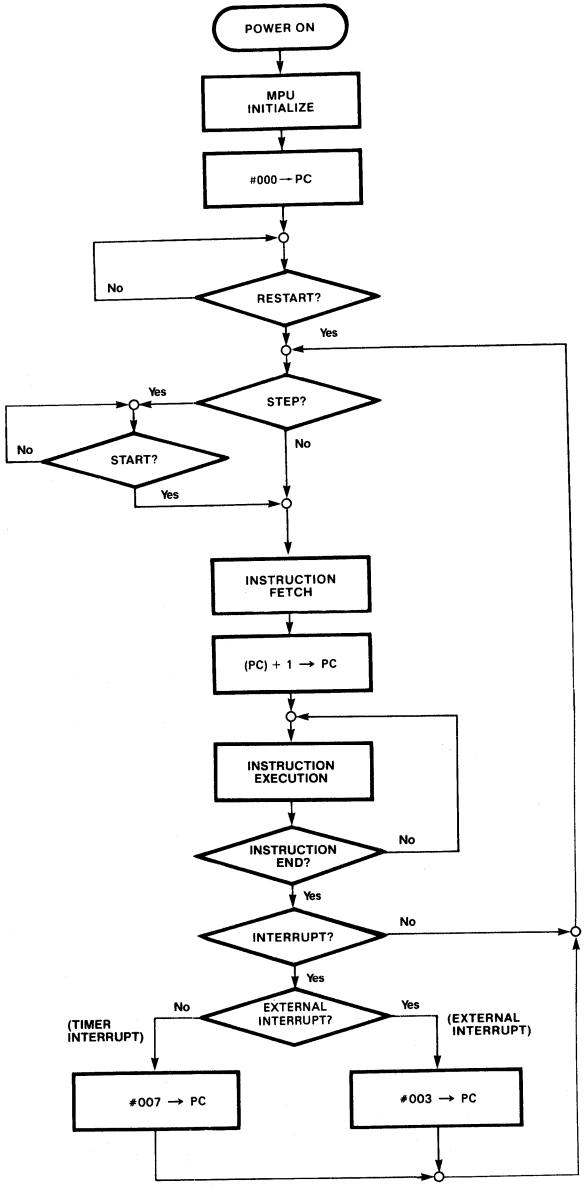
PC_n (Program Counter): In the above figure, "PC_n" indicates the content of the n^{th} bit in the Program Counter.

INTERRUPT OPERATION

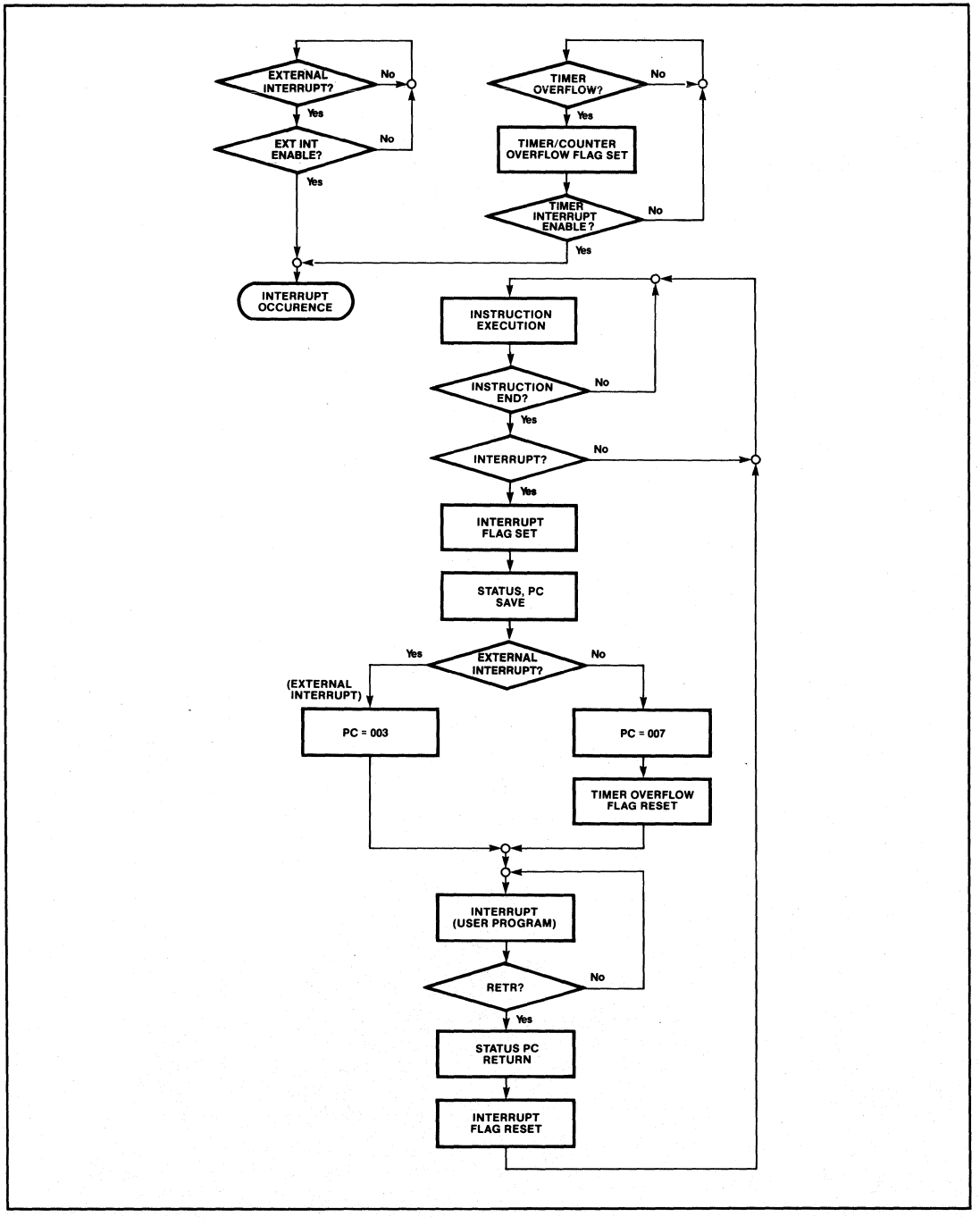
There are two modes for interrupt operation: external interrupts and timer/counter interrupts. A timer/counter interrupt is masked by an external input; thus, external interrupts always have priority. The basic operation for both types of interrupts are the same, except a timer/counter interrupt is initiated on overflow of the counter. Subsequent flowcharts provide operational detail for the interrupt procedures that follow.

- Upon executing the current instruction, the interrupt flag is set.
- Contents of the Status Register and Program Counter are saved in the stack.
- For an external interrupt, the Program Counter is loaded with address 003; for a timer/counter interrupt, address 007 is loaded in the PC.
- After the interrupt is serviced, a RETR instruction is executed which restores the pre-interrupt contents of the Status Register and Program Counter.
- The interrupt flag is reset.

OPERATION FLOWCHART



INTERRUPT FLOWCHART



PROGRAMMING AND VERIFYING EPROM MEMORY

Internal program memory of the MBL8749 is a 2K × 8-bit EPROM that can be electrically written into, and erased by using an ultraviolet (UV) light source. Pin functions for programming and verifying the EPROM are repeated here for convenience of the user.

Pin Descriptions

Name	Function
XTAL1, XTAL2	Clock signal (1 to 3MHz) input
$\overline{\text{RESET}}$	Initialize and address-latch signal input: Address data input to the data bus is internally latched on the rising edge of the $\overline{\text{RESET}}$ signal.
T0	Program mode is selected when this signal is low and verify mode is selected when it is high.
EA	Program and verify enable signal input: Either mode is enabled when 18 volts is applied to this pin.
BUS (D7 to D0)	Address and data inputs in the program mode and data output in the verify mode.
V_{DD}	Power supply
PROG	Input pulses for programming

PROGRAMMING PROCEDURE

Step 1: Initialization
V_{CC} and V_{DD} = 5V
Clock signal = 1 to 3MHz (Internal or external clock)
$\overline{\text{RESET}}$ = 0V
T0, EA = 5V
BUS and PROG pins floating.

Step 2: T0 = 0V
Select program mode.

Step 3: EA = 18V
Enable program or verify mode

Step 4: Input address signals.
BUS = 8 low-order bits
P22 to P20: = 3 high-order bits

Step 5: $\overline{\text{RESET}}$ = 5V
Internally latch the address inputs.

Step 6: Input write data to BUS.

Step 7: V_{DD} = 21V
Turn on programming power supply.

Step 8: Apply 0 volts to the PROG pin and then apply a programming pulse of 18 volts for 50 ms. Again apply 0 volts to the pin and then let it float.

Step 9: V_{DD} = 5V, BUS floating
Turn off programming power supply (V_{DD} = 21V → 5V), and let BUS float.

Step 10: T0 = 5V
Select verify mode.

Step 11: Externally read BUS data to verify data.

Step 12: T0 = 0V
Terminate verify mode and select program mode.

Step 13: $\overline{\text{RESET}}$ = 0V
Go to the next step when data has been written. If data is not valid, repeat procedures, beginning with Step 4.

Step 14: EA = 5V
Disable program or verify mode.

ERASING EPROM

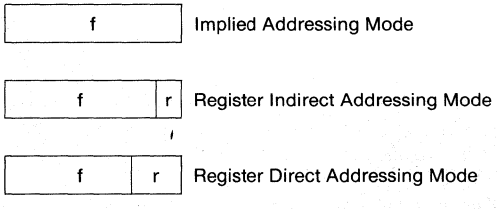
Data written into the EPROM can be erased by applying ultraviolet light rays with a wavelength of 2537 angstroms. With UV light source directly above the transparent lid at a distance of 2-to-3 centimeters, the time for complete erasure is between 15-and-20 minutes for most commercial lamps. The recommended amount of UV radiation is 10Wsec/cm^2; the luminous intensity on the package surface is designed to be approximately 12000μW/cm^2.

If the package surface is soiled by grease, adhesives, or other light inhibitors, the erasing time will increase. Before attempting to erase data, it is recommended that surface be cleaned with alcohol or some other detergent that will not damage the package.

INSTRUCTIONS

All instructions are one or two bytes and also execute in either one or two cycles. Addresing modes are classified as direct, expanded, indirect, immediate and implied. Single-byte and double-byte instruction formats are as follows:

1-Byte Instruction:



2-Byte Instruction:

f	OP

Immediate Addressing Mode

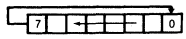
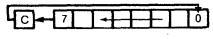
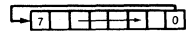
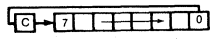
A_H	f	A_L

Expanded Addressing Mode

f: Instruction Operation Set
r: Register Set
OP: Operand Data
A_H, A_L: Operand Address

Table 1. Instruction Set Summary

Accumulator and Memory Instructions

Operation	Mnemonic	OP code	Byte	Cycle	Flag C	Flag AC	Flag F0	Flag F1	Notes
Add register to A	ADD A, Rr	6X	1	1	*	*	—	—	(A) ← (A) + (Rr)
Add data memory to A	ADD A, @R0	60	1	1	*	*	—	—	(A) ← (A) + ((R0))
	ADD A, @R1	61	1	1	*	*	—	—	(A) ← (A) + ((R1))
Add immediate to A	ADD A, #data	03	2	2	*	*	—	—	(A) ← (A) + data
Add register to A with carry	ADDC A, Rr	7X	1	1	*	*	—	—	(A) ← (A) + (Rr) + (C)
Add data memory to A with carry	ADDC A, @R0	70	1	1	*	*	—	—	(A) ← (A) + ((R0)) + (C)
	ADDC A, @R1	71	1	1	*	*	—	—	(A) ← (A) + ((R1)) + (C)
Add immediate to A with Carry	ADDC A, #data	13	2	2	*	*	—	—	(A) ← (A) + data + (C)
And register to A	ANL A, Rr	5X	1	1	—	—	—	—	(A) ← (A) ∩ (Rr)
And data memory to A	ANL A, @R0	50	1	1	—	—	—	—	(A) ← (A) ∩ ((R0))
	ANL A, @R1	51	1	1	—	—	—	—	(A) ← (A) ∩ ((R1))
And immediate to A	ANL A, #data	53	2	2	—	—	—	—	(A) ← (A) ∩ data
Clear A	CLR A	27	1	1	—	—	—	—	(A) ← 0
Complement A	CPL A	37	1	1	—	—	—	—	(A) ← $\overline{(A)}$
Decimal Adjust A	DA A	57	1	1	*	—	—	—	Note 1
Decrement A	DEC A	07	1	1	—	—	—	—	(A) ← (A) - 1
Increment A	INC A	17	1	1	—	—	—	—	(A) ← (A) + 1
Or register to A	ORL A, Rr	4X	1	1	—	—	—	—	(A) ← (A) ∪ (Rr)
Or data memory to A	ORL A, @R0	40	1	1	—	—	—	—	(A) ← (A) ∪ ((R0))
	ORL A, @R1	41	1	1	—	—	—	—	(A) ← (A) ∪ ((R1))
Or immediate to A	ORL A, #data	43	2	2	—	—	—	—	(A) ← (A) ∪ data
Rotate A left	RL A	E7	1	1	—	—	—	—	
Rotate A left through carry	RLC A	F7	1	1	*	—	—	—	
Rotate A right	RR A	77	1	1	—	—	—	—	
Rotate A right through carry	RRC A	67	1	1	*	—	—	—	
SWAP nibles of A	SWAP A	47	1	1	—	—	—	—	(A7~4) ⇄ (A3~0)
Exclusive or register to A	XRL A, Rr	DX	1	1	—	—	—	—	(A) ← (A) ⊕ (Rr)
Exclusive or data memory to A	XRL A, @R0	D0	1	1	—	—	—	—	(A) ← (A) ⊕ ((R0))
	XRL A, @R1	D1	1	1	—	—	—	—	(A) ← (A) ⊕ ((R1))
Exclusive or immediate to A	XRL A, #data	D3	2	2	—	—	—	—	(A) ← (A) ⊕ data

Input/Output Instructions (Cont)

Operation	Mnemonic	OP code	Byte	Cycle	Flag C	Flag AC	Flag F0	Flag F1	Notes
And immediate to BUS	ANL BUS, #data	98	2	2	—	—	—	—	(BUS) ← (BUS) ∩ data
P1	ANL P1, #data	99	2	2	—	—	—	—	(P1) ← (P1) ∩ data
P2	ANL P2, #data	9A	2	2	—	—	—	—	(P2) ← (P2) ∩ data
And A to Expander Port	ANLD P_p, A	9X	1	2	—	—	—	—	(P_p) ← (P_p) ∩ (A3~0)
Input BUS to A	INS A, BUS	08	1	2	—	—	—	—	(A) ← (BUS)
Port 1 to A	IN A, P1	09	1	2	—	—	—	—	(A) ← (P1)
Port 2 to A	IN A, P2	0A	1	2	—	—	—	—	(A) ← (P2)
Input Expander Port to A	MOVD A, P_p	0X	1	2	—	—	—	—	(A3~0) ← (P_p) (A7~0) ← 0
Or immediate to BUS	ORL BUS, #data	88	2	2	—	—	—	—	(BUS) ← (BUS) ∪ data
P1	ORL P1, #data	89	2	2	—	—	—	—	(P1) ← (P1) ∪ data
P2	ORL P2, #data	8A	2	2	—	—	—	—	(P2) ← (P2) ∪ data
Or A to Expander Port	ORLD P_p, A	8X	1	2	—	—	—	—	(P_p) ← (P_p) ∪ (A3~0)
Output A to BUS	OUTL BUS, A	02	1	2	—	—	—	—	(BUS) ← (A)
P1	OUTL P1, A	39	1	2	—	—	—	—	(P1) ← (A)
P2	OUTL P2, A	3A	1	2	—	—	—	—	(P2) ← (A)
Output A to Expander Port	MOVD P_p, A	3X	1	2	—	—	—	—	(P_p) ← (A3~0)
Data Move Instructions									
Move register to A	MOV A, Rr	FX	1	1	—	—	—	—	(A) ← (Rr)
Move data memory to A	MOV A, @R0	F0	1	1	—	—	—	—	(A) ← ((R0))
	MOV A, @R1	F1	1	1	—	—	—	—	(A) ← ((R1))
Move immediate to A	MOV A, #data	23	2	2	—	—	—	—	(A) ← data
Move A to register	MOV Rr, A	AX	1	1	—	—	—	—	(Rr) ← (A)
Move A to data memory	MOV @R0, A	A0	1	1	—	—	—	—	((R0)) ← (A)
	MOV @R1, A	A1	1	1	—	—	—	—	((R1)) ← (A)
Move immediate to register	MOV Rr, #data	BX	2	2	—	—	—	—	(Rr) ← data
Move immediate to data memory	MOV @R0, #data	B0	2	2	—	—	—	—	((R0)) ← data
	MOV @R1, #data	B1	2	2	—	—	—	—	((R1)) ← data
Move PSW to A	MOV A, PSW	C7	1	1	—	—	—	—	(A) ← (PSW)
Move A to PSW	MOV PSW, A	D7	1	1	*	*	*	—	(PSW) ← (A)
Move external data memory to A	MOVX A, @R0	80	1	2	—	—	—	—	(A) ← ((R0))
	MOVX A, @R1	81	1	2	—	—	—	—	(A) ← ((R1))
Move A to external data memory	MOVX @R0, A	90	1	2	—	—	—	—	((R0)) ← (A)
	MOVX @R1, A	91	1	2	—	—	—	—	((R1)) ← (A)
Move to A from current page	MOVP A, @A	A3	1	2	—	—	—	—	(A) ← ((A))
Move to A from Page 3	MOVP3A, @A	E3	1	2	—	—	—	—	(A) ← ((A)) within page 3
Exchange A and register	XCH A, Rr	2X	1	1	—	—	—	—	(A) ⇄ (Rr)
Exchange A and data memory	XCH A, @R0	20	1	1	—	—	—	—	(A) ⇄ ((R0))
	XCH A, @R1	21	1	1	—	—	—	—	(A) ⇄ ((R1))
Exchange nibble of A and data memory	XCHD A, @R0	30	1	1	—	—	—	—	(A3~0) ⇄ ((R0)3~0)
	XCHD A, @R1	31	1	1	—	—	—	—	(A3~0) ⇄ ((R1)3~0)
Register Instructions									
Decrement register	DEC Rr	CX	1	1	—	—	—	—	(Rr) ← (Rr) - 1
Increment register	INC Rr	1X	1	1	—	—	—	—	(Rr) ← (Rr) + 1
Increment data memory	INC @R0	10	1	1	—	—	—	—	((R0)) ← ((R0)) + 1
	INC @R1	11	1	1	—	—	—	—	((R1)) ← ((R1)) + 1

Timer/Counter Instructions (Cont)

Operation	Mnemonic	OP code	Byte	Cycle	Flag C	Flag AC	Flag F0	Flag F1	Notes
Disable Timer/Counter Interrupt	DIS TCNTI	35	1	1	—	—	—	—	
Enable Timer/Counter Interrupt	EN TCNTI	25	1	1	—	—	—	—	
Read Timer/Counter	MOV A, T	42	1	1	—	—	—	—	(A) ← (T)
Load Timer/Counter	MOV T, A	62	1	1	—	—	—	—	(T) ← (A)
Start Time	STRT T	55	1	1	—	—	—	—	
Start Counter	STRT CNT	45	1	1	—	—	—	—	
Stop Timer/Counter	STOP TCNT	65	1	1	—	—	—	—	
Control Instructions									
Disable external interrupt	DIS I	15	1	1	—	—	—	—	
Enable external interrupt	EN I	05	1	1	—	—	—	—	
Enable Clock output on T0	ENT0 CLK	75	1	1	—	—	—	—	
No Operation	NOP	00	1	1	—	—	—	—	
Select register bank 0	SEL RB0	C5	1	1	—	—	—	—	(BS) ← 0
Select register bank 1	SEL RB1	D5	1	1	—	—	—	—	(BS) ← 1
Select memory bank 0	SEL MB0	E5	1	1	—	—	—	—	(MBF) ← 0
Select memory bank 1	SEL MB1	F5	1	1	—	—	—	—	(MBF) ← 1
Branch and Jump Instructions									
Decrement register and test	DJNZ Rr, addr	EX	2	2	—	—	—	—	(Rr) ≠ 0 (Note 4)
Jump unconditional	JMP addr	%4	2	2	—	—	—	—	Unconditional Branch
Jump indirect	JMPP @A	B3	1	2	—	—	—	—	Unconditional Branch (Note 5)
Jump on Carry = 1	JC addr	F6	2	2	—	—	—	—	(C) = 1
Jump on Carry = 0	JNC addr	E6	2	2	—	—	—	—	(C) = 0
Jump on A zero	JZ addr	C6	2	2	—	—	—	—	(A) = 0
Jump on A not zero	JNZ addr	96	2	2	—	—	—	—	(A) ≠ 0
Jump on T0 = 1	JT0 addr	36	2	2	—	—	—	—	(T0) = 1
Jump on T0 = 0	JNT0 addr	26	2	2	—	—	—	—	(T0) = 0
Jump on T1 = 1	JT1 addr	56	2	2	—	—	—	—	(T1) = 1
Jump on T1 = 0	JNT1 addr	46	2	2	—	—	—	—	(T1) = 0
Jump on F0 = 1	JF0 addr	B6	2	2	—	—	—	—	(F0) = 1
Jump on F1 = 1	JF1 addr	76	2	2	—	—	—	—	(F1) = 1
Jump on timer flag	JTF addr	16	2	2	—	—	—	—	(TF) = 1
Jump on $\overline{INT}$ = 0	JNI addr	86	2	2	—	—	—	—	($\overline{INT}$) = 0
Jump on accumulator bit	JBr addr	%2	2	2	—	—	—	—	(Ar) = 1
Subroutine Instructions									
Jump to subroutine	CALL addr	%4	2	2	—	—	—	—	(Note 6)
Return	RET	83	1	2	—	—	—	—	(Note 7)
Return and restore status	RETR	93	1	2	*	*	*	—	(Note 8)
Flag Instructions									
Clear carry	CLR C	97	1	1	Z	—	—	—	(C) ← 0
Complement carry	CPL C	A7	1	1	CP	—	—	—	(C) ← ($\overline{C}$)
Clear Flag 0	CLR F0	85	1	1	—	—	Z	—	(F0) ← 0
Complement Flag 0	CPL F0	95	1	1	—	—	CP	—	(F0) ← ($\overline{F0}$)
Clear Flag 1	CLR F1	A5	1	1	—	—	—	Z	(F1) ← 0
Complement Flag 1	CPL F1	B5	1	1	—	—	—	CP	(F1) ← ($\overline{F1}$)

Table 2. OP Codes for Register Access

Mnemonic Rr	R0	R1	R2	R3	R4	R5	R6	R7
INC Rr	18	19	1A	1B	1C	1D	1E	1F
XCH A, Rr	28	29	2A	2B	2C	2D	2E	2F
ORL A, Rr	48	49	4A	4B	4C	4D	4E	4F
ANL A, Rr	58	59	5A	5B	5C	5D	5E	5F
ADD A, Rr	68	69	6A	6B	6C	6D	6E	6F
ADDC A, Rr	78	79	7A	7B	7C	7D	7E	7F
MOV Rr, A	A8	A9	AA	AB	AC	AD	AE	AF
MOV Rr, #data	B8	B9	BA	BB	BC	BD	BE	BF
DEC Rr	C8	C9	CA	CB	CC	CD	CE	CF
XRL A, Rr	D8	D9	DA	DB	DC	DD	DE	DF
DJNZ Rr, M	E8	E9	EA	EB	EC	ED	EE	EF
MOV A, Rr	F8	F9	FA	FB	FC	FD	FE	FF

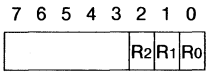


Table 3. OP Codes for Expander

Mnemonic Pp	P4	P3	P2	P1
MOVD A, Pp	0C	0D	0E	0F
MOVD Pp, A	3C	3D	3E	3F
ORLD Pp, A	8C	8D	8E	8F
ANLD Pp, A	9C	9D	9E	9F

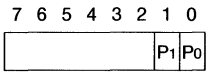
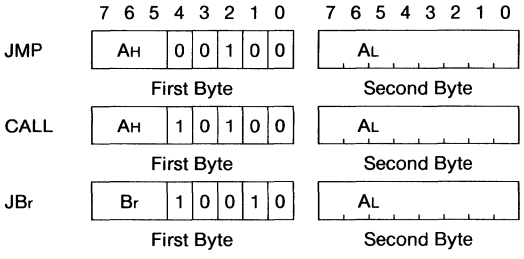


Table 4. OP Codes for JMP, CALL, and JBr Instructions



A_L: Address A_7 to A_0
A_H: Address A_{10}, A_9, A_8
B_r: r^{th} Bit on Accumulator

Notes:

1. Refer to Tables 1 and 2 for OP Code suffixes of "X"; refer to Table 3 for OP Code prefixes of "%".
2. Flag status:
   * = Set, or reset flag bit to the state it was in before instruction execution.
   z = Reset flag bit.
   CP = Complement flag bit.
3. The accumulator value is adjusted to form BCD digits following the binary addition of BCD number.
4. DJNZ R_r addr: $(R_r) - 1 \rightarrow (R_r)$
   if $(R_r) \neq 0$, add $\rightarrow$ $(PC_0$ to $PC_7)$.
   if $(R_r) = 0$, execute next instruction.
5. JMPP @A: $((A)) \rightarrow (PC_0$ to $PC_7)$
6. CALL addr
   $(PC_0$ to $PC_7) \rightarrow ((SP))$
   $(SP) + 1 \rightarrow (SP)$
   $(PC_8$ to $PC_{11})$, (MBF), $(PSW_4$ to $PSW_7) \rightarrow ((SP))$
   $(SP) + 1 \rightarrow (SP)$
   $A_L \rightarrow (PC_0$ to $PC_7)$
   $A_H \rightarrow (PC_8$ to $PC_{10})$
   MBF $\rightarrow (PC_{11})$
7. RET
   $(SP) - 1 \rightarrow (SP)$
   $((SP)_0$ to $(SP)_3) \rightarrow (PC)_8$ to $(PC)_{11})$
   $(SP) - 1 \rightarrow (SP)$
   $((SP)) \rightarrow (PC_0$ to $PC_7)$
8. RETR
   $(SP) - 1 \rightarrow (SP)$
   $((SP)_0$ to $(SP)_3 \rightarrow (PC_8$ to $PC_{11})$
   $((SP)_4$ to $(SP)_7 \rightarrow (PSW_4$ to $PSW_7)$
   $(SP) - 1 \rightarrow (SP)$
   $((SP)) \rightarrow (PC_0$ to $PC_7)$
   A_L : Lower 8 Bits of Address
   A_H : A_8, A_9, A_{10} of Address
   MBF: Memory Bank Flag

2

INSTRUCTION CODES

H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP		OUT (BSU, A)	ADD A, #	JMP 0 x x	EN 1		DEC A	INS (A, BUS)	IN A, P1	IN A, P2		MOVD A, P4	MOVD A, P5	MOVD A, P6	MOVD A, P7
1	INC @R0	INC @R1	JB0 addr	ADDC A, #	CALL 0 x x	DIS 1	JTF addr	INC A	INC R0	INC R1	INC R2	INC R3	INC R4	INC R5	INC R6	INC P7
2	XCH A, @R0	XCH A, @R1		MOV A, #	JMP 1 x x	EN TCNT1	JNT0 addr	CLR A	XCH A, R0	XCH A, R1	XCH A, R2	XCH A, R3	XCH A, R4	XCH A, R5	XCH A, R6	XCH A, R7
3	XCHD A, @R0	XCHD A, @R1	JB1 addr		CALL 1 x x	DIS TCNT1	JT0 addr	CPL A		OUTL P1, A	OUTL P2, A		MOVD P4, A	MOVD P5, A	MOVD P6, A	MOVD P7, A
4	ORL A, @R0	ORL A, @R1	MOV A, T	ORL A, #	JMP 2 x x	STRT CNT	JNT1 addr	SWAP A	ORL A, R0	ORL A, R1	ORL A, R2	ORL A, R3	ORL A, R4	ORL A, R5	OPL A, R6	ORL A, R7
5	ANL A, @R0	ANL A, @R1	JB2 addr	ANL A, #	CALL 2 x x	STRT T	JT1 addr	DA A	ANL A, R0	ANL A, R1	ANL A, R2	ANL A, R3	ANL A, R4	ANL A, R5	ANL A, R6	ANL A, R7
6	ADD A, @R0	ADD A, @R1	MOV T, A		JMP 3 x x	STOP TCNT		RRC A	ADD A, R0	ADD A, R1	ADD A, R2	ADD A, R3	ADD A, R4	ADD A, R5	ADD A, R6	ADD A, R7
7	ADDC A, @R0	ADDC A, @R1	JB3 addr		CALL 3 x x	ENT0 CLK	JF1 addr	RR A	ADDC A, R0	ADDC A, R1	ADDC A, R2	ADDC A, R3	ADDC A, R4	ADDC A, R5	ADDC A, R6	ADDC A, R7
8	MOVX (A, @ R0)	MOVX (A, @ R1)		RET	JMP 4 x x	CLR F0	JNI addr		ORL (BUS, #)	ORL P1, #	ORL P2, #		ORLD P4, A	ORLD P5, A	ORLD P6, A	ORLD P7, A
9	MOVX @R0, A	MOVX @R1, A	JB4 addr	RETR	CALL 4 x x	CPL F0	JNZ addr	CLR C	ANL (BUS, #)	ANL P1, #	ANL P2, #		ANLD P4, A	ANLD P5, A	ANLD P6, A	ANLD P7, A
A	MOV @R0, A	MOV @R1, A		MOVP A, @A	JMP 5 x x	CLR F1		CPL C	MOV R0, A	MOV R1, A	MOV R2, A	MOV R3, A	MOV R4, A	MOV R5, A	MOV R6, A	MOV R7, A
B	MOV @R0, #	MOV @R1, #	JB5 addr	JMPP @A	CALL 5 x x	CPL F1	JF0 addr		MOV R0, #	MOV R1, #	MOV R2, #	MOV R3, #	MOV R4, #	MOV R5, #	MOV R6, #	MOV R7, #
C					JMP 6 x x	SEL RB0	JZ addr	MOV A, PSW	DEC R0	DEC R1	DEC R2	DEC R3	DEC R4	DEC R5	DEC R6	DEC R7
D	XRL A, @R0	XRL A, @R1	JB6 addr	XRL A, #	CALL 6 x x	SEL RB1	JNIBF addr	MOV PSW, A	XRL A, R0	XRL A, R1	XRL A, R2	XRL A, R3	XRL A, R4	XRL A, R5	XRL A, R6	XRL A, R7
E				MOVP3 A, @A	JMP 7 x x	SEL MB0	JNC addr	RL A	DJNZ R0, M	DJNZ R1, M	DJNZ R2, M	DJNZ R3, M	DJNZ R4, M	DJNZ R5, M	DJNZ R6, addr	DJNZ R7, M
F	MOV A, @R0	MOV A, @R1	JB7 addr		CALL 7 x x	SEL MB1	JC addr	RLC A	MOV A, R0	MOV A, R1	MOV A, R2	MOV A, R3	MOV A, R4	MOV A, R5	MOV A, R6	MOV A, R7

Legend:

\# Immediate data

= 1 Byte, 1 Cycle Instruction

= 1 Byte, 2 Cycle Instruction

= 2 Byte, 2 Cycle Instruction

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}, V_{DD}	V_{SS} − 0.3 to V_{SS} + 7	V
Input Voltage	V_{IN}	V_{SS} − 0.3 to V_{SS} + 7	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	1.5	W

Note:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}, V_{DD}	4.5	5.0	5.5	V
	V_{SS}		0		V
Operating Temperature	T_A	0		+70	°C

DC CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = V_{DD} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	Applicable Pin/Device	Value		Unit	Test Conditions
			Min	Max		
Input Low Voltage	V_{IL}	All Except XTAL1, XTAL2, $\overline{RESET}$	-0.3	0.8	V	
	V_{IL1}	XTAL1, XTAL2, $\overline{RESET}$	-0.3	0.6	V	
Input High Voltage	V_{IH}	All Except XTAL1, XTAL2, $\overline{RESET}$	2.0	V_{CC}	V	
	V_{IH1}	XTAL1, XTAL2, $\overline{RESET}$	3.8	V_{CC}	V	
Output Low Voltage	V_{OL}	BUS		0.45	V	I_{OL} = 2.0mA
	V_{OL1}	$\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE		0.45	V	I_{OL} = 2.0mA
	V_{OL2}	PROG		0.45	V	I_{OL} = 1.0mA
	V_{OL3}	All Other Outputs		0.45	V	I_{OL} = 1.6mA
Output High Voltage	V_{OH}	BUS	2.4		V	I_{OH} = -400μA
	V_{OH1}	$\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE	2.4		V	I_{OH} = -100μA
	V_{OH2}	All Other Outputs	2.4		V	I_{OH} = -50μA
Input Leakage Current	I_{LI}	T1, $\overline{INT}$		±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
	I_{LI1}	P10–P17, P20–P27, EA, $\overline{SS}$		-500	μA	V_{SS} + 0.45V ≤ $V_{IN} \leq V_{CC}$
Output Leakage Current	I_{LO}	BUS, T0		±10	μA	V_{SS} + 0.45V ≤ $V_{IN} \leq V_{CC}$, In High-Z state
V_{DD} Supply Current	I_{DD}	V_{DD}		50	mA	
Total Supply Current	I_{CC} + I_{DD}	V_{CC}, V_{DD}		170	mA	

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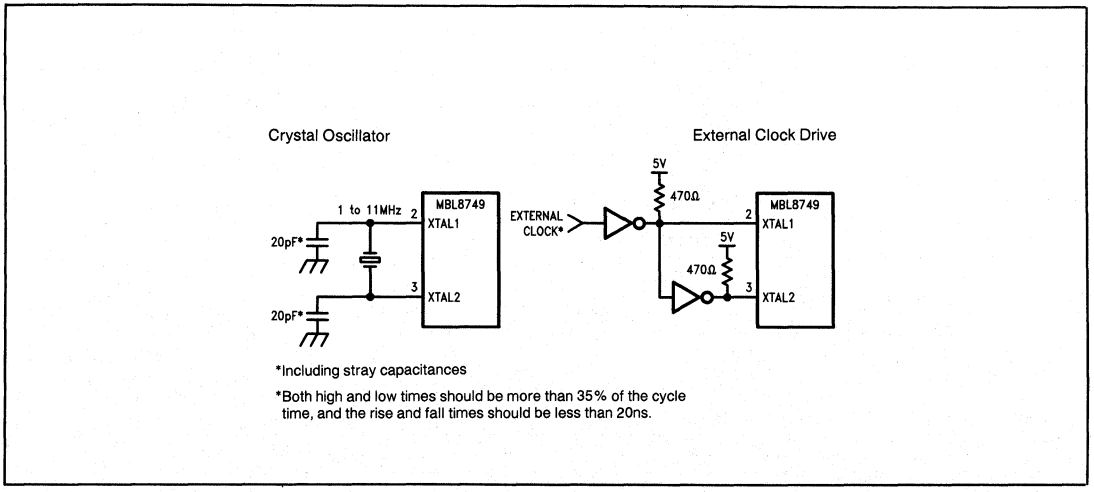
DC CHARACTERISTICS (Programming Mode)

(T_A = 25 ±5°C, V_{CC} = 5V ±5%, V_{DD} = 21 ±0.5V or 5V ±5%)

Parameter	Symbol	Value		Unit
		Min	Max	
V_{DD} Program Voltage High Level	V_{DDH}	20.5	21.5	V
V_{DD} Program Voltage Low Level	V_{DDL}	4.75	5.25	
PROG Program Voltage High Level	V_{PH}	17.5	18.5	V
PROG Program Voltage Low Level	V_{PL}	—	0.2	
EA Program/Verify Voltage High Level	V_{EAH}	17.5	18.5	V
EA Program/Verify Voltage Low Level	V_{EAL}	—	5.25	
V_{DD} High Voltage Supply Current	I_{DD}	—	30.0	mA
PROG High Voltage Supply Current	I_{PROG}	—	16.0	
EA High Voltage Supply Current	I_{EA}	—	1.0	

Notes:
1. High Level Voltage (V_{DDH}, V_{PH}) should not be applied to V_{DD} and PROG pins unless V_{CC} = 5V ±5% and EA = 18V ±0.5V.
2. V_{DD}, PROG, and EA should not exceed the above specified range, including overshoot and undershoot.

Oscillator Circuits



*Including stray capacitances

*Both high and low times should be more than 35% of the cycle time, and the rise and fall times should be less than 20ns.

AC CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ±10%, V_{SS} = 0V)

Parameter	Symbol	Value (MBL8749H)		Value (MBL8749N)		Unit	Test Conditons
		Min	Max	Min	Max		
ALE Pulse Width	t_{LL}	150		410		ns	Note 1
Address Setup Time (to ALE↓)	t_{AL}	70		230		ns	
Address Hold Time (from ALE↓)	t_{LA}	50		120		ns	
$\overline{RD}$ & $\overline{WR}$ Pulse Width	t_{CC1}	480		1050		ns	
$\overline{PSEN}$ Pulse Width	t_{CC2}	350		800		ns	
Data Setup Time (to $\overline{WR}$↑)	t_{DW}	390		880		ns	
Data Hold Time (from $\overline{WR}$↑)	t_{WD}	40		120		ns	Note 2
Data Hold Time (from $\overline{RD}$↑, $\overline{PSEN}$↑)	t_{DR}	0	110	0	220	ns	Note 1
Data Delay Time (from $\overline{RD}$↓)	t_{RD1}		350		800	ns	
Data Delay Time (from $\overline{PSEN}$↓)	t_{RD2}		210		550	ns	
Address Setup Time (to $\overline{WR}$↓)	t_{AW}	310		680		ns	
Data Delay Time ($\overline{RD}$)	t_{AD1}		760		1590	ns	
Data Delay Time ($\overline{PSEN}$)	t_{AD2}		480		1090	ns	
Address Floating Time (to $\overline{RD}$↓, $\overline{WR}$↓)	t_{AFC1}	140		290		ns	
Address Floating Time (to $\overline{PSEN}$↓)	t_{AFC2}	10		40		ns	
$\overline{RD}$ & $\overline{WR}$ Output Delay Time (from ALE↓)	t_{LAFC1}	200		420		ns	
PSEN Output Delay Time (from ALE↓)	t_{LAFC2}	60		170		ns	
ALE Delay Time (from $\overline{RD}$↑, $\overline{WR}$↑, PROG↑)	t_{CA1}	50		120		ns	
ALE Delay Time (from $\overline{PSEN}$↑)	t_{CA2}	320		620		ns	
Port Control Setup Time (to PROG↓)	t_{CP}	100		250		ns	
Port Control Hold Time (from PROG↓)	t_{PC}	160		460		ns	
Port 2 Input Data Delay Time (from PROG↓)	t_{PR}		700		1380	ns	
Port 2 Input Data Hold Time (from PROG↑)	t_{PF}	0	140	0	250	ns	
Output Data Setup Time (to PROG↑)	t_{DP}	400		850		ns	
Output Data Hold Time (from PROG↑)	t_{PD}	90		200		ns	
PROG Pulse Width	t_{PP}	700		1500		ns	
Port 2 I/O Data Setup Time (to ALE↑)	t_{PL}	160		460		ns	
Port 2 I/O Data Hold Time (from ALE↑)	t_{LP}	40		80		ns	
Port Data Output Time (from ALE↓)	t_{PV}		510		850	ns	
Cycle Time	t_{CY}	1.36		2.5		μs	
T0 Output Frequency	t_{OPRR}	270		500		ns	

Notes:
1. Load Conditions: BUS C_L = 150pF, Other Outputs C_L = 80pF, 1 TTL
2. Load Conditions C_L = 20pF, High impedance

↓ Falling edge
↑ Rising edge

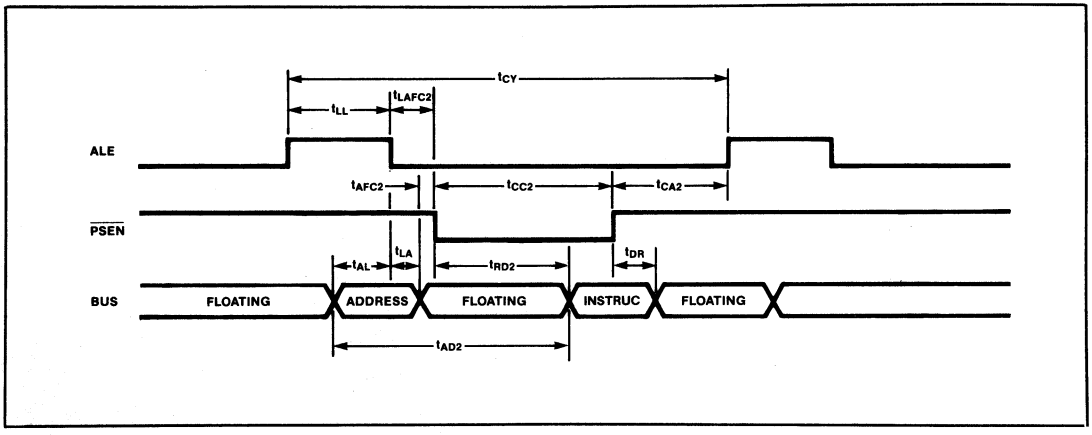
AC CHARACTERISTICS (Programming Mode)

(T_A = 25 ±5°C, V_{CC} = 5V ±5%, V_{DD} = 21V ±0.5V or 5V ±5%)

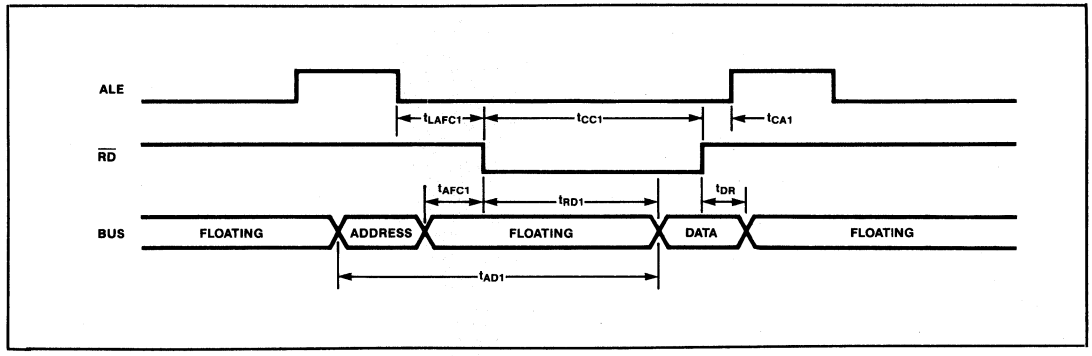
Parameter	Symbol	Value	
		Min	Max
Address setup time (before $\overline{\text{RESET}}$↑)	t_{AW}	$4 \cdot t_{CY}$	—
Address hold time (after $\overline{\text{RESET}}$↑)	t_{WA}	$4 \cdot t_{CY}$	—
Input data setup time (before PROG↑)	t_{DW}	$4 \cdot t_{CY}$	—
Input data hold time (after PROG↓)	t_{WD}	$4 \cdot t_{CY}$	—
$\overline{\text{RESET}}$ hold time (after EA↓)	t_{PH}	$4 \cdot t_{CY}$	—
V_{DD} setup time (before PROG↑)	t_{VDDW}	$4 \cdot t_{CY}$	—
V_{DD} hold time (after PROG↓)	t_{VDDH}	0	—
Program Pulse width	t_{PW}	50 ms	60 ms
T0 setup time (before $\overline{\text{RESET}}$↑)	t_{TW}	$4 \cdot t_{CY}$	—
T0 hold time (after V_{DD}↓)	t_{WT}	$4 \cdot t_{CY}$	—
Data output delay time (after T0↑)	t_{D0}	—	$4 \cdot t_{CY}$
RESET pulse width (to latch Address)	t_{WW}	$4 \cdot t_{CY}$	—
V_{DD} and PROG rise/fall time	t_r, t_f	0.5μs	2.0μs
MPU cycle time	t_{CY}	5.0μs	—
$\overline{\text{RESET}}$ setup time (before EA↑)	t_{RE}	$4 \cdot t_{CY}$	—
EA setup time (before $\overline{\text{RESET}}$↑)	t_{EA}	10 ms	—

TIMING DIAGRAMS

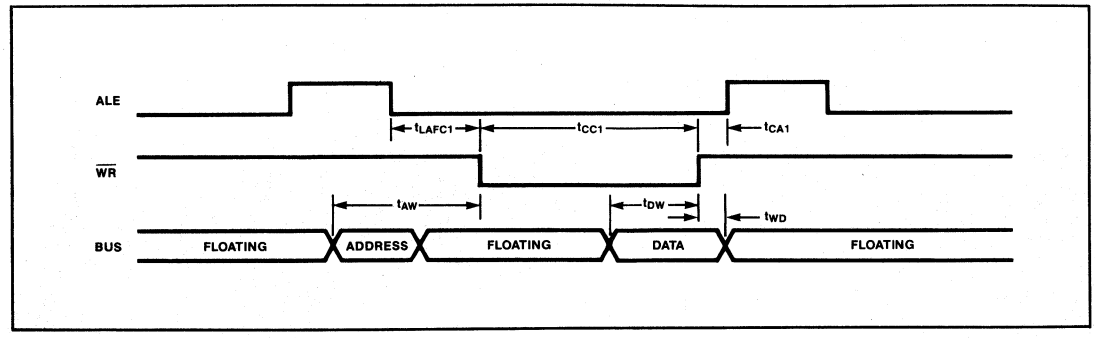
External Program Memory Operations (Instruction Fetch)



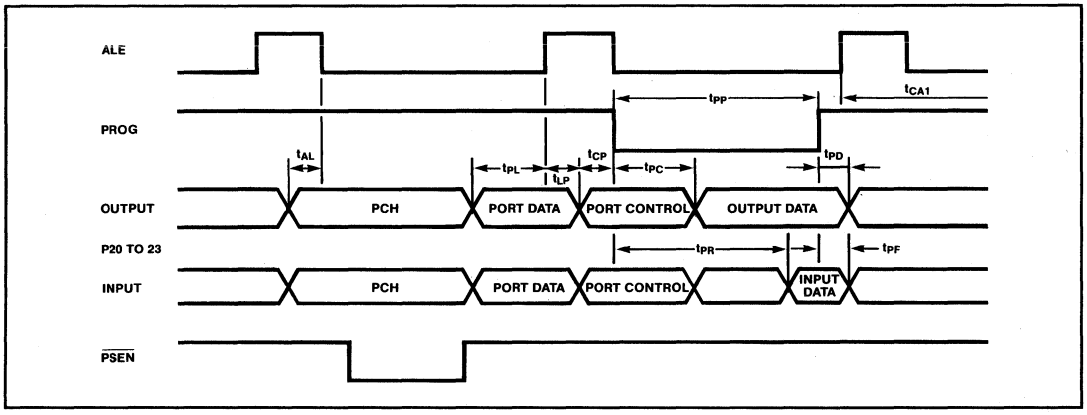
External Data Memory Read Operation



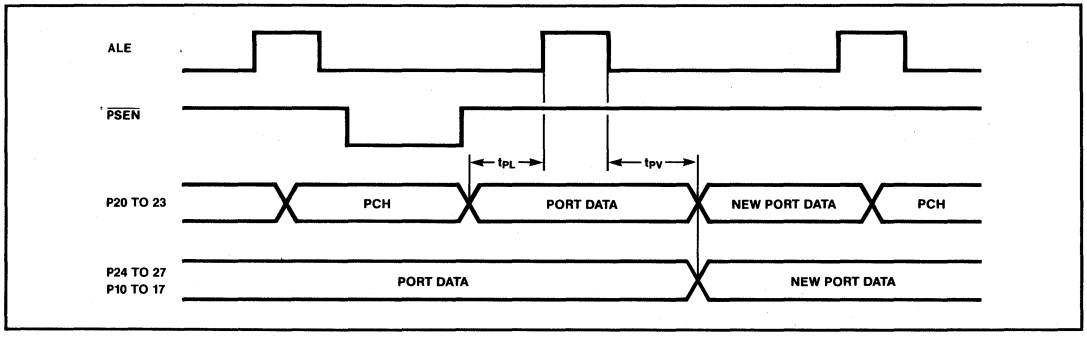
External Data Memory Write Operation



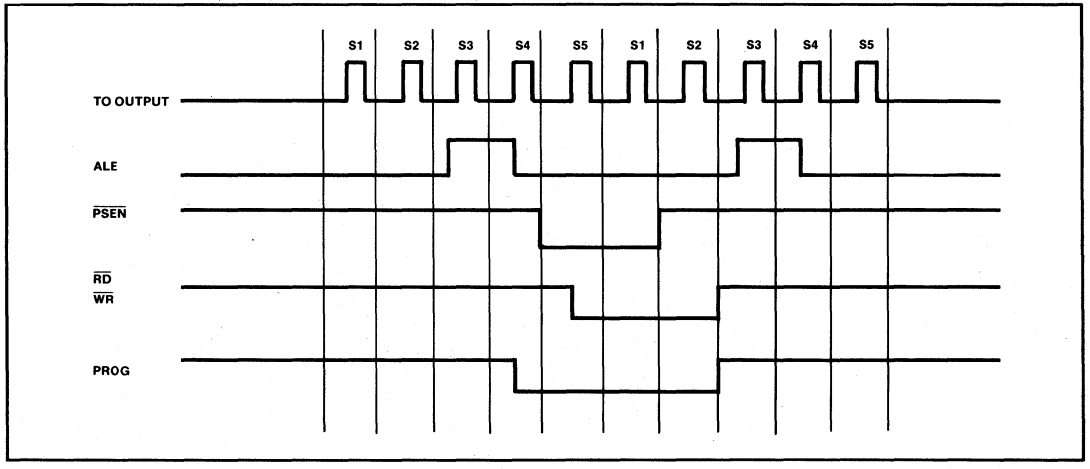
TIMING DIAGRAMS (continued)
Four Low-Order Bits of Port 2 When Expander Port And External Program Memory Are Used



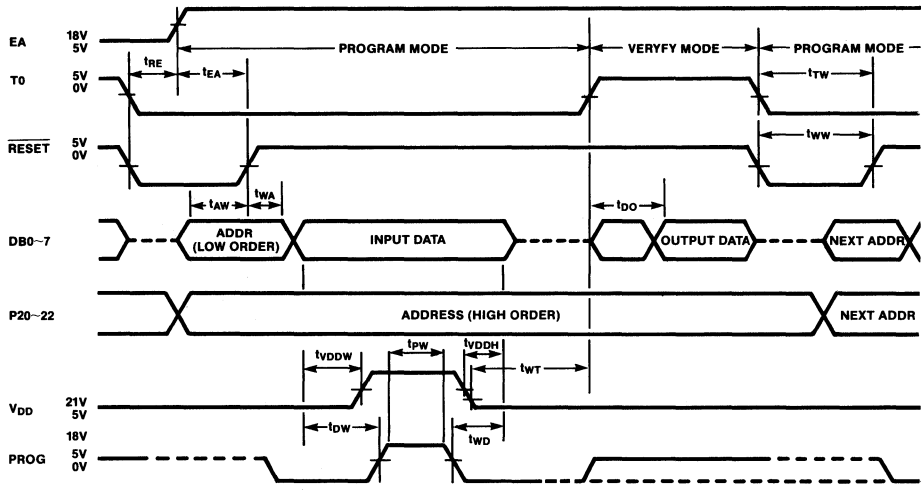
I/O Port Output Timing



Clock Output Timing



TIMING DIAGRAM (Programming the EPROM)



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PACKAGE DIMENSIONS

40-Lead Ceramic (Metal Seal)
Dual In-Line Package
(Case No.: DIP-40C-A04)