

BIPOLAR CLOCK GENERATOR AND READY INTERFACE FOR MBL 80286 PROCESSORS

The Fujitsu MBL 82284 is a clock generator/driver which provides clock signals for MBL 80286 processors and support components. It also contains logic to supply **READY** to the CPU from either asynchronous or synchronous sources and synchronous **RESET** from an asynchronous input with hysteresis.

- Generates System Clock for MBL 80286 Processors
- Uses Crystal or TTL Signal for Frequency Source
- Provides Local **READY** and Multibus* **READY** Synchronization
- Generates System Reset Output from Schmitt Trigger Input
- Single +5V Power Supply
- Two Package Options:
 - 18-pin Cerdip (Suffix: CZ)
 - 18-pin Plastic DIP (Suffix: P)

Fig. 1 – BLOCK DIAGRAM

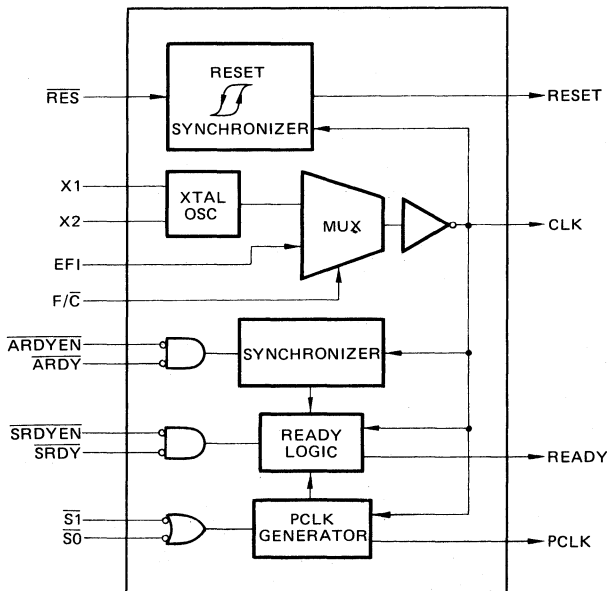
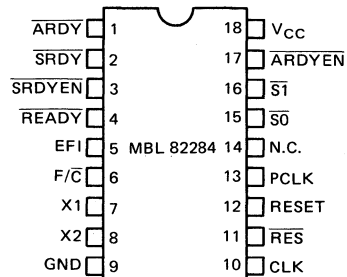


Fig. 2 – PIN CONFIGURATION



PIN DESCRIPTION

The following pin function descriptions are for the MBL 82284 clock generator.

Table 1 – PIN DESCRIPTION

Symbol	Type	Name and Function
CLK	O	System Clock is the signal used by the processor and support devices which must be synchronous with the processor. The frequency of the CLK output has twice the desired internal processor clock frequency. CLK can drive both TTL and MOS level inputs.
F/C	I	Frequency/Crystal Select is a strapping option to select the source for the CLK output. When F/C is strapped LOW, the internal crystal oscillator drives CLK. When F/C is strapped HIGH, the EFI input drives the CLK output.
X1, X2	I	Crystal In are the pins to which a parallel resonant fundamental mode crystal is attached for the internal oscillator. When F/C is LOW, the internal oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the desired internal processor clock frequency.
EFI	I	External Frequency In drives CLK when the F/C input is strapped HIGH. The EFI input frequency must be twice the desired internal processor clock frequency.
PCLK	O	Peripheral Clock is an output which provides a 50% duty cycle clock with 1/2 the frequency of CLK. PCLK will be in phase with the internal processor clock following the first bus cycle after the processor has been reset.
ARDYEN	I	Asynchronous Ready Enable is an active LOW input which qualifies the ARDY input. ARDYEN selects ARDY as the source of ready for the current bus cycle. Inputs to ARDYEN may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
ARDY	I	Asynchronous Ready is an active LOW input used to terminate the current bus cycle. The ARDY input is qualified by ARDYEN. Inputs to ARDY may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
SRDYEN	I	Synchronous Ready Enable is an active LOW input which qualifies SRDY. SRDYEN selects SRDY as the source for READY to the CPU for the current bus cycle. Setup and hold times must be satisfied for proper operation.
SRDY	I	Synchronous Ready is an active LOW input used to terminate the current bus cycle. The SRDY input is qualified by the SRDYEN input. Setup and hold times must be satisfied for proper operation.
READY	O	Ready is an active LOW output which signals the current bus cycle is to be completed. The SRDY, SRDYEN, ARDY, ARDYEN, S1, S0 and RES inputs control READY as explained later in the READY generator section. READY is an open collector output requiring an external 910Ω pullup resistor.
S0, S1	I	Status inputs prepare the MBL 82284 for a subsequent bus cycle. S0 and S1 synchronize PCLK to the internal processor clock and control READY. These inputs have pullup resistors to keep them HIGH if nothing is driving them. Setup and hold times must be satisfied for proper operation.
RESET	O	Reset is an active HIGH output which is derived from the RES input. RESET is used to force the system into an initial state. When RESET is active, READY will be active (LOW).
RES	I	Reset In is an active LOW input which generates the system reset signal RESET. Signals to RES may be applied asynchronously to CLK. A Schmitt trigger input is provided on RES, so that an RC circuit can be used to provide a time delay. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
V _{CC}		System Power: +5V power supply.
GND		System Ground: 0 volts.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The MBL 82284 generates the clock, ready, and reset signals required for MBL 80286 processors and support components. The MBL 82284 is packaged in an 18-pin DIP and contains a crystal controlled oscillator, MOS clock generator, peripheral clock generator, Multibus ready synchronization logic and system reset generation logic.

CLOCK GENERATOR

The CLK output provides the basic timing control for an MBL 80286 system. CLK has output characteristics sufficient to drive MOS devices. CLK is generated by either an internal crystal oscillator or an external source as selected by the F/C strapping option. When F/C is LOW, the crystal oscillator drives the CLK output. When F/C is HIGH, the EFI input drives the CLK output.

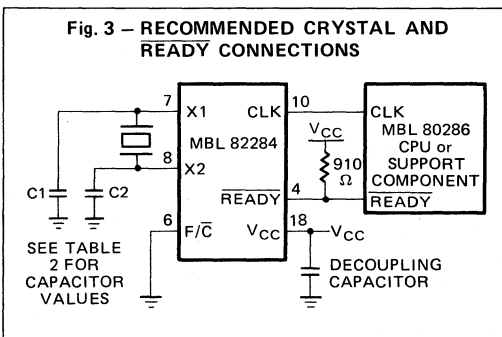
The MBL 82284 provides a second clock output (PCLK) for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and TTL output drive characteristics. PCLK is normally synchronized to the internal processor clock.

After reset, the PCLK signal may be out of phase with the internal processor clock. The S1 and S0 signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its HIGH time beyond one system clock (see waveforms). PCLK is forced HIGH whenever either S0 or S1 were active (LOW) for the two previous CLK cycles. PCLK continues to oscillate when both S0 and S1 are HIGH.

Since the phase of the internal processor clock will not change except during reset, the phase of PCLK will not change except during the first bus cycle after reset.

OSCILLATOR

The oscillator circuit of the MBL 82284 is a linear Pierce oscillator which requires an external parallel resonant, fundamental mode, crystal. The output of the oscillator



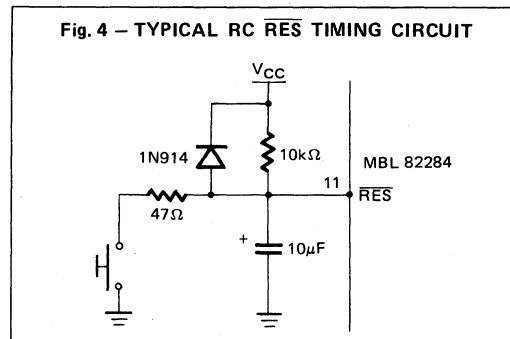
is internally buffered. The crystal frequency chosen should be twice the required internal processor clock frequency. The crystal should have a typical load capacitance of 32 pF.

X1 and X2 are the oscillator crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in Table 2. The sum of the board capacitance and loading capacitance should equal the values shown. It is advisable to limit stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) to less than 10 pF between the X1 and X2 pins. Decouple VCC and GND as close to the MBL 82284 as possible.

RESET OPERATION

The reset logic provides the RESET output to force the system into a known, initial state. When the RES input is active (LOW), the RESET output becomes active (HIGH). RES is synchronized internally at the falling edge of CLK before generating the RESET output (see waveforms). Synchronization of the RES input introduces a one or two CLK delay before affecting the RESET output.

At power up, a system does not have a stable VCC and CLK. To prevent spurious activity, RES should be asserted until VCC and CLK stabilize at their operating values. MBL 80286 processors and support components also require their RESET inputs be HIGH a minimum of 16 CLK cycles. An RC network, as shown in Fig. 4, will keep RES LOW long enough to satisfy both needs.



A Schmitt trigger input with hysteresis on RES assures a single transition of RESET with an RC circuit on RES. The hysteresis separates the input voltage level at which the circuit output switches between HIGH to LOW from the input voltage level at which the circuit output switches between LOW to HIGH. The RES HIGH to LOW input transition voltage is lower than the RES LOW to HIGH input transition voltage. As long as the slope of the RES input voltage remains in the same direction (increasing

or decreasing) around the $\overline{\text{RES}}$ input transition voltage, the RESET output will make a single transition.

READY OPERATION

The MBL 82284 accepts two ready sources for the system ready signal which terminates the current bus cycle. Either a synchronous (SRDY) or asynchronous ready (ARDY) source may be used. Each ready input has an enable (SRDYEN and ARDYEN) for selecting the type of ready source required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.

$\overline{\text{READY}}$ is enabled (LOW), if either $\overline{\text{SRDY}} + \overline{\text{SRDYEN}} = 0$ or $\overline{\text{ARDY}} + \overline{\text{ARDYEN}} = 0$ when sampled by the MBL 82284 $\overline{\text{READY}}$ generation logic. $\overline{\text{READY}}$ will remain active for at least two CLK cycles.

The $\overline{\text{READY}}$ output has an open-collector driver allowing other ready circuits to be wire or'ed with it, as shown in Fig. 3. The $\overline{\text{READY}}$ signal of an MBL 80286 system requires an external $910\ \Omega \pm 5\%$ pull-up resistor. To force the $\overline{\text{READY}}$ signal inactive (HIGH) at the start of a bus

cycle, the $\overline{\text{READY}}$ output floats when either $\overline{\text{S1}}$ or $\overline{\text{S0}}$ are sampled LOW at the falling edge of CLK. Two system clock periods are allowed for the pull-up resistor to pull the $\overline{\text{READY}}$ signal to V_{IH} . When RESET is active, $\overline{\text{READY}}$ is forced active one CLK later (see waveforms).

Fig. 5 illustrates the operation of $\overline{\text{SRDY}}$ and $\overline{\text{SRDYEN}}$. These inputs are sampled on the falling edge of CLK when $\overline{\text{S1}}$ and $\overline{\text{S0}}$ are inactive and PCLK is HIGH. $\overline{\text{READY}}$ is forced active when both $\overline{\text{SRDY}}$ and $\overline{\text{SRDYEN}}$ are sampled as LOW.

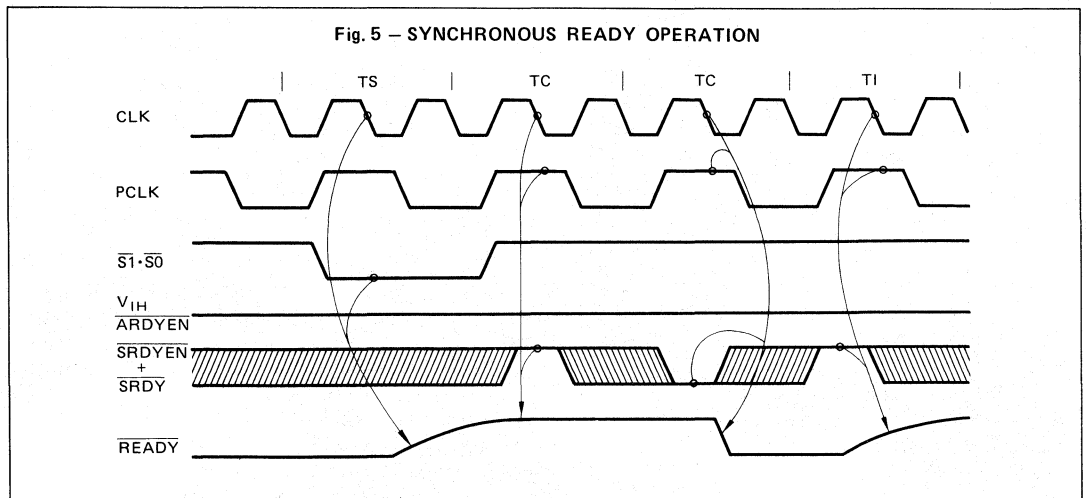
Fig. 6 shows the operation of $\overline{\text{ARDY}}$ and $\overline{\text{ARDYEN}}$. These inputs are sampled by an internal synchronizer at each falling edge of CLK. The output of the synchronizer is then sampled when PCLK is HIGH. If the synchronizer resolved both the $\overline{\text{ARDY}}$ and $\overline{\text{ARDYEN}}$ have been resolved as active, the $\overline{\text{SRDY}}$ and $\overline{\text{SRDYEN}}$ inputs are ignored. Either $\overline{\text{ARDY}}$ or $\overline{\text{ARDYEN}}$ must be HIGH at end of TS (see Fig. 6).

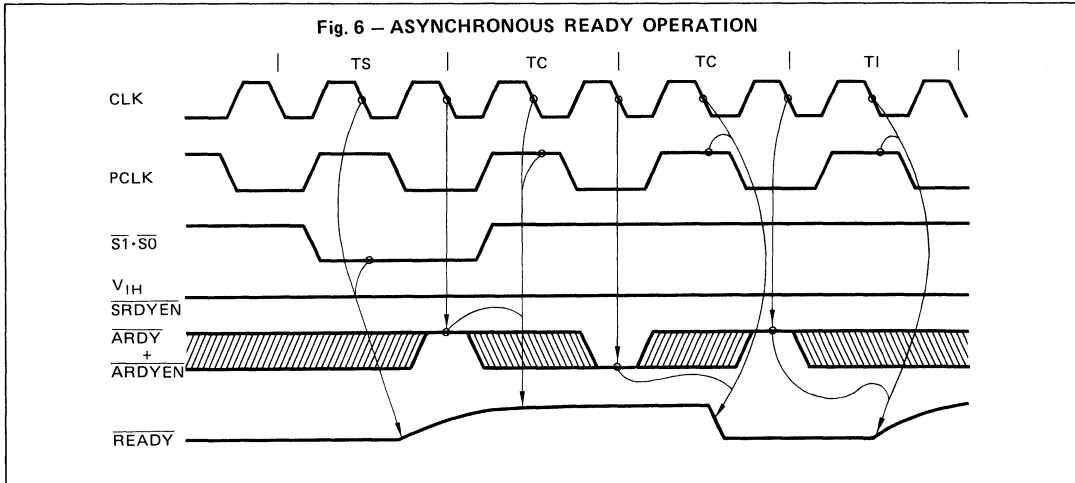
$\overline{\text{READY}}$ remains active until either $\overline{\text{S1}}$ or $\overline{\text{S0}}$ are sampled LOW, or the ready inputs are sampled as inactive.

Table 2 – MBL 82284 CRYSTAL LOADING CAPACITANCE VALUES

Crystal Frequency	C1 Capacitance (pin 7)	C2 Capacitance (pin 8)
1 to 8 MHz	60 pF	40 pF
8 to 16 MHz	25 pF	15 pF

NOTE: Capacitance values must include stray board capacitance.





ABSOLUTE MAXIMUM RATINGS*

- Temperature Under Bias 0°C to 70°C
- Storage Temperature -65°C to +150°C
- All Output and Supply Voltages -0.5V to +7V
- All Input Voltages -1.0V to +5.5V
- Power Dissipation 1 Watt

***NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS ($V_{CC} = 5V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$)

Symbol	Parameter	MBL 82284-6 (6 MHz)		MBL 82284-8 (8 MHz)		Unit	Test Condition
		Min	Max	Min	Max		
V_{IL}	Input LOW Voltage		0.8		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		2.0		V	
V_{IHR}	RES and EFI Input HIGH Voltage	2.6		2.6		V	
V_{HYS}	RES Input Hysteresis	0.25		0.25		V	
V_{OL}	RESET, PCLK Output LOW Voltage		0.45		0.45	V	$I_{OL} = 5mA$
V_{OH}	RESET, PCLK Output HIGH Voltage	2.4		2.4		V	$I_{OH} = -1mA$
V_{OLR}	READY Output LOW Voltage		0.45		0.45	V	$I_{OL} = 7mA$
V_{OLC}	CLK Output LOW Voltage		0.45		0.45	V	$I_{OL} = 5mA$
V_{OHC}	CLK Output HIGH Voltage	4.0		4.0		V	$I_{OH} = -800\mu A$
V_C	Input Forward Clamp Voltage		-1.0		-1.0	V	$I_C = -5mA$
I_F	Forward Input Current		-0.5		-0.5	mA	$V_F = 0.45V$
I_R	Reverse Input Current		50		50	μA	$V_R = V_{CC}$
I_{CC}	Power Supply Current		145		145	mA	
C_I	Input Capacitance		10		10	pF	$F_C = 1MHz$

A.C. CHARACTERISTICS ($V_{CC} = 5V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$)

AC timings are referenced to 0.8V and 2.0V points of signals as illustrated in datasheet waveforms, unless otherwise noted.

Symbol	Parameter	MBL 82284-6 (6 MHz)		MBL 82284-8 (8 MHz)		Unit	Test Condition
		Min	Max	Min	Max		
1	EFI to CLK Delay		35		30	ns	at 1.5V Note 1
2	EFI LOW Time	40		25		ns	at 1.5V Note 1, Note 7
3	EFI HIGH Time	35		25		ns	at 1.5V Note 1, Note 7
4	CLK Period	83	500	62	500	ns	
5	CLK LOW Time	20		15		ns	at 1.0V Note 1, Note 2, 8
6	CLK HIGH Time	25		25		ns	at 3.6V Note 1, Note 2, 8
7	CLK Rise Time		10		10	ns	1.0V to 3.6V Note 1
8	CLK Fall Time		10		10	ns	3.6V to 1.0V Note 1
9	Status Setup Time	28		22		ns	Note 1
10	Status Hold Time	1		1		ns	Note 1
11	SRDY or SRDYEN Setup Time	25		15		ns	Note 1
12	SRDY or SRDYEN Hold Time	0		0		ns	Note 1
13	ARDY or ARDYEN Setup Time	5		0		ns	Note 1, Note 3
14	ARDY or ARDYEN Hold Time	30		30		ns	Note 1, Note 3
15	RES Setup Time	25		20		ns	Note 1, Note 3
16	RES Hold Time	10		10		ns	Note 1, Note 3
17	READY Inactive Delay	5		5		ns	at 0.8V Note 4
18	READY Active Delay	0	33	0	24	ns	at 0.8V Note 4
19	PCLK Delay	0	45	0	45	ns	Note 5
20	RESET Delay	5	50	5	34	ns	Note 5
21	PCLK LOW Time	t4-20		t4-20		ns	Note 5, Note 6
22	PCLK HIGH Time	t4-20		t4-20		ns	Note 5, Note 6

NOTE 1: CLK loading: $C_L = 150pF$.

NOTE 2: With the internal crystal oscillator using recommended crystal and capacitive loading; or with the EFI input meeting specifications t_2 , and t_3 . Use a parallel-resonant, fundamental mode crystal. The recommended crystal loading for CLK frequencies of 8-16MHz are 25pF from pin X1 to ground, and 15pF from pin X2 to ground. These recommended values are $\pm 5pF$ and include all stray capacitance, Decouple V_{CC} and GND as close to the MBL 82284 as possible.

NOTE 3: This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at specific CLK edge.

NOTE 4: READY loading: $I_{OL} = 7mA$, $C_L = 150pF$. In system application, use $910 \Omega \pm 5\%$ pullup resistor to meet MBL 80286-8 and 80286-6 timing requirements.

NOTE 5: PCLK and RESET loading: $C_L = 75pF$. PCLK also has 750Ω pullup.

NOTE 6: t4 refers to any allowable CLK period.

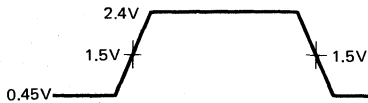
NOTE 7: When driving the MBL 82284 with EFI, provide minimum EFI HIGH and LOW times as follows:

CLK Output Frequency:	8MHz CLK	12MHz CLK	16MHz CLK*
Min. required EFI HIGH time	52ns	35ns	25ns
Min. required EFI LOW time	52ns	40ns	25ns

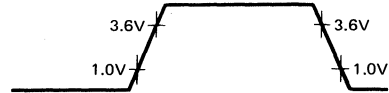
*At CLK frequencies above 12MHz, CLK output HIGH and LOW times are guaranteed only when using crystal with recommended capacitive loading per Table 2, *not* when driving component from EFI. All features of the MBL 82284 remain functional whether EFI or crystal is used to drive the MBL 82284.

NOTE 8: When using crystal (with recommended capacitive loading per Table 2) appropriate for speed of MBL 80286, CLK output HIGH and LOW times guaranteed to meet MBL 80286 requirements.

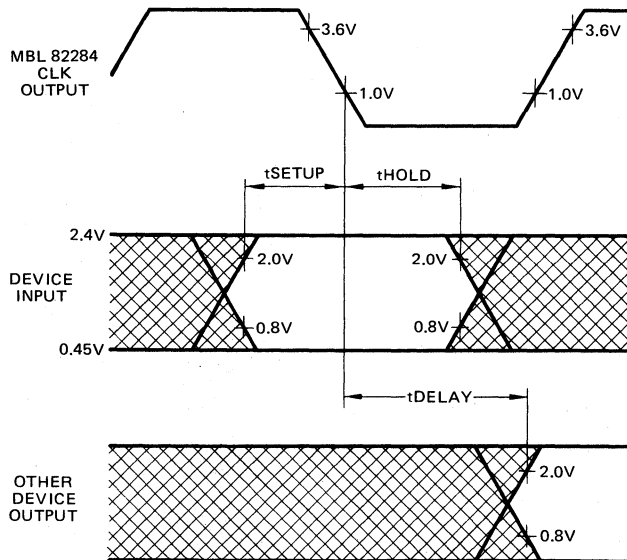
NOTE 9: EFI Drive and Measurement Points



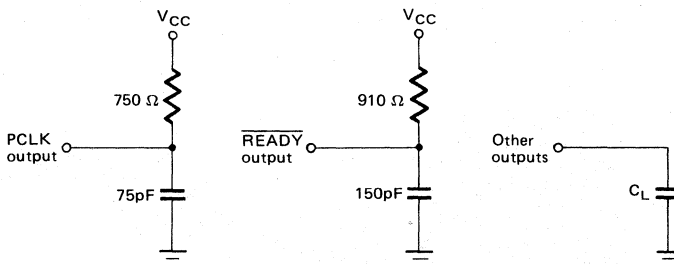
NOTE 10: CLK Output Measurement Points



NOTE 11: AC Setup, Hold and Delay Time Measurement — General

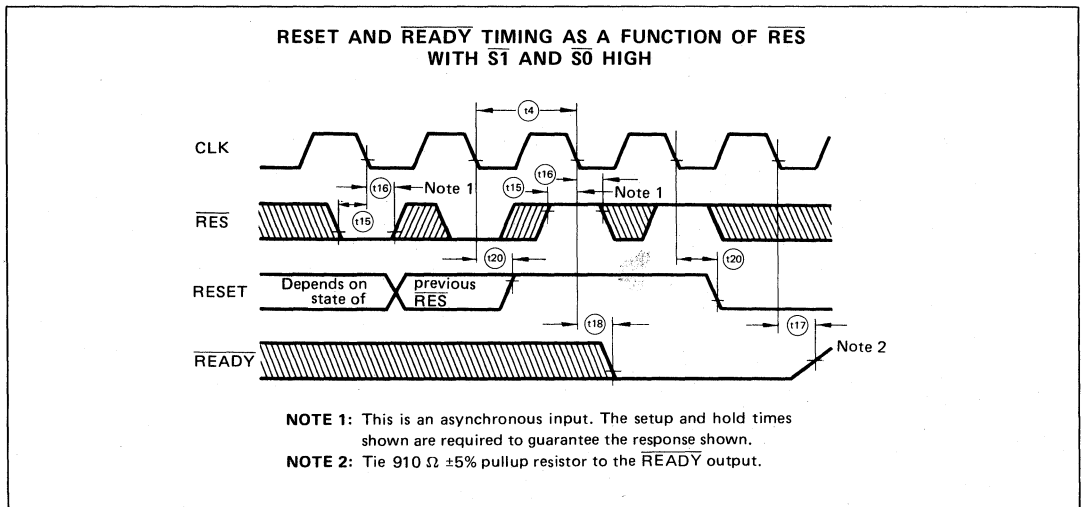
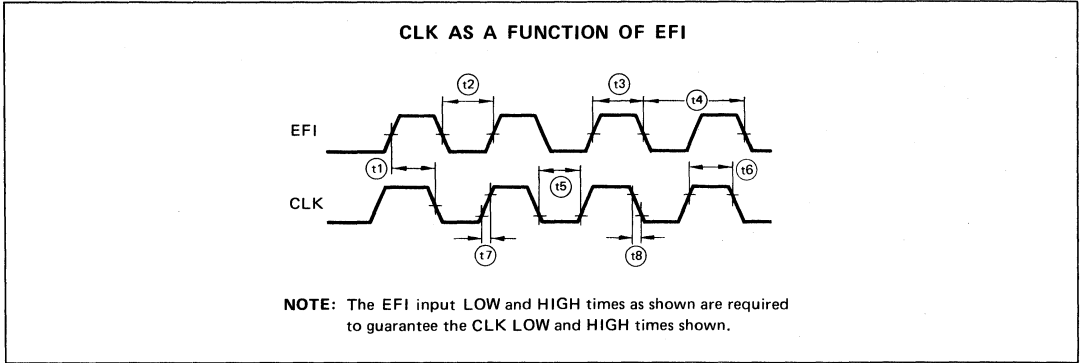


NOTE 12: AC Test Loading on Outputs

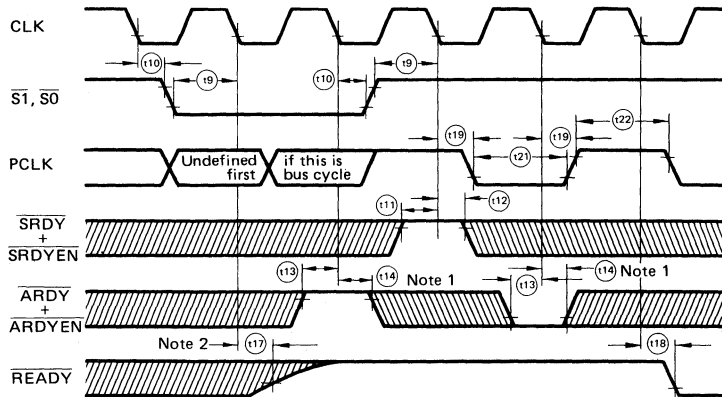




WAVEFORMS



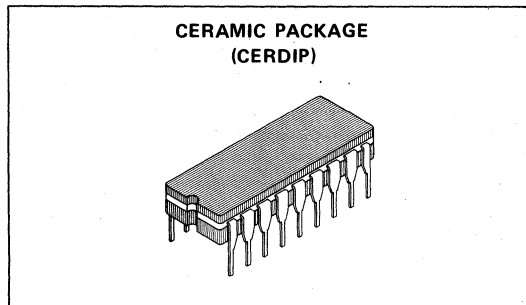
READY AND PCLK TIMING WITH RES HIGH



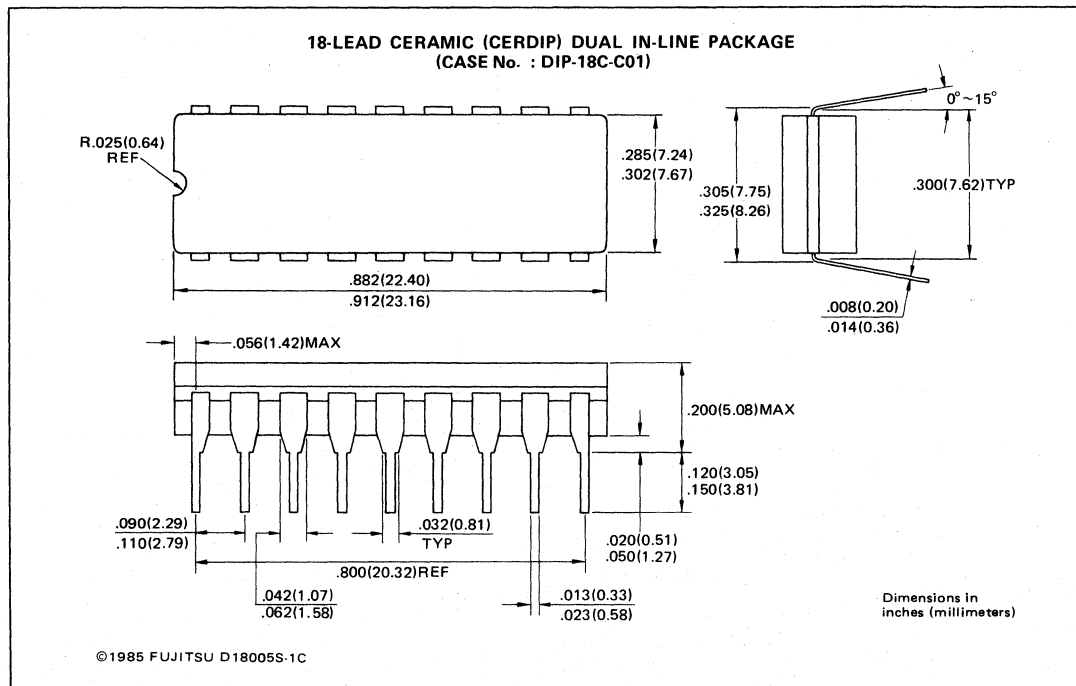
NOTE 1: This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

NOTE 2: Tie $910 \Omega \pm 5\%$ pullup resistor to the READY output.

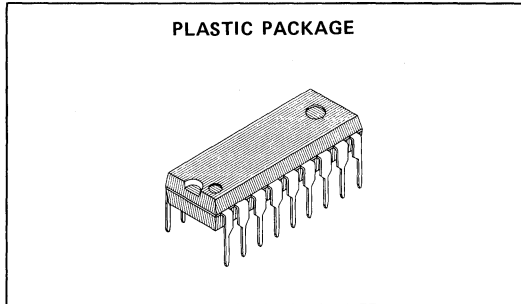
PACKAGE ILLUSTRATION



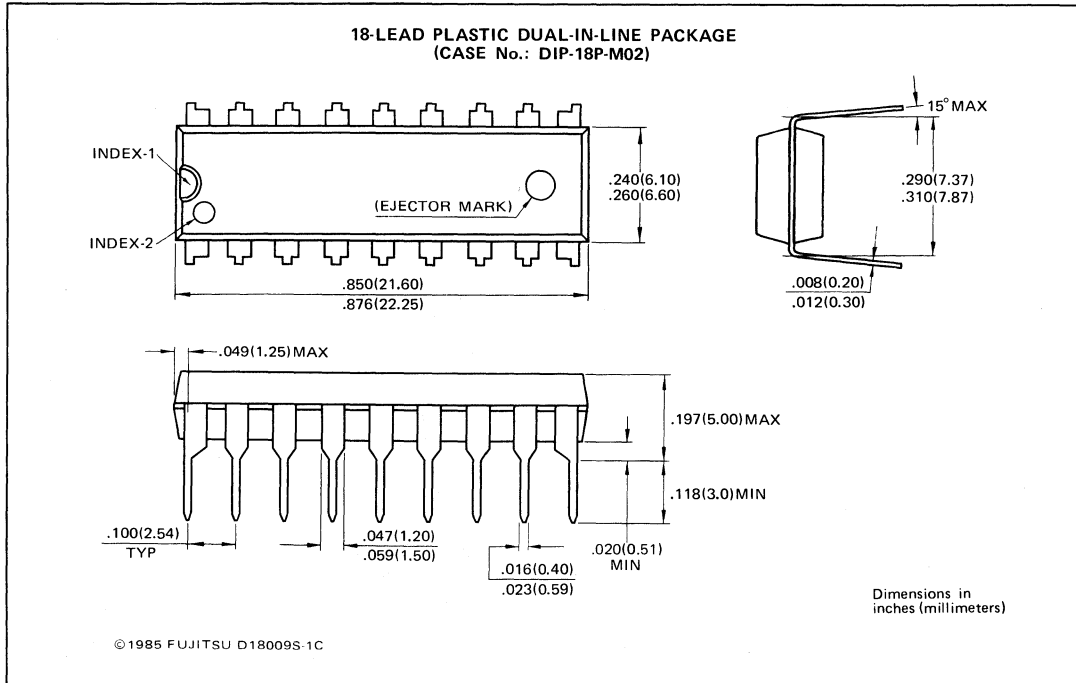
PACKAGE DIMENSIONS (Suffix: CZ)



PACKAGE ILLUSTRATION



PACKAGE DIMENSIONS (Suffix: P)



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