FUJITSU

NMOS BUS CONTROLLER FOR MBL 80286 PROCESSORS

MBL 82288-8
MBL 82288-6

December 1985
Edition 1.0

NMOS BUS CONTROLLER FOR MBL 80286 PROCESSORS

The Fujitsu MBL 82288 Bus Controller is a 20-pin NMOS component for use in MBL 80286 microsystems. The bus controller provides command and control outputs with flexible timing options. Separate command outputs are used for memory and I/O devices. The data bus is controlled with separate data enable and direction control signals.

Two modes of operation are possible via a strapping option: Multibus compatible bus cycles, and high speed bus cycles.

- **Provides Commands and Control for Local and System Bus**
- **Offers Wide Flexibility in System Configurations**
- **Flexible Command Timing**
- **Optional Multibus* Compatible Timing**
- **Control Drivers with 16 mA I_{OL} and 3-State Command Drivers with 32 mA I_{OL}**
- **Single +5V Supply**
- **Two Package Options:**
  –20-Pin Cerdip (Suffix: -CZ)
  –20-Pin Plastic DIP (Suffix: -P)

Fig. 1 – BLOCK DIAGRAM

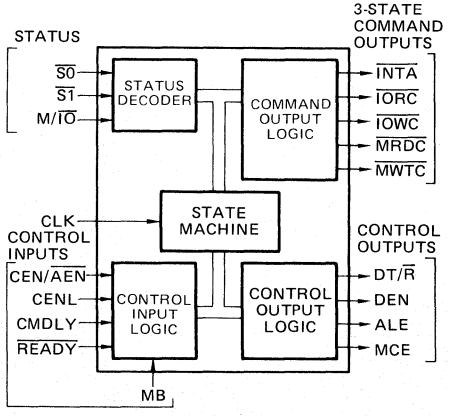
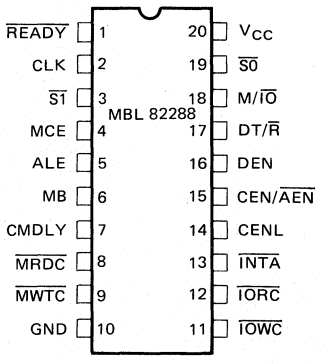


Fig. 2 – PIN CONFIGURATION



*Multibus is a patented bus of Intel.

PIN DESCRIPTION

The following pin function descriptions are for the MBL 82288 bus controller.

Table 1 – PIN DESCRIPTION

Symbol	Type	Name and Function
CLK	I	**System Clock** provides the basic timing control for the MBL 82288 in an MBL 80286 microsystem. Its frequency is twice the internal processor clock frequency. The falling edge of this input signal establishes when inputs are sampled and command and control outputs change.
$\overline{S0}$, $\overline{S1}$	I	**Bus Cycle Status** starts a bus cycle and, along with M/$\overline{IO}$, defines the type of bus cycle. These inputs are active LOW. A bus cycle is started when either $\overline{S1}$ or $\overline{S0}$ is sampled LOW at the falling edge of CLK. Setup and hold times must be met for proper operation.

MBL 80286 Bus Cycle Status Definition

M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Type of Bus Cycle
0	0	0	Interrupt acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	None; Idle
1	0	0	Halt or shutdown
1	0	1	Memory read
1	1	0	Memory write
1	1	1	None; Idle

M/$\overline{IO}$	I	**Memory or I/O Select** determines whether the current bus cycle is in the memory space or I/O space. When LOW, the current bus cycle is in the I/O space. Setup and hold times must be met for proper operation.
MB	I	**Multibus Mode Select** determines timing of the command and control outputs. When HIGH, the bus controller operates with Multibus-compatible timings. When LOW, the bus controller optimizes the command and control output timing for short bus cycles. The function of the CEN/$\overline{AEN}$ input pin is selected by this signal. This input is typically a strapping option and not dynamically changed.
CENL	I	**Command Enable Latched** is a bus controller select signal which enables the bus controller to respond to the current bus cycle being initiated. CENL is an active HIGH input latched internally at the end of each TS cycle. CENL is used to select the appropriate bus controller for each bus cycle in a system where the CPU has more than one bus it can use. This input may be connected to V_{CC} to select this MBL 82288 for all transfers. No control inputs affect CENL. Setup and hold times must be met for proper operation.
CMDLY	I	**Command Delay** allows delaying the start of a command. CMDLY is an active HIGH input. If sampled HIGH, the command output is not activated and CMDLY is again sampled at the next CLK cycle. When sampled LOW the selected command is enabled. If $\overline{READY}$ is detected LOW before the command output is activated, the MBL 82288 will terminate the bus cycle, even if no command was issued. Setup and hold times must be satisfied for proper operation. This input may be connected to GND if no delays are required before starting a command. This input has no effect on MBL 82288 control outputs.
$\overline{READY}$	I	**Ready** indicates the end of the current bus cycle. $\overline{READY}$ is an active LOW input. Multibus mode requires at least one wait state to allow the command outputs to become active. $\overline{READY}$ must be LOW during reset, to force the MBL 82288 into the idle state. Setup and hold times must be met for proper operation. The MBL 82284 drives $\overline{READY}$ LOW during RESET.

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Table 1 – PIN DESCRIPTION (Continued)

Symbol	Type	Name and Function
CEN/$\overline{AEN}$	I	**Command Enable/Address Enable** controls the command and DEN outputs of the bus controller. CEN/$\overline{AEN}$ inputs may be asynchronous to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs. This input may be connected to V_{CC} or GND. When MB is HIGH, this pin has the $\overline{AEN}$ function. $\overline{AEN}$ is an active LOW input which indicates that the CPU has been granted use of a shared bus and the bus controller command outputs may exit 3-state OFF and become inactive (HIGH). $\overline{AEN}$ HIGH indicates that the CPU does not have control of the shared bus and forces the command outputs into 3-state OFF and DEN inactive (LOW). $\overline{AEN}$ would normally be controlled by an 82289 bus arbiter which activates $\overline{AEN}$ when that arbiter owns the bus to which the bus controller is attached. When MB is LOW this pin has the CEN function. CEN is an unlatched active HIGH input which allows the bus controller to activate its command and DEN outputs. With MB LOW, CEN LOW forces the command and DEN outputs inactive but does not tristate them.
ALE	O	**Address Latch Enable** controls the address latches used to hold an address stable during a bus cycle. This control output is active HIGH. ALE will not be issued for the halt bus cycle and is not affected by any of the control inputs.
MCE	O	**Master Cascade Enable** signals that a cascade address from a master MBL 8259A interrupt controller may be placed onto the CPU address bus for latching by the address latches under ALE control. The CPU's address bus may then be used to broadcast the cascade address to slave interrupt controllers so only one of them will respond to the interrupt acknowledge cycle. This control output is active HIGH. MCE is only active during interrupt acknowledge cycles and is not affected by any control input. Using MCE to enable cascade address drivers requires latches which save the cascade address on the falling edge of ALE.
DEN	O	**Data Enable** controls when data transceivers connected to the local data bus should be enabled. DEN is an active HIGH control output. DEN is delayed for write cycles in the Multibus mode.
DT/$\overline{R}$	O	**Data Transmit/Receive** establishes the direction of data flow to or from the local data bus. When HIGH, this control output indicates that a write bus cycle is being performed. A LOW indicates a read bus cycle. DEN is always inactive when DT/$\overline{R}$ changes states. This output is HIGH when no bus cycle is active. DT/$\overline{R}$ is not affected by any of the control inputs.
$\overline{IOWC}$	O	**I/O Write Command** instructs an I/O device to read the data on the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.
$\overline{IORC}$	O	**I/O Read Command** instructs an I/O device to place data onto the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.
$\overline{MWTC}$	O	**Memory Write Command** instructs a memory device to read the data on the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.
$\overline{MRDC}$	O	**Memory Read Command** instructs the memory device to place data onto the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.
$\overline{INTA}$	O	**Interrupt Acknowledge** tells an interrupting device that its interrupt request is being acknowledged. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.
V_{CC}		**System Power:** +5V power supply.
GND		**System Ground:** 0 volts.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The MBL 82288 bus controller is used in MBL 80286 systems to provide address latch control, data transceiver control, and standard level-type command outputs. The command outputs are timed and have sufficient drive capabilities for large TTL buses and meet all IEEE-796 requirements for Multibus. A special Multibus mode is provided to satisfy all address/data setup and hold time requirements. Command timing may be tailored to special needs via a CMDLY input to determine the start of a command and $\overline{\text{READY}}$ to determine the end of a command.

Connection to multiple buses are supported with a latched enable input (CENL). An address decoder can determine which, if any, bus controller should be enabled for the bus cycle. This input is latched to allow an address decoder to take full advantage of the pipelined timing on the MBL 80286 local bus.

Bus shared by several bus controllers are supported. An $\overline{\text{AEN}}$ input prevents the bus controller from driving the shared bus command and data signals except when enabled by an external bus arbiter such as the 82289.

Separate DEN and DT/$\overline{\text{R}}$ outputs control the data transceivers for all buses. Bus contention is eliminated by disabling DEN before changing DT/$\overline{\text{R}}$. The DEN timing allows sufficient time for tristate bus drivers to enter 3-state OFF before enabling other drivers onto the same bus.

The term CPU refers to any MBL 80286 processor or MBL 80286 support component which may become an MBL 80286 local bus master and thereby drive the MBL 82288 status inputs.

PROCESSOR CYCLE DEFINITION

Any CPU which drives the local bus uses an internal clock which is one half the frequency of the system clock (CLK) (see Fig. 3). Knowledge of the phase of the local bus master internal clock is required for proper operation of the MBL 80286 local bus. The local bus master informs the bus controller of its internal clock phase when it asserts the status signals. Status signals are always asserted beginning in Phase 1 of the local bus master's internal clock.

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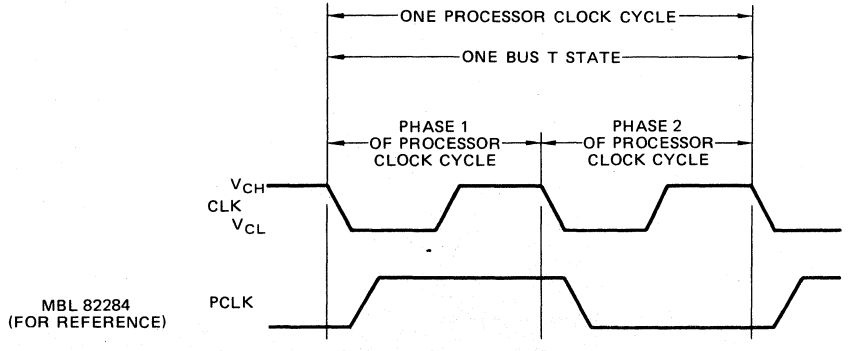
Fig. 3 – CLK RELATIONSHIP TO THE PROCESSOR CLOCK AND BUS T-STATES

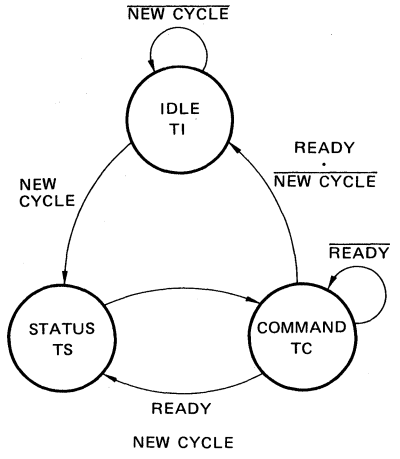


BUS STATE DEFINITION

The MBL 82288 bus controller has three bus states (see Fig. 4): Idle (TI), Status (TS) and Command (TC). Each bus state is two CLK cycles long. Bus state phases correspond to the internal CPU processor clock phases.

The TI bus state occurs when no bus cycle is currently active on the MBL 80286 local bus. This state may be repeated indefinitely. When control of the local bus is being passed between masters, the bus remains in the TI state.

Fig. 4 – MBL 82288 BUS STATES



BUS CYCLE DEFINITION

The $\overline{S1}$ and $\overline{S0}$ inputs signal the start of a bus cycle. When either input becomes LOW, a bus cycle is started. The TS bus state is defined to be the two CLK cycles during which either $\overline{S1}$ or $\overline{S0}$ are active (see Fig. 5). These inputs are sampled by the MBL 82288 at every falling edge of CLK. When either $\overline{S1}$ or $\overline{S0}$ are sampled LOW, the next CLK cycle is considered the second phase of the internal CPU clock cycle.

The local bus enters the TC bus state after the TS state. The shortest bus cycle may have one TS state and one TC state. Longer bus cycles are formed by repeating TC states. A repeated TC bus state is called a wait state.

The $\overline{READY}$ input determines whether the current TC bus state is to be repeated. The $\overline{READY}$ input has the same timing and effect for all bus cycles. $\overline{READY}$ is sampled at the end of each TC bus state to see if it is active. If sampled HIGH, the TC bus state is repeated. This is called inserting a wait state. The control and command outputs do not change during wait states.

When $\overline{READY}$ is sampled LOW, the current bus cycle is terminated. Note that the bus controller may enter the TS bus state directly from TC if the status lines are sampled active at the next falling edge of CLK.

Fig. 5 – BUS CYCLE DEFINITION

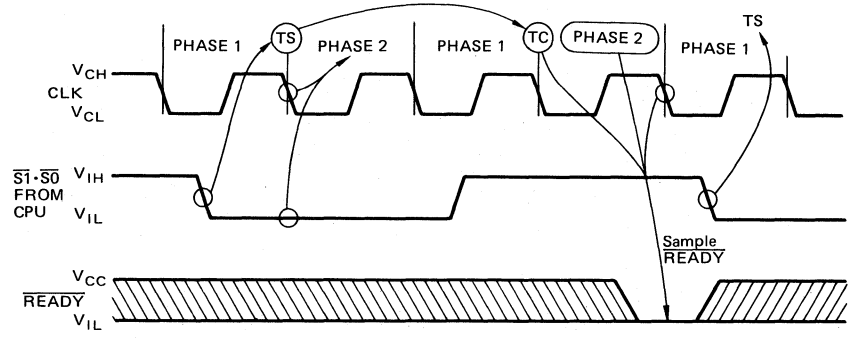


Table 2 – COMMAND AND CONTROL OUTPUTS FOR EACH TYPE OF BUS CYCLE

Type of Bus Cycle	M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Command Activated	DT/$\overline{R}$ State	ALE, DEN Issued?	MCE Issued?
Interrupt Acknowledge	0	0	0	$\overline{INTA}$	LOW	YES	YES
I/O Read	0	0	1	$\overline{IORC}$	LOW	YES	NO
I/O Write	0	1	0	$\overline{IOWC}$	HIGH	YES	NO
None; Idle	0	1	1	None	HIGH	NO	NO
Halt/Shutdown	1	0	0	None	HIGH	NO	NO
Memory Read	1	0	1	$\overline{MRDC}$	LOW	YES	NO
Memory Write	1	1	0	$\overline{MWTC}$	HIGH	YES	NO
None; Idle	1	1	1	None	HIGH	NO	NO

OPERATING MODES

Two types of buses are supported by the MBL 82288: Multibus and non-Multibus. When the MB input is strapped HIGH, Multibus timing is used. In Multibus mode, the MBL 82288 delays command and data activation to meet IEEE-796 requirements on address to command active and write data to command active setup timing. Multibus mode requires at least one wait state in the bus cycle since the command outputs are delayed. The non-Multibus mode does not delay any outputs and does not require wait states. The MB input affects the timing of the command and DEN outputs.

COMMAND AND CONTROL OUTPUTS

The type of bus cycle performed by the local bus master is encoded in the M/$\overline{IO}$, $\overline{S1}$, and $\overline{S0}$ inputs. Different command and control outputs are activated depending on the type of bus cycle. Table 2 indicates the cycle decode done by the MBL 82288 and the effect on command, DT/$\overline{R}$, ALE, DEN, and MCE outputs.

Bus cycles come in three forms: read, write, and halt. Read bus cycles include memory read, I/O read, and interrupt acknowledge. The timing of the associated read command outputs ($\overline{MRDC}$, $\overline{IORC}$, and $\overline{INTA}$), control outputs (ALE, DEN, DT/$\overline{R}$) and control inputs (CEN/$\overline{AEN}$, CENL, CMDLY, MB, and $\overline{READY}$) are identical for all read bus cycles. Read cycles differ only in which command output is activated. The MCE control output is only asserted during interrupt acknowledge cycles.

Write bus cycles activate different control and command outputs with different timing than read bus cycles. Memory write and I/O write are write bus cycles whose timing for command outputs ($\overline{MWTC}$ and $\overline{IOWC}$), control outputs (ALE, DEN, DT/$\overline{R}$) and control inputs (CEN/$\overline{AEN}$, CENL, CMDLY, MB, and $\overline{READY}$) are identical. They differ only in which command output is activated.

Halt bus cycles are different because no command or control output is activated. All control inputs are ignored until the next bus cycle is started via $\overline{S1}$ and $\overline{S0}$.

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Fig. 6-10 show the basic command and control output timing for read and write bus cycles. Halt bus cycles are not shown since they activate no outputs. The basic idle-read-idle and idle-write-idle bus cycles are shown. The signal label CMD represents the appropriate command output for the bus cycle. For Fig. 6–10, the CMDLY input is connected to GND and CENL to V_{CC}. The effects of CENL and CMDLY are described later in the section on control inputs.

Fig. 6, 7 and 8 show non-Multibus cycles. MB is connected to GND while CEN is connected to V_{CC}. Fig. 6 shows a read cycle with no wait states while Fig. 7 shows a write cycle with one wait state. The $\overline{READY}$ input is shown to illustrate how wait states are added.

Fig. 6 – IDEL-READ-IDEL BUS CYCLES WITH MB = 0

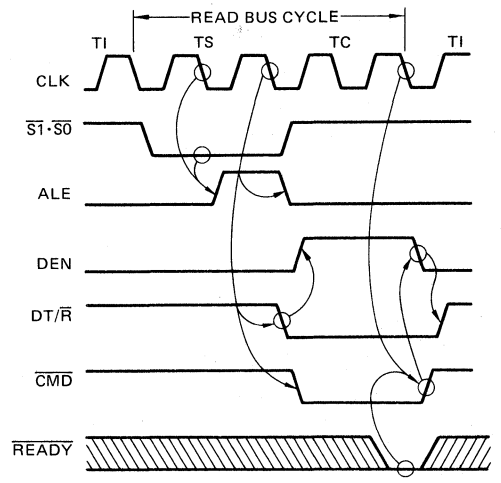
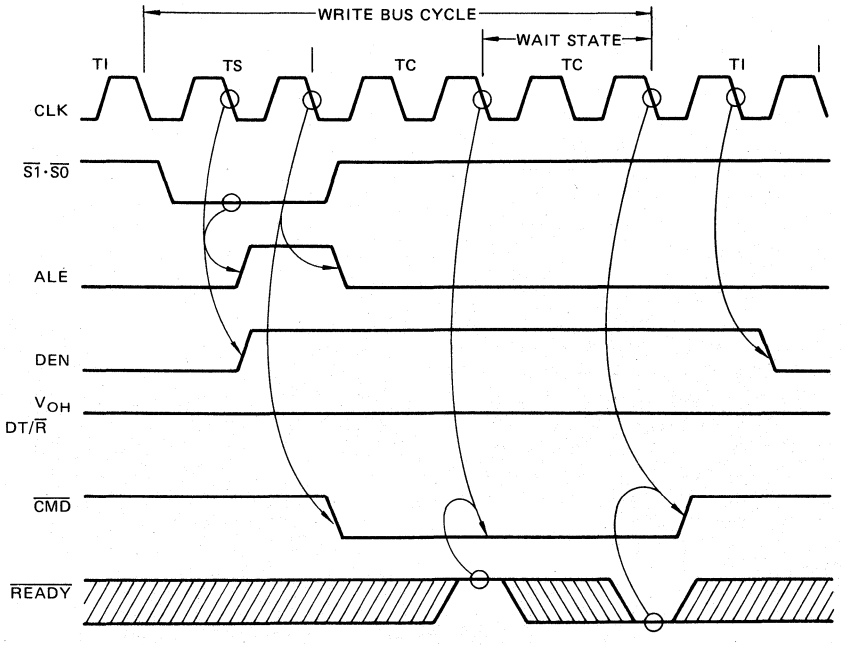


Fig. 7 – IDLE-WRITE-IDLE BUS CYCLES WITH MB = 0



Bus cycles can occur back to back with no TI bus states between TC and TS. Back to back cycles do not affect the timing of the command and control outputs. Command and control outputs always reach the states shown for the same clock edge (within TS, TC, or following bus state) of a bus cycle.

A special case in control timing occurs for back to back write cycles with MB = 0. In this case, DT/$\overline{R}$ and DEN remain HIGH between the bus cycles (see Fig. 8). The command and ALE output timing does not change.

Fig. 9 and 10 show a Multibus cycle with MB = 1. $\overline{AEN}$ and CMDLY are connected to GND. The effects of CMDLY and $\overline{AEN}$ are described later in the section on control inputs. Fig. 9 shows a read cycle with one wait state and Fig. 10 shows a write cycle with two wait states. The second wait state of the write cycle is shown only for example purposes and is not required. The $\overline{READY}$ input is shown to illustrate how wait states are added.

Fig. 8 – WRITE-WRITE BUS CYCLES WITH MB = 0

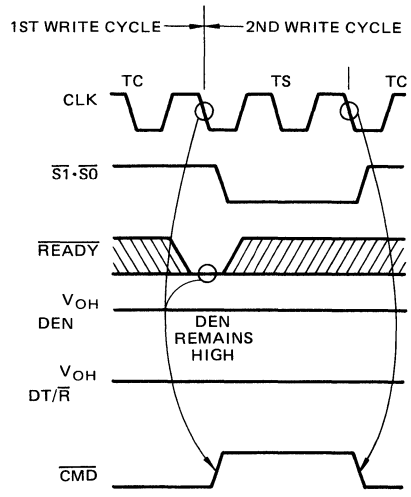


Fig. 9 – IDLE-READ-IDLE BUS CYCLES WITH MB = 1

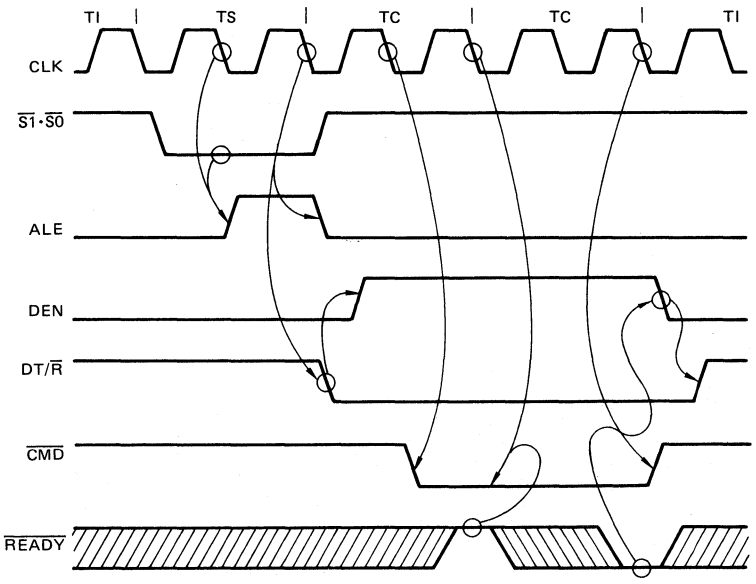
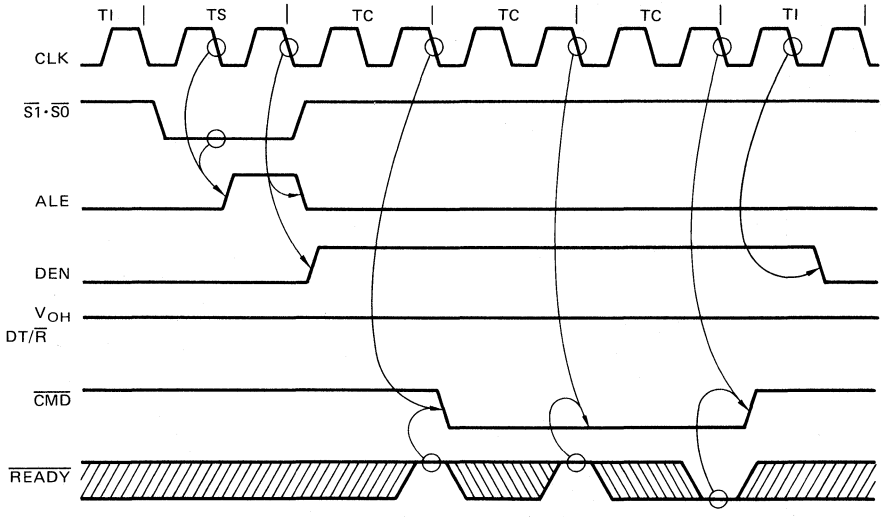


Fig. 10 – IDEL-WRITE-IDLE BUS CYCLES WITH MB = 1



The MB control input affects the timing of the command and DEN outputs. These outputs are automatically delayed in Multibus mode to satisfy three requirements:

1) 50 ns minimum setup time for valid address before any command output becomes active.

2) 50 ns minimum setup time for valid write data before any write command output becomes active.

3) 65 ns maximum time from when any read command becomes inactive until the slave's read data drivers reach 3-state OFF.

Three signal transitions are delayed by MB = 1 as compared to MB = 0:

1) The HIGH to LOW transition of the read command outputs ($\overline{IORC}$, $\overline{MRDC}$, and $\overline{INTA}$) are delayed one CLK cycle.

2) The HIGH to LOW transition of the write command outputs ($\overline{IOWC}$ and $\overline{MWTC}$) are delayed two CLK cycles.

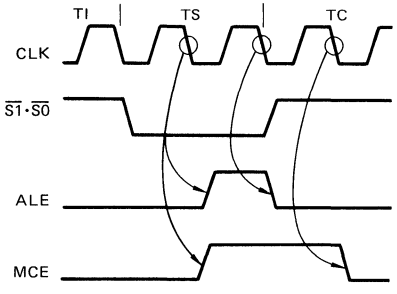
3) The LOW to HIGH transition of DEN for write cycles is delayed one CLK cycle.

Back to back bus cycles with MB = 1 do not change the timing of any of the command of control outputs. DEN always becomes inactive between bus cycles with MB = 1.

Except for a halt or shutdown bus cycle, ALE will be issued during the second half of TS for any bus cycle. ALE becomes inactive at the end of the TS to allow latching the address to keep it stable during the entire bus cycle. The address outputs may change during Phase 2 of any TC bus state. ALE is not affected by any control input.

Fig. 11 shows how MCE is timed during interrupt acknowledge (INTA) bus cycles. MCE is one CLK cycle longer than ALE to hold the cascade address from a master MBL 8259A valid after the falling edge of ALE. With the exception of the MCE control output, an INTA bus cycle is identical in timing to a read bus cycle. MCE is not affected by any control input.

Fig. 11 – MCE OPERATION FOR AN INTA BUS CYCLE



CONTROL INPUTS

The control inputs can alter the basic timing of command outputs, allow interfacing to multiple buses, and share a bus between different masters. For many MBL 80286 systems, each CPU will have more than one bus which may be used to perform a bus cycle. Normally, a CPU will only have one bus controller active for each bus cycle. Some buses may be shared by more than one CPU (i.e. Multibus) requiring only one of them use the bus at a time.

Systems with multiple and shared buses use two control input signals of the MBL 82288 bus controller, CENL and $\overline{AEN}$ (see Fig. 12). CENL enables the bus controller to control the current bus cycle. The $\overline{AEN}$ input prevents a bus controller from driving its command outputs. $\overline{AEN}$ HIGH means that another bus controller may be driving the shared bus.

In Fig. 12, two buses are shown: a local bus and a Multibus. Only one bus is used for each CPU bus cycle. The CENL inputs of the bus controllers select which bus controller is to perform the bus cycle. An address decoder determines which bus to use for each bus cycle. The MBL 82288 connected to the shared Multibus must be selected by CENL and be given access to the Multibus by $\overline{AEN}$ before it will begin a Multibus operation.

CENL must be sampled HIGH at the end of the TS bus state (see waveforms) to enable the bus controller to activate its command and control outputs. If sampled LOW the commands and DEN will not go active and DT/$\overline{R}$ will remain HIGH. The bus controller will ignore the CMDLY, CEN, and $\overline{READY}$ inputs until another bus cycle is started via $\overline{S1}$ and $\overline{S0}$. Since an address decoder is commonly used to identify which bus is required for each bus cycle, CENL is latched to avoid the need for latching its input.

The CENL input can affect the DEN control output. When MB = 0, DEN normally becomes active during Phase 2 of TS in write bus cycles. This transition occurs before CENL is sampled. If CENL is sampled LOW, the DEN output will be forced LOW during TC as shown in the timing waveforms.

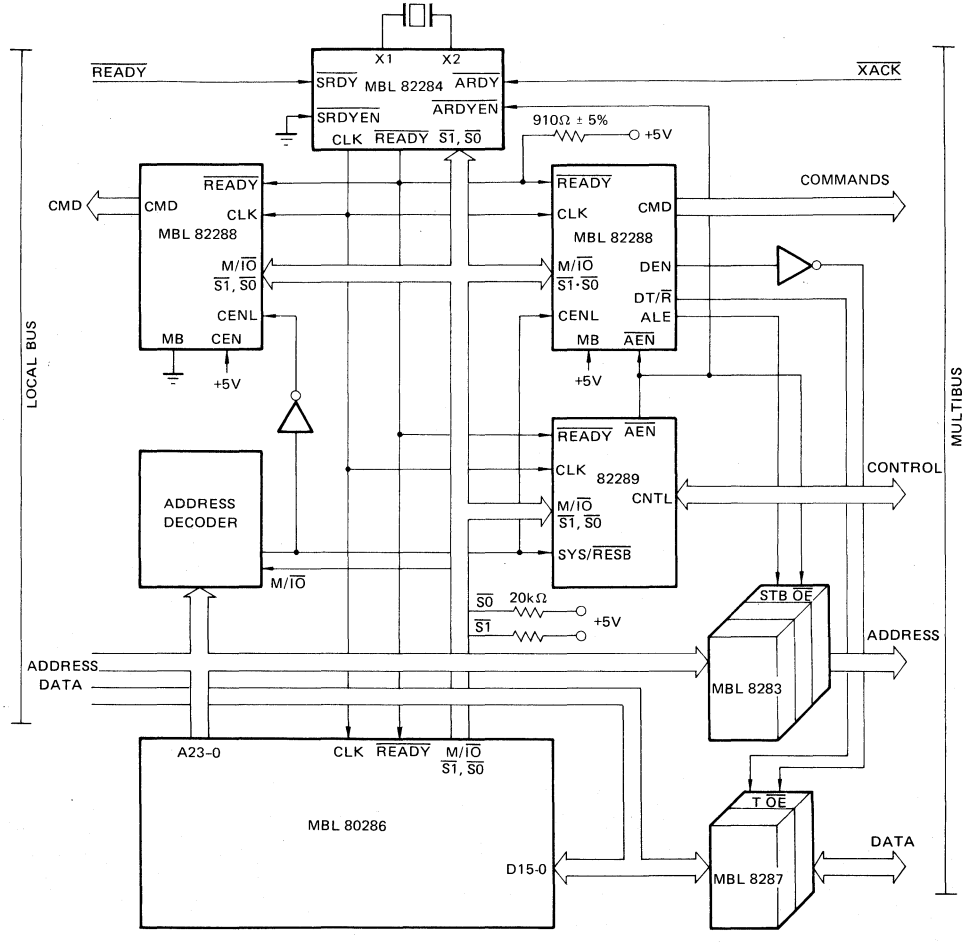
When MB = 1, CEN/$\overline{AEN}$ becomes $\overline{AEN}$. $\overline{AEN}$ controls when the bus controller command outputs enter and exit 3-state OFF. $\overline{AEN}$ is intended to be driven by a bus arbiter, like the 82289, which assures only one bus controller is driving the shared bus at any time. When $\overline{AEN}$ makes a LOW to HIGH transition, the command outputs immediately enter 3-state OFF and DEN is forced inactive. An inactive DEN should force the local data transceivers connected to the shared data bus into 3-state OFF (see Fig. 12). The LOW to HIGH transition of $\overline{AEN}$ should only occur during TI or TS bus states.

The HIGH to LOW transition of $\overline{AEN}$ signals that the bus controller may now drive the shared bus command signals. Since a bus cycle may be active or be in the process of starting, $\overline{AEN}$ can become active during any T-state. $\overline{AEN}$ LOW immediately allows DEN to go to the appropriate state. Three CLK edges later, the command outputs will go active (see timing waveforms). The Multibus requires this delay for the address and data to be valid on the bus before the commands become active.

When MB=0, CEN/$\overline{AEN}$ becomes CEN. CEN is an synchronous input which immediately affects the command and DEN outputs. When CEN makes a HIGH to LOW transition, the commands and DEN are immediately forced inactive. When CEN makes a LOW to HIGH transition, the commands and DEN outputs immediately go to the appropriate state (see timing waveforms). $\overline{READY}$ must still become active to terminate a bus cycle if CEN remains LOW for a selected bus controller (CENL was latched HIGH).

Some memory or I/O systems may require more address or write data setup time to command active than provided by the basic command output timing. To provide flexible command timing, the CMDLY input can delay the activation of command outputs. The CMDLY input must be sampled LOW to activate the command outputs. CMDLY does not affect the control outputs ALE, MCE, DEN, and DT/$\overline{R}$.

Fig. 12 – SYSTEM USE OF $\overline{AEN}$ AND CENL



CMDLY is first sampled on the falling edge of the CLK ending TS. If sampled HIGH, the command output is not activated, and CMDLY is again sampled on the next falling edge of CLK. Once sampled LOW, the proper command output becomes active immediately if MB = 0. If MB = 1, the proper command goes active no earlier than shown in Fig. 9 and 10.

$\overline{\text{READY}}$ can terminate a bus cycle before CMDLY allows a command to be issued. In this case no commands are issued and the bus controller will deactivate DEN and DT/$\overline{\text{R}}$ in the same manner as if a command had been issued.

WAVEFORMS DISCUSSION

The waveforms show the timing relationships of inputs and outputs and do not show all possible transitions of all signals in all modes. Instead, all signal timing relationships are shown via the general cases. Special cases are shown when needed. The waveforms provide some functional descriptions of the MBL 82288; however, most functional descriptions are provided in Fig. 5 through 11.

To find the timing specification for a signal transition in a particular mode, first look for a special case in the waveforms. If no special case applies, then use a timing specification for the same or related function in another mode.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.5V to +7V
Power Dissipation . . . . . 1 Watt

*NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (V_{CC} = 5V ±5%, T_A = 0°C to 70°C)

Symbol	Parameter	MBL 82288-6 (6 MHz)		MBL 82288-8 (8 MHz)		Unit	Test Condition
		Min	Max	Min	Max		
V_{IL}	Input LOW Voltage	−0.5	0.8	−0.5	0.8	V	
V_{IH}	Input HIGH Voltage	2.0	V_{CC}+0.5	2.0	V_{CC}+0.5	V	
V_{ILC}	CLK Input LOW Voltage	−0.5	0.6	−0.5	0.6	V	
V_{IHC}	CLK Input HIGH Voltage	3.8	V_{CC}+0.5	3.8	V_{CC}+0.5	V	
V_{OL}	Output LOW Voltage:						
	Command Outputs		0.45		0.45	V	I_{OL} = 32mA, Note 1
	Control Outputs		0.45		0.45	V	I_{OL} = 16mA, Note 2
V_{OH}	Output HIGH Voltage:						
	Command Outputs	2.4		2.4		V	I_{OH} = −5mA, Note 1
	Control Outputs	2.4		2.4		V	I_{OH} = −1mA, Note 2
I_F	Input Current ($\overline{S0}$ and $\overline{S1}$ inputs)		−0.5		−0.5	mA	V_f = 0.45V
I_{IL}	Input Leakage current (all other inputs)		±10		±10	μA	$0V \leqq V_{IN} \leqq V_{CC}$
I_{LO}	Output Leakage Current		±10		±10	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
I_{CC}	Power Supply Current		120		120	mA	
C_{CLK}	CLK Input Capacitance		12		12	pF	F_C = 1MHz
C_I	Input Capacitance		10		10	pF	F_C = 1MHz
C_O	Input/Output Capacitance		20		20	pF	F_C = 1MHz

NOTE: 1. Command Outputs are $\overline{INTA}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{MRDC}$, and $\overline{MWRC}$.
2. Control Outputs are DT/$\overline{R}$, DEN, ALE and MCE.

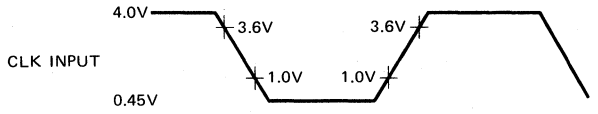
A.C. CHARACTERISTICS (V_{CC} = 5V ±5%, T_A = 0°C to 70°C)

AC timings are referenced to 0.8V and 2.0V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

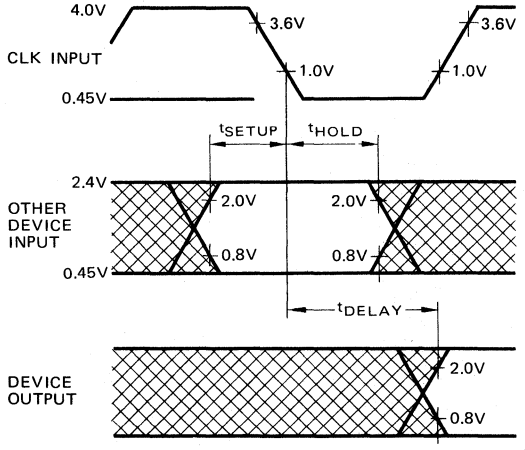
Symbol	Parameter	MBL 82288-6 (6 MHz)		MBL 82288-8 (8 MHz)		Unit	Test Condition
		Min	Max	Min	Max		
1	CLK Period	83	250	62	250	ns	
2	CLK HIGH Time	25	230	20	235	ns	at 3.6V
3	CLK LOW Time	20	225	15	230	ns	at 1.0V
4	CLK Rise Time		10		10	ns	1.0V to 3.6V
5	CLK Fall Time		10		10	ns	3.6V to 1.0V
6	M/$\overline{IO}$ and Status Setup Time	28		22		ns	
7	M/$\overline{IO}$ and Status Hold Time	1		1		ns	
8	CENL Setup Time	30		20		ns	
9	CENL Hold Time	1		1		ns	
10	$\overline{READY}$ Setup Time	50		38		ns	
11	$\overline{READY}$ Hold Time	35		25		ns	
12	CMDLY Setup Time	25		20		ns	
13	CMDLY Hold Time	1		1		ns	
14	$\overline{AEN}$ Setup Time	25		20		ns	Note 3
15	$\overline{AEN}$ Hold Time	0		0		ns	Note 3
16	ALE, MCE Active Delay from CLK	3	25	3	20	ns	Note 4
17	ALE, MCE Inactive Delay from CLK		35		25	ns	Note 4
18	DEN (Write) Inactive from CENL		35		35	ns	Note 4
19	DT/$\overline{R}$ LOW from CLK		40		25	ns	Note 4
20	DEN (Read) Active from DT/$\overline{R}$	5	50	5	35	ns	Note 4
21	DEN (Read) Inactive Delay from CLK	3	40	3	35	ns	Note 4
22	DT/$\overline{R}$ HIGH from DEN Inactive	5	45	5	35	ns	Note 4
23	DEN (Write) Active Delay from CLK		35		30	ns	Note 4
24	DEN (Write) Inactive Delay from CLK	3	35	3	30	ns	Note 4
25	DEN Inactive from CEN		40		30	ns	Note 4
26	DEN Active from CEN		35		30	ns	Note 4
27	DT/$\overline{R}$ HIGH from CLK (when CEN = LOW)		50		35	ns	Note 4
28	DEN Active from $\overline{AEN}$		35		30	ns	Note 4
29	$\overline{CMD}$ Active Delay from CLK	3	40	3	25	ns	Note 5
30	$\overline{CMD}$ Inactive Delay from CLK	3	30	3	25	ns	Note 5
31	$\overline{CMD}$ Inactive from CEN		35		25	ns	Note 5
32	$\overline{CMD}$ Active from CEN		45		25	ns	Note 5
33	$\overline{CMD}$ Inactive Enable from $\overline{AEN}$		40		40	ns	Note 5
34	$\overline{CMD}$ Float Delay from $\overline{AEN}$		40		40	ns	Note 6
35	MB Setup Time	25		20		ns	
36	MB Hold Time	0		0		ns	
37	Command Inactive Enable from MB↓		40		40	ns	Note 5
38	Command Float Time from MB↑		40		40	ns	Note 6
39	DEN Inactive from MB↑		40		30	ns	Note 4
40	DEN Active from MB↓		35		30	ns	Note 4

NOTE: 3. $\overline{AEN}$ is an asynchronous input. This specification is for testing purposes only, to assure recognition at a specific CLK edge.
4. Control output load: C_L = 150pF.
5. Command output load: C_L = 300pF.
6. Float condition occurs when output current is less than I_{LO} in magnitude.

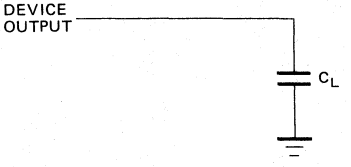
NOTE 7: AC Drive and Measurement Points – CLK Input



NOTE 8: AC Setup, Hold and Delay Time Measurement – General

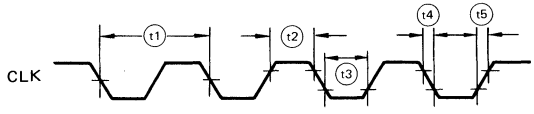


NOTE 9: AC Test Loading on Outputs

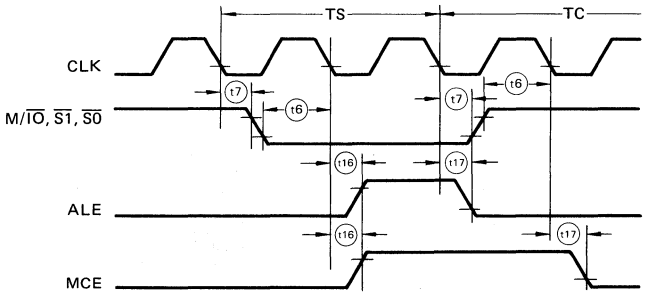


WAVEFORMS

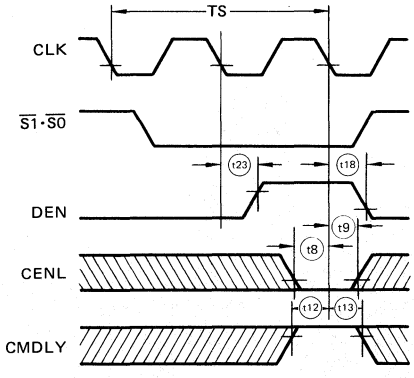
CLK CHARACTERISTICS



STATUS, ALE, MCE, CHARACTERISTICS

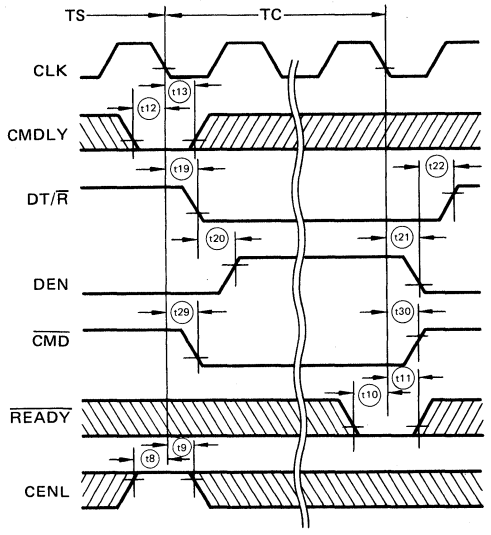


CENL, CMDLY, DEN CHARACTERISTICS WITH MB = 0 AND CEN = 1 DURING WRITE CYCLE

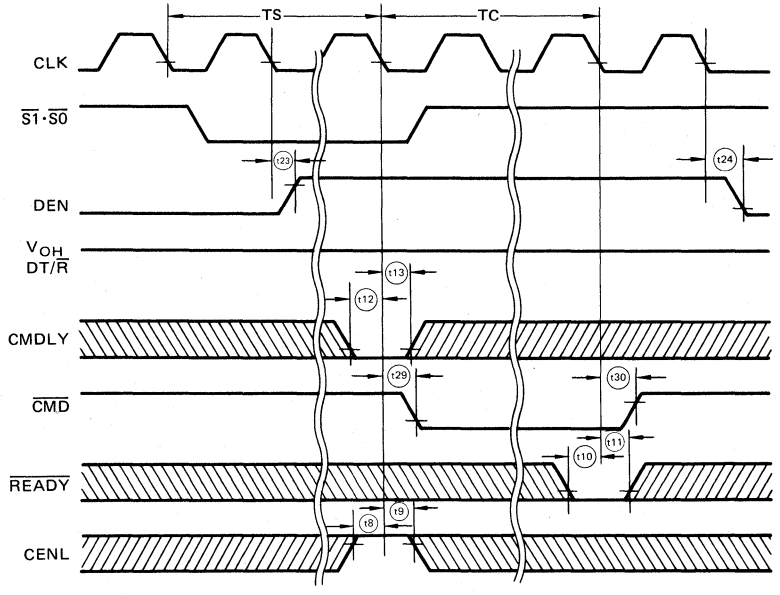


WAVEFORMS (Continued)

READ CYCLE CHARACTERISTICS WITH MB = 0 AND CEN = 1

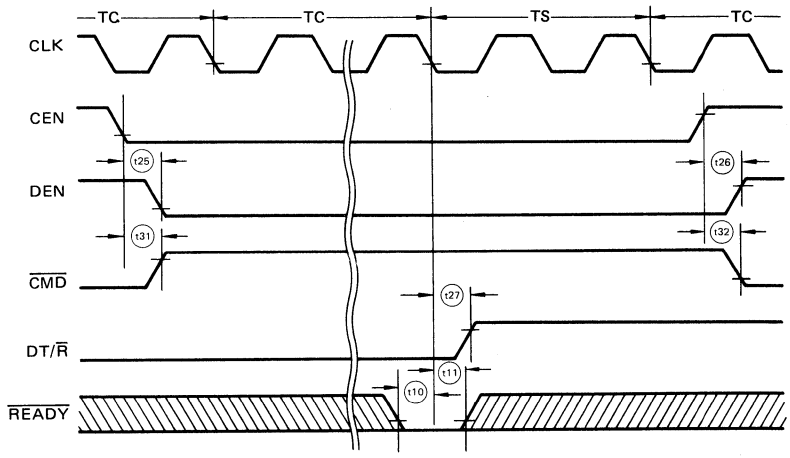


WRITE CYCLE CHARACTERISTICS WITH MB = 0 AND CEN = 1

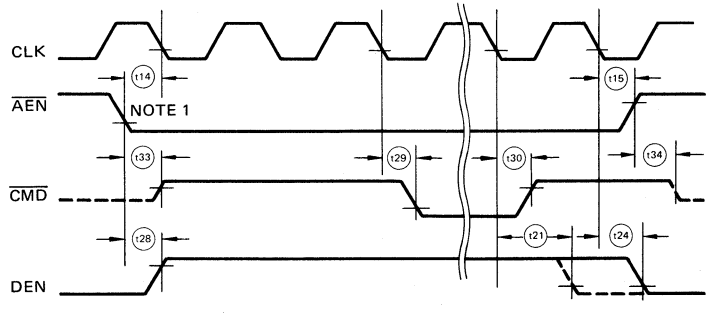


WAVEFORMS (Continued)

CEN CHARACTERISTICS WITH MB = 0



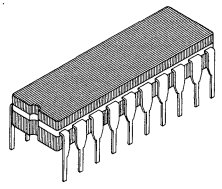
AEN CHARACTERISTICS WITH MB = 1



NOTE 1: AEN is an asynchronous input. AEN setup and hold times are specified to guarantee the response shown in the waveforms.

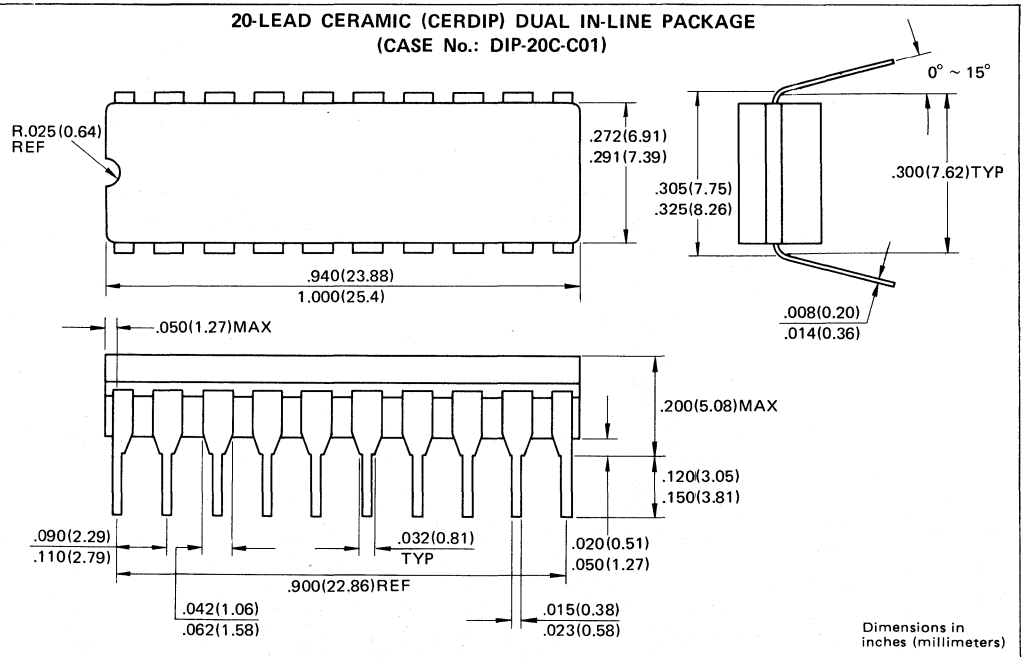
PACKAGE ILLUSTRATION

CERAMIC PACKAGE
(CERDIP)



PACKAGE DIMENSIONS (Suffix -CZ)

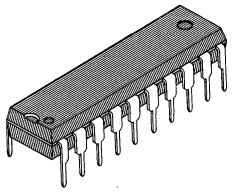
20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C01)



Dimensions in
inches (millimeters)

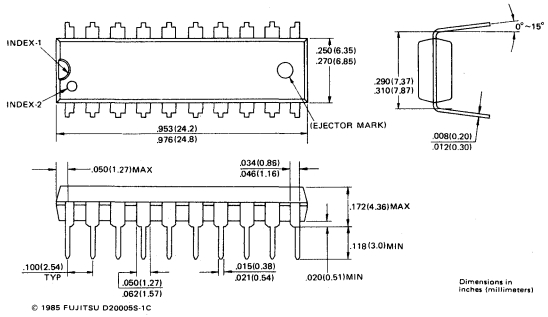
PACKAGE ILLUSTRATION

PLASTIC PACKAGE



PACKAGE DIMENSIONS (Suffix: -P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M01)



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