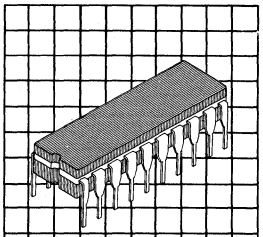
MBL8282
MBL8283
Bipolar Octal Latch

November 1986
Edition 4.0

Description

The MBL8282 and MBL8283 are 8-bit bipolar latches with 3-state output buffers. They can be used to implement latches, buffers or multiplexers. The MBL8283 inverts the input data at its outputs while the MBL8282 does not. Thus, all of the principle peripherals and input/output functions of a microcomputer system can be implemented with these devices.

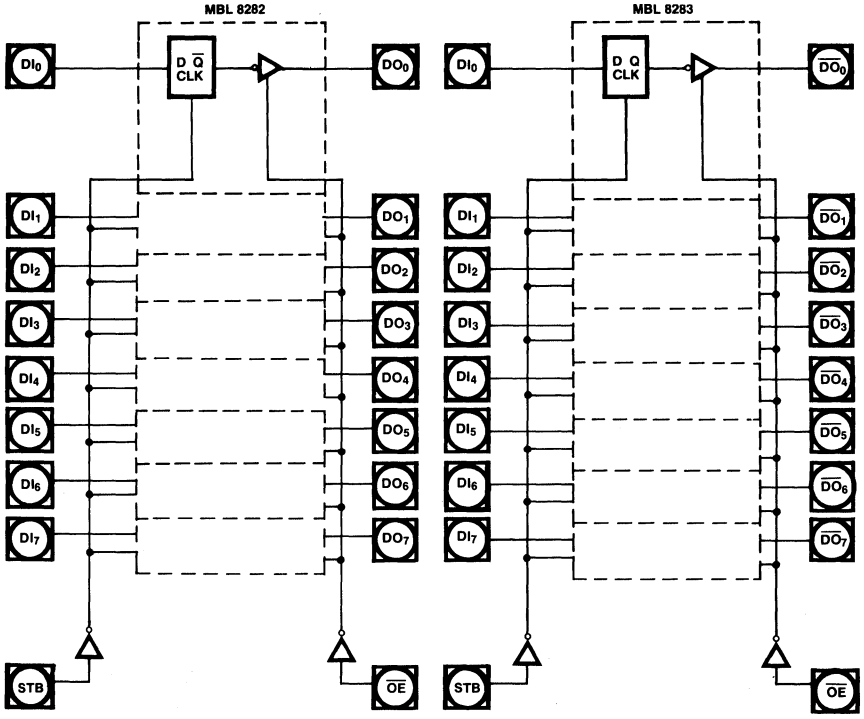


Ceramic Package
DIP-20C-C01

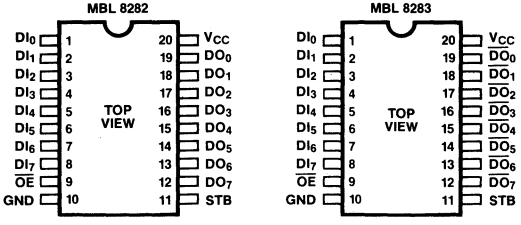
Features

- **Address Latch for MBL8086, MBL8088, MBL8089, MCS-80*, MCS-85*, MCS-48* Families**
- **High Output Drive Capability for Driving System Data Bus**
- **Fully Parallel 8-Bit Data Register and Buffer**
- **Transparent during Active Strobe**
- **3-State Outputs**
- **20-Pin DIP Package**
- **No Output Low Noise when Entering or Leaving High Impedance State**

Logic Diagrams



Pin Configurations



Functional Description

The MBL8282 and MBL8283 are 8-bit latches with 3-state output buffers. Data having satisfied the setup time requirements is clocked into the data latches by strobing the STB line HIGH to LOW.

Holding the STB line in its active HIGH state makes the latches appear transparent. Data is presented to the data output pins by activating the $\overline{OE}$ input line. When $\overline{OE}$ is inactive HIGH the output buffers are in their high impedance state. Enabling or disabling the output buffers will not cause negative-going transients to appear on the data output bus.

Pin Description

Pin	Description
STB	STROBE (Input). STB is an input control pulse used to strobe data at the data input pins (A_0-A_7) into the data latches. This signal is active to HIGH to allow data in. The data is latched during the HIGH to LOW transition of STB.
$\overline{OE}$	OUTPUT ENABLE (Input) $\overline{OE}$ is an input control signal which when active LOW enables the contents of the data latches to be sent to the data output pins (B_0-B_7). $\overline{OE}$ being inactive HIGH forces the output buffers to their high impedance state.
DI_0-DI_7	DATA INPUT PINS (Input). Data present at these pins is clocked into the data input latches when STB is strobed.
DO_0-DO_7 (MBL 8282) $\overline{DO}_0$-$\overline{DO}_7$ (MBL8283)	DATA OUTPUT PINS (Output). When $\overline{OE}$ is low, the data in the data latches appears as inverted (MBL8283) or non-inverted (MBL8282) data on the data output pins.

Absolute Maximum Ratings*

Parameter	Rating	Unit
Temperature Under Bias	0° to 70°	°C
Storage Temperature	−65° to +150°	°C
Supply Voltage	−0.5 to +7.0	V
All Input Voltages	−0.5 to +7.0	V
All Output Voltages (3-State Output)	+5.5	V
Power Dissipation	1.0	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(V_{CC} = 5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_C	Input Clamp Voltage		-1	V	I_C = -5 mA
I_{CC}	Power Supply Current		160	mA	
I_F	Forward Input Current		-0.2	mA	V_F = 0.45V
I_R	Reverse Input Current		50	μA	V_R = 5.25V
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 32 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -5 mA
I_{OFF}	Output Off Current		±50	μA	V_{OFF} = 0.45V to 5.25V
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = 5.0V See Note 1
V_{IH}	Input High Voltage	2.0		V	V_{CC} = 5.0V See Note 1
C_{IN}	Input Capacitance		12	pF	F = 1 MHz V_{BIAS} = 2.5V, V_{CC} = 5V T_A = 25°C

Note:
1. Output Loading I_{OL} = 32mA, I_{OH} = -5mA, C_L = 300pF.

A.C. Characteristics

(V_{CC} = 5V ±10%, T_A = 0°C to 70°C, Loading: Outputs— I_{OL} = 32mA, I_{OH} = -5mA, C_L = 300pF)

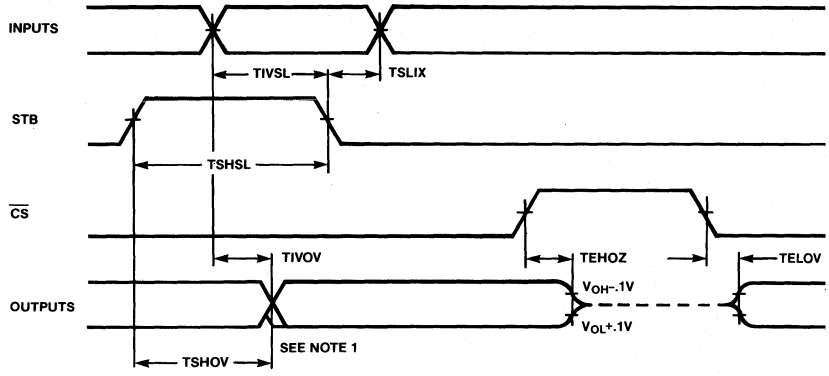
Symbol	Parameter		Min.	Max.	Units	Test Conditions
TIVOV	Input to Output Delay					
	—Inverting	(MBL8283)	5	22	ns	
	—Non-Inverting	(MBL8282)	5	30	ns	
TSHOV	STB to Output Delay					
	—Inverting	(MBL8283)	10	40	ns	
	—Non-Inverting	(MBL8282)	10	45	ns	
TEHOZ	Output Disable Time		5	18	ns	(See Note 1)
TELOV	Output Enable Time		10	30	ns	
TIVSL	Input to STB Setup Time		0		ns	
TSLIX	Input to STB Hold Time		25		ns	
TSHSL	STB High Time		15		ns	
TILIH, TOLOH	Input, Output Rise Time			20	ns	From 0.8V to 2.0V
TIHIL, TOHOL	Input, Output Fall Time			12	ns	From 2.0V to 0.8V

Note:
1. See waveforms and test load circuit on following page.

A.C. Testing Input/ Output Waveform

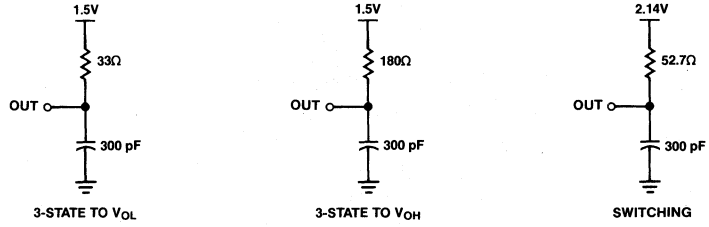
A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 1.5V FOR BOTH A LOGIC "1" AND "0". INPUT RISE AND FALL TIMES ARE MEASURED FROM).8V TO 2.0V AND ARE DRIVEN AT 5±2ns.

Waveforms

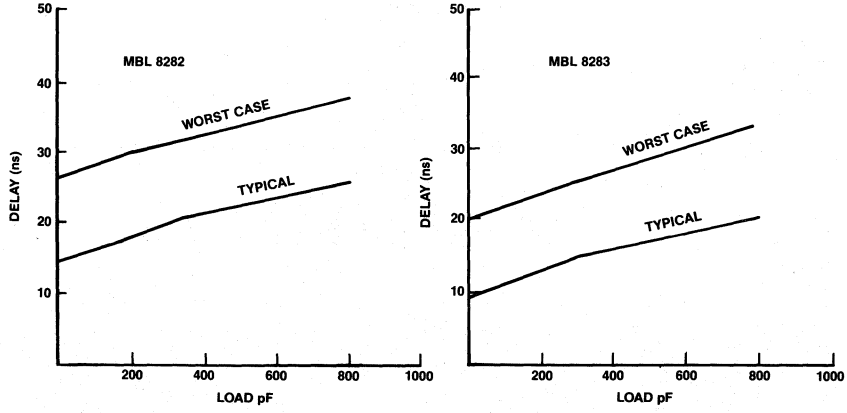


NOTE: 1. FOR MBL 8283 ONLY—OUTPUT MAY BE MOMENTARILY INVALID FOLLOWING THE HIGH GOING STB TRANSITION.
2. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.

Output Test Load Circuits

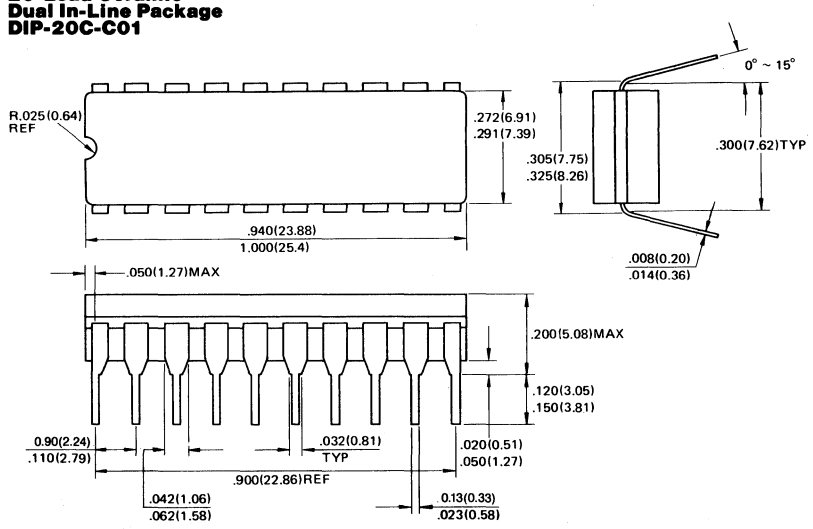


Output Delay vs. Capacitance



Package Dimensions
Dimensions in inches
(millimeters)

20-Lead Ceramic
Dual In-Line Package
DIP-20C-C01



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