FUJITSU

BIPOLAR CLOCK GENERATOR/DRIVER

MBL 8284A
MBL 8284A-1

April 1986
Edition 4.0

BIPOLAR CLOCK GENERATOR AND DRIVER FOR MBL 8086/8088/8089

- Generates the System Clock for the MBL 8086/8088/8089 Processors:
  5MHz and 8MHz with MBL 8284A
  10MHz with MBL 8284A-1
- Uses a Crystal or a TTL Signal for Frequency Source
- Provides Local READY and Multibus* READY Synchronization
- Generates System Reset Output from Schmitt Trigger Input
- Capable of Clock Synchronization with Other MBL 8284As
- Single +5V Power Supply
- 18-Pin Cerdip (Suffix: -CZ)

Fig. 1 BLOCK DIAGRAM

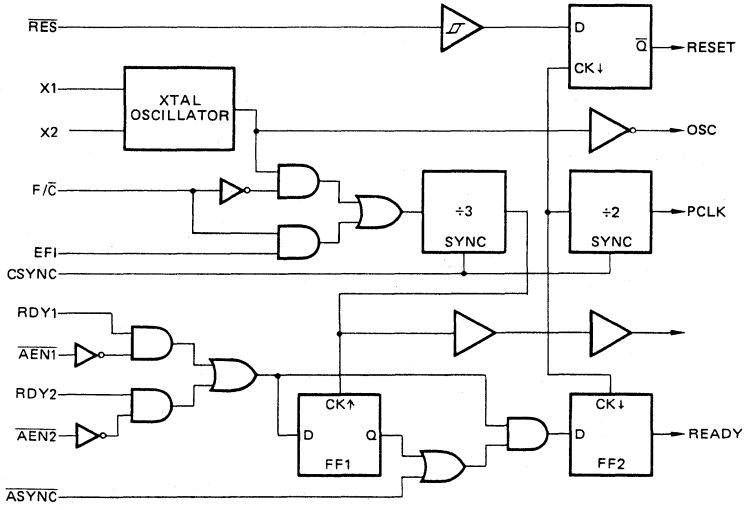
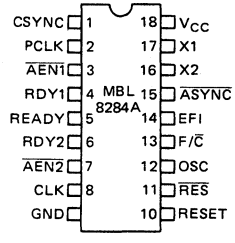


Fig. 2 – PIN CONFIGURATION



*Trade Mark of Intel Corporation

PIN DESCRIPTION

TABLE 1 – PIN DISCRIPTION

Symbol	Type	Name and Function
$\overline{AEN1}$, $\overline{AEN2}$	I	**Address Enable:** $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two $\overline{AEN}$ signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non Multi-Master configurations the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY1, RDY2	I	**Bus Ready:** (Transfer Complete), RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
$\overline{ASYNC}$	I	**Ready Synchronization Select:** $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open (internal pull-up resistor is provided.) or HIGH a single stage of READY synchronization is provided.
READY	O	**Ready:** READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	I	**Crystal In:** X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency.
F/$\overline{C}$	I	**Frequency/Crystal Select:** F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input.
EFI	I	**External Frequency:** When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
CLK	O	**Processor Clock:** CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (i.e., the bipolar support chips and other MOS devices). CLK has an output frequency which is 1/3 of the crystal or EFI input frequency and a 1/3 duty cycle. An output HIGH of 4.5 volts (V_{CC} = 5V) is provided on this pin to drive MOS devices.
PCLK	O	**Peripheral Clock:** PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
OSC	O	**Oscillator Output:** OSC is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{RES}$	I	**Reset In:** $\overline{RES}$ is an active LOW signal which is used to generate RESET. The MBL 8284A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	O	**Reset:** RESET is an active HIGH signal which is used to reset the MBL 8086 family processors, its timing characteristics are determined by $\overline{RES}$.
CSYNC	I	**Clock Synchronization:** CSYNC is an active HIGH signal which allows multiple MBL 8284A to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND		**Ground.**
V_{CC}		**Power:** +5V supply.

FUNCTIONAL DESCRIPTION

GENERAL

The MBL 8284A is a single chip clock generator/driver for the MBL 8086/MBL 8088/MBL 8089 processors. The chip contains a crystal-controlled oscillator, a divide-by-three counter, complete MULTIBUS* "Ready" synchronization and reset logic. Refer to Figure 1 for Block Diagram and Figure 2 for Pin Configuration.

OSCILLATOR

The oscillator circuit of the MBL 8284A is designed primarily for use with an external series resonant, fundamental mode, crystal from which the basic operating frequency is derived.
The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two series resistors ($R_1 = R_2 = 510\Omega$) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

For systems which have a V_{CC} ramp time $\geqslant$ 1V/ms and/or have inherent board capacitance between X1 or X2, exceeding 10pF (not including MBL 8284A pin capacitance), the two 510Ω resistors should be used. This circuit provides optimum stability for the oscillator in such extreme conditions. It is advisable to limit stray capacitances to less than 10pF on X1 and X2 to minimize deviation from operating at the fundamental frequency. For notes of using MBL 8284A, see page 10.

CLOCK GENERATOR

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another MBL 8284A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the MBL 8284A. This is accomplished with two Schottky flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

CLOCK OUTPUTS

The CLK output is a 33% duty cycle MOS clock driver designed to drive the MBL 8086/MBL 8088/MBL 8089 processors directly. PCLK is a TTL level peripheral clock signal whose output frequency is ½ that of CLK, PCLK has a 50% duty cycle.

RESET LOGIC

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the MBL 8284A.

READY SYNCHRONIZATION

Two READY inputs (RDY1, RDY2) are provided to accommodate two Multi-Master system busses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation.

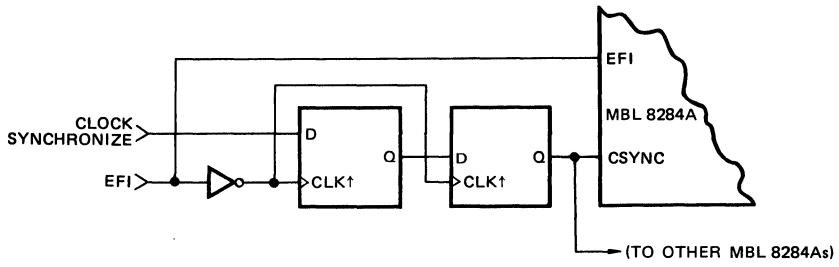
When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one at the rising edge of CLK and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, t_{R1VCL}, on each bus cycle.

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

$\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

* Trade Mark of Intel Corporation, USA

Fig. 3 – CSYNC SYNCHRONIZATION



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
Supply Voltages . . . . . -0.5V to +7.0V
All Input and Output Voltages. . . . . -0.5V to V_{CC}
Power Dissipation . . . . . 1.0 W

* **NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

D.C. CHARACTERISTICS (V_{CC} = 5V±10%, T_A = 0°C to 70°C)

Symbol	Parameter		Min.	Max.	Units	Test Conditions
I_F	Forward Input Current	$\overline{\text{ASYNC}}$ Other Inputs		-1.3 -0.5	mA mA	V_F = 0.45V V_F = 0.45V
I_R	Reverse Input Current	$\overline{\text{ASYNC}}$ Other Inputs		50 50	μA μA	$V_R = V_{CC}$ V_R = 5.25V
V_C	Input Forward Clamp Voltage			-1.0	V	I_C = -5mA
I_{CC}	Power Supply Current			162	mA	
V_{IL}	Input LOW Voltage			0.8	V	
V_{IH}	Input HIGH Voltage		2.0		V	
V_{IHR}	Reset Input HIGH Voltage		2.6		V	
V_{OL}	Output LOW Voltage			0.45	V	I_{OL} = 5mA
V_{OH}	Output HIGH Voltage	CLK Other Outputs	4 2.4		V V	I_{OH} = -1mA I_{OH} = -1mA
$V_{IHR}-V_{ILR}$	$\overline{\text{RES}}$ Input Hysteresis		0.25		V	

A.C. CHARACTERISTICS (V_{CC} = 5V±10%, T_A = 0°C to 70°C)

TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{EHEL}	External Frequency HIGH Time	13		ns	(90% - 90%)V_{IN}
t_{ELEH}	External Frequency LOW Time	13		ns	(10% - 10%)V_{IN}
t_{ELEL}	EFI Period (Note 1)	40		ns	For MBL 8284A
		33			For MBL 8284A-1
	XTAL Frequency	12	25	MHz	For MBL 8284A
			30		For MBL 8284A-1
t_{R1VCL}	RDY1, RDY2 Active Setup to CLK	35		ns	$\overline{ASYNC}$ = HIGH
t_{R1VCH}	RDY1, RDY2 Active Setup to CLK	35		ns	$\overline{ASYNC}$ = LOW
t_{R1VCL}	RDY1, RDY2 Inactive Setup to CLK	35		ns	
t_{CLR1X}	RDY1, RDY2 Hold to CLK	0		ns	
t_{AYVCL}	$\overline{ASYNC}$ Setup to CLK	50		ns	
t_{CLAYX}	$\overline{ASYNC}$ Hold to CLK	0		ns	
t_{A1VR1V}	$\overline{AEN1}$, $\overline{AEN2}$ Setup to RDY1, RDY2	15		ns	
t_{CLA1X}	$\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK	0		ns	
t_{YHEH}	CSYNC Setup to EFI	20		ns	
t_{EHYL}	CSYNC Hold to EFI	10		ns	
t_{YHYL}	CSYNC Width	$2 \cdot t_{ELEL}$		ns	
t_{I1HCL}	$\overline{RES}$ Setup to CLK	65		ns	(Note 1)
t_{CLI1H}	$\overline{RES}$ Hold to CLK	20		ns	(Note 1)

A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

Symbol	Parameter	MBL 8284A Min.	MBL 8284A-1 Min.	Max.	Units	Test Conditions
t_{CLCL}	CLK Cycle Period	125	100		ns	
t_{CHCL}	CLK HIGH Time	$(\frac{1}{3}\ t_{CLCL})+2$	39		ns	
t_{CLCH}	CLK LOW Time	$(\frac{2}{3}\ t_{CLCL})-15$	53		ns	
t_{CH1CH2}	CLK Rise Time			10	ns	From 1.0V to 3.5V
t_{CL2CL2}	CLK Fall time			10	ns	From 3.5V to 1.0V
t_{PHPL}	PCLK HIGH Time	$t_{CLCL}-20$	$t_{CLCL}-20$		ns	
t_{PLPH}	PCLK LOW Time	$t_{CLCL}-20$	$t_{CLCL}-20$		ns	
t_{RYLCL}	Ready Inactive to CLK	-8	-8		ns	(Note 3)
t_{RYHCH}	Ready Active to CLK	$(\frac{2}{3}\ t_{CLCL})-15$	53		ns	(Note 2)
t_{CLIL}	CLK to Reset Delay			40	ns	
t_{CLPH}	CLK to PCLK HIGH Delay			22	ns	
t_{CLPL}	CLK to PCLK LOW Delay			22	ns	
t_{OLCH}	OSC to CLK HIGH Delay	-5	-5	22	ns	
t_{OLCL}	OSC to CLK LOW Delay	2	-2	35	ns	
t_{OLOH}	Output Rise Time (except CLK)			20	ns	From 0.8V to 2.0V
t_{OHOL}	Output Fall Time (except CLK)			12	ns	From 2.0V to 0.8V

NOTES:
1. Setup and hold necessary only to guarantee recognition at next clock.
2. Applies only to T_3 and T_w states.
3. Applies only to T_2 states.

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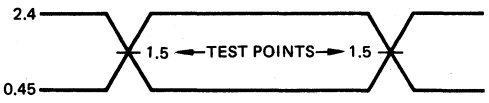
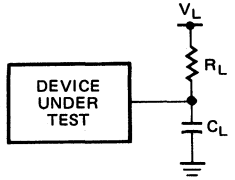
A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".timing measurements are made at 1.5V for both a logic "1" and "0". Input rise and fall times (measured between 0.8V and 2.0V) are 5±2ns.

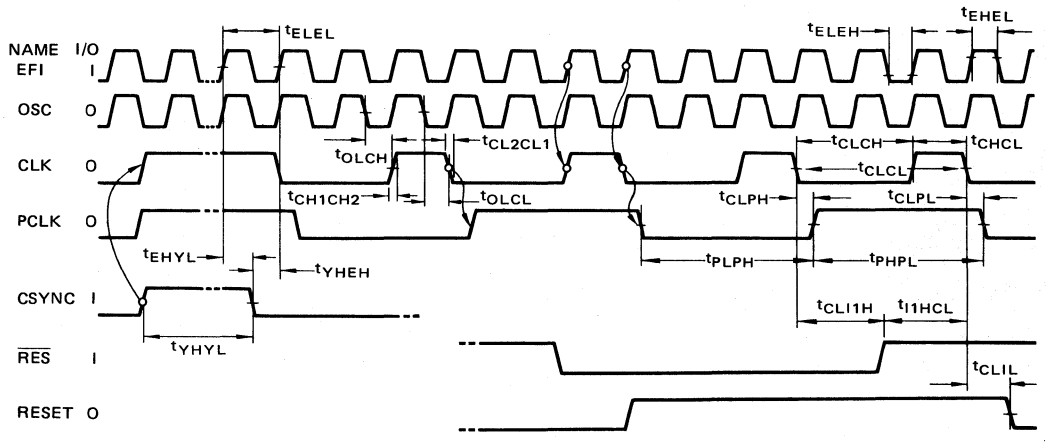
A.C. TESTING LOAD CIRCUIT



	V_L(V)	R_L(Ω)	C_L(pF)
CLK	3.41V	590	100
READY	2.08V	325	30

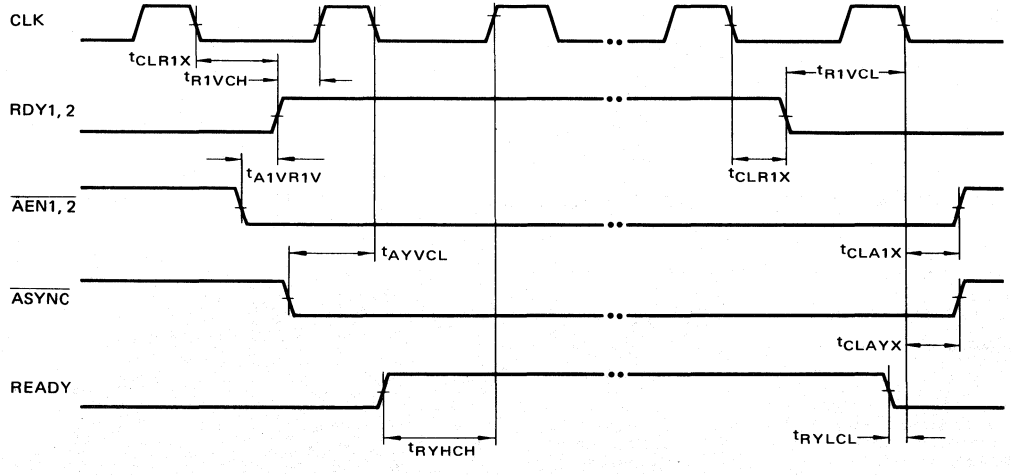
WAVEFORMS

CLOCKS AND RESET SIGNALS



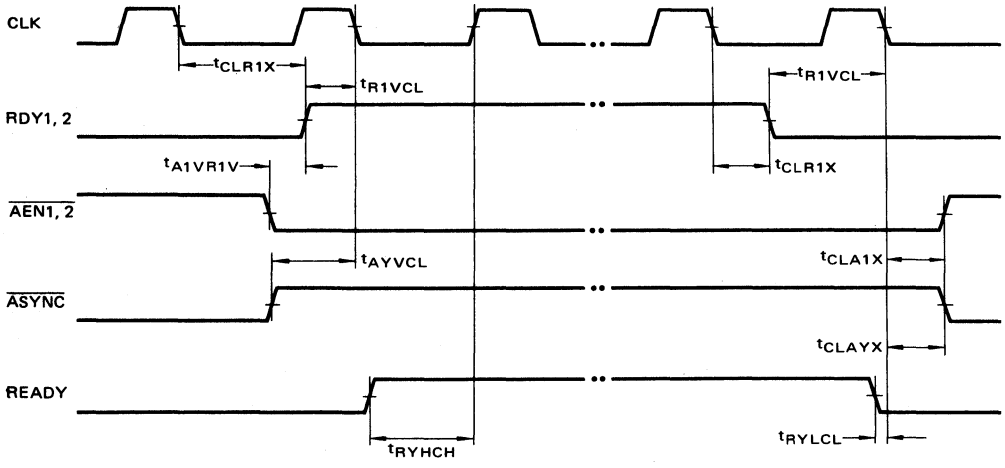
NOTE: All timing measurements are made at 1.5 volts, unless otherwise noted.

READY SIGNALS (FOR ASYNCHRONOUS DEVICES)

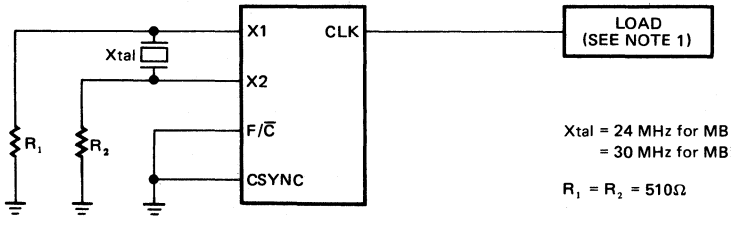


WAVEFORMS (Continued)

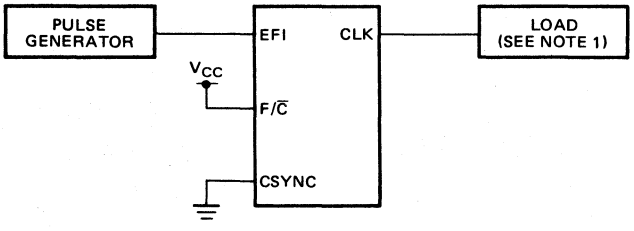
READY SIGNALS (FOR SYNCHRONOUS DEVICES)



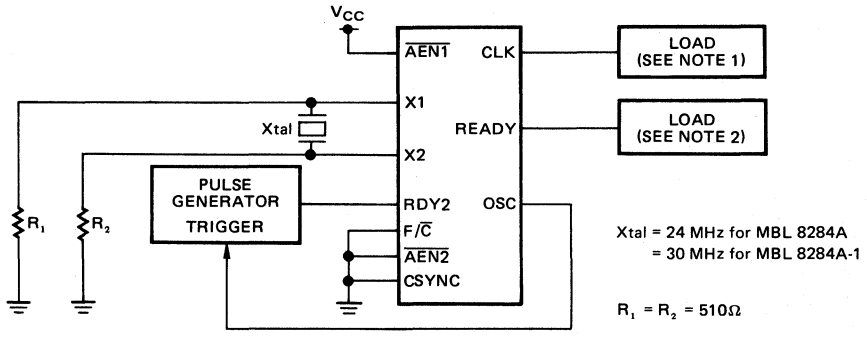
CLOCK HIGH AND LOW TIME (USING X1, X2)



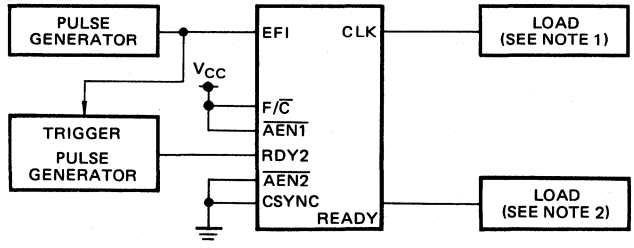
CLOCK HIGH AND LOW TIME (USING EFI)



READY TO CLOCK (USING X1, X2)



READY TO CLOCK (USING EFI)



NOTES:
1. C_L = 100 pF
2. C_L = 30 pF

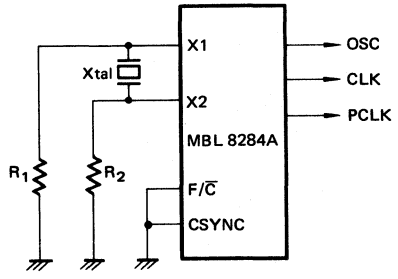
NOTES FOR USING MBL 8284A

For MBL 8284A's stable operation, the following things should be noted:

1. The fundamental mode crystal should be used.
2. Stray capacitances between X1 and X2 should be limited to less than 10pF.
3. External resistors for stable crystal oscillation should be connected as Configuration (I) or (II) shown below. Especially, for Configuration (I) circuit, the minimum frequency of crystal is limitted to 15MHz. A low frequency crystal (less than 15MHz) with Configuration (I) circuit may cause an abnormal oscillation. For more stable osciallation over the specified frequency range (12MHz to 25MHz or 30MHz), Configuration (II) circuit is recommendable.
4. The rise time of the power supply voltage V_{CC} should be more than 10ms. A steep V_{CC} rising (with the rise time less than 10ms) may cause an overtone oscillation.
5. In the power-on reset circuit shown below, the ground terminal of the external capacitor C should be grounded as near to the GND pin of MBL 8284A as possible.
6. When the crystal oscillator circuit is not used (i.e., an external clock source is used), X1 should be pulled up to V_{CC} with an approx. 1kΩ resistor and X2 should be left open. At this time, OSC output is clamped at high level.

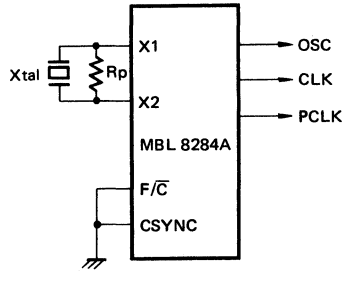
CRYSTAL OSCILLATOR CIRCUIT

• Configuration (I)



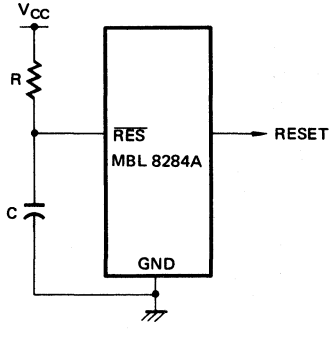
$R_1 = R_2 = 510\Omega$, Xtal = 15MHz to 25MHz (MBL 8284A)
= 15MHz to 30MHz (MBL 8284A-1)

• Configuration (II)

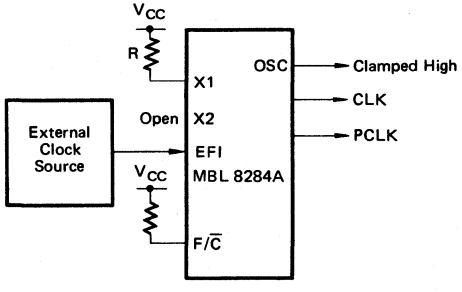


$R_p = 510\Omega$, Xtal = 12MHz to 25MHz (MBL 8284A)
= 12MHz to 30MHz (MBL 8284A-1)

POWER-ON RESET CIRCUIT



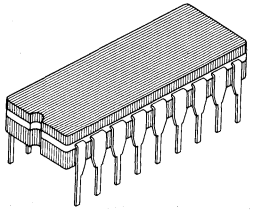
EXTERNAL CLOCK CONFIGURATION



R = 1kΩ, EFI ≤ 25MHz (MBL 8284A)
≤ 30MHz (MBL 8284A-1)

PACKAGE ILLUSTRATION

CERAMIC DIP
(CERDIP)



PACKAGE DIMENSIONS

CERAMIC DIP (Suffix: -CZ)

18-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-18C-C01)