FUJITSU

BUS CONTROLLER FOR MBL 8086/MBL 8088 /MBL 8089 PROCESSORS

MBL 8288

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Edition 3.0

BUS CONTROLLER
FOR MBL 8086/MBL 8088/MBL 8089 PROCESSORS

The Fujitsu MBL 8288 Bus Controller is a 20-pin bipolar component for use with medium-to-large MBL 8086/MBL 8088 processing systems. The bus controller provides command and control timing generation as well as bipolar bus drive capability while optimizing system performance.

A strapping option on the bus controller configures it for use with a multi-master system bus and separate I/O bus.

- **Bipolar Drive Capability**
- **Provides Advanced Commands**
- **Provides Wide Flexibility in System Configurations**
- **3-State Command Output Drivers**
- **Configurable for Use with an I/O Bus**
- **Facilitates Interface to One or Two Multi-Master Busses**
- **10 MHz Clock Rate**
- **Standard 20-pin Cerdip (Suffix-CZ)**

Fig. 1 – BLOCK DIAGRAM

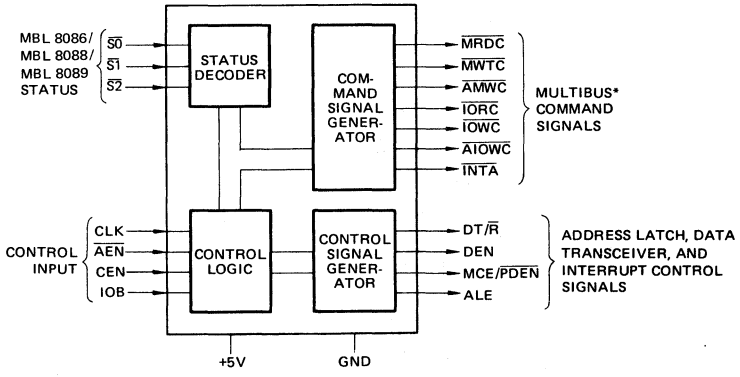
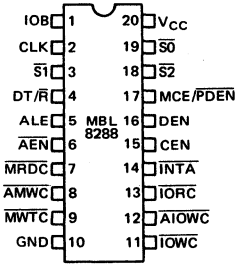


Fig. 2 – PIN ASSIGNMENT



*Trade Mark of Intel Corporation, USA.

TABLE 1 – PIN DESCRIPTION

Symbol	Type	Name and Function
V_{CC}		**Power:** +5V supply
GND		**Ground**
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	I	**Status Input Pins:** These pins are the status input pins from the MBL 8086, MBL 8088 or MBL 8089 processors. The MBL 8288 decodes these inputs to generate command and control signals at the appropriate time. When these pins are not in use (passive) they are all HIGH. (See chart under Command and Control Logic.)
CLK	I	**Clock:** This is a clock signal from the MBL 8284 clock generator and serves to establish when command and control signals are generated.
ALE	O	**Address Latch Enable:** This signal serves to strobe and address into the address latches. This signal is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches.
DEN	O	**Data Enable:** This signal serves to enable data transceivers onto either the local or system data bus. This signal is active HIGH.
DT/$\overline{R}$	O	**Data Transmit/Receive:** This signal establishes the direction of data flow through the transceivers. A HIGH on this line indicates Transmit (Write to I/O or memory) and a LOW indicates Receive (Read).
$\overline{AEN}$	I	**Address Enable:** $\overline{AEN}$ enables command outputs of the MBL 8288 Bus Controller at least 85 ns after it becomes active (LOW). $\overline{AEN}$ going inactive immediately 3-states the command output drivers. $\overline{AEN}$ does not affect the I/O command lines if the MBL 8288 is in the I/O Bus mode (IOB tied HIGH).
CEN	I	**Command Enable:** When this signal is LOW all MBL 8288 command outputs and the DEN and $\overline{PDEN}$ control outputs are forced to their inactive state. When this signal is HIGH, these same outputs are enabled.
IOB	I	**Input/Output Bus Mode:** When the IOB is strapped HIGH the MBL 8288 functions in the I/O Bus mode. When it is strapped LOW, the MBL 8288 functions in the System Bus mode. (See sections on I/O Bus and System Bus modes).
$\overline{AIOWC}$	O	**Advanced I/O Write Command:** The $\overline{AIOWC}$ issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AIOWC}$ is active LOW.
$\overline{IOWC}$	O	**I/O Write Command:** This command line instructs an I/O device to read the data on the data bus. This signal is active LOW.
$\overline{IORC}$	O	**I/O Read Command:** This command line instructs an I/O device to drive its data onto the data bus. This signal is active LOW.
$\overline{AMWC}$	O	**Advanced Memory Write Command:** The $\overline{AMWC}$ issues a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction, its timing is the same as a read command signal, $\overline{AMWC}$ is active LOW.
$\overline{MWTC}$	O	**Memory Write Command:** This command line instructs the memory to record the data present on the data bus. This signal is active LOW.
$\overline{MRDC}$	O	**Memory Read Command:** This command line instructs the memory to drive its data onto the data bus. This signal is active LOW.
$\overline{INTA}$	O	**Interrupt Acknowledge:** This command line tells an interrupting device that its interrupt has been acknowledged and that it should drive vectoring information onto the data bus. This signal is active LOW.
MCE/$\overline{PDEN}$	O	This is a dual function pin. **MCE (IOB is tied LOW):** Master Cascade Enable occurs during an interrupt sequence and serves to read a Cascade Address from a master PIC (Priority Interrupt Controller) onto the data bus. The MCE signal is active HIGH. **$\overline{PDEN}$ (IOB is tied HIGH):** Peripheral Data Enable enables the data bus transceiver for the I/O bus that DEN performs for the system bus. $\overline{PDEN}$ is active LOW.

FUNCTIONAL DESCRIPTION

COMMAND AND CONTROL LOGIC

The command logic decodes the three MBL 8086, MBL 8088 or MBL 8089 CPU status lines ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) to determine what command is to be issued.
This chart shows the meaning of each status "word".

$\overline{S0}$ $\overline{S1}$ $\overline{S2}$	Processor State	MBL 8288 Command
0 0 0	Interrupt Acknowledge	$\overline{INTA}$
0 0 1	Read I/O Port	$\overline{IORC}$
0 1 0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0 1 1	Halt	None
1 0 0	Code Access	$\overline{MRDC}$
1 0 1	Read Memory	$\overline{MRDC}$
1 1 0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1 1 1	Passive	None

The command is issued in one of two ways dependent on the mode of the MBL 8288 Bus Controller.
I/O Bus Mode – The MBL 8288 is in the I/O Bus mode if the IOB pin is strapped HIGH. In the I/O Bus mode all I/O command lines ($\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) are always enabled (i.e., not dependent on $\overline{AEN}$). When an I/O command is initiated by the processor, the MBL 8288 immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one MBL 8288 Bus Controller to handle two external busses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a "Bus Ready" signal ($\overline{AEN}$ LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or peripherals dedicated to one processor exist in a multi-processor system.
System Bus Mode – The MBL 8288 is in the System Bus mode if the IOB pin is strapped LOW. In this mode no command is issued until 85 ns after the $\overline{AEN}$ Line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the $\overline{AEN}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

COMMAND OUTPUTS

The advanced write commands are made available to initiate write procedures early in the machine cycle. This signal can be used to prevent the processor from entering an unnecessary wait state.

The command outputs are:

- $\overline{MRDC}$ – Memory Read Command
- $\overline{MWTC}$ – Memory Write Command
- $\overline{IORC}$ – I/O Read Command
- $\overline{IOWC}$ – I/O Write Command
- $\overline{AMWC}$ – Advanced Memory Write Command
- $\overline{AIOWC}$ – Advanced I/O Write Command
- $\overline{INTA}$ – Interrupt Acknowledge

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

CONTROL OUTPUTS

The control outputs of the MBL 8288 are Data Enable (DEN), Data Transmit/Receive (DT/$\overline{R}$) and Master Cascade Enable/Peripheral Data Enable (MCE/$\overline{PDEN}$). The DEN signal determines when the external bus should be enabled onto the local bus and the DT/$\overline{R}$ determines the direction of data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The MCE/$\overline{PDEN}$ pin changes function with the two modes of the MBL 8288. When the MBL 8288 is in the IOB mode (IOB HIGH) the $\overline{PDEN}$ signal serves as a dedicated data enable signal for the I/O or Peripheral System bus.

INTERRUPT ACKNOWLEDGE AND MCE

The MCE signal is used during an interrupt acknowledge cycle if the MBL 8288 is in the System Bus mode (IOB LOW). During any interrupt sequence there are two interrupt acknowledge cycles that occur back to back. During the first interrupt cycle no data or address transfers take place. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

If the system contains only one PIC, the MCE signal is not used. In this case the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

ADDRESS LATCH ENABLE AND HALT

Address Latch Enable (ALE) occurs during each machine cycle and serves to strobe the current address into the address latches. ALE also serves to strobe the status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) into a latch for halt state decoding.

COMMAND ENABLE

The Command Enable (CEN) input acts as a command qualifier for the MBL 8288. If the CEN pin is high the MBL 8288 functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
All Output and Supply Voltages . . . . . -0.5V to +7.0V
All Input Voltages . . . . . -0.5V to +5.5V
Power Dissipation . . . . . 1.5 W

* **NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (V_{CC}=5V±10%, T_A=0°C to 70°C)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_C	Input Clamp Voltage		-1	V	I_C = -5 mA
I_{CC}	Power Supply Current		230	mA	
I_F	Forward Input Current		-0.7	mA	V_F = 0.45V
I_R	Reverse Input Current		50	μA	$V_R = V_{CC}$
V_{OL}	Output Low Voltage: Command Outputs Control Outputs		 0.5 0.5	 V V	 I_{OL} = 32 mA I_{OL} = 16 mA
V_{OH}	Output High Voltage: Command Outputs Control Outputs	 2.4 2.4		 V V	 I_{OH} = -5 mA I_{OH} = -1 mA
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
I_{OFF}	Output Off Current		100	μA	V_{OFF} = 0.4 to 5.25V

A.C. CHARACTERISTICS (V_{CC}=5V±10%, T_A=0°C to 70°C)

TIMING REQUIREMENTS

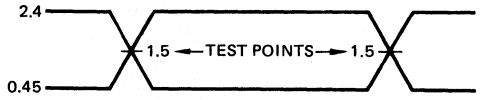
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
TCLCL	CLK Cycle Period	100		ns	
TCLCH	CLK Low Time	50		ns	
TCHCL	CLK High Time	30		ns	
TSVCH	Status Active Setup Time	35		ns	
TCHSV	Status Active Hold Time	10		ns	
TSHCL	Status Inactive Setup Time	35		ns	
TCLSH	Status Inactive Hold Time	10		ns	

A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

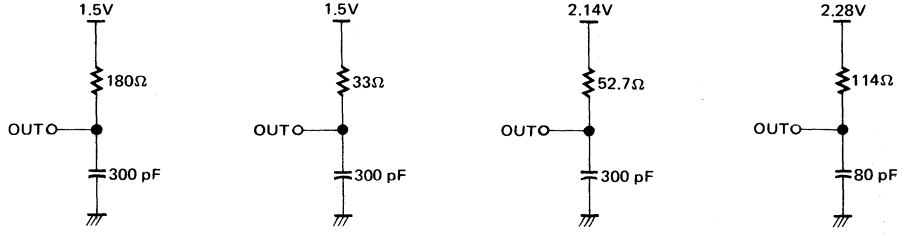
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
TCVNV	Control Active Delay	5	45	ns	
TCVNX	Control Inactive Delay	10	45	ns	
TCLLH, TCLMCH	ALE MCE Active Delay (from CLK)		20	ns	
TSVLH, TSVMCH	ALE MCE Active Delay (from Status)		20	ns	$\overline{MRDC}$, $\overline{IORC}$, $\overline{MWTC}$, $\overline{IOWC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{AIOWC}$: I_{OL} = 32 mA, I_{OH} = -5 mA, C_L = 300 pF
TCHLL	ALE Inactive Delay	4	15	ns	
TCLML	Command Active Delay	10	35	ns	
TCLMH	Command Inactive Delay	10	35	ns	
TCHDTL	Direction Control Active Delay		50	ns	
TCHDTH	Direction Control Inactive Delay		30	ns	
TAELCH	Command Enable Time		40	ns	Other: I_{OL} = 16 mA, I_{OH} = -1 mA, C_L = 80 pF
TAEHCZ	Command Disable Time		40	ns	
TAELCV	Enable Delay Time	85	200	ns	
TAEVNV	AEN to DEN		20	ns	
TCEVNV	CEN to DEN, PDEN		25	ns	
TCELRH	CEN to Command		TCLML	ns	
TOLOH	Output Rise Time		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12	ns	From 2.0V to 0.8V

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". The clock is driven at 4.3V and 0.25V. Timing measurements are made at 1.5V for both a logic "1" and "0". Input rise and fall times are 5±2ns, (measured between 0.8V and 2.0V.)

TEST LOAD CIRCUITS – 3-STATE COMMAND OUTPUT TEST LOAD



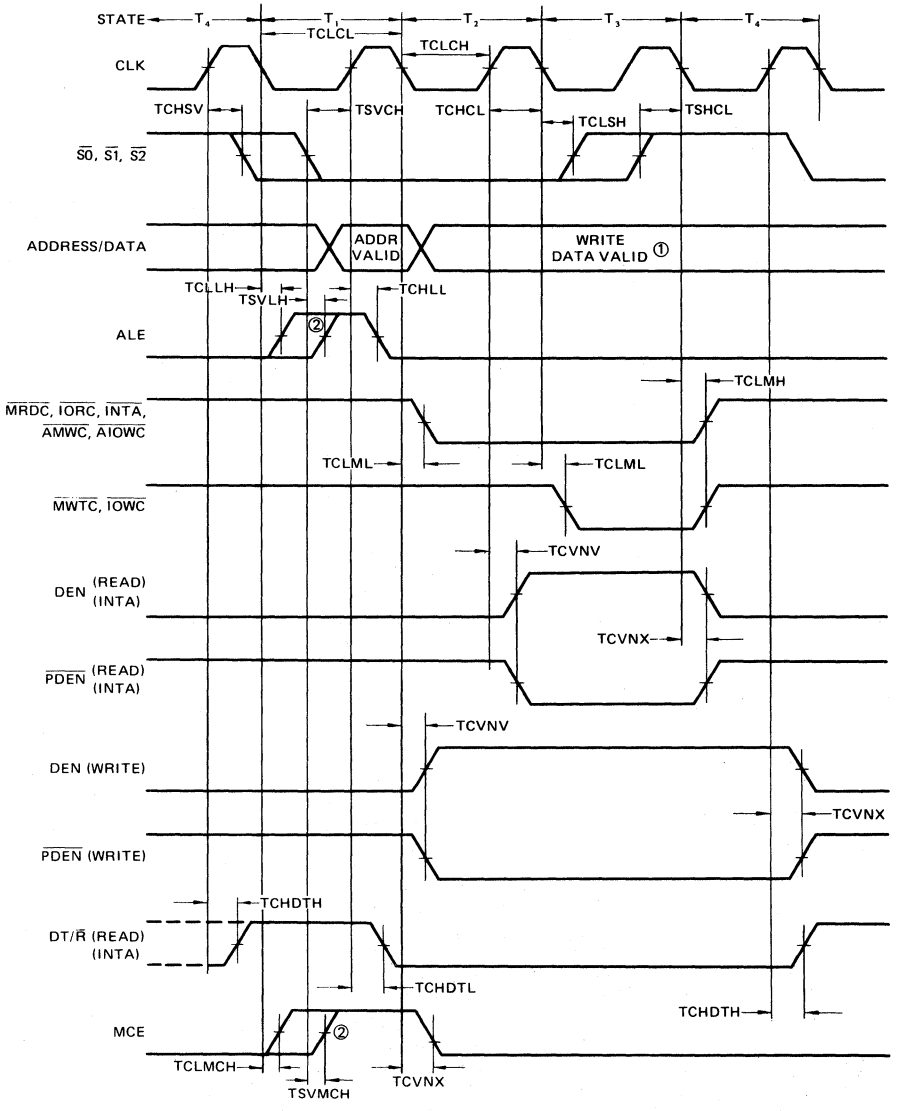
3-STATE TO HIGH

3-STATE TO LOW

COMMAND OUTPUT TEST LOAD

CONTROL OUTPUT TEST LOAD

WAVEFORMS

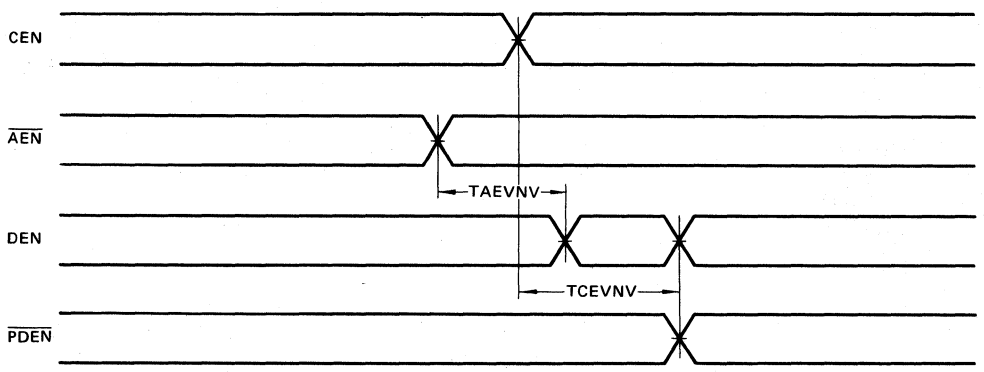


NOTES:

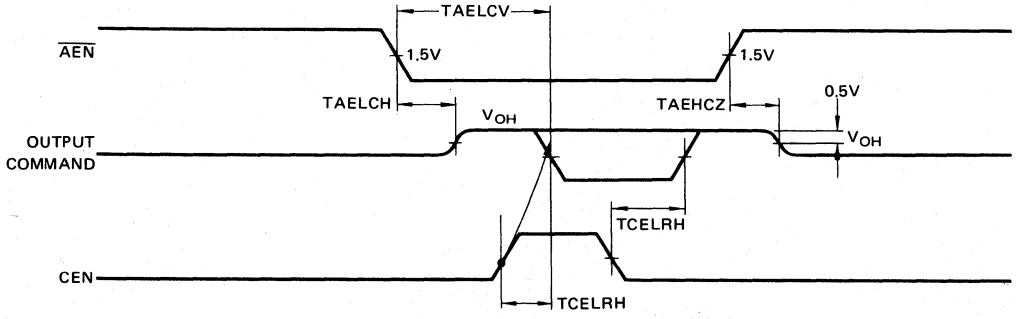
1. ADDRESS/DATA Bus is shown only for reference purposes.
2. Leading edge of ALE and MCE is determined by the falling edge of CLK or status going active, whichever occurs last.
3. All timing measurements are made at 1.5V unless specified otherwise.

WAVEFORMS (Continued)

DEN, $\overline{PDEN}$ QUALIFICATION TIMING



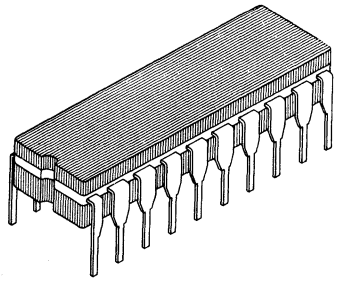
ADDRESS ENABLE (AEN) TIMING (3-STATE ENABLE/DISABLE)



NOTE: CEN must be low or valid prior to T2 to prevent the command from being generated.

PACKAGE ILLUSTRATION

CERAMIC PACKAGE
(CERDIP)



PACKAGE DIMENSIONS

(Suffix: -CZ)

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C01)