

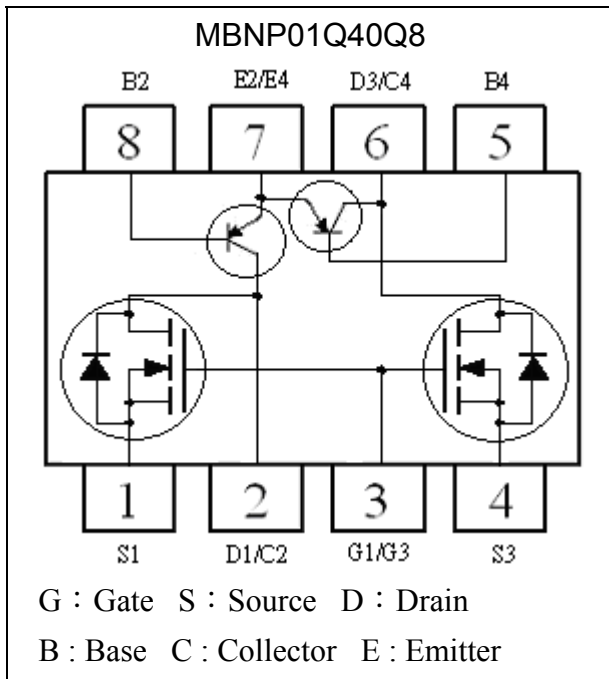
Complex Transistors

MBNP01Q40Q8

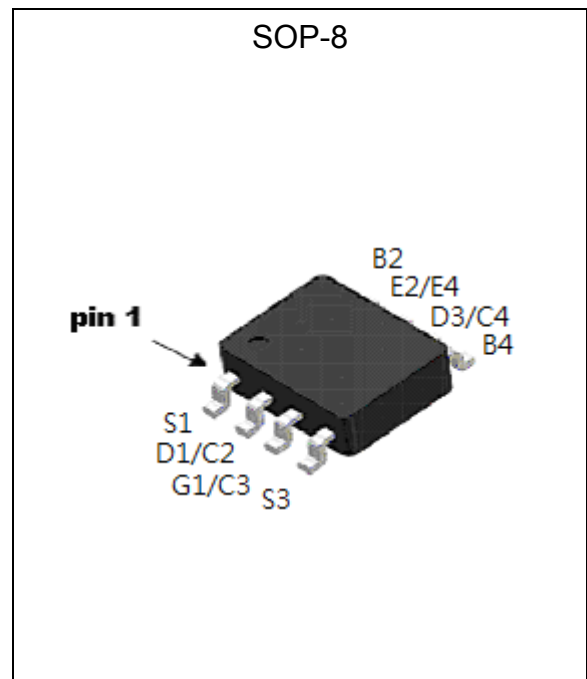
Features

- Two PNP and two NMOS chips are assembled in a standard SOP-8 package
- Mounting area could be greatly reduced.
- Pb-free lead plating and halogen-free package

Equivalent Circuit

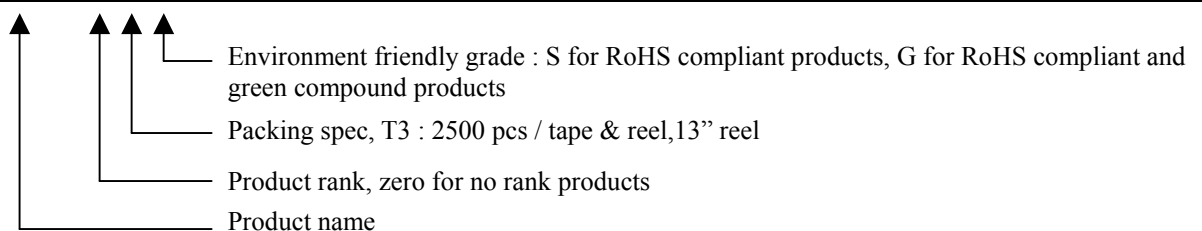


Outline



Ordering Information

Device	Package	Shipping
MBNP01Q40Q8-0-T3-G	SOP-8 (Pb-free lead plating & halogen-free package)	2500 pcs / Tape & Reel



**Absolute Maximum Ratings** ($T_C=25^{\circ}\text{C}$, unless otherwise noted)**NMOS**

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DS}	400	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current @ $T_A=25^{\circ}\text{C}$, $V_{GS}=10\text{V}$ (Note 2)	I_D	0.36	A
Continuous Drain Current @ $T_A=70^{\circ}\text{C}$, $V_{GS}=10\text{V}$ (Note 2)		0.29	
Pulsed Drain Current (Note 1)	I_{DM}	5.2	
Maximum Power Dissipation @ $T_A=25^{\circ}\text{C}$ (Note 2)	P_D	1.6	W
Linear Derating Factor		0.01	$\text{W}/^{\circ}\text{C}$
Operating Junction and Storage Temperature Range	T_j, T_{stg}	-55~+150	$^{\circ}\text{C}$

PNP

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	-400	V
Collector-Emitter Voltage	V_{CEO}	-400	
Emitter-Base Voltage	V_{EBO}	-5	
Collector Current	I_C	-300	mA
Total Power Dissipation	P_D	1.5	W
Linear Derating Factor		0.01	$\text{W}/^{\circ}\text{C}$
Operating Junction and Storage Temperature Range	T_j, T_{stg}	-55~+150	$^{\circ}\text{C}$

Thermal Data

Parameter	Symbol	Value		Unit
		NMOS	PNP	
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	6		$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-ambient, max	$R_{th,j-a}$	70 (Note 2)	83 (Note 2)	

- Note : 1.Pulse width limited by maximum junction temperature.
2.Surface mounted on 1 in² copper pad of FR-4 board, pulse width $\leq 10\text{s}$.



NMOS Electrical Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	400	-	-	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	1.0	-	2.5		V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	-	-	±100	nA	V _{GS} =±3V, V _{DS} =0V
	-	-	±10	μA	V _{GS} =±12V, V _{DS} =0V
I _{DSS}	-	-	100	nA	V _{DS} =320V, V _{GS} =0V
	-	-	10	μA	V _{DS} =320V, V _{GS} =0V, Tj=125°C
*R _{DS(ON)}	-	4.2	5.5	Ω	V _{GS} =10V, I _D =100mA
	-	4.2	5.5		V _{GS} =4.5V, I _D =100mA
*G _{FS}	-	300	-	mS	V _{DS} =10V, I _D =30mA
Dynamic					
C _{iss}	-	173	-	pF	V _{DS} =30V, V _{GS} =0V, f=1MHz
C _{oss}	-	20	-		
C _{rss}	-	19	-		
*t _{d(ON)}	-	3.4	-	ns	V _{DS} =200V, I _D =1A, V _{GS} =10V, R _G =6Ω
*t _r	-	5.8	-		
*t _{d(OFF)}	-	10.6	-		
*t _f	-	23.4	-		
*Q _g	-	7.5	-	nC	V _{DS} =320V, I _D =100mA, V _{GS} =10V
*Q _{gs}	-	0.7	-		
*Q _{gd}	-	3.2	-		
Body Diode					
*I _S	-	-	0.36	A	
*I _{SM}	-	-	5.2		
*V _{SD}	-	0.72	1	V	V _{GS} =0V, I _S =100mA
*t _{rr}	-	96	-	ns	I _F =0.5A, V _{GS} =0V, dI _F /dt=100A/μs
*Q _{rr}	-	67	-	nC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%



PNP Electrical Characteristics (Tj=25°C, unless otherwise specified)

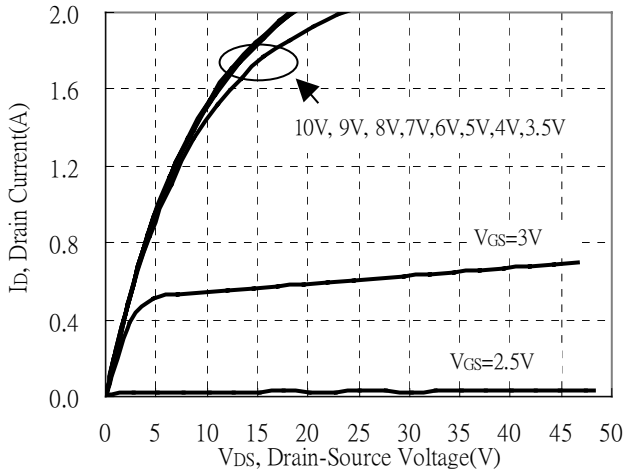
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CB0}	-400	-	-	V	I _C =-50μA
BV _{CEO}	-400	-	-	V	I _C =-1mA
BV _{EBO}	-5	-	-	V	I _E =-50μA
I _{CB0}	-	-	-100	nA	V _{CB} =-400V
I _{CES}	-	-	-100	nA	V _{CE} =-300V, R _{EB} =0Ω
I _{EBO}	-	-	-100	nA	V _{EB} =-5V
*V _{CE(sat)}	-	-0.17	-0.35	V	I _C =-20mA, I _B =-1mA
*V _{CE(sat)}	-	-0.18	-0.35	V	I _C =-50mA, I _B =-5mA
*V _{CE(sat)}	-	-0.18	-0.35	V	I _C =-100mA, I _B =-20mA
*V _{BE(sat)}	-	-0.73	-1	V	I _C =-20mA, I _B =-2mA
*h _{FE}	80	-	300	-	V _{CE} =-10V, I _C =-10mA
*h _{FE}	30	-	-	-	V _{CE} =-10V, I _C =-100mA
f _T	-	100	-	MHz	V _{CE} =-10V, I _C =-10mA, f=5MHz
Cob	-	4.6	-	pF	V _{CB} =-10V, I _E =0A, f=1MHz

*Pulse Test: Pulse Width ≤380μs, Duty Cycle≤2%

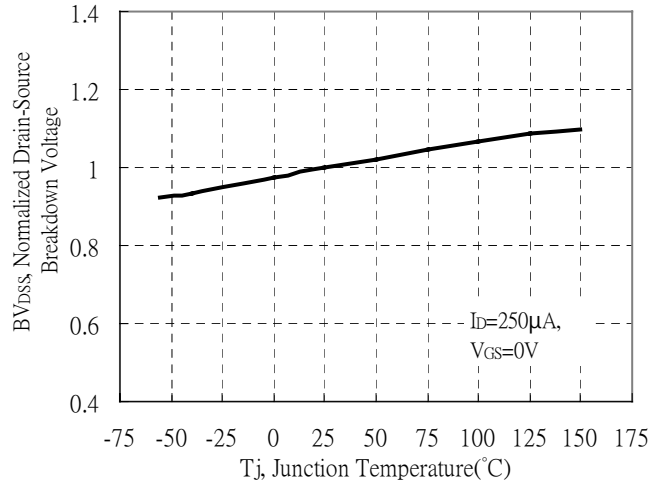


Typical Characteristics : NMOS

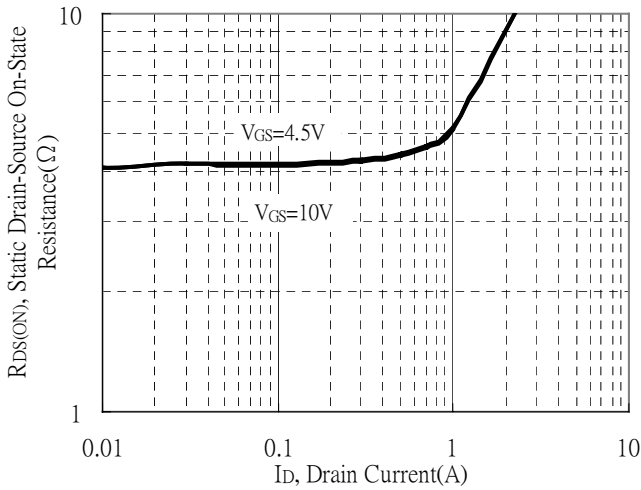
Typical Output Characteristics



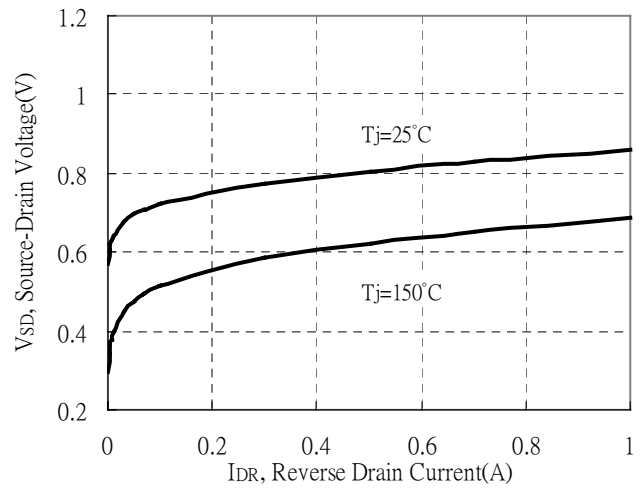
Brekdown Voltage vs Ambient Temperature



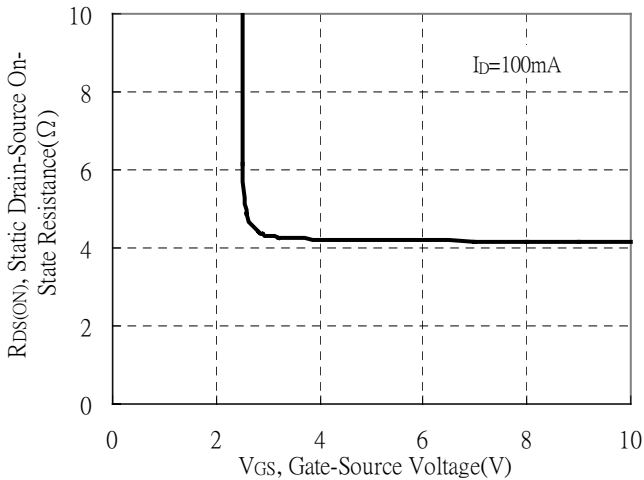
Static Drain-Source On-State resistance vs Drain Current



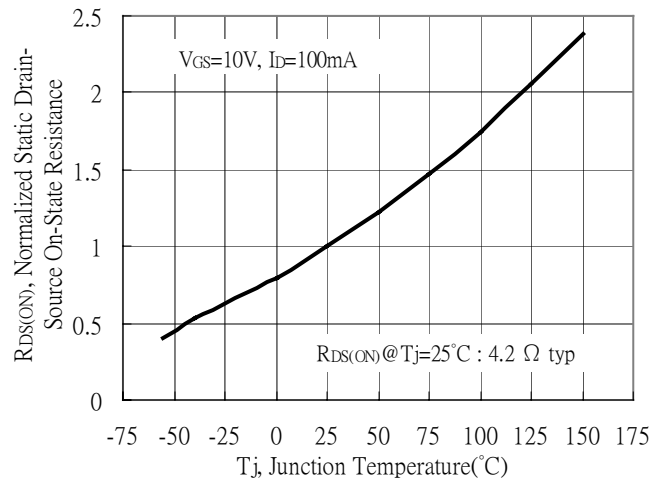
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

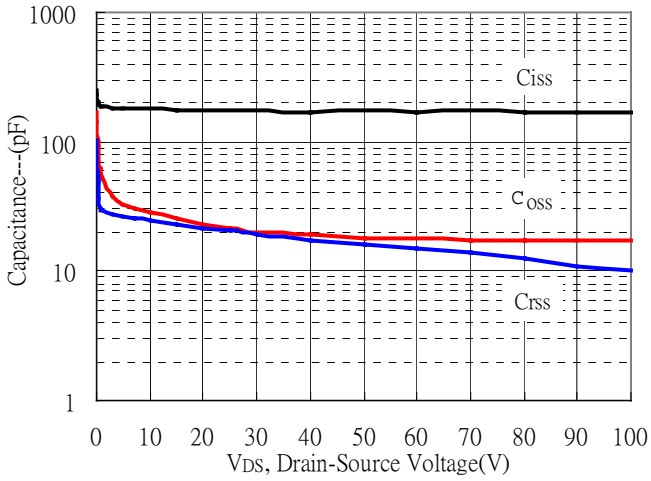


Drain-Source On-State Resistance vs Junction Temperature

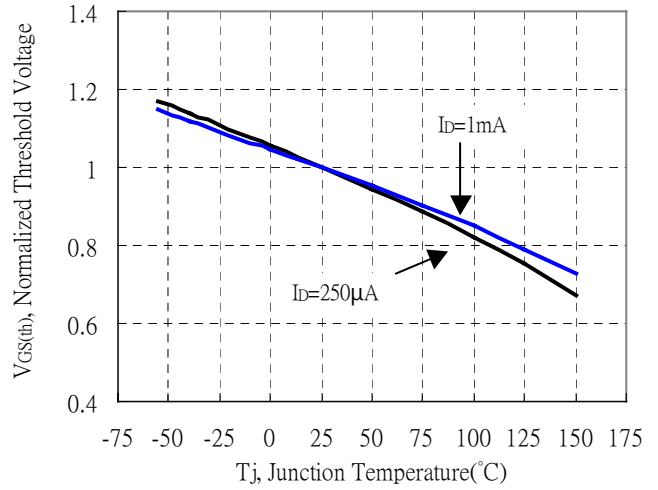


Typical Characteristics(Cont.) : NMOS

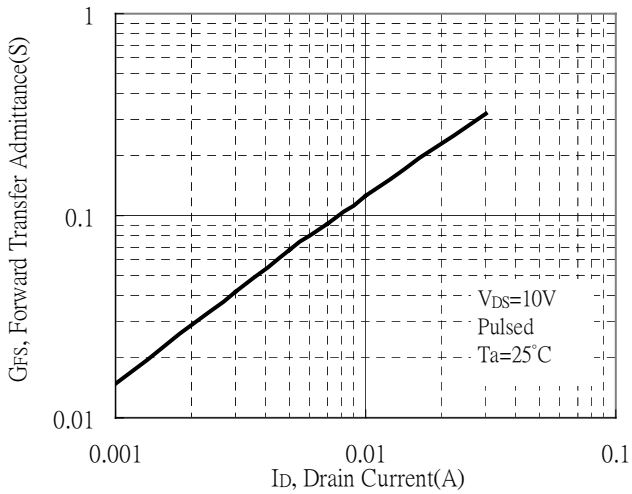
Capacitance vs Drain-to-Source Voltage



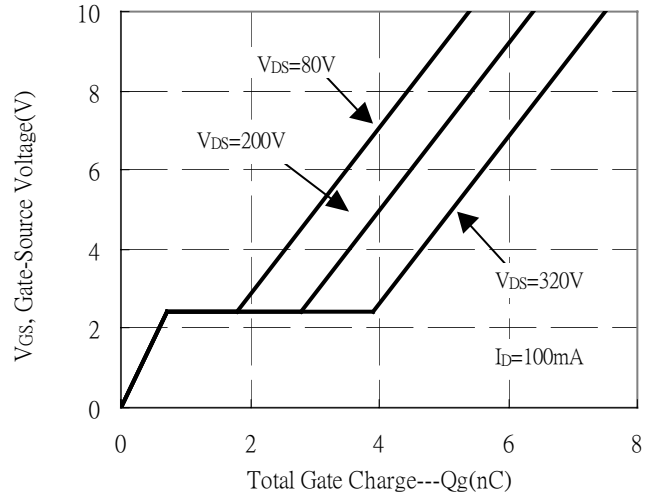
Normalized Threshold Voltage vs Junction Temperature



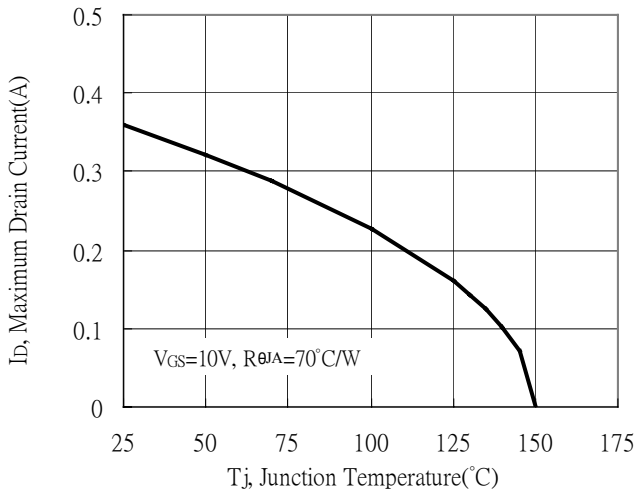
Forward Transfer Admittance vs Drain Current



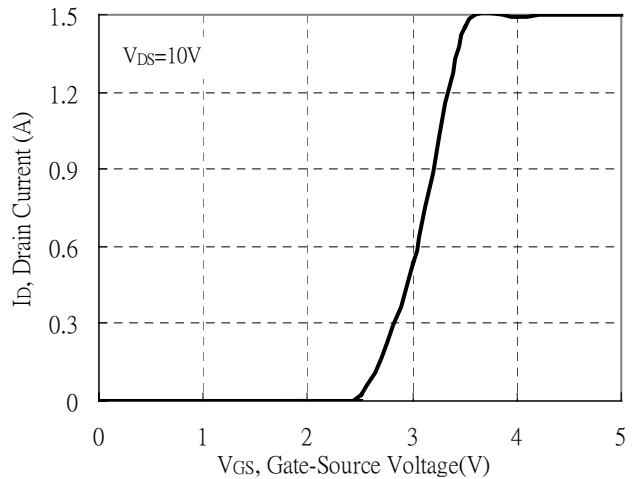
Gate Charge Characteristics



Maximum Drain Current vs Junction Temperature

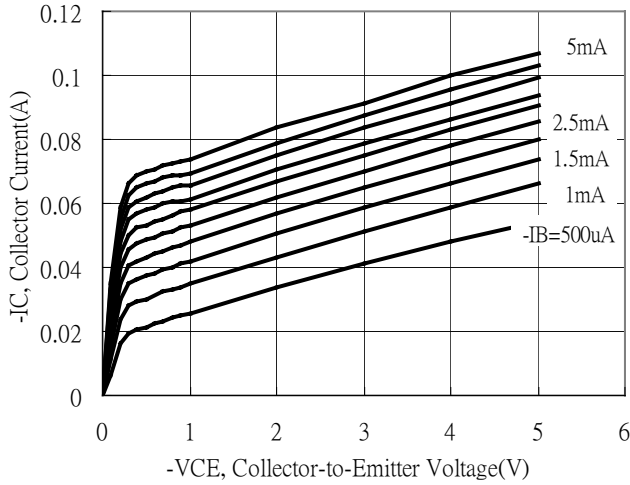


Typical Transfer Characteristics

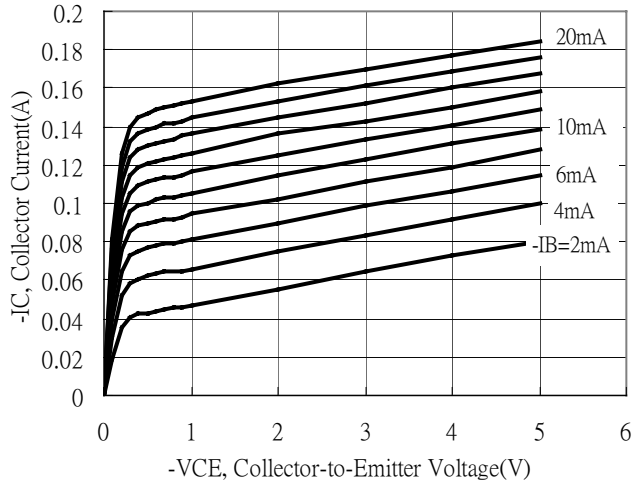


Typical Characteristics : PNP

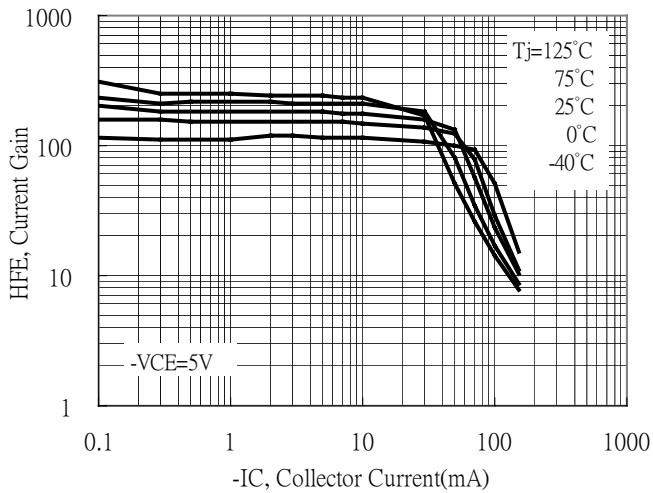
Emitter Grounded Output Characteristics



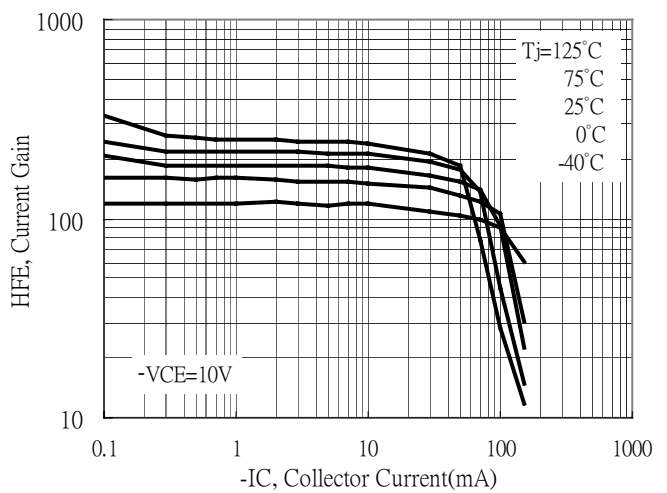
Emitter Grounded Output Characteristics



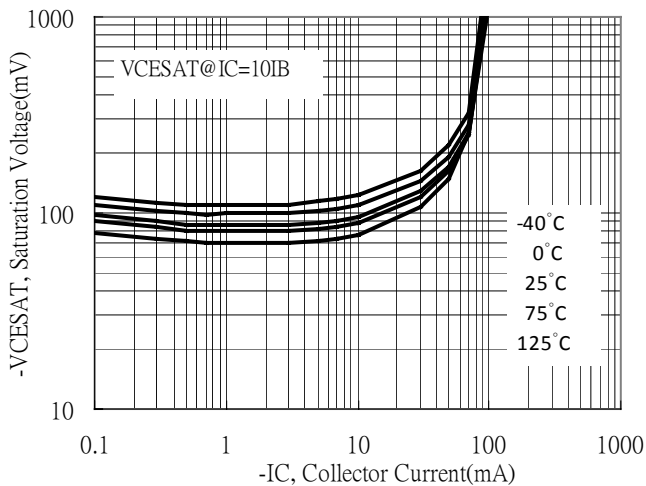
Current Gain vs Collector Current



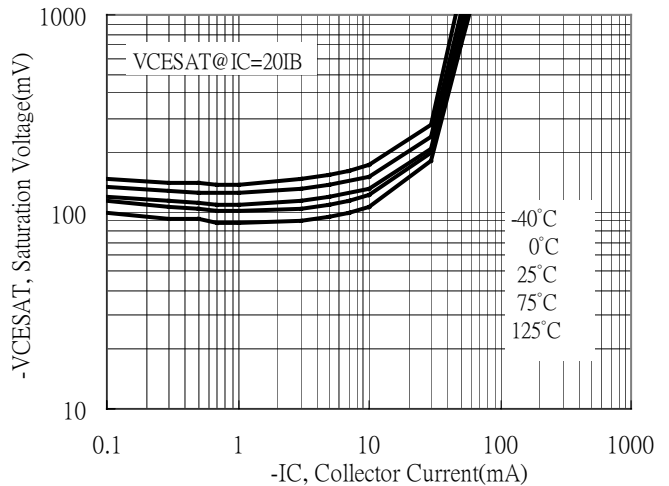
Current Gain vs Collector Current



Saturation Voltage vs Collector Current

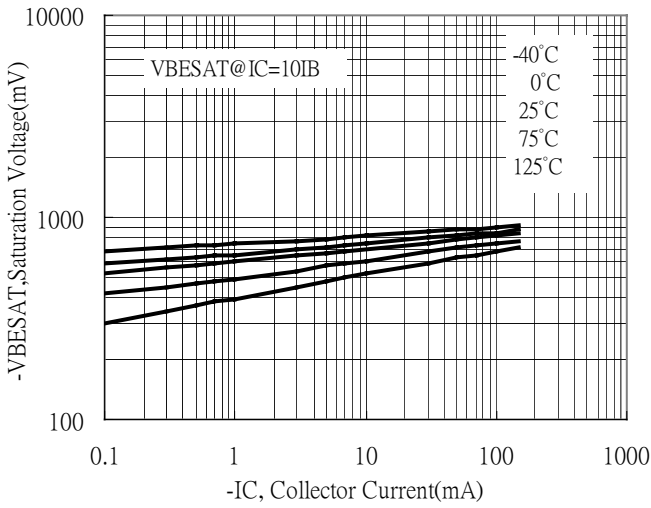


Saturation Voltage vs Collector Current

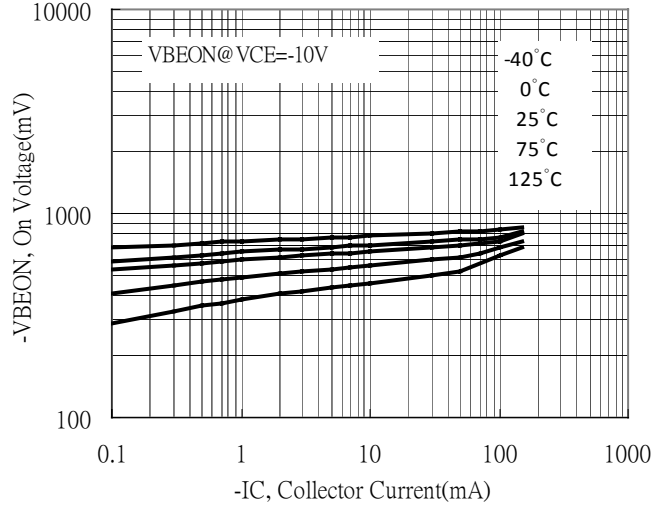


Typical Characteristics(Cont.) : FET 2

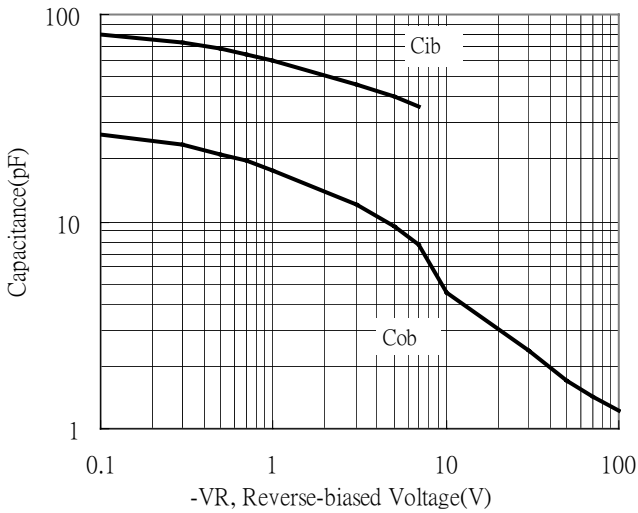
Saturation Voltage vs Collector Current



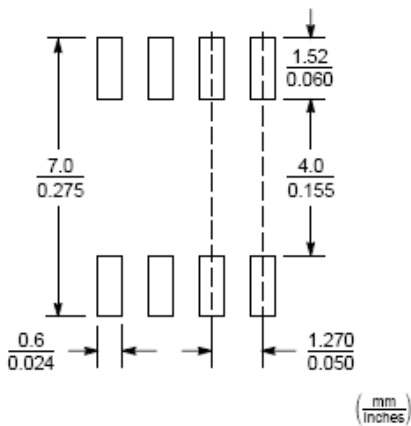
On Voltage vs Collector Current



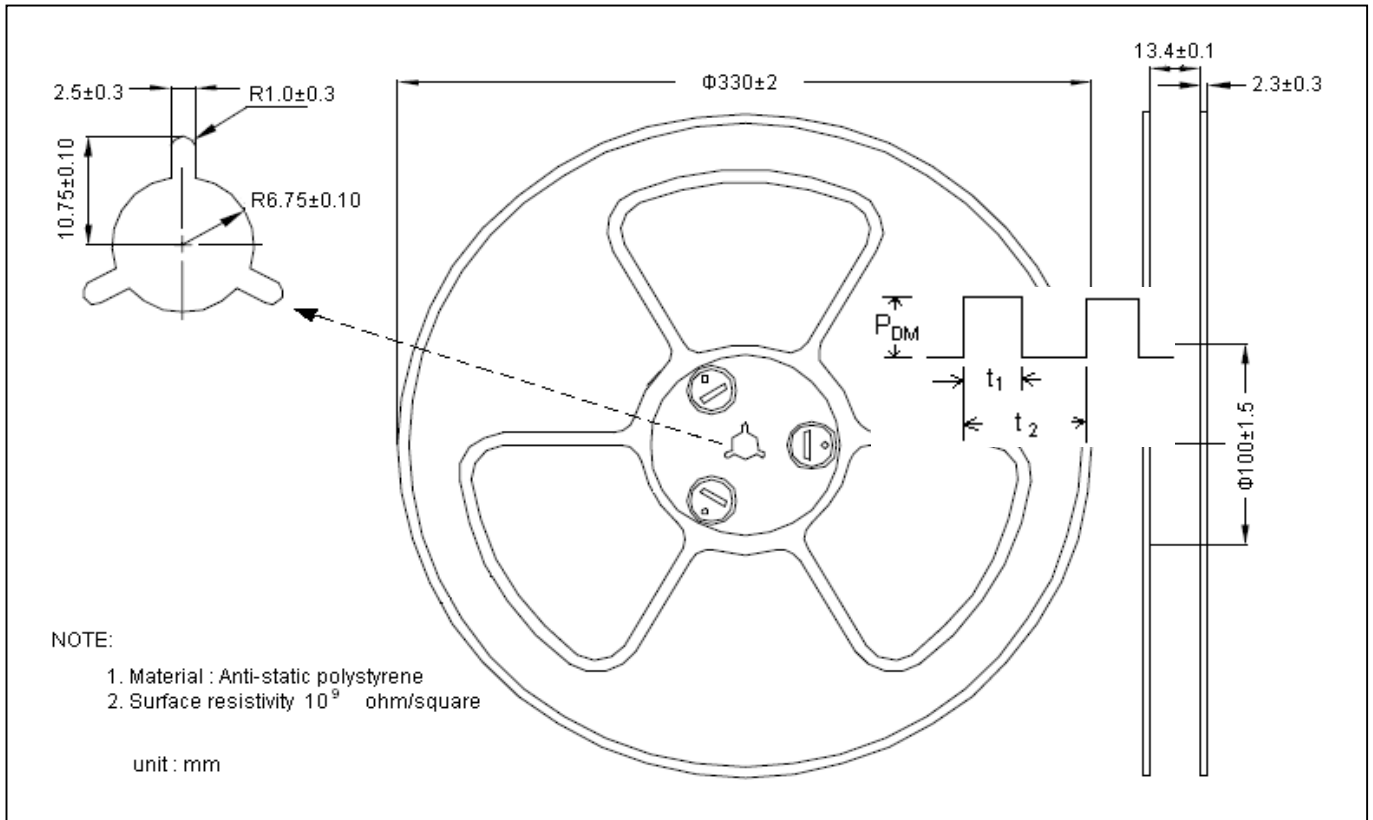
Capacitance vs Reverse-biased Voltage



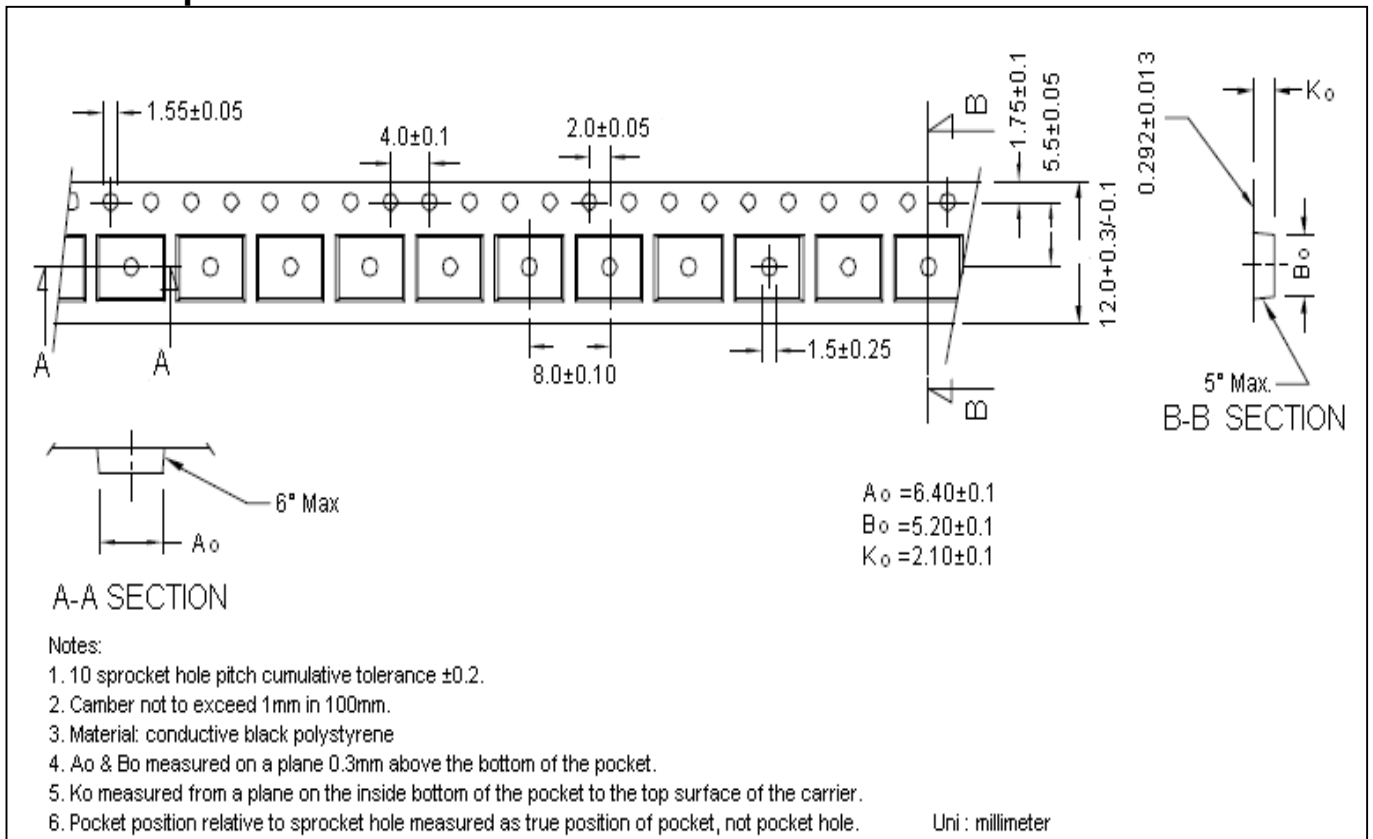
Recommended Soldering Footprint



Reel Dimension



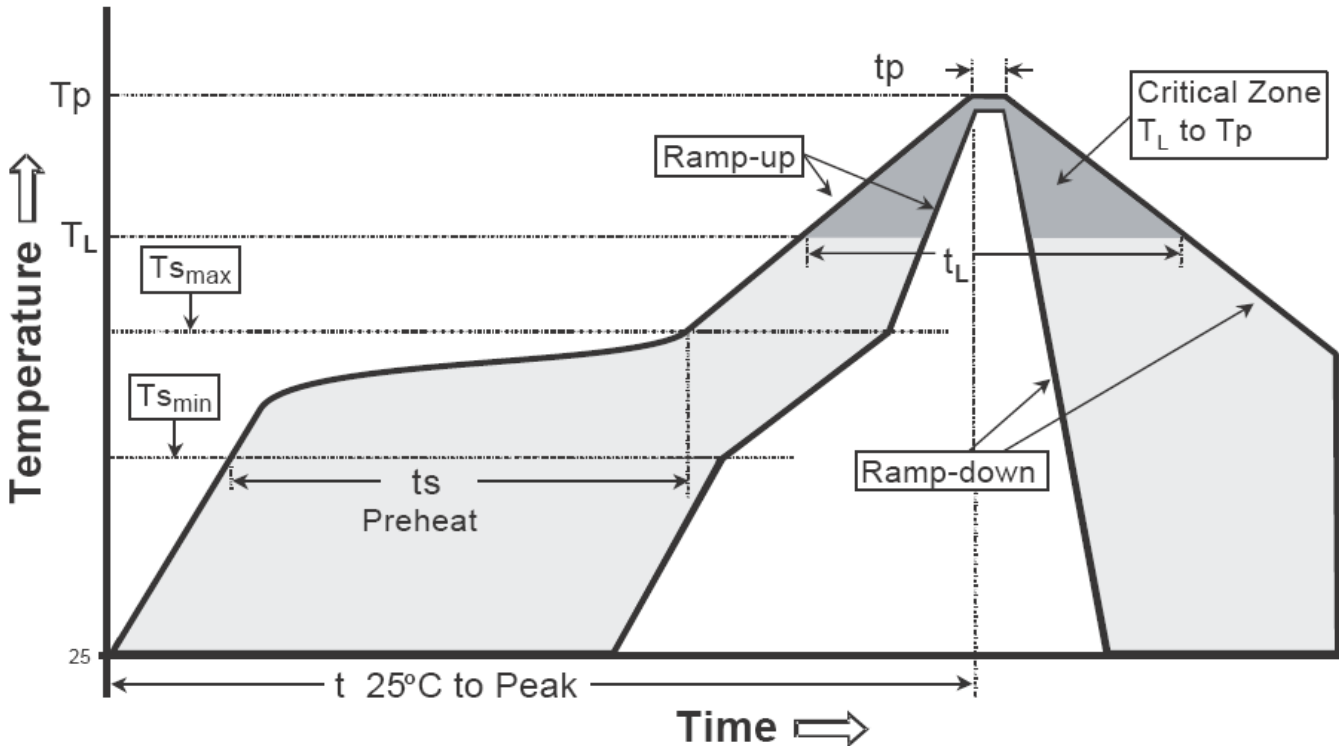
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

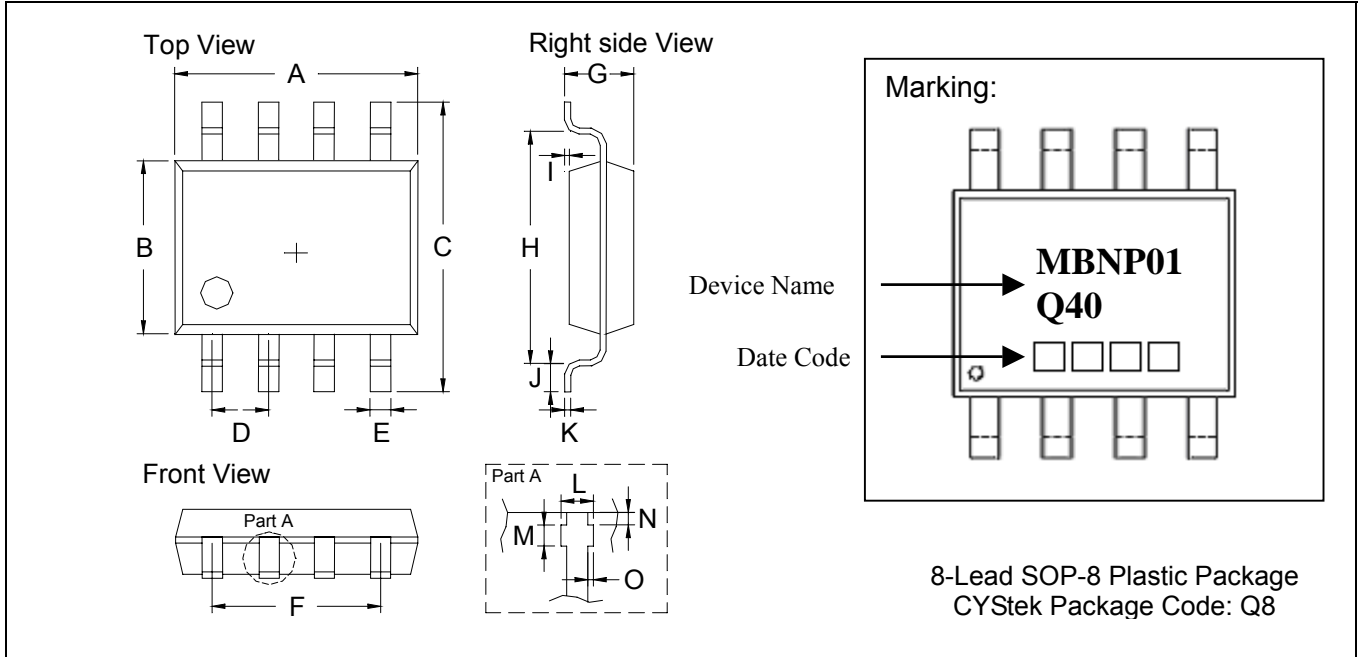
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOP-8 Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1909	0.2007	4.85	5.10	I	0.0019	0.0078	0.05	0.20
B	0.1515	0.1555	3.85	3.95	J	0.0118	0.0275	0.30	0.70
C	0.2283	0.2441	5.80	6.20	K	0.0074	0.0098	0.19	0.25
D	0.0480	0.0519	1.22	1.32	L	0.0145	0.0204	0.37	0.52
E	0.0145	0.0185	0.37	0.47	M	0.0118	0.0197	0.30	0.50
F	0.1472	0.1527	3.74	3.88	N	0.0031	0.0051	0.08	0.13
G	0.0570	0.0649	1.45	1.65	O	0.0000	0.0059	0.00	0.15
H	0.1889	0.2007	4.80	5.10					

Notes: 1. Controlling dimension: millimeters.
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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