5 V ECL 3-Bit Differential Flip-Flop

Description

The MC10E/100E431 is a 3-bit flip-flop with differential clock, data input and data output.

The asynchronous Set and Reset controls are edge-triggered rather than level controlled. This allows the user to rapidly set or reset the flip-flop and then continue clocking at the next clock edge, without the necessity of de-asserting the set/reset signal (as would be the case with a level controlled set/reset).

The E431 is also designed with larger internal swings, an approach intended to minimize the time spent crossing the threshold region and thus reduce the metastability susceptibility window.

The differential input structures are clamped so that the inputs of unused registers can be left open without upsetting the bias network of the device. The clamping action will assert the \overline{D} and the \overline{CLK} sides of the inputs. Because of the edge triggered flip-flop nature of the device simultaneously opening both the clock and data inputs will result in an output which reaches an unidentified but valid state. Note that the input clamps only operate when both inputs fall to 2.5 V below V_{CC} .

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a $0.01~\mu F$ capacitor and limit current sourcing or sinking to 0.5~mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

Features

- Edge-Triggered Asynchronous Set and Reset
- Differential D, CLK and Q; V_{BB} Reference Available
- 1100 MHz Min. Toggle Frequency
- PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -4.2 V to -5.7 V
- Internal Input 50 kΩ Pulldown Resistors
- ESD Protection:
 - ♦ > 2 kV Human Body Model
 - ♦ > 200 V Machine Model
 - → 2 kV Charged Device Model
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity: Level 3 (Pb-Free)
 (For Additional Information, see Application Note <u>AND8003/D</u>)
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 348 Devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



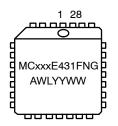
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PLCC-28 FN SUFFIX CASE 776-02

MARKING DIAGRAM*



xxx = 10 or 100

A = Assembly Location

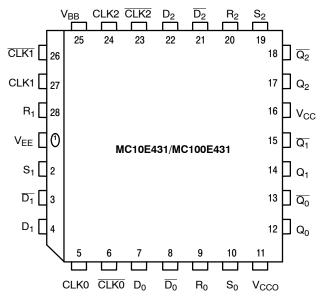
WL = Wafer Lot
 YY = Year
 WW = Work Week
 G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
MC10E431FNG	PLCC-28 (Pb-Free)	37 Units / Tube
MC10E431FNR2G	PLCC-28 (Pb-Free)	500 Tape & Reel
MC100E431FNR2G	PLCC-28 (Pb-Free)	500 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}For additional marking information, refer to Application Note AND8002/D.



^{*} All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC} , V_{CCO} , and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Pinout: PLCC-28 (Top View)

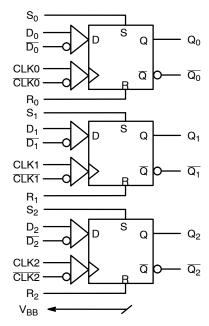


Figure 2. Logic Diagram

Table 1. PIN DESCRIPTION

PIN	FUNCTION
D[0:2], \overline{D} [0:2]	ECL Differential Data Inputs
CLK[0:2], CLK[0:2]	ECL Differential Clock
S[0:2]	ECL Edge Triggered Set Inputs
R[0:2]	ECL Edge Triggered Reset Input
Q[0:2], Q[0:2]	ECL Differential Data Outputs
V _{BB}	Reference Voltage Output
V _{CC} , V _{CCO}	Positive Supply
V _{EE}	Negative Supply

Table 2. FUNCTION TABLE

Dn	CLKn	Rn	Sn	Qn
L	Z	L	L	L
Н	Z	L	L	Н
Х	Х	Z	L	L
Х	Х	L	Z	Н

Z = Low to high transition

X = Don't Care

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		8	V
V _I	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	$V_{I} \leq V_{CC}$ $V_{I} \geq V_{EE}$	6 -6	V
l _{out}	Output Current	Continuous Surge		50 100	mA
I _{BB}	V _{BB} Sink/Source			±0.5	mA
T _A	Operating Temperature Range			0 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
$\theta_{\sf JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	PLCC-28 PLCC-28	63.5 43.5	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	PLCC-28	22 to 26	°C/W
T _{sol}	Wave Solder (Pb-Free)			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. 10E SERIES PECL DC CHARACTERISTICS (V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1))

			0°C		25°C			85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current		110	132		110	132		110	132	mA
V _{OH}	Output HIGH Voltage (Note 2)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V _{OL}	Output LOW Voltage (Note 2)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V _{IH}	Input HIGH Voltage (Single-Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V _{IL}	Input LOW Voltage (Single-Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V _{BB}	Output Voltage Reference	3.62		3.74	3.65		3.75	3.69		3.81	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.7		5.0	2.7		5.0	2.7		5.0	٧
I _{IH}	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 1. Input and output parameters vary 1:1 with $V_{CC}.\ V_{EE}$ can vary –0.46 V / +0.06 V.
- 2. Outputs are terminated through a 50 Ω resistor to V_{CC} 2.0 V.
- 3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

Table 5. 10E SERIES NECL DC CHARACTERISTICS (V_{CCx}= 0.0 V; V_{EE}= -5.0 V (Note 1)

		0°C		25°C			85°C				
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current		110	132		110	132		110	132	mA
V _{OH}	Output HIGH Voltage (Note 2)	-1020	-930	-840	-980	-895	-810	-910	-815	-720	mV
V _{OL}	Output LOW Voltage (Note 2)	-1950	-1790	-1630	-1950	-1790	-1630	-1950	-1773	-1595	mV
V _{IH}	Input HIGH Voltage (Single-Ended)	-1170	-1005	-840	-1130	-970	-810	-1060	-890	-720	mV
V _{IL}	Input LOW Voltage (Single-Ended)	-1950	-1715	-1480	-1950	-1715	-1480	-1950	-1698	-1445	mV
V_{BB}	Output Voltage Reference	-1.38		-1.27	-1.35		-1.25	-1.31		-1.19	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	-2.3		0.0	-2.3		0.0	-2.3		0.0	V
I _{IH}	Input HIGH Current			150			150			150	μА
I _{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 1. Input and output parameters vary 1:1 with V $_{CC}$. V $_{EE}$ can vary -0.46 V / +0.06 V.
- 2. Outputs are terminated through a 50 Ω resistor to V_{CC} 2.0 V.
- 3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

Table 6. 100E SERIES PECL DC CHARACTERISTICS (V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1))

		0°C		25°C			85°C				
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current		110	132		110	132		127	152	mA
V _{OH}	Output HIGH Voltage (Note 2)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V _{OL}	Output LOW Voltage (Note 2)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V _{IH}	Input HIGH Voltage (Single-Ended)	3835	3975	4120	3835	3975	4120	3835	3975	4120	mV
V _{IL}	Input LOW Voltage (Single-Ended)	3190	3355	3525	3190	3355	3525	3190	3355	3525	mV
V _{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.7		5.0	2.7		5.0	2.7		5.0	V
I _{IH}	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary -0.46~V / +0.8~V.
- 2. Outputs are terminated through a 50 Ω resistor to V_{CC} 2.0 V.
- 3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

Table 7. 100E SERIES NECL DC CHARACTERISTICS (V_{CCx} = 0.0 V; V_{EE} = -5.0 V (Note 1))

		0°C		25°C			85°C				
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current		110	132		110	132		127	152	mA
V _{OH}	Output HIGH Voltage (Note 2)	-1025	-950	-880	-1025	-950	-880	-1025	-950	-880	mV
V _{OL}	Output LOW Voltage (Note 2)	-1810	-1705	-1620	-1810	-1745	-1620	-1810	-1740	-1620	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1165	-1025	-880	-1165	-1025	-880	-1165	-1025	-880	mV
V _{IL}	Input LOW Voltage (Single-Ended)	-1810	-1645	-1475	-1810	-1645	-1475	-1810	-1645	-1475	mV
V _{BB}	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	-2.3		0.0	-2.3		0.0	-2.3		0.0	V
I _{IH}	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 1. Input and output parameters vary 1:1 with V $_{CC}$. V $_{EE}$ can vary -0.46 V / +0.8 V. 2. Outputs are terminated through a 50 Ω resistor to V $_{CC}$ 2.0 V. 3. V $_{IHCMR}$ min varies 1:1 with V $_{EE}$, max varies 1:1 with V $_{CC}$.

Table 8. AC CHARACTERISTICS (V_{CCx} = 5.0 V; V_{EE} = 0.0 V or V_{CCx} = 0.0 V; V_{EE} = -5.0 V (Note 1))

			-40°C			25°C		85°C				
Symbol	Characteristic		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f _{MAX}	Maximum Toggle Frequency						1.1					GHz
t _{PLH} t _{PHL}	Propagation Delay to Output CLK R S		550 500 500	700 725 725	850 975 975	550 550 550	700 725 725	850 925 925	550 550 550	700 725 725	850 925 925	ps
t _S	Setup Time D R (Note 2) S (Note 2)		250 1100 1100	0 700 700		200 1000 1000	0 700 700		200 1000 1000	0 700 700		ps
t _H	Hold Time	D	250	0		200	0		200	0		ps
t _{PW}	Minimum Pulse Width	CLK	400			400			400			ps
t _{skew}	Within-Device Skew (Note 3)			50						50		ps
t _{JITTER}	Random Clock Jitter (RMS)			< 1			< 1			< 1		ps
V _{PP}	Input Voltage Swing (Differential Configuration)		150		1000	150		1000	150		1000	mV
t _r /t _f	Rise/Fall Times (20-80%)		250	450	700				275	450	650	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

 ^{1. 10} Series: V_{EE} can vary -0.46 V / +0.06 V.
 1. 10 Series: V_{EE} can vary -0.46 V / +0.8 V.
 2. These setup times define the minimum time the CLK or SET/RESET input must wait after the assertion of the RESET/SET input to assure the proper operation of the flip-flop.

^{3.} Within-device skew is defined as identical transitions on similar paths through a device.

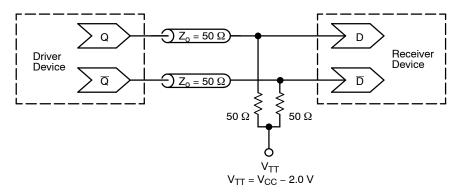


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note <u>AND8020/D</u> – Termination of ECL Logic Devices)

Resource Reference of Application Notes

AN1405/D - ECL Clock Distribution Techniques

AN1406/D - Designing with PECL (ECL at +5.0 V)

AN1503/D - ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D - Metastability and the ECLinPS Family

Interfacing Between LVDS and ECL

AN1672/D - The ECL Translator Guide

AND8001/D - Odd Number Counters Design

AND8002/D - Marking and Date Codes

AN1568/D

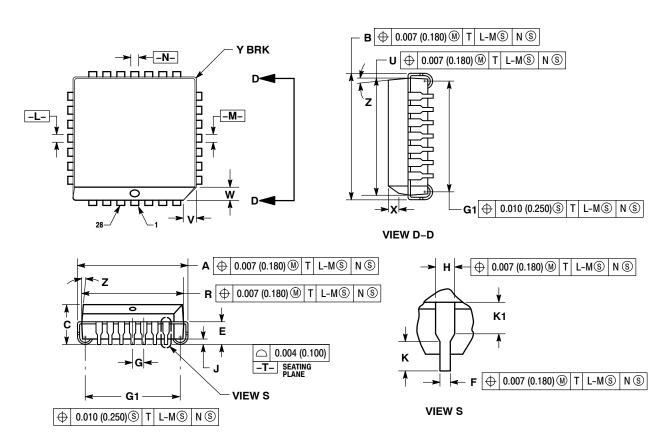
AND8020/D - Termination of ECL Logic Devices

AND8066/D - Interfacing with ECLinPS

AND8090/D - AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

28 LEAD PLLC **FN SUFFIX** CASE 776-02 **ISSUE F**



- O LES:

 1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.

 2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.

 3. DIMENSIONS R AND U DO NOT INCLUDE
- MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- ANSI Y14.5M, 1982.

 5. CONTROLLING DIMENSION: INCH.

 6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURDS. CATE PURPS AND INTERLIED. BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- PLASTIC BODY TO DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.485	0.495	12.32	12.57
В	0.485	0.495	12.32	12.57
С	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.021	0.33	0.53
G	0.050	BSC	1.27	BSC
Н	0.026	0.032	0.66	0.81
J	0.020		0.51	
K	0.025		0.64	
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
٧	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50
Z	2 °	10°	2 °	10°
G1	0.410	0.430	10.42	10.92
K1	0.040		1.02	

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