

## ÷2, ÷4, ÷8 Clock Generation Chip

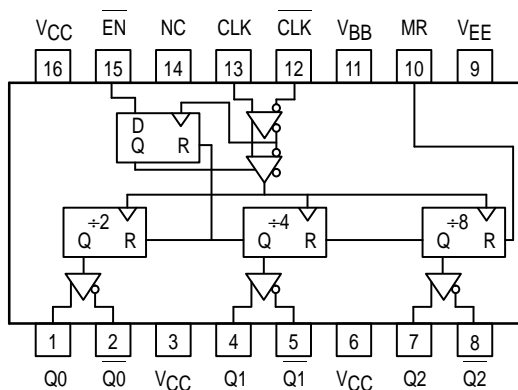
The MC10/100EL34 is a low skew ÷2, ÷4, ÷8 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the V<sub>BB</sub> output, a sinusoidal source can be AC coupled into the device (see Interfacing section of the ECLinPS™ Data Book DL140/D). If a single-ended input is to be used, the V<sub>BB</sub> output should be connected to the CLK input and bypassed to ground via a 0.01µF capacitor. The V<sub>BB</sub> output is designed to act as the switching reference for the input of the EL34 under single-ended input conditions, as a result, this pin can only source/sink up to 0.5mA of current.

The common enable ( $\overline{EN}$ ) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

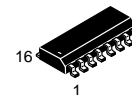
Upon startup, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as multiple EL34s in a system.

- 50ps Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection

### LOGIC DIAGRAM AND PINOUT ASSIGNMENT



## MC10EL34 MC100EL34



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751B-05

### PIN DESCRIPTION

PIN	FUNCTION
CLK	Diff Clock Inputs
EN	Sync Enable
MR	Master Reset
V <sub>BB</sub>	Reference Output
Q <sub>0</sub>	Diff ÷2 Outputs
Q <sub>1</sub>	Diff ÷4 Outputs
Q <sub>2</sub>	Diff ÷8 Outputs

### FUNCTION TABLE

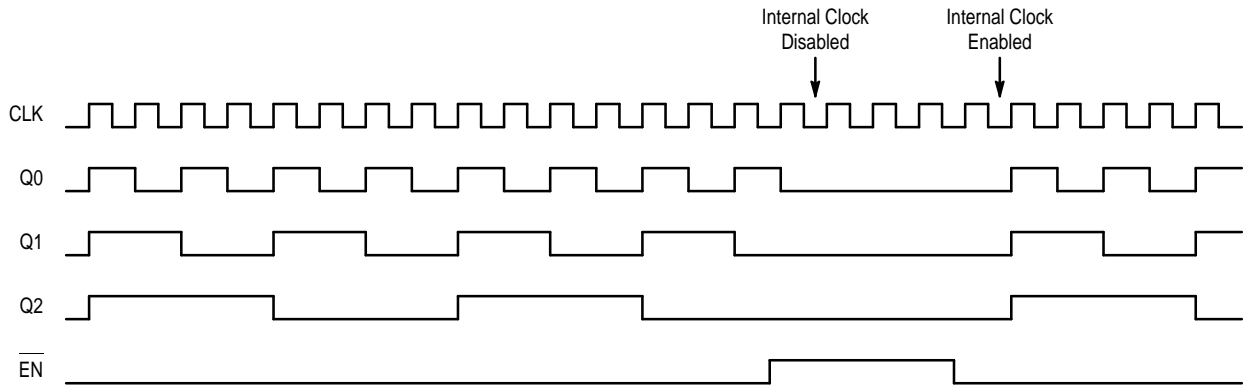
CLK	$\overline{EN}$	MR	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q <sub>0-3</sub>
X	X	H	Reset Q <sub>0-3</sub>

Z = Low-to-High Transition  
ZZ = High-to-Low Transition



**AC/DC CHARACTERISTICS** ( $V_{EE} = V_{EE(min)}$  to  $V_{EE(max)}$ ;  $V_{CC} = GND$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f <sub>MAX</sub>	Max Toggle Frequency	1100			1100			1100			1100			MHz
I <sub>EE</sub>	Power Supply Current			39 39			39 39			39 39			39 42	mA
V <sub>BB</sub>	Output Reference Voltage	10EL 100EL	-1.43 -1.38	-1.30 -1.26	-1.38 -1.38		-1.27 -1.26	-1.35 -1.38		-1.25 -1.26	-1.31 -1.38		-1.19 -1.26	V
I <sub>IH</sub>	Input High Current		150				150			150			150	μA
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay to Output	CLK→Q0 CLK→Q1,2 MR→Q	960 900 750	1200 1140 1060	960 900 750		1200 1140 1060	960 900 750		1200 1140 1060	970 910 790		1210 1150 1090	ps
t <sub>SKEW</sub>	Within-Device Skew			100			100			100			100	ps
t <sub>S</sub>	Setup Time EN		400		400			400			400			ps
t <sub>H</sub>	Hold Time EN		250		250			250			250			ps
V <sub>PP</sub>	Minimum Input Swing CLK		250		250			250			250			mV
V <sub>CMR</sub>	Common Mode Range CLK		-2.0	-0.4	-2.0		-0.4	-2.0		-0.4	-2.0		-0.4	V
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Times Q (20% – 80%)		275	525	275		525	275		525	275		525	ps

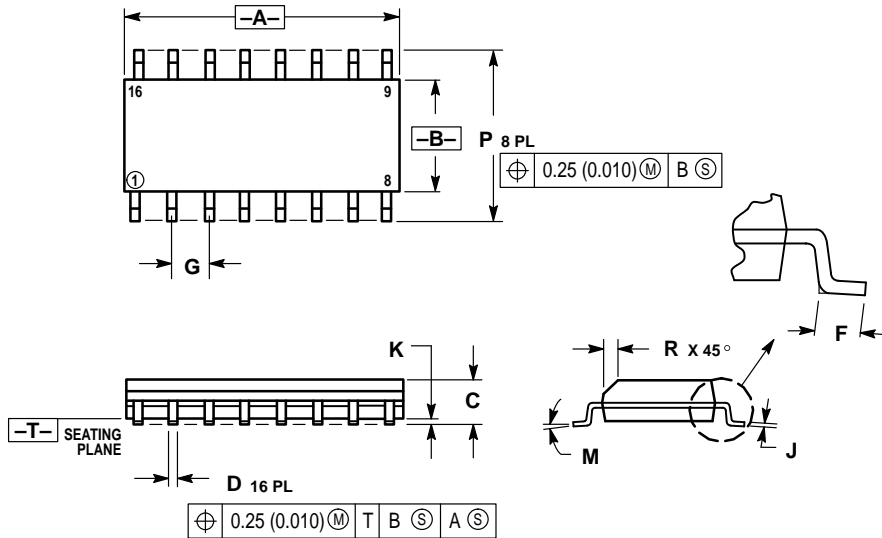


The EN signal will freeze the internal clocks to the flip-flops on the first falling edge of CLK after its assertion. The internal dividers will maintain their state during the internal clock freeze and will return to clocking once the internal clocks are unfrozen. The outputs will transition to their next states in the same manner, time and relationship as they would have had the EN signal not been asserted.

**Figure 1. Timing Diagram**

OUTLINE DIMENSIONS

D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751B-05  
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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