

MC100EPT23

3.3 V Dual Differential LVPECL/LVDS/CML to LVTTL/LVCMOS Translator

Description

The MC100EPT23 is a dual differential LVPECL/LVDS/CML to LVTTL/LVCMOS translator. Because LVPECL (Positive ECL), LVDS, and positive CML input levels and LVTTL/LVCMOS output levels are used, only + 3.3 V and ground are required. The small outline 8-lead SOIC package and the dual gate design of the EPT23 makes it ideal for applications which require the translation of a clock or data signal.

The EPT23 is available in only the ECL 100K standard. Since there are no LVPECL outputs or an external V_{BB} reference, the EPT23 does not require both ECL standard versions. The LVPECL/LVDS inputs are differential. Therefore, the MC100EPT23 can accept any standard differential LVPECL/LVDS input referenced from a V_{CC} of + 3.3 V.

Features

- 1.5 ns Typical Propagation Delay
- Maximum Operating Frequency > 275 MHz
- LVPECL/LVDS/CML Inputs, LVTTL/LVCMOS Outputs
- 24 mA LVTTL Outputs
- Operating Range:
 - ◆ $V_{CC} = 3.0\text{ V to }3.6\text{ V with GND} = 0\text{ V}$
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



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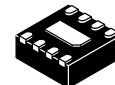
www.onsemi.com



SOIC-8 NB
D SUFFIX
CASE
751-07

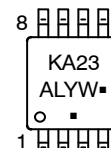
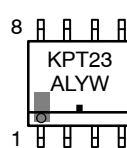


TSSOP-8
DT SUFFIX
CASE
948R-02



DFN-8
MN SUFFIX
CASE 506AA

MARKING DIAGRAMS*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- M̄ = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------------|------------------------|------------------|
| MC100EPT23DG | SOIC-8 NB (Pb-Free) | 98 Units/Tube |
| MC100EPT23DR2G | SOIC-8 NB (Pb-Free) | 2500/Tape & Reel |
| MC100EPT23DTG | TSSOP-8 (Pb-Free) | 100 Units/Tube |
| MC100EPT23DTR2G | TSSOP-8 (Pb-Free) | 2500/Tape & Reel |
| MC100EPT23MNR4G | DFN-8 (Pb-Free) | 1000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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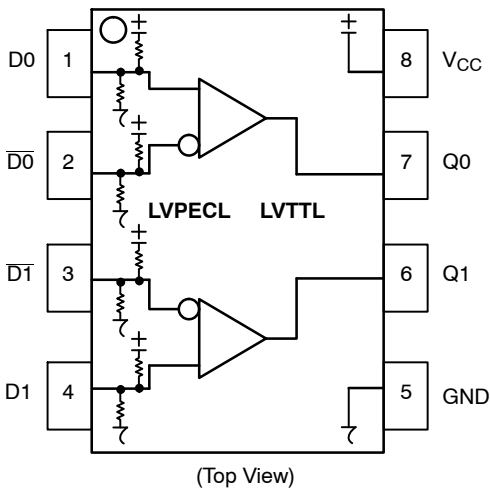


Figure 1. Logic Diagram and 8-Lead Pinout

Table 1. PIN DESCRIPTION

| Pin | Function |
|----------------------------------|---|
| Q0, Q1 | LVTTL/LVCMOS Outputs |
| D0**, D1** D0-bar**, D1-bar** | Differential LVPECL/LVDS/CML Inputs |
| V _{CC} | Positive Supply |
| GND | Ground |
| EP | (DFN-8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open. |

** Pins will default to $V_{CC}/2$ when left open.

Table 2. ATTRIBUTES

| Characteristics | Value |
|---|-------------------------------|
| Internal Input Pulldown Resistor | 50 k Ω |
| Internal Input Pullup Resistor | 50 k Ω |
| ESD Protection Human Body Model Machine Model Charged Device Model | > 1500 V > 100 V > 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Pb-Free Pkg |
| SOIC-8 NB TSSOP-8 DFN-8 | Level 1 Level 3 Level 1 |
| Flammability Rating Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | 91 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note [AND8003/D](#).

Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|--|---------------------|---------------------------------------|-------------|----------------|
| V _{CC} | Power Supply | GND = 0 V | | 3.8 | V |
| V _I | Input Voltage | GND = 0 V | V _I \leq V _{CC} | 3.8 | V |
| I _{out} | Output Current | Continuous Surge | | 50 100 | mA |
| T _A | Operating Temperature Range | | | -40 to +85 | $^{\circ}$ C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | $^{\circ}$ C |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | SOIC-8 NB | 190 130 | $^{\circ}$ C/W |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | SOIC-8 NB | 41 to 44 | $^{\circ}$ C/W |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | TSSOP-8 | 185 140 | $^{\circ}$ C/W |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | TSSOP-8 | 41 to 44 | $^{\circ}$ C/W |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | DFN-8 | 129 84 | $^{\circ}$ C/W |

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Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---------------|---------------------------------------|---------------------|-------------|----------|------|
| T_{sol} | Wave Solder (Pb-Free) | <2 to 3 sec @ 260°C | | 265 | °C |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | (Note 1) | DFN-8 | 35 to 40 | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

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Table 4. PECL DC CHARACTERISTICS ($V_{CC} = 3.3\text{ V}$, $GND = 0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|---|--------------|-----|------|--------------|-----|------|--------------|-----|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{CCH} | Power Supply Current (Outputs set to HIGH) | 10 | 20 | 35 | 10 | 20 | 35 | 10 | 20 | 35 | mA |
| I_{CCL} | Power Supply Current (Outputs set to LOW) | 15 | 27 | 40 | 15 | 27 | 40 | 15 | 27 | 40 | mA |
| V_{IH} | Input HIGH Voltage | 2075 | | 2420 | 2075 | | 2420 | 2075 | | 2420 | mV |
| V_{IL} | Input LOW Voltage | 1355 | | 1675 | 1355 | | 1675 | 1355 | | 1675 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Note 2) | 1.2 | | 3.3 | 1.2 | | 3.3 | 1.2 | | 3.3 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current D \bar{D} | -150 -150 | | | -150 -150 | | | -150 -150 | | 0.5 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- All values vary 1:1 with V_{CC} .
- V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 5. LVTTTL/LVC MOS OUTPUT DC CHARACTERISTICS ($V_{CC} = 3.3\text{ V}$, $GND = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to 85°C)

| Symbol | Characteristic | Condition | Min | Typ | Max | Unit |
|----------|------------------------------|---------------------------|------|-----|-----|------|
| V_{OH} | Output HIGH Voltage | $I_{OH} = -3.0\text{ mA}$ | 2.4 | | | V |
| V_{OL} | Output LOW Voltage | $I_{OL} = 24\text{ mA}$ | | | 0.5 | V |
| I_{OS} | Output Short Circuit Current | | -180 | | -50 | mA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 6. AC CHARACTERISTICS ($V_{CC} = 3.0\text{ V}$ to 3.6 V , $GND = 0.0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--|--|-------|----------------|-----------------|------|----------------|-----------------|------|-----------------|------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{max} | Maximum Frequency (Figure 2) | 275 | 350 | | 275 | 350 | | 275 | 350 | | MHz |
| t_{PLH} , t_{PHL} | Propagation Delay to Output Differential (Note 2) | 1.1 | 1.5 | 1.8 | 1.1 | 1.5 | 1.8 | 1.1 | 1.5 | 1.8 | ns |
| t_{SK++} t_{SK--} t_{SKPP} | Output-to-Output Skew++ Output-to-Output Skew-- Part-to-Part Skew (Note 3) | | 15 35 70 | 60 80 500 | | 15 40 70 | 70 80 500 | | 30 40 140 | 125 80 500 | ps |
| t_{JITTER} | Random Clock Jitter (RMS) (Figure 2) | | 5 | 10 | | 5 | 10 | | 5 | 10 | ps |
| V_{PP} | Input Voltage Swing (Differential Configuration) | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| t_r , t_f | Output Rise/Fall Times (0.8 V – 2.0 V) Q , \bar{Q} | 330 | 600 | 900 | 330 | 600 | 900 | 330 | 650 | 900 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Measured with a 750 mV 50% duty-cycle clock source. $R_L = 500\ \Omega$ to GND and $C_L = 20\text{ pF}$ to GND. Refer to Figure 3.
- Reference ($V_{CC} = 3.3\text{ V} \pm 5\%$; $GND = 0\text{ V}$)
- Skews are measured between outputs under identical conditions.

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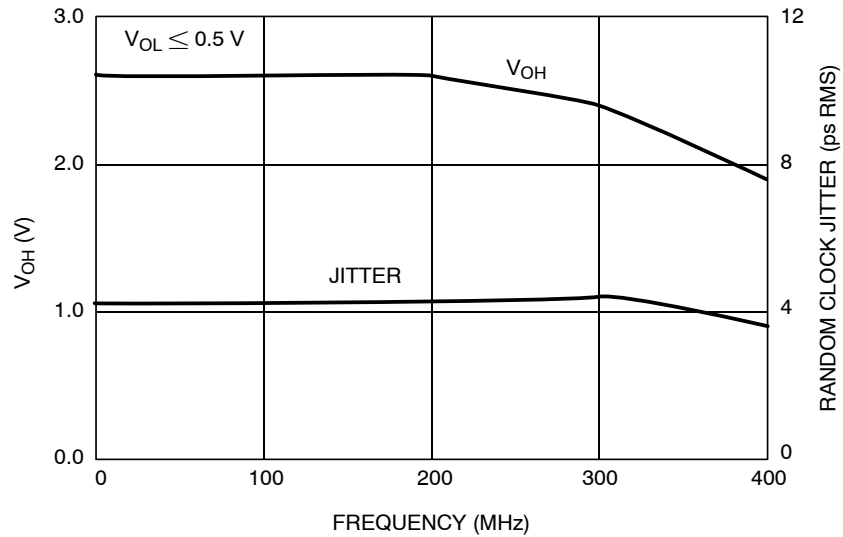


Figure 2. Typical V_{OH} / Jitter Versus Frequency (25°C)

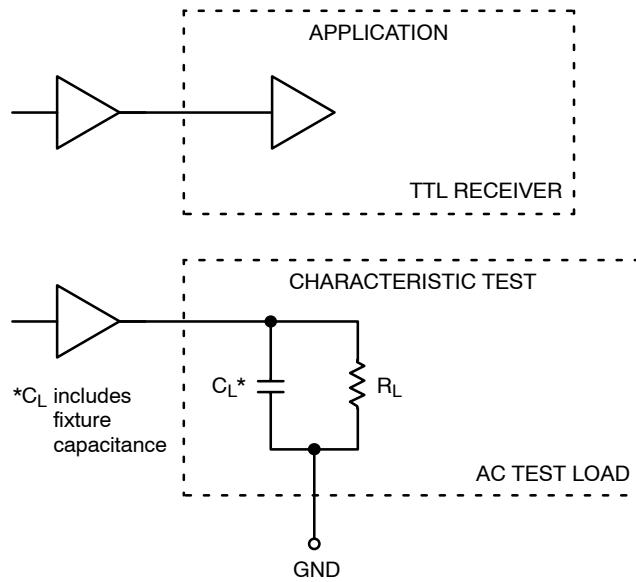


Figure 3. TTL Output Loading Used for Device Evaluation

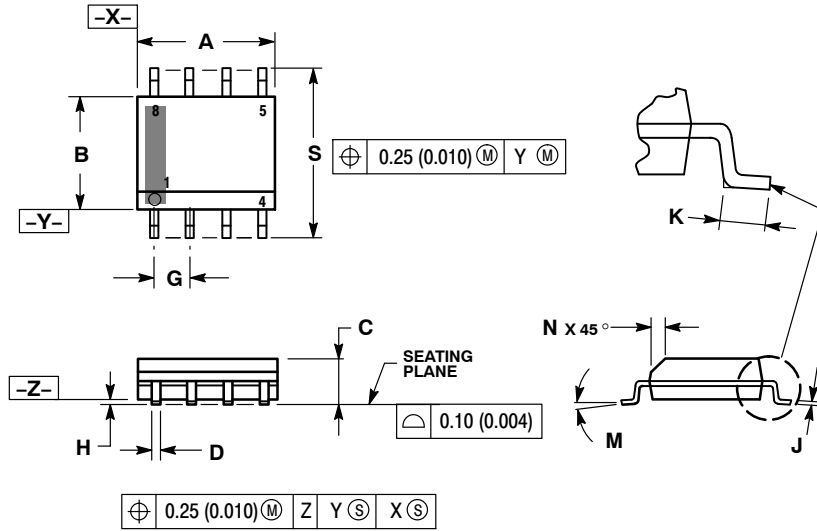
Resource Reference of Application Notes

- AN1405/D – ECL Clock Distribution Techniques
- AN1406/D – Designing with PECL (ECL at +5.0 V)
- AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D – Metastability and the ECLinPS Family
- AN1568/D – Interfacing Between LVDS and ECL
- AN1672/D – The ECL Translator Guide
- AND8001/D – Odd Number Counters Design
- AND8002/D – Marking and Date Codes
- AND8020/D – Termination of ECL Logic Devices
- AND8066/D – Interfacing with ECLinPS
- AND8090/D – AC Characteristics of ECL Devices

MC100EPT23

PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AK

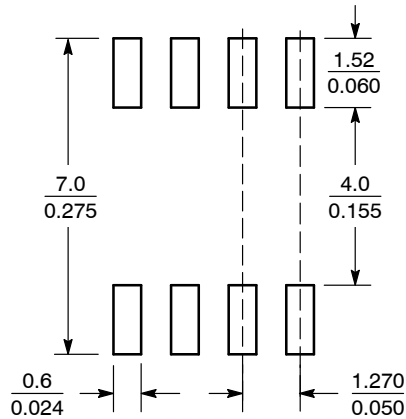


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*



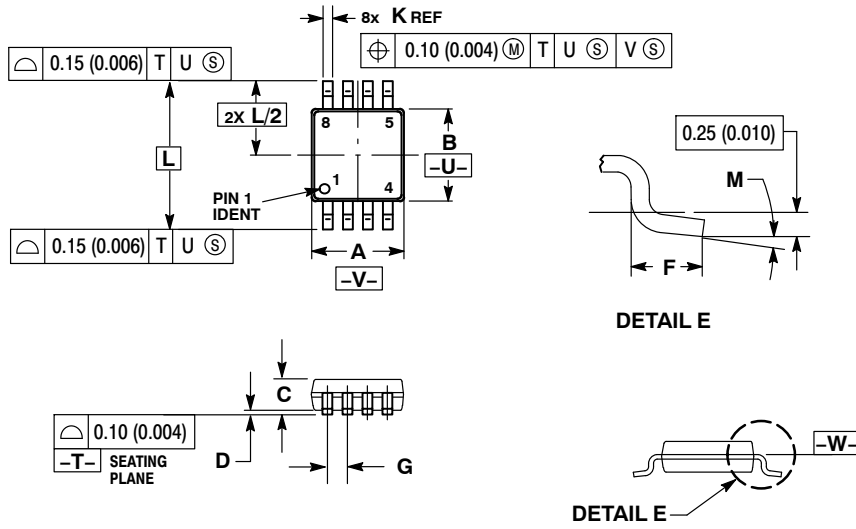
SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, [SOLDDERM/D](#).

MC100EPT23

PACKAGE DIMENSIONS

TSSOP-8
CASE 948R-02
ISSUE A



NOTES:

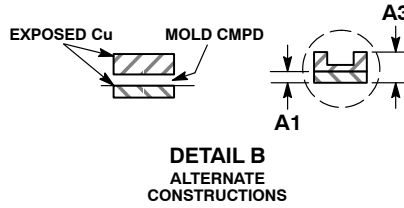
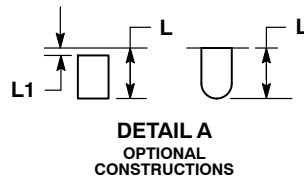
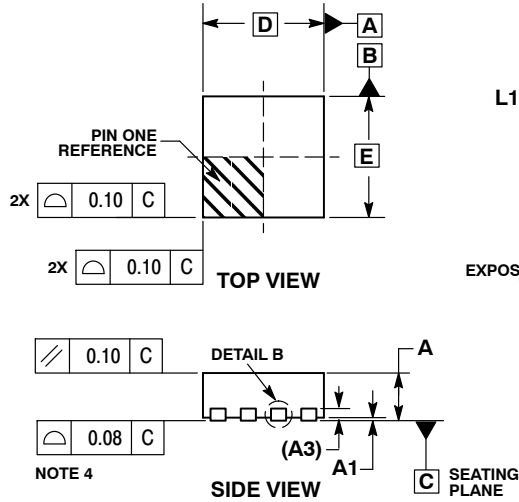
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 2.90 | 3.10 | 0.114 | 0.122 |
| C | 0.80 | 1.10 | 0.031 | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.40 | 0.70 | 0.016 | 0.028 |
| G | 0.65 BSC | | 0.026 BSC | |
| K | 0.25 | 0.40 | 0.010 | 0.016 |
| L | 4.90 BSC | | 0.193 BSC | |
| M | 0° | 6° | 0° | 6° |

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PACKAGE DIMENSIONS

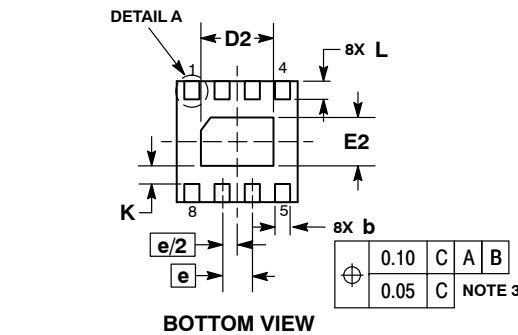
DFN-8 2x2, 0.5P
CASE 506AA
ISSUE F



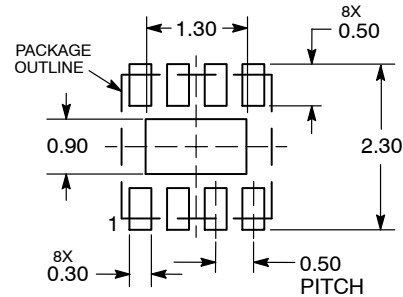
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 | REF |
| b | 0.20 | 0.30 |
| D | 2.00 | BSC |
| D2 | 1.10 | 1.30 |
| E | 2.00 | BSC |
| E2 | 0.70 | 0.90 |
| e | 0.50 | BSC |
| K | 0.30 | REF |
| L | 0.25 | 0.35 |
| L1 | --- | 0.10 |



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, [SOLDDRRM/D](#).

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