MC10H681, MC10H681

Hex ECL to TTL Transceiver with Latches

The MC10/100H681 is a dual supply Hex ECL/TTL transceiver with latches in both directions. ECL controlled Direction and Chip Enable Bar pins. There are two Latch Enable pins, one for each direction.

The ECL outputs are single ended and drive 50 Ω. The TTL outputs are specified to source 15 mA and sink 48 mA, allowing the ability to drive highly capacitive loads. The high driving ability of the TTL outputs make the device ideal for bussing applications.

The ECL output levels are standard V_{OH} and V_{OL} cutoff equal to −2.0 V (V_{TT}). When the ECL ports are disabled the outputs go to the V_{OL} cutoff level. Multiple ECL V_{CCO} pins are utilized to minimize switching noise.

The TTL ports have standard levels. The TTL input receivers have PNP input devices to significantly reduce loading. Multiple TTL power and ground pins are utilized to minimize switching noise.

The 10H version is compatible with MECL™ 10H ECL logic levels. The 100H version is compatible with 100K levels.

- Separate Latch Enable Controls for each Direction
- ECL Single Ended 50 Ω I/O Port
- High Drive TTL I/O Ports
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- Direction and Chip Enable Control Pins

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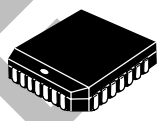


PLCC−28
FN SUFFIX
CASE 776

MARKING DIAGRAM

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H681FN	PLCC−28	37 Units/Rail
MC100H681FN	PLCC−28	37 Units/Rail

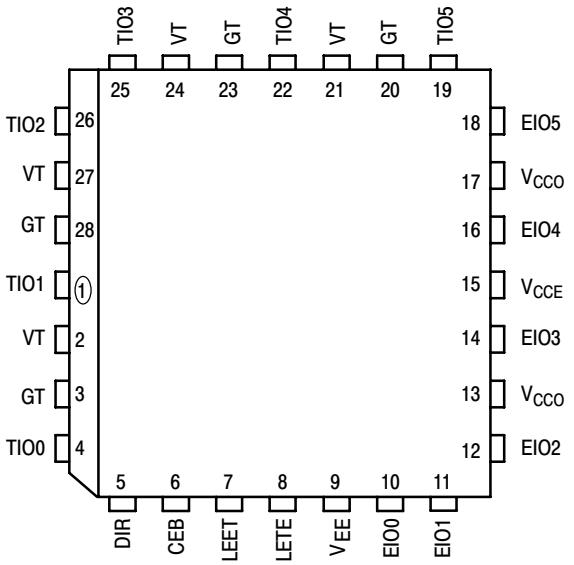


Figure 1. Pinout: PLCC−28 (Top View)

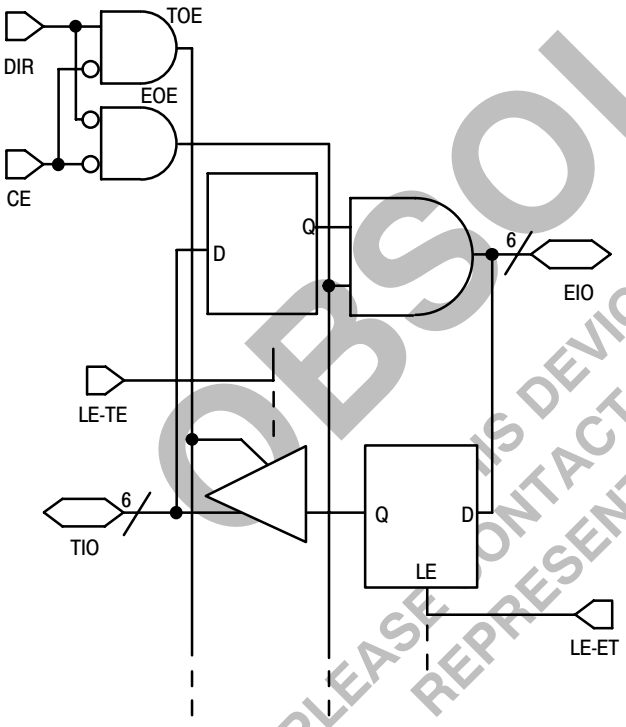


Figure 2. Logic Diagram

Table 1. PIN DESCRIPTION

Pin	Symbol	Description
1	TI01	TTL I/O BIT 1
2	VT	TTL V_{CC} (5.0 V)
3	GT	TTL GND (0 V)
4	TI00	TTL I/O Bit 0
5	DIR	Direction Control (ECL)
6	CEB	Chip Enable Bar Control (ECL)
7	LEET	Latch Enable ECL-TTL Control (ECL)
8	LETE	Latch Enable TTL-ECL Control (ECL)
9	V_{EE}	ECL Supply (−5.2/−4.5 V)
10	EI00	ECL I/O BIT 0
11	EI01	ECL I/O BIT 1
12	EI02	ECL I/O BIT 2
13	V_{CCO}	ECL V_{CC} (0 V) − Outputs
14	EIO3	TTL I/O BIT 3
15	V_{CCE}	ECL V_{CC} (0 V)
16	EIO4	ECL I/O BIT 4
17	V_{CCO}	ECL V_{CC} (0 V) − Outputs
18	EIO5	ECL I/O BIT 5
19	TI05	TTL I/O BIT 5
20	GT	TTL GND (0 V)
21	VT	TTL V_{CC} (5.0 V)
22	TI04	TTL I/O BIT 4
23	GT	TTL GND (0 V)
24	VT	TTL V_{CC} (5.0 V)
25	TIO3	TTL I/O BIT 3
26	TIO2	TTL I/O BIT 2
27	VT	TTL V_{CC} (5.0 V)
28	GT	TTL V_{CC} (0 V)

Table 2. TRUTH TABLE

CEB	DIR	LEET	LETE	EOUT	TOUT
H	X	X	X	Z	Z
L	H	L	L	Z	EIN
L	H	H	L	Z	Qo
L	L	L	L	TIN	Z
L	L	L	H	Qo	Z

Hex
Bi-Directional
ECL/TTL Translation
Dual Supply
ECL Outputs, 50 Ω S.E., V_{OH}/Cutoff
TTL Outputs, 48 mA Sink, 15 mA Source
Multi Power and Ground Pins
Separate LE Controls

Table 3. ABSOLUTE RATINGS (Do not exceed):

Power Supply Voltage	V_{EE} (ECL)	−8.0 to 0	Vdc
Power Supply Voltage	V_{CCT} (TTL)	−0.5 to +7.0	Vdc
Input Voltage	V_I (ECL) V_I (TTL)	0.0 to V_{EE} −0.5 to +7.0	Vdc
Disabled 3-State Output	V_{out} (TTL)	0.0 to V_{CCT}	Vdc
Output Source Current Continuous	I_{out} (ECL)	100	mAdc
Output Source Current Surge	I_{out} (ECL)	200	mAdc
Storage Temperature	T_{stg}	−65 to 150	°C
Operating Temperature	T_{amb}	0.0 to +75	°C

Table 4. ECL DC CHARACTERISTICS: V_{CCT} = +5.0 V ±10%, V_{EE} = −5.2 ±5% (10H Version); V_{EE} = −4.2 V to −5.5 V (100H Version)

			T_A = 0°C		T_A = 25°C		T_A = 75°C		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Unit
I_{EE}	Supply Current/ECL		–	−113	–	−113	–	−113	mA
I_{INH}	Input HIGH Current		–	255	–	175	–	175	μA
I_{INL}	Input LOW Current		0.5	–	0.5	–	0.3	–	μA
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	50 Ω to −2.1 V	−1020 −2.1	−840 −2.03	−980 −2.1	−810 −2.03	−920 −2.1	−735 −2.03	mV V

Table 5. 10H ECL DC CHARACTERISTICS: V_{CCT} = +5.0 ±10%, V_{EE} = −5.2 ±5%

		T_A = 0°C		T_A = 25°C		T_A = 75°C		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	−1170 −1950	−840 −1480	−1130 −1950	−810 −1480	−1070 −1950	−735 −1450	mV

Table 6. 100H ECL DC CHARACTERISTICS: V_{CCT} = +5.0 ±10%, V_{EE} = −4.2 V to −5.5 V

		T_A = 0°C		T_A = 25°C		T_A = 75°C		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	−1165 −1810	−880 −1475	−1165 −1810	−880 −1475	−1165 −1810	−880 −1475	mV

Table 7. TTL DC CHARACTERISTICS: V_{CCT} = +5.0 V ±10%, V_{EE} = −5.2 ±5% (10H Version); V_{EE} = −4.2 V to −5.5 V (100H Version)

Symbol	Parameter	Condition	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit
			Min	Max	Min	Max	Min	Max	
V_{IH} V_{IL}	Standard Input Standard Input		2.0 –	– 0.8	2.0 –	– 0.8	2.0 –	– 0.8	Vdc
V_{IK}	Input Clamp	I_{IN} = −18 mA	–	−1.2	–	−1.2	–	−1.2	Vdc
V_{OH}	Output HIGH Voltage Output HIGH Voltage	I_{OH} = −3.0 mA I_{OH} = −15 mA	2.5 2.0	– –	2.5 2.0	– –	2.5 2.0	– –	V
V_{OL}	Output LOW Voltage	I_{OL} = 48 mA	–	0.55	–	0.55	–	0.55	V
I_{IH}/I_{OZH} I_{IL}/I_{OZL}	Output Disable Current	V_{OUT} = 2.7 V V_{OUT} = 0.5 V	– –	70 200	– –	70 200	– –	70 200	μA
I_{CCL}	Supply Current		–	63	–	63	–	63	mA
I_{CCH}	Supply Current		–	63	–	63	–	63	mA
I_{CCZ}	Supply Current		–	63	–	63	–	63	mA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V	−100	−225	−100	−225	−100	−225	mA

Table 8. ECL TO TTL DIRECTION AC CHARACTERISTICS

Symbol	Parameter	Condition	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay to Output	C_L = 50 pF	4.0	7.8	4.0	7.8	4.2	8.0	ns
t_{PLH} t_{PHL}	LEET to Output	C_L = 50 pF	5.5 5.5	8.3 7.6	5.5 5.5	8.3 7.6	5.7 5.8	8.5 8.0	ns
t_{PZH} t_{PZL}	CEB to Output Enable Time	C_L = 50 pF	5.5 5.3	8.3 8.3	5.5 5.3	8.3 8.3	4.7 5.4	8.5 8.4	ns
t_{PHZ} t_{PLZ}	CEB to Output Disable Time	C_L = 50 pF	3.5 3.5	7.2 5.3	3.5 3.5	7.2 5.3	3.7 4.1	7.3 5.8	ns
t_r/t_f	1.0 Vdc to 2.0 Vdc	C_L = 50 pF	0.4	2.2	0.4	2.2	0.4	2.2	ns

Table 9. TTL TO ECL DIRECTION AC CHARACTERISTICS

Symbol	Parameter	Condition	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay to Output	50 Ω to −2.0 V	1.9	3.9	1.9	3.9	2.2	4.4	ns
t_{PHL} t_{PLH}	CEB to Output	50 Ω to −2.0 V	2.2 2.3	4.0 4.6	2.2 2.3	4.0 4.6	2.5 2.7	4.3 5.0	ns
t_{PHL} t_{PLH}	LETE to Output	50 Ω to −2.0 V	2.4	3.9	2.4	3.9	2.7	4.3	ns
t_r/t_f	Output Rise/Fall Time 20% − 80%	50 Ω to −2.0 V	0.4	2.2	0.4	2.2	0.4	2.2	ns

TEST CIRCUITS AND WAVEFORMS

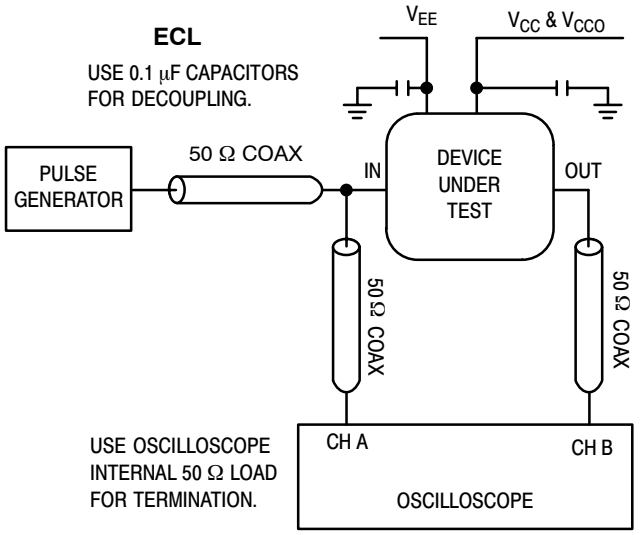


Figure 3. Test Circuit ECL

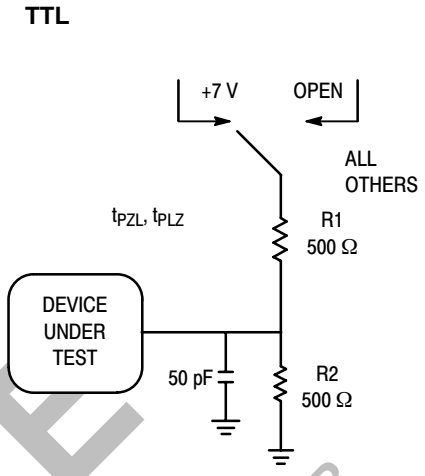


Figure 4. Test Circuit TTL

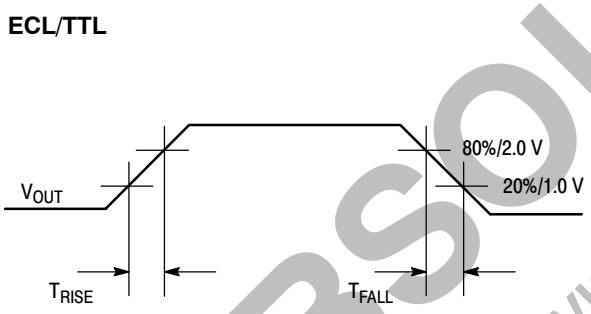


Figure 5. Rise and Fall Times

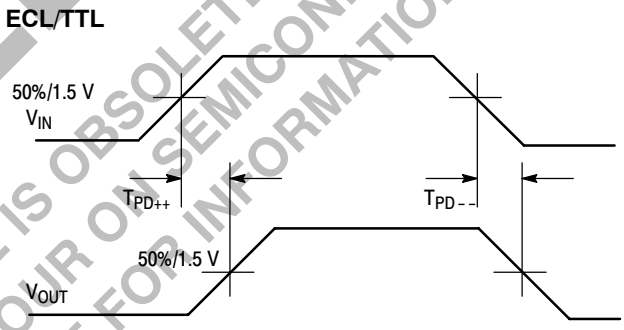


Figure 6. Propagation Delay – Single–Ended

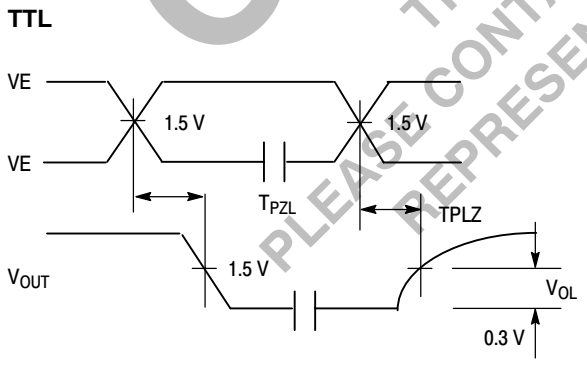


Figure 7. 3-State Output Low Enable and Disable Times

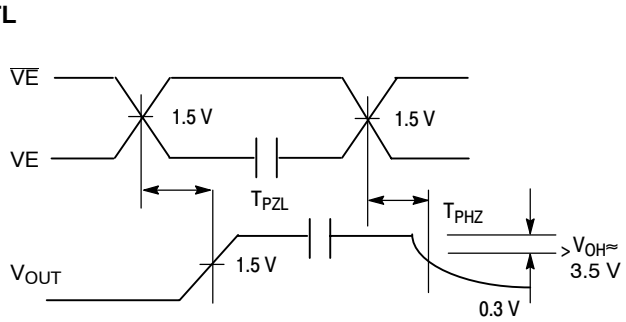
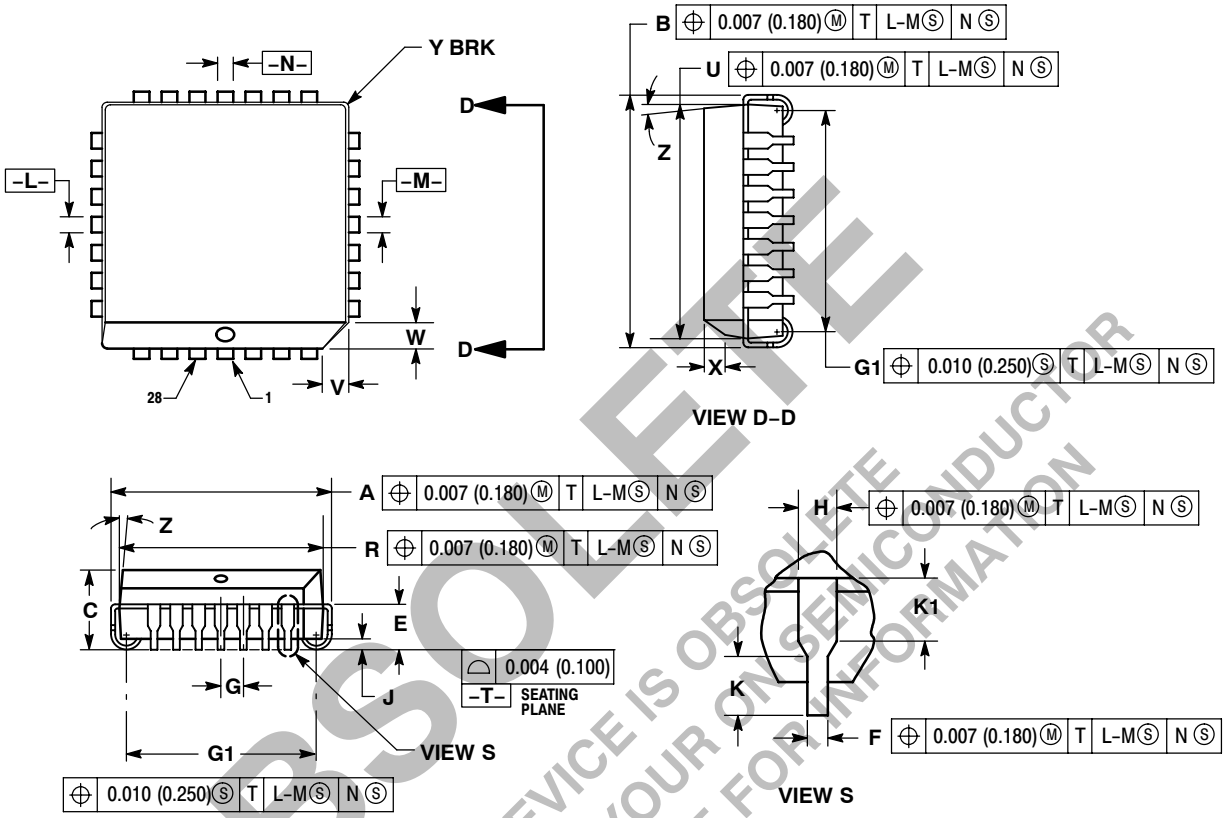


Figure 8. 3-State Output High Enable and Disable Times

PACKAGE DIMENSIONS

PLCC−28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776−02
ISSUE E



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

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