

Differential Clock D Flip-Flop

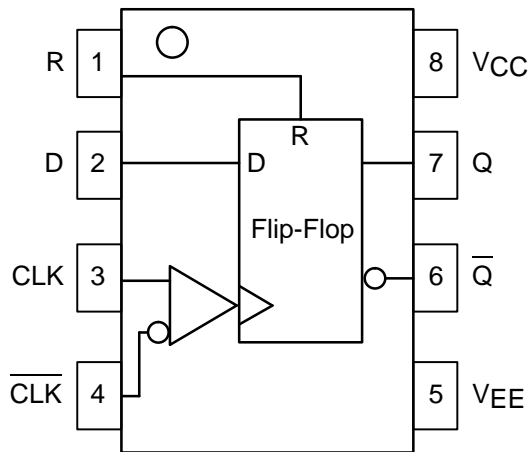
The MC100LVEL51 is a differential clock D flip-flop with reset. The device is functionally equivalent to the EL51 device, but operates from a low voltage supply. With propagation delays and output transition times essentially equal to the EL51, the LVEL51 is ideally suited for those applications which require the ultimate in AC performance at 3.3V V_{CC} .

The reset input is an asynchronous, level triggered signal. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the LVEL51 allow the device to be used as a negative edge triggered flip-flop.

The differential input employs clamp circuitry to maintain stability under open input conditions. When left open, the CLK input will be pulled down to V_{EE} and the CLK input will be biased at $V_{CC}/2$.

- 475ps Propagation Delay
- 2.8GHz Toggle Frequency
- Operates from -3.3V (or 3.3V) Supply
- 75k Ω Internal Input Pulldown Resistors
- >2000V ESD Protection

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



MC100LVEL51



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05

TRUTH TABLE

D	R	CLK	Q
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition



MC100LVEL51

DC CHARACTERISTICS ($V_{EE} = V_{EE}(\text{min})$ to $V_{EE}(\text{max})$; $V_{CC} = \text{GND}$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		30	35		30	35		30	35		32	37	mA
V_{EE}	Power Supply Voltage	-3.0	-3.3	-3.8	-3.0	-3.3	-3.8	-3.0	-3.3	-3.8	-3.0	-3.3	-3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{IL}	Input LOW Current CLK Other	-600 0.5			-600 0.5			-600 0.5			-600 0.5			μA

AC CHARACTERISTICS ($V_{EE} = V_{EE}(\text{min})$ to $V_{EE}(\text{max})$; $V_{CC} = \text{GND}$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency	2.7			2.9			2.9			2.9			GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK R	330 340		510 540	330 340		510 540	340 350		520 550	370 390		550 590	ps
t_{S}	Setup Time	150	0		150	0		150	0		150	0		ps
t_{H}	Hold Time	200	100		200	100		200	100		200	100		ps
t_{RR}	Reset Recovery	350	200		350	200		350	200		350	200		ps
t_{PW}	Minimum Pulse Width CLK Reset	400 500			400 500			400 500			400 500			ps
V_{PP}	Minimum Input Swing ¹	150			150			150			150			mV
V_{CMR}	Common Mode Range ² $V_{\text{PP}} < 500\text{mV}$ $V_{\text{PP}} \geq 500\text{mV}$	-2.0 -1.8		-0.4 -0.4	-2.1 -1.9		-0.4 -0.4	-2.1 -1.9		-0.4 -0.4	-2.1 -1.9		-0.4 -0.4	V
t_{r} t_{f}	Output Rise/Fall Times Q (20% – 80%)	120		320	120		320	120		320	120		320	ps

1. Minimum input swing for which AC parameters are guaranteed.

2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PPmin} and 1V. The lower end of the CMR range varies 1:1 with V_{EE} . The numbers in the spec table assume a nominal $V_{\text{EE}} = -3.3\text{V}$. Note for PECL operation, the $V_{\text{CMR}(\text{min})}$ will be fixed at $3.3\text{V} - |V_{\text{CMR}(\text{min})}|$.

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05
ISSUE P



NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. DIMENSIONS ARE IN MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
6. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.35	0.49
F	0.40	1.25
G	1.27 BSC	
J	0.18	0.25
K	0.10	0.25
M	0°	7°
P	5.80	6.20
R	0.25	0.50

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