

MC10125

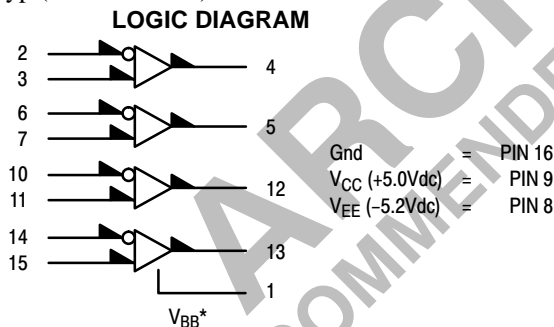
Quad MECL to TTL Translator

The MC10125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10125 incorporates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/ non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available on pin 1 for use in single-ended input biasing. The outputs of the MC10125 go to a low logic level whenever the inputs are left floating.

Power supply requirements are ground, +5.0 Volts and -5.2 Volts. Propagation delay of the MC10125 is typically 4.5 ns. The MC10125 has fanout of 10 TTL loads. The dc levels are MECL 10,000 in and Schottky TTL, or TTL out. This device has an input common mode noise rejection of ± 1.0 Volt.

An advantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL logic from the noisy TTL environment. This device is useful in computers, instrumentation, peripheral controllers, test equipment and digital communications systems.

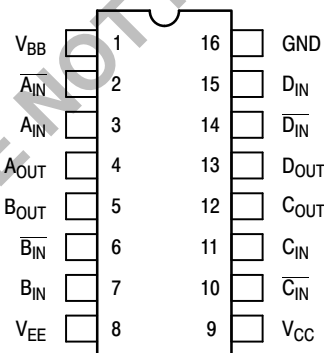
- $P_D = 380$ mW typ/pkg (No Load)
- $t_{pd} = 4.5$ ns typ (50% to +1.5 Vdc out)
- $t_r, t_f = 2.5$ ns typ (1.0 V to 2.0 V)



* V_{BB} to be used to supply bias to the MC10125 only and bypassed (when used) with 0.01 μ F to 0.1 μ F capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

When the input pin with the bubble goes positive, the output goes negative.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.

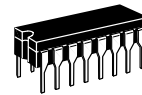
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



ON Semiconductor

<http://onsemi.com>

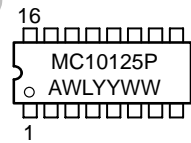
MARKING DIAGRAMS



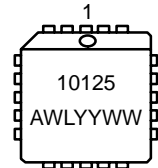
CDIP-16
L SUFFIX
CASE 620



PDIP-16
P SUFFIX
CASE 648



PLCC-20
FN SUFFIX
CASE 775



A = Assembly Location
 WL = Wafer Lot
 YY = Year
 WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10125L	CDIP-16	25 Units / Rail
MC10125P	PDIP-16	25 Units / Rail
MC10125FN	PLCC-20	46 Units / Rail

MC10125

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			-30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Negative Power Supply Drain Current	I_E	8		-44			-40		-44	mAdc
Positive Power Supply Drain Current	I_{CCH}	9		52			52		52	mAdc
	I_{CCL}	9		39			39		39	mAdc
Input Current	I_{inH}^1	2		180			115		115	μ Adc
Input Leakage Current	I_{CBO}	2		1.5			1.0		1.0	μ Adc
High Output Voltage	V_{OH}	4	2.5		2.5			2.5		Vdc
Low Output Voltage	V_{OL}	4		0.5			0.5		0.5	Vdc
High Threshold Voltage	V_{OHA}	4	2.5		2.5			2.5		Vdc
Low Threshold Voltage	V_{OLA}	4		0.5			0.5		0.5	Vdc
Indeterminate Input Protection Tests	V_{OLS1}	4		0.5			0.5		0.5	Vdc
	V_{OLS2}	4		0.5			0.5		0.5	Vdc
Short Circuit Current	I_{OS}	4	40	100	40		100	40	100	mAdc
Reference Voltage	V_{BB}	1	-1.420	-1.280	-1.350		-1.230	-1.295	-1.150	Vdc
Common Mode Rejection Tests	V_{OH}	4	2.5		2.5			2.5		Vdc
		4	2.5		2.5			2.5		Vdc
	V_{OL}	4		0.5			0.5		0.5	Vdc
		4		0.5			0.5		0.5	Vdc
Switching Times (50 Ω Load)										ns
Propagation Delay (50% to +1.5Vdc)	t_{6+5-}	5	1.0	6.0	1.0	4.5	6.0	1.0	6.0	
	t_{6-5+}	5	1.0	6.0	1.0	4.5	6.0	1.0	6.0	
	t_{2+4-}	4	1.0	6.0	1.0	4.5	6.0	1.0	6.0	
	t_{2-4+}	4	1.0	6.0	1.0	4.5	6.0	1.0	6.0	
Rise Time (+1.0V to 2.0V)	t_{4+}	4		3.3			3.3		3.3	
Fall Time (+1.0V to 2.0V)	t_{4-}	4		3.3			3.3		3.3	

1. Individually test each output, apply V_{IHmax} to pin under test.

MC10125

ELECTRICAL CHARACTERISTICS (continued)

			TEST VOLTAGE VALUES (Volts)						Gnd	Output Condition
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmx}	V _{IHH}	V _{ILH}		
@ Test Temperature										
-30°C			-0.890	-1.890	-1.205	-1.500	+0.110	-0.890		
+25°C			-0.810	-1.850	-1.105	-1.475	+0.190	-0.850		
+85°C			-0.700	-1.825	-1.035	-1.440	+0.300	-0.825		
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						Gnd	Output Condition
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmx}	V _{IHH}	V _{ILH}		
Negative Power Supply Drain Current	I _E	8							16	
Positive Power Supply Drain Current	I _{CCH}	9	2,6,10,14						16	
	I _{CCL}	9		2,6,10,14					16	
Input Current	I _{inH} ¹	2	2,6,10,14						16	
Input Leakage Current	I _{CBO}	2							16	
High Output Voltage	V _{OH}	4		2,6,10,14					16	-2.0mA
Low Output Voltage	V _{OL}	4	2,6,10,14						16	20mA
High Threshold Voltage	V _{OHA}	4		6,10,14		2			16	-2.0mA
Low Threshold Voltage	V _{OLA}	4	6,10,14		2				16	20mA
Indeterminate Input Protection Tests	V _{OLS1}	4							16	20mA
	V _{OLS2}	4							16	20mA
Short Circuit Current	I _{OS}	4		2,6,10,14					4, 16	
Reference Voltage	V _{BB}	1		2,6,10,14						
Common Mode Rejection Tests	V _{OH}	4					3	2	16	-2.0mA
		4							16	-2.0mA
	V _{OL}	4					2	3	16	20mA
		4							16	20mA
Switching Times (50Ω Load)			Pulse In	Pulse Out	C _L (pF)					
Propagation Delay (50% to +1.5Vdc)	t ₆₊₅₋	5	6	5	25				16	
	t ₆₋₅₊	5	6	5	25				16	
	t ₂₊₄₋	4	2	4	25				16	
	t ₂₋₄₊	4	2	4	25				16	
Rise Time(+1.0V to 2.0V)	t ₄₊	4	2	4	25				16	
Fall Time (+1.0V to 2.0V)	t ₄₋	4	2	4	25				16	

1. Individually test each output, apply V_{IHmax} to pin under test.

MC10125

ELECTRICAL CHARACTERISTICS (continued)

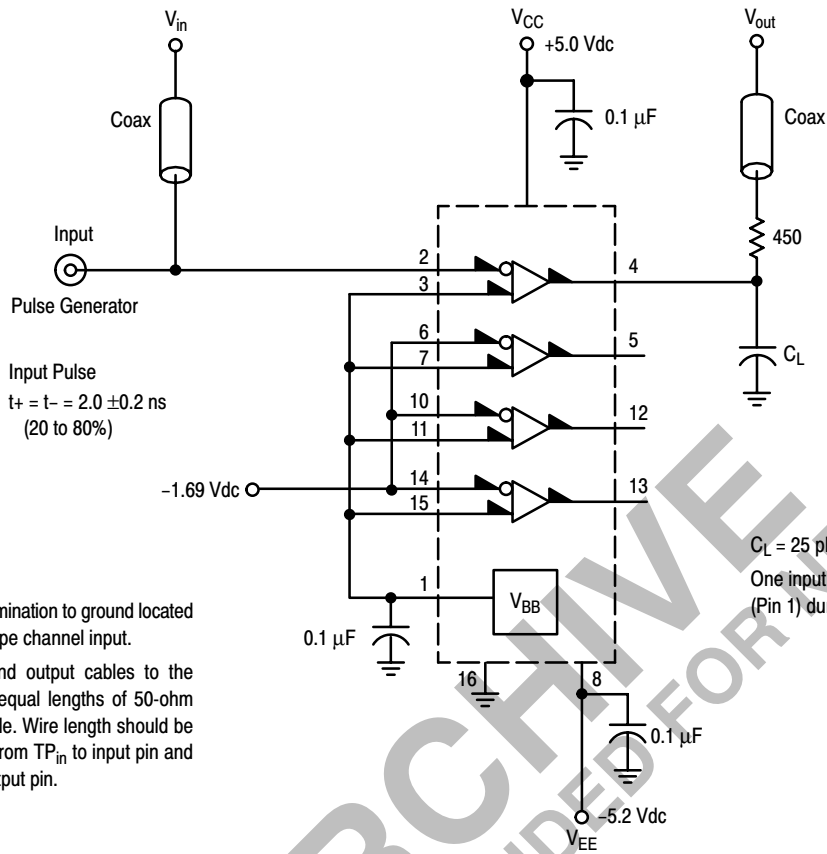
@ Test Temperature -30°C +25°C +85°C			TEST VOLTAGE VALUES (Volts)					Gnd	Output Condition
			V _{IHH}	V _{ILH}	V _{BB}	V _{CC}	V _{EE}		
			-1.890	-2.890	From Pin 1	+5.0	-5.2		
			-1.810	-2.850		+5.0	-5.2		
-1.700	-2.825	+5.0	-5.2						
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					Gnd	Output Condition
			V _{IHH}	V _{ILH}	V _{BB}	V _{CC}	V _{EE}		
Negative Power Supply Drain Current	I _E	8			3,7,11,15	9	8	16	
Positive Power Supply Drain Current	I _{CCH}	9			3,7,11,15	9	8	16	
	I _{CCL}	9			3,7,11,15	9	8	16	
Input Current	I _{inH} ¹	2			3,7,11,15	9	8	16	
Input Leakage Current	I _{CBO}	2			3,7,11,15	9	2,6,8,10,14	16	
High Output Voltage	V _{OH}	4			3,7,11,15	9	8	16	-2.0mA
Low Output Voltage	V _{OL}	4			3,7,11,15	9	8	16	20mA
High Threshold Voltage	V _{OHA}	4			3,7,11,15	9	8	16	-2.0mA
Low Threshold Voltage	V _{OLA}	4			3,7,11,15	9	8	16	20mA
Indeterminate Input Protection Tests	V _{OLS1}	4				9	2,3,6,7,8,10,11,14,15	16	20mA
	V _{OLS2}	4				9	8	16	20mA
Short Circuit Current	I _{OS}	4			3,7,11,15	9	8	4, 16	
Reference Voltage	V _{BB}	1			3,7,11,15				
Common Mode Rejection Tests	V _{OH}	4				9	8	16	-2.0mA
		4	3	2		9	8	16	-2.0mA
	V _{OL}	4				9	8	16	20mA
		4	2	3		9	8	16	20mA
Switching Times (50Ω Load)									
Propagation Delay (50% to +1.5Vdc)	t ₆₊₅₋	5			3,7,11,15	9	8	16	
	t ₆₋₅₊	5			3,7,11,15	9	8	16	
	t ₂₊₄₋	4			3,7,11,15	9	8	16	
	t ₂₋₄₊	4			3,7,11,15	9	8	16	
Rise Time (+1.0V to 2.0V)	t ₄₊	4			3,7,11,15	9	8	16	
Fall Time (+1.0V to 2.0V)	t ₄₋	4			3,7,11,15	9	8	16	

1. Individually test each output, apply V_{IHmax} to pin under test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10125

SWITCHING TIME TEST CIRCUIT



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

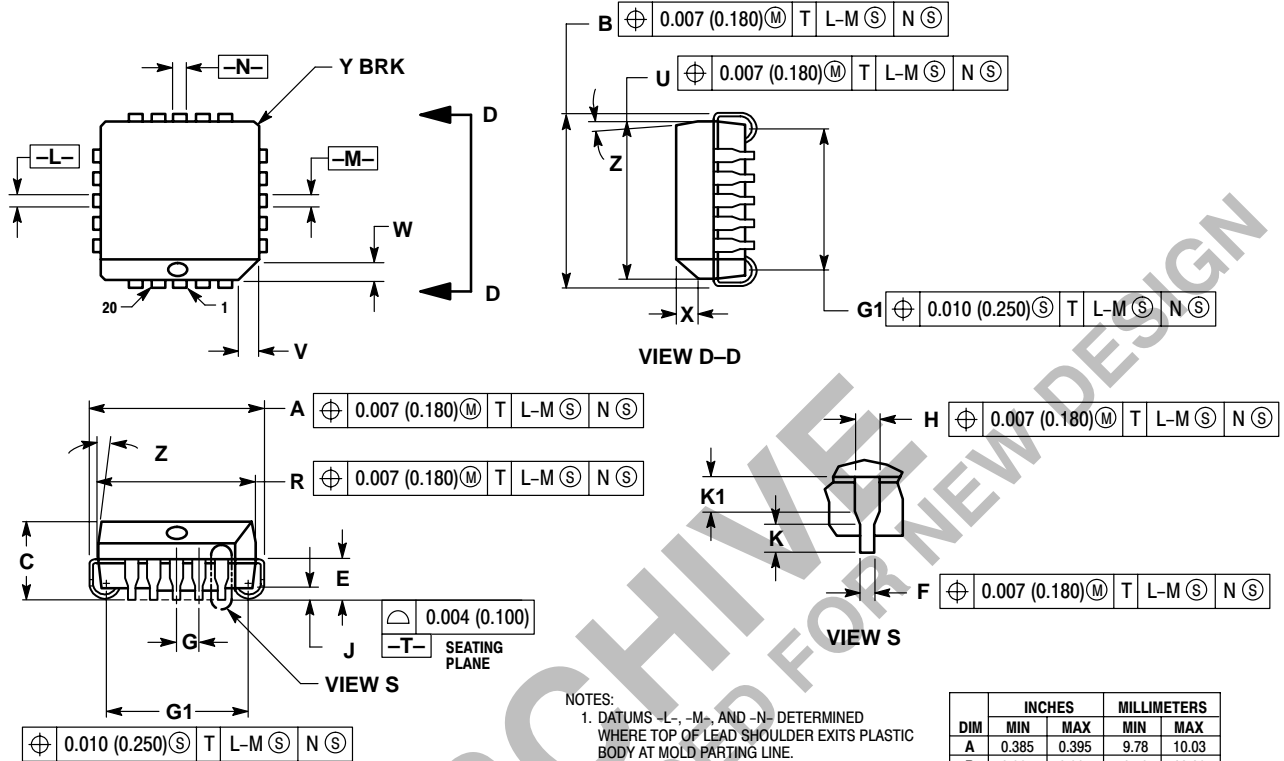
$C_L = 25$ pF, including test fixture
One input from each gate must be tied to V_{BB} (Pin 1) during testing.

ARCHIVED FOR NEW DESIGN
DEVICE NOT RECOMMENDED

MC10125

PACKAGE DIMENSIONS

PLCC-20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775-02
ISSUE C



NOTES:

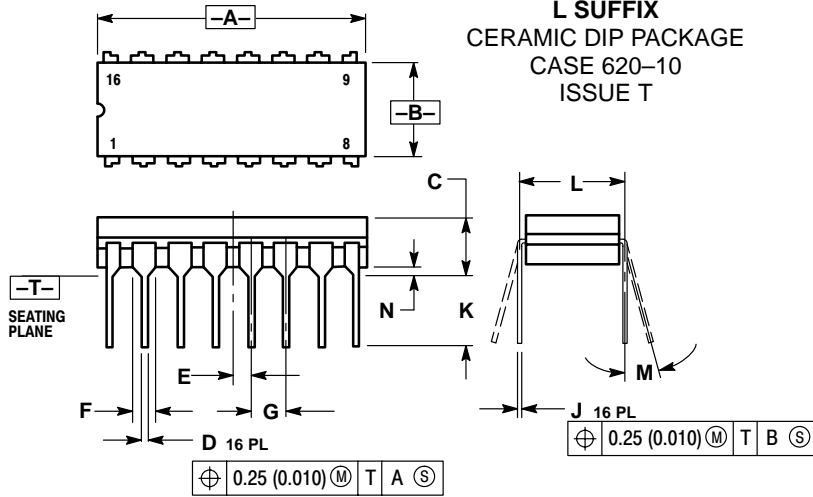
- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°		10°	
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

MC10125

PACKAGE DIMENSIONS

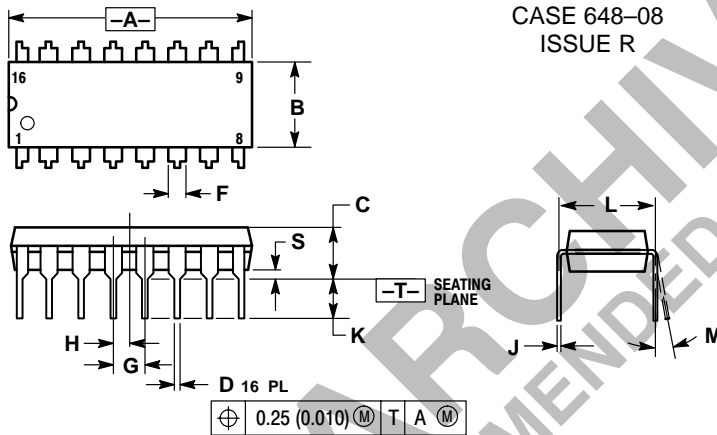
CDIP-16 L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

ARCHIVE
RECOMMENDED FOR NEW DESIGN

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031
Phone: 81-3-5740-2700
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.