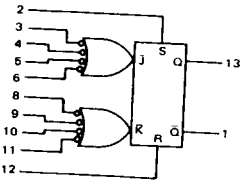
MC1027

Designed for use at clock frequencies to 100 MHz minimum (120 MHz typical). Logic performing inputs ($\bar{J}$ and $\bar{K}$) are available, as well as dc SET and RESET inputs.

POSITIVE LOGIC



DC Input Loading Factor = 2
DC Output Loading Factor = 25
Power Dissipation = 250 mW typical

*Any $\bar{J}$ or $\bar{K}$ input, not used for $\bar{C}_D$.
**$\bar{C}_D$ obtained by connecting one $\bar{J}$ and one $\bar{K}$ input together.

The $\bar{J}$ and $\bar{K}$ inputs refer to logic levels while the $\bar{C}_D$ input refers to dynamic logic swings. The $\bar{J}$ and $\bar{K}$ inputs should be changed to a logical "1" only while the $\bar{C}_D$ input is in a logic "1" state. ($\bar{C}_D$ maximum "1" level = V_{CC} −0.6 V). Clock $\bar{C}_D$ is obtained by tying one $\bar{J}$ and one $\bar{K}$ input together.

R S TRUTH TABLE

Pin No.

R	S	Q^{n+1}
12	2	13
0	0	Q^n
0	1	1
1	0	0
1	1	N.D.

All $\bar{J}$ $\bar{K}$ inputs are static
N.D. = Not defined

$\bar{J}_D$ $\bar{K}_D$ TRUTH TABLE

Pin No.

$\bar{J}_D$	$\bar{K}_D$	Q^{n+1}
*	*	13
0	0	Q^n
0	1	0
1	0	1
1	1	$\bar{Q}^n$

All other $\bar{J}$ $\bar{K}$ inputs and the R S inputs are at a "0" level.

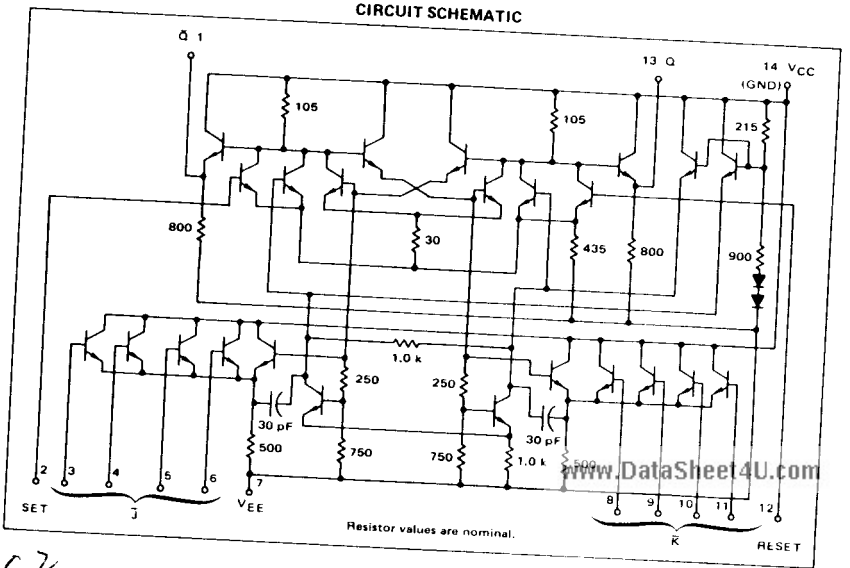
CLOCKED $\bar{J}$ $\bar{K}$ TRUTH TABLE

Pin No.

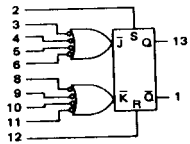
$\bar{J}$	$\bar{K}$	$\bar{C}_D$	Q^n
*	*	**	13
ϕ	ϕ	0	Q^n
0	0	1	$\bar{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n

All other $\bar{J}$ $\bar{K}$ inputs and the R S inputs are at a "0" level.
ϕ = Either state will result in the desired output.

CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1027 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	58	-	-	mAdc
Input Current	I_{in}	2	-	-	-	200	-	-	μAdc
		3	-	-	-		-	-	
		4	-	-	-		-	-	
		5	-	-	-		-	-	
		6	-	-	-		-	-	
		8	-	-	-		-	-	
		9	-	-	-		-	-	
		10	-	-	-		-	-	
		11	-	-	-		-	-	
		12	-	-	-		-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	1.0	-	5.0	μAdc
"Q" Logical "1" Output Voltage‡	V_{OH}‡	13	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	13	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	1	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	1	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"Q" or "$\bar{Q}$" Latch Voltage	V_L	2	-1.31	-1.13	-1.27	-1.11	-1.21	-1.04	Vdc
		12	-1.31	-1.13	-1.27	-1.11	-1.21	-1.04	Vdc
Input Toggle Frequency (See Figures 3 & 4)	f_{Tog}	13	-	-	100	-	-	-	MHz
Sensitivity (No Toggle)	-	1	←		See Figure 1		→		
		13	←		See Figure 1		→		
Sensitivity (Toggle)	-	1, 13	←		See Figure 2		→		
Switching Times④			Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{6+1+}	1	4.0	6.0	4.0	6.0	5.0	8.0	ns
	t_{6+1-}	1							
	t_{8+13+}	13							
	t_{8+13-}	13							
Rise Time	t_{1+}	1							
	t_{13+}	13							
Fall Time	t_{1-}	1							
	t_{13-}	13							

* Individually test each input using the pin connections shown.

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA)

① $V_{in(set)} = V_{OH}$ then $V_{OL(max)}$.

② $V_{in(reset)} = V_{OH}$ then $V_{OL(max)}$.

③ Input voltage is adjusted to obtain $dV_{in}/dV_{in} = \infty$.

④ AC fan-out = 3

@Test Temperature	TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	mAdc I_L
0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	dV_{in}	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
Input Current	I_{in}	2	-	-	2	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
		3	-	-	3	2, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	
		4	-	-	4	2, 3, 5, 6, 7, 8, 9, 10, 11, 12	-	-	
		5	-	-	5	2, 3, 4, 6, 7, 8, 9, 10, 11, 12	-	-	
		6	-	-	6	2, 3, 4, 5, 7, 8, 9, 10, 11, 12	-	-	
		8	-	-	8	2, 3, 4, 5, 6, 7, 9, 10, 11, 12	-	-	
		9	-	-	9	2, 3, 4, 5, 6, 7, 8, 10, 11, 12	-	-	
		10	-	-	10	2, 3, 4, 5, 6, 7, 8, 9, 11, 12	-	-	
		11	-	-	11	2, 3, 4, 5, 6, 7, 8, 9, 10, 12	-	-	
		12	-	-	12	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
"Q" Logical "1" Output Voltage†	V_{OH}†	13	-	-	2 ①	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	13	-	14
"Q" Logical "0" Output Voltage	V_{OL}	13	-	-	12 ②	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	-	-	14
"$\bar{Q}$" Logical "1" Output Voltage†	V_{OH}†	1	-	-	12 ②	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1	-	14
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	1	-	-	2 ①	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
"Q" or "$\bar{Q}$" Latch Voltage	V_L	2	-	-	-	3, 4, 5, 6, 7, 8, 9, 10, 11	-	2 ③	14
		12	-	-	-	3, 4, 5, 6, 7, 8, 9, 10, 11	-	12 ③	14
			Pulse In	Pulse Out					
Input Toggle Frequency (See Figures 3 & 4)	f_{Tog}	13	6, 8	13	-	2, 3, 4, 5, 7, 9, 10, 11, 12	-	-	14
Sensitivity (No Toggle)	-	1	6, 8	1	-		-	-	14
		13	6, 8	13			-	-	
Sensitivity (Toggle)	-	1, 13	6, 8	1, 13	-		-	-	
Switching Times ④						V_{EE} = −4.0 Vdc			+1.2V
Propagation Delay	t_{6+1+}	1	6	1	-	2, 3, 4, 5, 7, 9, 10, 11, 12	-	-	14
	t_{6+1-}	1	6	1	-		-	-	
	t_{8+13+}	13	8	13	-		-	-	
	t_{8+13-}	13	8	13	-		-	-	
Rise Time	t_{1+}	1	6	1	-		-	-	
	t_{13+}	13	8	13	-		-	-	
Fall Time	t_{1-}	1	6	1	-		-	-	
	t_{13-}	13	8	13					

FIGURE 1 - SENSITIVITY (NO TOGGLE)

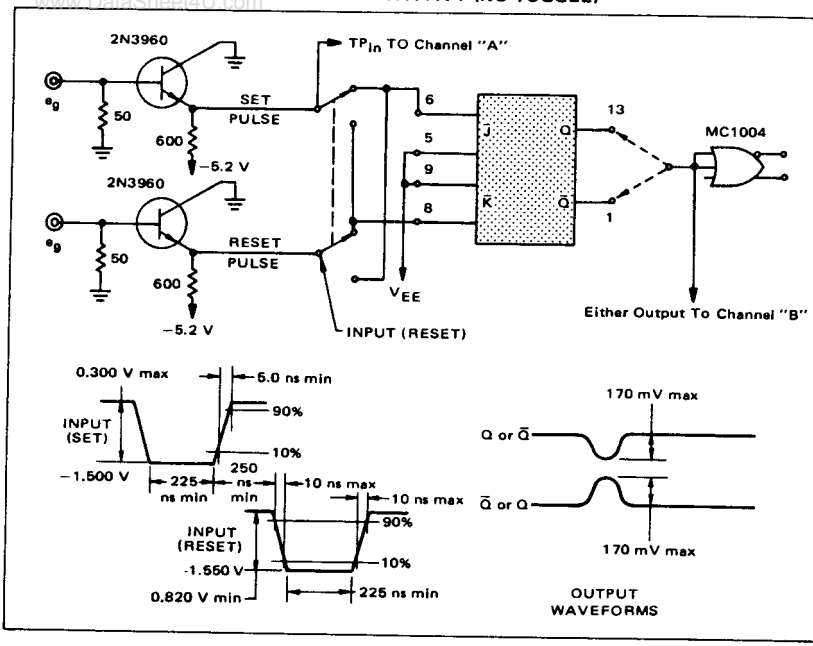
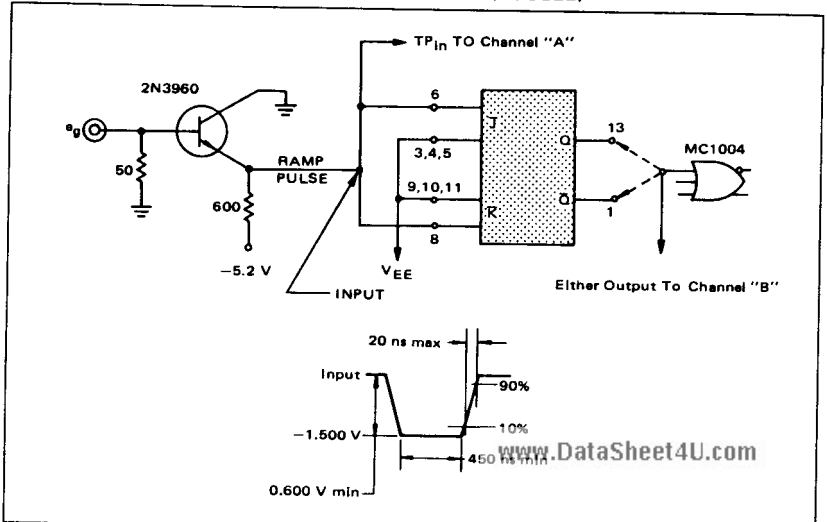
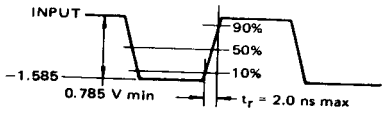


FIGURE 2 - SENSITIVITY (TOGGLE)

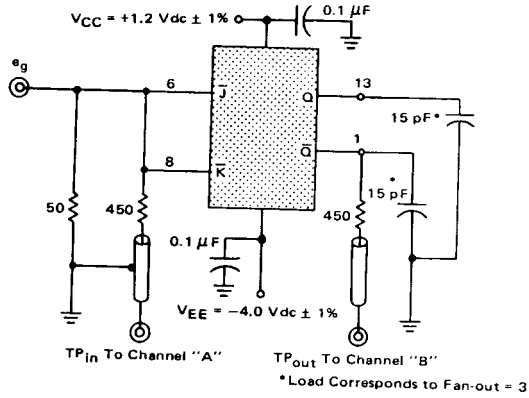


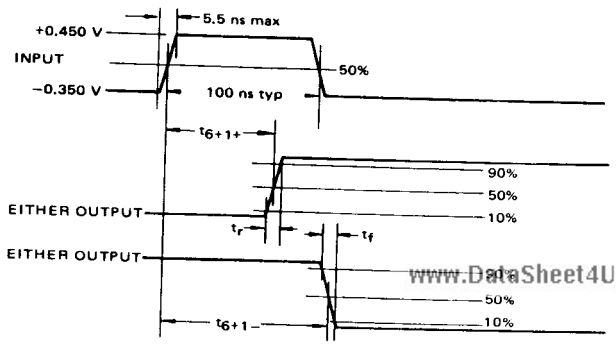


Input Frequency = 100 MHz @ 50% Duty Cycle
Output Frequency = 1/2 Input Frequency

FIGURE 3 - INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

FIGURE 4 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C





APPLICATIONS INFORMATION

The MC1027 flip-flop is obtained by reducing all resistor values of the MC1013 by a factor of two. The resultant flip-flop is no longer limited by circuit design, but by device speeds. Typically the MC1027 will operate 50% faster than the MC1013. Power dissipation is doubled over that of the MC1013, but circuit operation is the same. The MC1023 clock driver is recommended for driving the MC1027 to its full capability. (The MC1023 high-speed clock driver exhibits propagation delay and rise times of about 2.0 ns when driving five flip-flops.) Maximum operating frequency depends upon layout techniques. Short lead lengths with low impedance lines are recommended. A 100+MHz shift counter is shown in Figure 5.

Operation of the MC1027 is very uniform with negligible variation observed with temperature change from 0°C to +75°C. Propagation delay is nominally 4.5 ns, with rise and fall times varying from 3.5 to 4.0 ns with a load of another flip-flop on the output.

FIGURE 5 - 100 + MHz "SWITCH-TAIL" RING COUNTER

Shift pattern of five "0"s and five "1"s is assured by logic feedback from the fourth to first stage.