



MOTOROLA

MC10H423

TRIPLE-3 INPUT BUS DRIVER WITH ENABLE

The MC10H423 is a triple 3 Input Bus Driver with a common enable.

The MC10H423 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with $V_{OL} = -2.1$ Vdc so that the bus may be terminated to -2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the MC10H423 are "turned off." This eliminates discontinuities in the characteristic impedance of the bus.

The V_{OH} level is specified when driving a 25-ohm load terminated to -2.0 Vdc, the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10H423, higher impedance values may be used with this part. A typical 50 ohm bus is shown in Figure 1.

- Propagation Delay, 1.5 ns Typical
- Voltage Compensated
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply ($V_{CC} = 0$)	V_{EE}	-8.0 to 0	Vdc
Input Voltage ($V_{CC} = 0$)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous	I_{out}	50	mA
— Surge		100	
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic	T_{stg}	-55 to +150	°C
— Ceramic		-55 to +165	°C

ELECTRICAL CHARACTERISTICS ($V_{EE} = -5.2$ V $\pm 5\%$) (See Note)

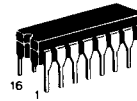
Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	60	—	56	—	60	mA
Input Current High Pins 4,5,6,9,10, 11,12,13,14 Pin 7	I_{inH}	—	495 765	—	310 475	—	310 475	μ A
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μ A
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-2.1	-2.03	-2.1	-2.03	-2.1	-2.03	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Characteristic	Symbol	0.95	1.85	1.0	2.0	1.1	2.1	ns
Propagation Delay Pin 7 Only Exclude Pin 7	t_{pd}	0.7	1.45	0.75	1.6	0.8	1.7	
Rise Time	t_r	0.55	2.0	0.55	2.1	0.6	2.2	ns
Fall Time	t_f	0.55	2.0	0.55	2.1	0.6	2.2	ns

NOTE:

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.1 volts.



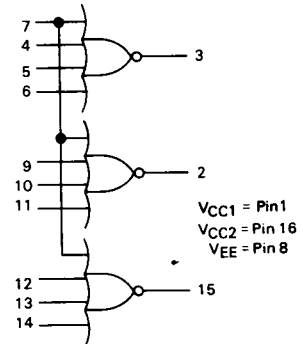
**L SUFFIX
CERAMIC PACKAGE
CASE 620**

**P SUFFIX
PLASTIC PACKAGE
CASE 648**

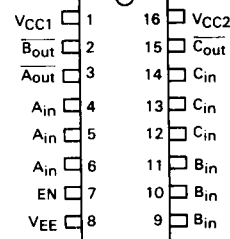


**FN SUFFIX
PLCC
CASE 775**

LOGIC DIAGRAM



**DIP
PIN ASSIGNMENT**



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

FIGURE 1 — 50-OHM BUS DRIVER (25-OHM LOAD)

