4-Bit ECL/TTL Load Reducing DRAM Driver

MC10H660
MC100H660

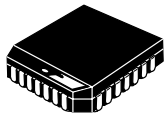
The MC10H/100H660 is a 4–bit ECL input, translating DRAM address driver, ideally suited for driving TTL compatible DRAM inputs from an ECL system. It is designed for use in high capacity, highly interleaved DRAM memory boards, that directly interface to a high speed, pipelined ECL bus interface, where new operations may be initiated to the board at up to a 50 MHz rate.

The latch provides the capability for the memory controller to propagate new addresses to different banks without having to wait for the address timing constraints to be satisfied from a previous memory operation. The dual output fanout reduces input loading from the controller by a factor of two, thus significantly improving board etch propagation delays from the controller, without the need for additional ECL buffering.

The H660 features special TTL outputs which do not have an IOS limiting resistor, therefore allowing rapid charging of the load capacitance. Output voltage levels are designed specifically for driving DRAM inputs. The output stages feature separate power and ground pins to isolate output switching noise from internal circuitry, and also to improve simultaneous switching performance.

The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

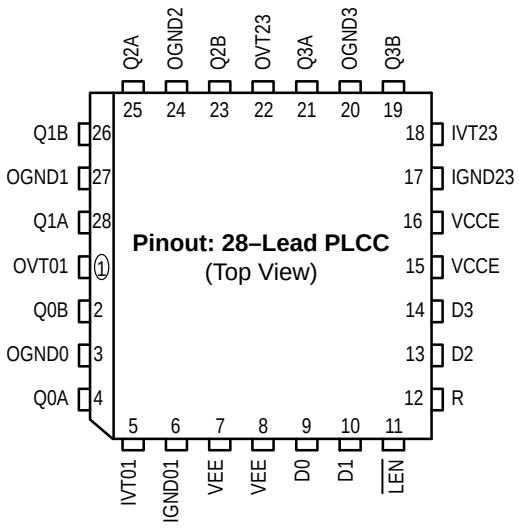
- High Capacitive Drive Outputs to Drive DRAM Address Inputs
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- 10.7 ns Max. D to Q into 300 pF



FN SUFFIX
PLASTIC PACKAGE
CASE 776–02

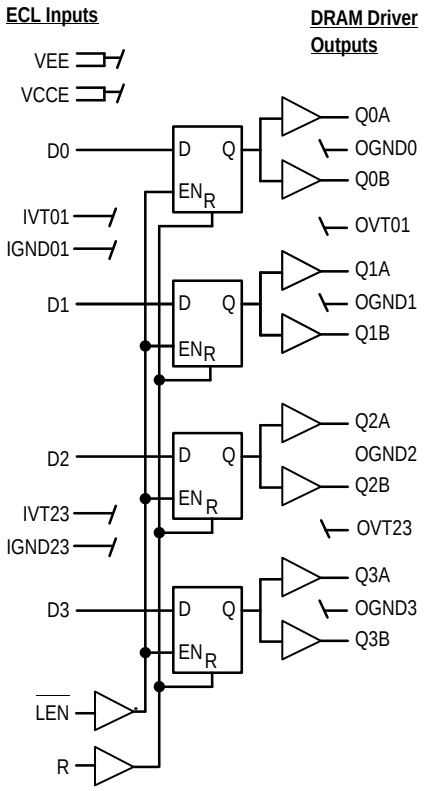
PIN NAMES

PIN	FUNCTION
OGND[0:3]	Output Ground (0V)
OVT01, OVT23	Output VCCT (+5.0 V)
IGND01, IGND23	Internal TTL Ground (OV)
IVT01, IVT23	Internal TTL VCCT (+5.0 V)
VEE	ECL Neg. Supply (–5.2/ –4.5 V)
VCCE	ECL Ground (0V)
D[0:3]	Data Inputs (ECL)
Q[0:3]A, Q[0:3]B	Data Outputs (TTL levels)
LEN	Latch Enable (ECL)
R	Reset (ECL)



Pinout: 28–Lead PLCC
(Top View)

LOGIC SYMBOL



TRUTH TABLE

D	$\overline{\text{LEN}}$	R	Q
L	H	L	L
H	H	L	H
X	L	L	Q_0
X	X	H	L

MOTOROLA

DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ±5% (10H version); V_{EE} = –4.2 V to –5.5 V (100H version)

			0°C		25°C		85°C			
Symbol	**Characteristic**		**min**	**max**	**min**	**max**	**min**	**max**	**Unit**	**Condition**
I_{EE}	Power Supply Current	ECL		41.8		44.0		46.2	mA	
I_{CCH}		TTL		77.0		77.1		79.2	mA	
I_{CCL}				94.6		95.7		96.8	mA	

TTL CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ±5% (10H version); V_{EE} = –4.2 V to –5.5 V (100H version)

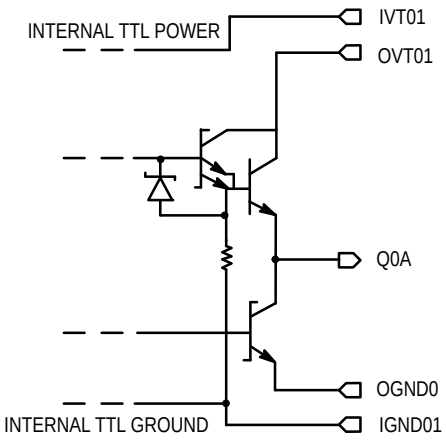
		0°C		25°C		85°C			
Symbol	**Characteristic**	**min**	**max**	**min**	**max**	**min**	**max**	**Unit**	**Condition**
V_{OH}	Output HIGH Voltage	2.6		2.6		2.6		V	I_{OH} = –24 mA
V_{OL}	Output LOW Voltage		0.50		0.50		0.50	V	I_{OL} = 24 mA
I_{OS}	Output Short Circuit Current*		*		*		*	V	See Note 1

1. The outputs must not be shorted to ground, as this will result in permanent damage to the device. The high drive outputs of this device do not include a limiting IOS resistor. Minimum recommended load capacitance is 100 pF. Precise output performance and waveforms will depend on the exact nature of the actual load. The lumped load is of course an approximation to a real memory system load.

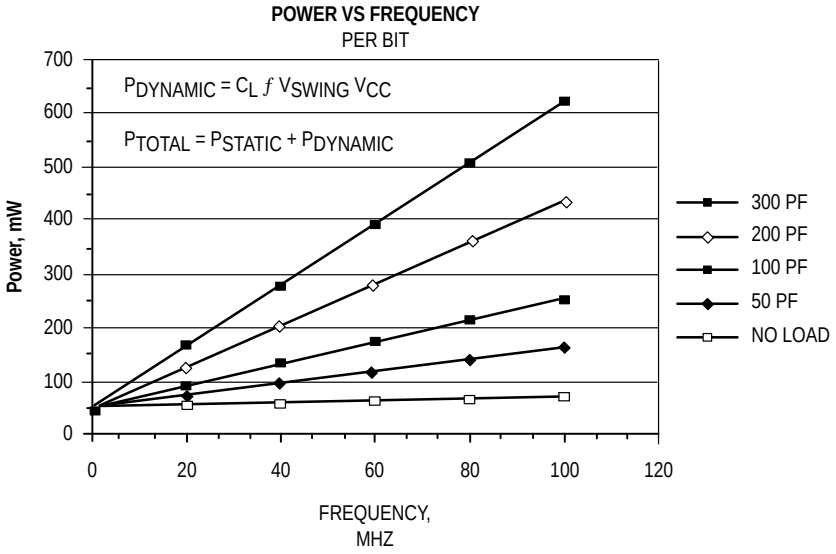
AC Characteristics: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ±5% (10H version) V_{EE} = –4.2 V to –5.5 V (100H version)

			0°C		25°C		85°C			
Symbol	**Characteristic**		**min**	**max**	**min**	**max**	**min**	**max**	**Unit**	**Condition**
t_S	Set–up Time, D to $\overline{LEN}$		0.5		0.5		0.5		ns	
t_n	Hold Time, D to $\overline{LEN}$		1.5		1.5		1.5		ns	
$t_W(H)$	LEN Pulse Width, HIGH		2.0		2.0		2.0		ns	
t_R t_F	Output Rise/Fall Time 0.8 V – 2.0 V		0.5	2.0	0.5	2.0	0.5	2.0	ns	C_L = 200 pF
t_{PLH} t_{PHL}	Propagation Delay to Output	D	3.0 4.0 4.5	6.0 8.0 9.5	3.0 4.0 4.5	6.0 8.0 9.5	3.0 4.0 4.5	6.0 8.0 9.5	ns	C_L = 100 pF C_L = 200 pF C_L = 300 pF
	50% point of ECL input to 1.5 V point of TTL output	$\overline{LEN}$	4.3 4.9 5.4	6.9 8.9 10.4	4.3 4.9 5.4	6.9 8.9 10.4	4.3 4.9 5.4	6.9 8.9 10.4	ns	C_L = 100 pF C_L = 200 pF C_L = 300 pF
t_{PHL}	Propagation Delay to Output	R	4.1 4.5 5.0	9.1 8.5 10.0	4.1 4.5 5.0	9.1 8.5 10.0	4.1 4.5 5.0	9.1 8.5 10.0	ns	C_L = 100 pF C_L = 200 pF C_L = 300 pF
t_{PLH}	Propagation Delay to Output	D	3.9 4.8 5.8	5.9 7.2 8.8	3.9 4.8 5.8	5.9 7.2 8.8	4.0 5.0 5.9	6.1 7.4 8.9	ns	C_L = 100 pF C_L = 200 pF C_L = 300 pF
	50% point of ECL input to 2.4 V point of TTL output	$\overline{LEN}$	4.7 5.5 6.3	7.1 8.3 9.5	4.7 5.5 6.3	7.1 8.3 9.5	4.8 5.6 6.4	7.2 8.4 9.6	ns	C_L = 100 pF C_L = 200 pF C_L = 300 pF
t_{PHL}	Propagation Delay to Output	D	4.5 6.0 7.0	6.7 9.0 10.6	4.5 6.0 7.0	6.7 9.0 10.6	4.4 6.0 6.9	6.6 9.0 10.3	ns	C_L = 100 pF C_L = 200 pF C_L = 300 pF
	50% point of ECL input to 0.8 V point of TTL output	$\overline{LEN}$	4.0 4.9 6.0	6.0 7.3 9.0	4.0 4.9 6.0	6.0 7.3 9.0	4.0 4.9 5.9	6.0 7.3 8.9	ns	C_L = 100 pF C_L = 200 pF C_L = 300 pF
		R	4.3 6.1 7.2	6.5 9.1 10.8	4.3 6.1 7.2	6.5 9.1 10.8	4.3 6.1 7.2	6.5 9.1 10.8	ns	C_L = 100 pF C_L = 200 pF C_L = 300 pF

OUTPUT STRUCTURE
– Output Q0A Structure Shown



POWER VS FREQUENCY
– typical



10H ECL DC Characteristics: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5%

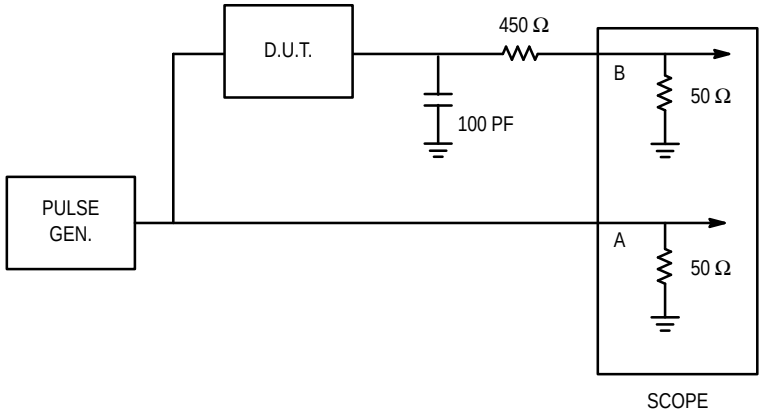
		0°C		25°C		85°C			
Symbol	**Characteristic**	**min**	**max**	**min**	**max**	**min**	**max**	**Unit**	**Condition**
I_{IH}	Input HIGH Current		225		145		145	µA	
I_{IL}	Input LOW Current	1.5		1.0		1.0		µA	
V_{IH}	Input HIGH Voltage	–1170	–840	–1130	–810	–1060	–720	mV	
V_{IL}	Input LOW Voltage	–1950	–1480	–1950	–1480	–1950	–1445	mV	

100H ECL DC Characteristics: V_{CCT} = 5.0 V ± 10%; V_{EE} = –4.2 V to –5.5 V

		0°C		25°C		85°C			
Symbol	**Characteristic**	**min**	**max**	**min**	**max**	**min**	**max**	**Unit**	**Condition**
I_{IH}	Input HIGH Current		225		145		145	µA	
I_{IL}	Input LOW Current	1.5		1.0		1.0		µA	
V_{IH}	Input HIGH Voltage	–1165	–880	–1165	–880	–1165	–880	mV	
V_{IL}	Input LOW Voltage	–1810	–1475	–1810	–1475	–1810	–1475	mV	

AC TEST SET–UP

C_L = 100 pF



The MC10H/100 H660 ECL–TTL DRAM Address Driver

The MC 10H/100H660 was designed for use in high capacity, highly interleaved DRAM memory boards, that directly interface to a high speed, pipelined ECL bus interface, where new operations may be initiated to the board at a 50 MHz rate (e.g. bipolar RISC systems).

The following briefly discusses the major design features of the part over existing semiconductor devices traditionally used in interfacing DRAMs in high performance system environments.

1. ECL Translator

High performance memory systems of the past that were interfaced to ECL buses had to rely on separate ECL translators and DRAM drivers to interface to large DRAM arrays, which is acceptable if the module is not highly interleaved and the bus cycle time is comparable to the DRAM access time. This becomes inadequate as the cycle time of the interface becomes significantly faster than the address timing requirements of the RAM, and as the degree of internal board interleaving increases. These higher performance demands require that the internal address and control signals propagated to the DRAM drivers be implemented in ECL, thus requiring the integration of the driver and translator functions.

Integration of the translator/drive function also reduces access latency, as well as keeping DRAM timing parameters from being violated, due to the excessive delays encountered with separate parts.

2. MOS Drive Capacity

Outputs are specifically designed for driving large numbers of DRAMs ($\approx$300 pF), which reduce the number of parts and power requirements needed per board. Output voltage levels are designed specifically for driving DRAM inputs. No ECL translator parts on the market today provide the designer with this drive capability as well as the flexibility to vary the number of DRAMs that are driven by the part.

3. Transparent Latch

The latch is added to provide the capability for a memory controller to propagate new addresses to different banks without having to wait for the address timing constraints to be satisfied from a previous memory operation. For system implementations where this is acceptable, the user has the capability to keep the latch open, thus having the part act as an address translator/buffer, with minimal performance impact due to the additional propagation delay incurred from the internal latch. The latch is controlled within an already existing DRAM timing signal.

4. 1:2 Output Fanout

This function is useful in that it reduces input loading from the controller by a factor of two, thus significantly improving board etch propagation delays from the controller to the large number of translators, without the addition of ECL glue logic parts to reduce the loading. In large memory boards, so many translators are needed that this type of organization is not a handicap.

5. Low Skew, Low Propagation Delay

Low skew of the part as well as fast propagation delay enable faster overall DRAM operation to be attained than is possible with existing parts.

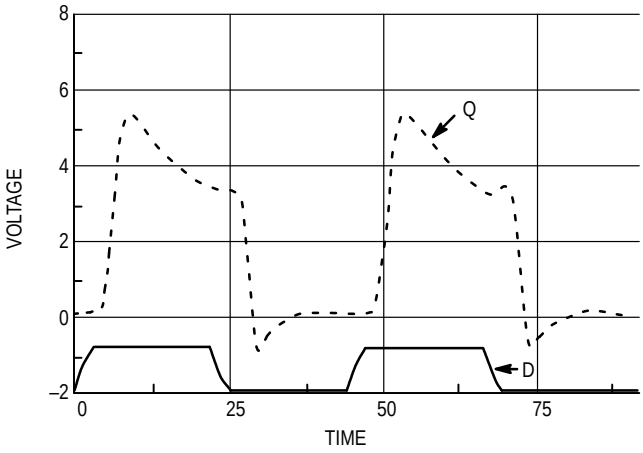
6. Power and Package Pin Layout

The H660 is specifically designed with additional power and ground pins to greatly improve simultaneous switching performance over existing driver parts.

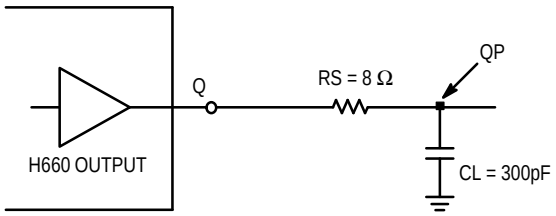
OUTPUT WAVEFORMS

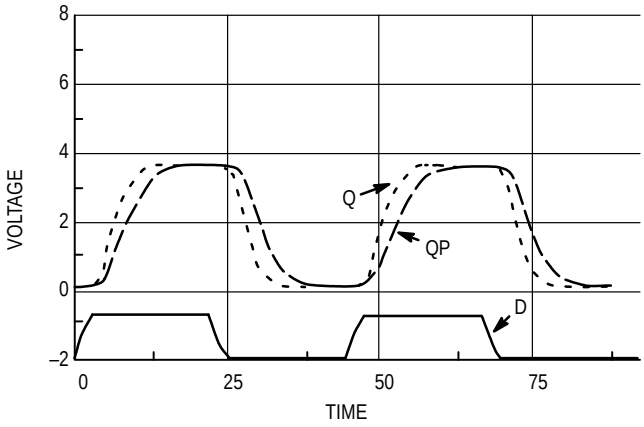
simulated

Example 1. An output load consisting of just CL = 50 pF results in overshoot at the output Q:



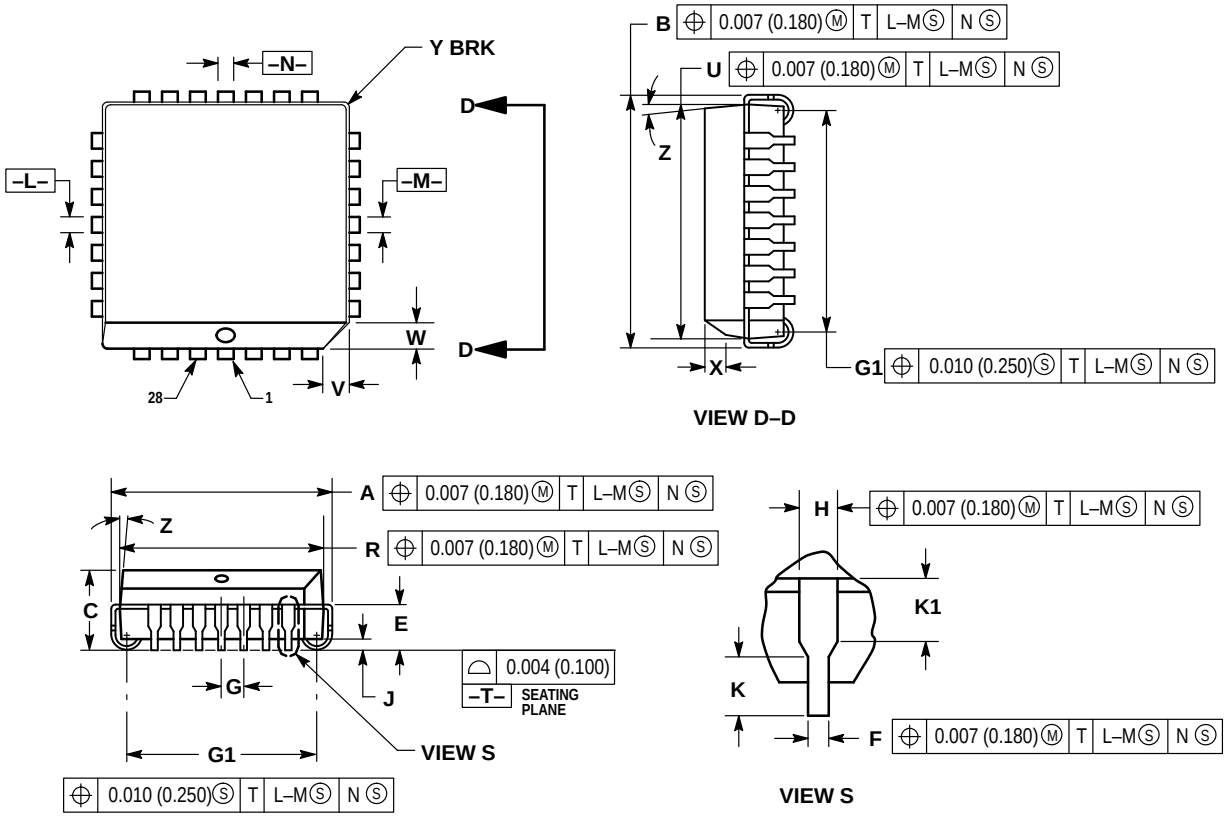
Example 2. In a memory system application, use of an external source resistor is suggested. Simulations run with RS = 8Ω and CL = 300pF leads to clean waveforms both at the output, Q, and at point Qp:





OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE D



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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