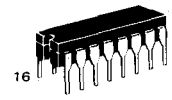
TWO-MODULUS PRESCALER

MC12012

The MC12012 is a two-modulus prescaler which consists of three functional blocks: 1) a controllable divide by 5/divide by 6 prescaler; 2) a divide by 2 prescaler; and 3) a MECL to MTTL translator. When used with the MC12014 Counter Control Logic function and the MC4016 programmable counter, a divide by N programmable counter can be constructed for operation to 200 MHz. This arrangement is especially useful in frequency synthesizer applications.

- ÷2, ÷5/÷6, ÷10/÷11, ÷10/÷12
- MECL to MTTL Translator on Chip
- +5.0 or -5.2 V Operation*
- 200 MHz (typ) Toggle Frequency

*When using +5.0 V supply, apply +5.0 V to pin 16 (V_{CC}) and ground pin 8 (V_{EE}). When using -5.2 V supply, ground pin 16 (V_{CC}) and apply -5.2 V to pin 8 (V_{EE}).



L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT

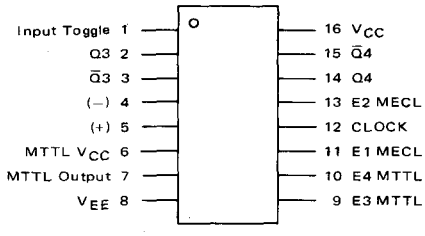


FIGURE 1 – LOGIC DIAGRAM

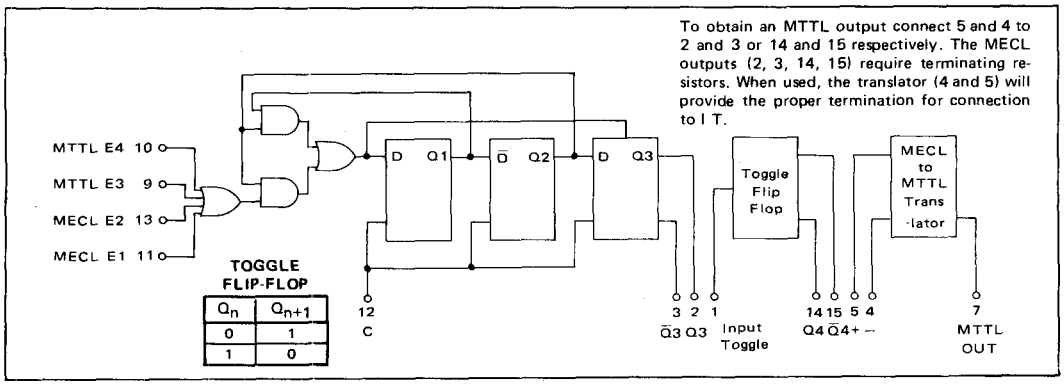
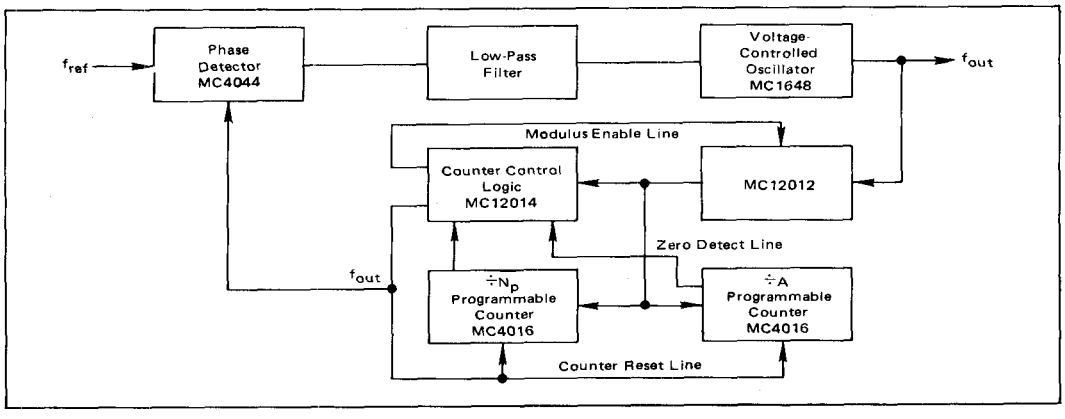


FIGURE 2 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION



6

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8.0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to $V_{IL\,min}$	Vdc
Output Source Current	I_o	20	mAdc
Storage Temperature Range	T_{stg}	-55 to +125	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	0 to +75	°C
DC Fan-Out* (Gates and Flip-Flops)	n	70	–

*AC fan-out is limited by desired system performance.

ELECTRICAL CHARACTERISTICS

Supply Voltage -5.2 V

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IHH}	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}
	TEST VOLTAGE/CURRENT VALUES											
	Volts									mA		
0°C	-0.840	-1.870	-1.145	-1.490	-4.7	+0.3	-3.2	-4.4	-5.2	-2.5	16	-1.6
25°C	-0.810	-1.850	-1.105	-1.475	-4.7	+0.3	-3.2	-4.4	-5.2	-2.5	16	-1.6
75°C	-0.720	-1.880	-1.045	-1.450	-4.7	+0.3	-3.2	-4.4	-5.2	-2.5	16	-1.6

Characteristic	Symbol	Pin Under Test	MC12012 0°C Min	MC12012 0°C Max	MC12012 +25°C Min	MC12012 +25°C Typ	MC12012 +25°C Max	MC12012 +75°C Min	MC12012 +75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IHH}	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	100	–	–	–	mAdc	–	–	–	–	–	–	–	–	8	–	–	–	6,16
Input Current	I_{INH1}	12	–	–	–	100	200	–	–	µAdc	12	–	–	–	–	–	–	–	8	–	–	–	16
	I_{INH2}	1	–	–	–	40	100	–	–	µAdc	1	–	–	–	–	–	–	–	8	–	–	–	16
		11	–	–	–	40	100	–	–		11	–	–	–	–	–	–	–	8	–	–	–	16
		13	–	–	–	40	100	–	–		13	–	–	–	–	–	–	–	8	–	–	–	16
	I_{INH3}	9	–	–	–	–	40	–	–	µAdc	–	–	–	–	–	9	–	–	8	–	–	–	16
		10	–	–	–	–	40	–	–		–	–	–	–	–	10	–	–	8	–	–	–	16
	I_{INH4}	4	–	–	3.5	–	5.5	–	–	mAdc	5	4	–	–	–	–	–	–	8	–	–	–	6
		5	–	–	3.5	–	5.5	–	–	mAdc	5	4	–	–	–	–	–	–	8	–	–	–	6
Leakage Current	I_{INL1}	1	–	–	–	–	2.0	–	–	µAdc	–	–	–	–	–	–	–	–	1,8	–	–	–	16
		11	–	–	–	–	↓	–	–	↓	–	–	–	–	–	–	–	–	8,11	–	–	–	↓
		12	–	–	–	–		–	–		–	–	–	–	–	–	–	–	8,12	–	–	–	
		13	–	–	–	–		–	–		–	–	–	–	–	–	–	–	8,13	–	–	–	
	I_{INL2}	9	–	–	1.1	–	2.2	–	–	mAdc	–	–	–	–	9	–	–	–	8	–	–	–	16
		10	–	–	1.1	–	2.2	–	–	mAdc	–	–	–	–	10	–	–	–	8	–	–	–	16
	I_{INL3}	4	–	–	3.8	–	6.5	–	–	mAdc	4	5	–	–	–	–	–	–	8	–	–	–	16
		5	–	–	2.0	–	4.0	–	–	mAdc	4	5	–	–	–	–	–	–	8	–	–	–	16
Logic "1" Output Voltage ②	V_{OH1}	2	-1.000	-0.840	-0.960	–	-0.810	-0.900	-0.720	Vdc	–	11,13	–	–	9,10	–	–	–	8	2	–	–	16
		3	↓	↓	↓	–	↓	↓	↓	↓	–	11,13	–	–	9,10	–	–	–		3	–	–	↓
		14				–					–	–	–	–	–	–	–	–		14	–	–	
		15				–					–	–	–	–	–	–	–	–		15	–	–	
	V_{OH2}	7	-2.800	–	-2.800	–	–	-2.800	–	Vdc	5	4	–	–	–	–	–	–	8	–	–	7	6
Logic "0" Output Voltage ②	V_{OL1}	2	-1.870	-1.635	-1.850	–	-1.620	-1.830	-1.595	Vdc	–	11,13	–	–	9,10	–	–	–	8	2	–	–	16
		3	↓	↓	↓	–	↓	↓	↓	↓	–	11,13	–	–	9,10	–	–	–		3	–	–	↓
		14				–					–	–	–	–	–	–	–	–		14	–	–	
		15				–					–	–	–	–	–	–	–	–		15	–	–	
	V_{OL2}	7	–	-4.700	–	–	-4.700		-4.700	Vdc	4	5		–	–	–	–	–	8	–	7	–	6
Logic "1" Threshold Voltage	V_{OHA}	2 ③	-1.020	–	-0.980	–	–	-0.920	–	Vdc	–	–	11,13	–	–	–	9,10	–	8	2	–	–	16
		3 ③	↓	–	↓	–	–	↓	–	↓	–	–	11,13	–	–	–	9,10	–		3	–	–	↓
		14 ④		–		–	–		–		–	–	–	–	–	–	–	–		14	–	–	
		15 ④		–		–	–		–		–	–	–	–	–	–	–	–		15	–	–	
Logic "0" Threshold Voltage	V_{OLA}	2 ⑤	–	-1.615	–	–	-1.600	–	-1.575	Vdc	–	–	–	11,13	–	–	–	9,10	8	2	–	–	16
		3 ⑤	–	↓	–	–	↓	–	↓	↓	–	–	–	11,13	–	–	–	9,10		3	–	–	↓
		14 ④	–		–	–		–			–	–	–	–	–	–	–	–		14	–	–	
		15 ④	–		–	–		–			–	–	–	–	–	–	–	–		15	–	–	
Short Circuit Current	I_{OS}	7	-20	-65	-20	–	-65	-20	-65	mAdc	5	4	–	–	–	–	–	–	8	–	–	–	6

ELECTRICAL CHARACTERISTICS

Supply Voltage +5.0 V

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES											
	Volts									mA		
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IHH}	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}
0°C	+4.160	+3.130	+3.855	+3.510	+0.5	+5.5	+2.0	+0.8	+5.0	-2.5	16	-1.6
25°C	+4.190	+3.150	+3.895	+3.525	+0.5	+5.5	+2.0	+0.8	+5.0	-2.5	16	-1.6
75°C	+4.280	+3.170	+3.955	+3.550	+0.5	+5.5	+2.0	+0.8	+5.0	-2.5	16	-1.6

Characteristic	Symbol	Pin Under Test	MC12012 0°C Min	MC12012 0°C Max	MC12012 +25°C Min	MC12012 +25°C Typ	MC12012 +25°C Max	MC12012 +75°C Min	MC12012 +75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IHH}	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	(V_{EE}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	95	–	–	–	mAdc	–	–	–	–	–	–	–	–	6,16	–	–	–	8
Input Current	I_{INH1}	12	–	–	–	100	200	–	–	µAdc	12	–	–	–	–	–	–	–	16	–	–	–	8
	I_{INH2}	1	–	–	–	40	100	–	–	µAdc	1	–	–	–	–	–	–	–	16	–	–	–	8
		11	–	–	–	40	100	–	–		11	–	–	–	–	–	–	–	16	–	–	–	8
		13	–	–	–	40	100	–	–		13	–	–	–	–	–	–	–	16	–	–	–	8
	I_{INH3}	9	–	–	–	–	40	–	–	µAdc	–	–	–	–	–	9	–	–	16	–	–	–	8
		10	–	–	–	–	40	–	–		–	–	–	–	–	10	–	–	16	–	–	–	8
	I_{INH4}	4	–	–	3.5	–	5.5	–	–	mAdc	5	4	–	–	–	–	–	–	6	–	–	–	8
		5	–	–	3.5	–	5.5	–	–	mAdc	5	4	–	–	–	–	–	–	6	–	–	–	8
Leakage Current	I_{INL1}	1	–	–	–	–	2.0	–	–	µAdc	–	–	–	–	–	–	–	–	16	–	–	–	1,8
		11	–	–	–	–	↓	–	–	↓	–	–	–	–	–	–	–	–	↓	–	–	–	8,11
		12	–	–	–	–		–	–		–	–	–	–	–	–	–	–		–	–	–	8,12
		13	–	–	–	–		–	–		–	–	–	–	–	–	–	–		–	–	–	8,13
	I_{INL2}	9	–	–	1.1	–	2.2	–	–	mAdc	–	–	–	–	9	–	–	–	16	–	–	–	8
		10	–	–	1.1	–	2.2	–	–	mAdc	–	–	–	–	10	–	–	–	16	–	–	–	8
	I_{INL3}	4	–	–	3.8	–	6.5	–	–	mAdc	4	5	–	–	–	–	–	–	6	–	–	–	8
		5	–	–	2.0	–	4.0	–	–	mAdc	4	5	–	–	–	–	–	–	6	–	–	–	8
Logic "1" Output Voltage ②	V_{OH1}	2	4.000	4.160	4.040	–	4.190	4.100	4.280	Vdc	–	11,13	–	–	9,10	–	–	–	16	2	–	–	8
		3	↓	↓	↓	–	↓	↓	↓	↓	–	11,13	–	–	9,10	–	–	–	↓	3	–	–	↓
		14				–					–	–	–	–	–	–	–	–		14	–	–	
		15				–					–	–	–	–	–	–	–	–		15	–	–	
	V_{OH2}	7	2.400	–	2.400	–	–	2.400	–	Vdc	5	4	–	–	–	–	–	–	6	–	–	7	8
Logic "0" Output Voltage ②	V_{OL1}	2	3.190	3.430	3.210	–	3.440	3.230	3.470	Vdc	–	11,13	–	–	9,10	–	–	–	16	2	–	–	8
		3	↓	↓	↓	–	↓	↓	↓	↓	–	11,13	–	–	9,10	–	–	–	↓	3	–	–	↓
		14				–					–	–	–	–	–	–	–	–		14	–	–	
		15				–					–	–	–	–	–	–	–	–		15	–	–	
	V_{OL2}	7		0.500	–	–	0.500	–	0.500	Vdc	4	5	–	–	–	–	–	–	6	–	–	7	8
Logic "1" Threshold Voltage	V_{OHA}	2 ③	3.980	–	4.020	–	–	4.080	–	Vdc	–	–	11,13	–	–	–	9,10	–	16	2	–	–	8
		3 ③	↓	–	↓	–	–	↓	–	↓	–	–	11,13	–	–	–	9,10	–	↓	3	–	–	↓
		14 ④		–		–	–		–		–	–	–	–	–	–	–	–		14	–	–	
		15 ④		–		–	–		–		–	–	–	–	–	–	–	–		15	–	–	
Logic "0" Threshold Voltage	V_{OLA}	2 ⑤	–	3.450	–	–	3.460	–	3.490	Vdc	–	–	–	11,13	–	–	–	9,10	16	2	–	–	8
		3 ⑤	–	↓	–	–	↓	–	↓	↓	–	–	–	11,13	–	–	–	9,10	↓	3	–	–	↓
		14 ④	–		–	–		–			–	–	–	–	–	–	–	–		14	–	–	
		15 ④	–		–	–		–			–	–	–	–	–	–	–	–		15	–	–	
Short Circuit Current	I_{OS}	7	-20	-65	-20	–	-65	-20	-65	mAdc	5	4	–	–	–	–	–	–	6	–	–	–	8

Characteristic	Symbol	Pin Under Test	MC12012 0°C Min	MC12012 0°C Max	MC12012 +25°C Min	MC12012 +25°C Typ	MC12012 +25°C Max	MC12012 +75°C Min	MC12012 +75°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	V_{IHmin} +1.100	V_{ILmin} +0.130	V_F -3.0 V	V_{EE} -3.0 or -3.2	V_{CC} +2.0
Propagation Delay (See Figures 3 and 4)	t_{12+2+}	12,2	–	–	2.0	3.0	4.0	–	–	ns	12	–	–	–	11,13	9,10	8	6,16
	t_{12+3+}	12,3	–	–	↓	3.0	↓	–	–	↓	↓	–	–	–	11,13	9,10	↓	↓
	t_{12+}	12,2	–	–		2.8		–	–			–	–	–	11,13	9,10		
	t_{12+3-}	12,3	–	–		2.8		–	–		↓	–	–	–	11,13	9,10		
	t_{1+14+}	1,14	–	–		3.0		–	–		1	–	–	–	–	–		
	t_{1+15+}	1,15	–	–		3.0		–	–		↓	–	–	–	–	–		
	t_{1+14-}	1,14	–	–		2.8		–	–			–	–	–	–	–		
	t_{1+15-}	1,15	–	–		2.8	↓	–	–		↓	–	–	–	–	–		
	t_{5+7+}	5,7	–	–		8.0	12.0	–	–		A	–	–	–	–	–		
	t_{5-7-}	5,7	–	–	↓	5.0	10.0	–	–	↓	A	–	–	–	–	–	↓	↓
Output Rise Time (See Figure 4)	t_{2+}	2	–	–	–	2.0	–	–	–	ns	12	–	–	–	11,13	9,10	8	6,16
	t_{3+}	3	–	–	–	2.0	–	–	–		12	–	–	–	11,13	9,10		
	t_{14+}	14	–	–	–	2.0	–	–	–		1	–	–	–	–	–		
	t_{15+}	15	–	–	–	2.0	–	–	–	↓	1	–	–	–	–	–	↓	↓
Output Fall Time (See Figure 4)	t_{2-}	2	–	–	–	2.0	–	–	–	ns	12	–	–	–	11,13	9,10	8	6,16
	t_{3-}	3	–	–	–	2.0	–	–	–		12	–	–	–	11,13	9,10		
	t_{14-}	14	–	–	–	2.0	–	–	–		1	–	–	–	–	–		
	t_{15-}	15	–	–	–	2.0	–	–	–	↓	1	–	–	–	–	–	↓	↓
Setup Time (See Figure 5)	t_{setup1}	11,13	–	4.0	–	2.4	3.0	–	4.0	ns	12	11/13	–	–	13/11	9,10	8	6,16
	t_{setup2}	9,10	–	7.0	–	5.0	7.0	–	8.5	ns	12	–	9/10	–	11,13	10/9	8	6,16
Release Time (See Figure 5)	t_{rel1}	11,13	–	2.5	–	1.2	2.0	–	2.0	ns	12	11/13	–	–	13/11	9,10	8	6,16
	t_{rel2}	9,10	–	4.0	–	2.5	3.5	–	2.0	ns	12	–	9/10	–	11,13	10/9	8	6,16
Toggle Frequency	f_{max}									MHz								
Figure 6 (÷5)	↓	2	–	–	175	200	–	–	–	↓	–	–	–	11	13	9,10	8	16
(÷6)		2	–	–	↓	↓	–	–	–		–	–	–	–	11,13	9,10	↓	↓
(÷2)		14	–	–			–	–	–		–	–	–	–	–	–		
Figure 7 (÷10 or 11)		14	–	–			–	–	–	↓	–	–	–	–	–	–		

① All MECL outputs (2,3,14,15) are terminated to V_{EE} through an external 510 Ω resistor during the DC tests.

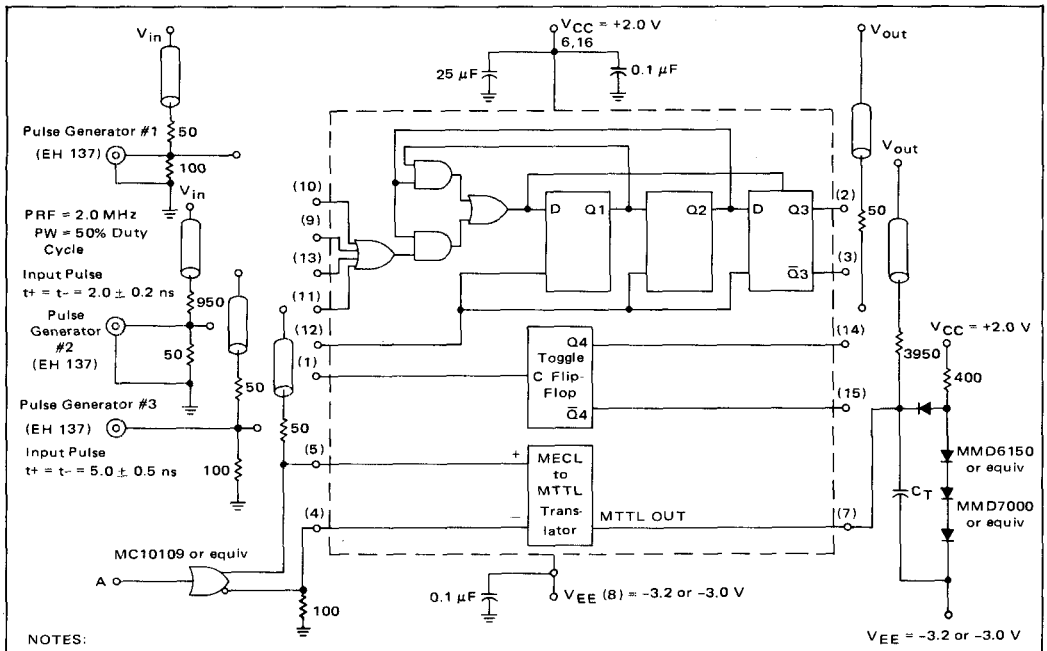
② Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is

③ In addition to meeting the output levels specified, the device must divide by 5 during this test. The clock input is

④ In addition to meeting the output levels specified the device must divide by 2 with a clock input of

⑤ In addition to meeting the output levels specified, the device must divide by 6 during this test. The clock input is

FIGURE 3 – AC TEST CIRCUIT



NOTES:

All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.

All unused cables must be terminated with 50 ohms.

All resistors are ± 1%.

C_T = 15 pF = total parasitic capacitance which includes probe, wiring, and load capacitance.

The 950-ohm resistor and the scope termination impedance constitute a 20:a attenuator probe.

The 50-ohm resistor and the scope termination impedance constitute a 2:1 attenuator probe.

FIGURE 4 – AC VOLTAGE WAVEFORMS

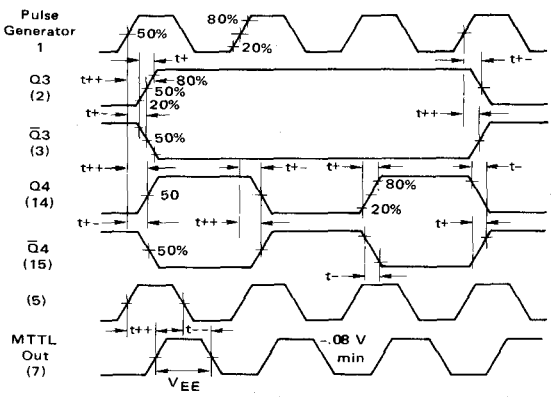


FIGURE 5 – SETUP AND RELEASE TIME WAVEFORMS

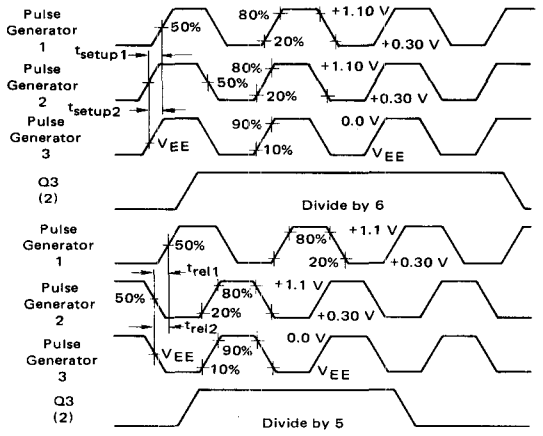
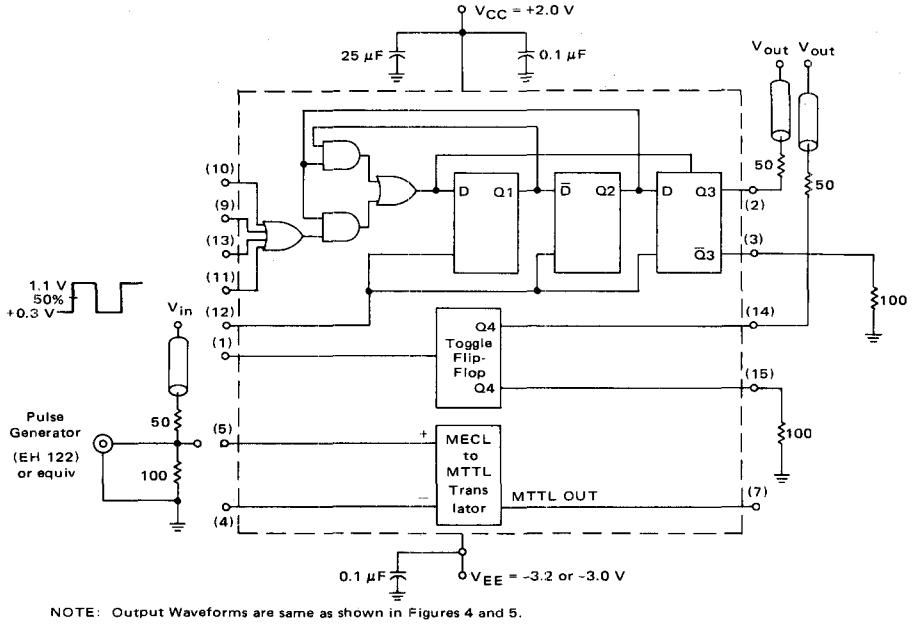


FIGURE 6 – MAXIMUM FREQUENCY TEST CIRCUIT



NOTE: Output Waveforms are same as shown in Figures 4 and 5.

FIGURE 7 – MAXIMUM FREQUENCY TEST CIRCUIT

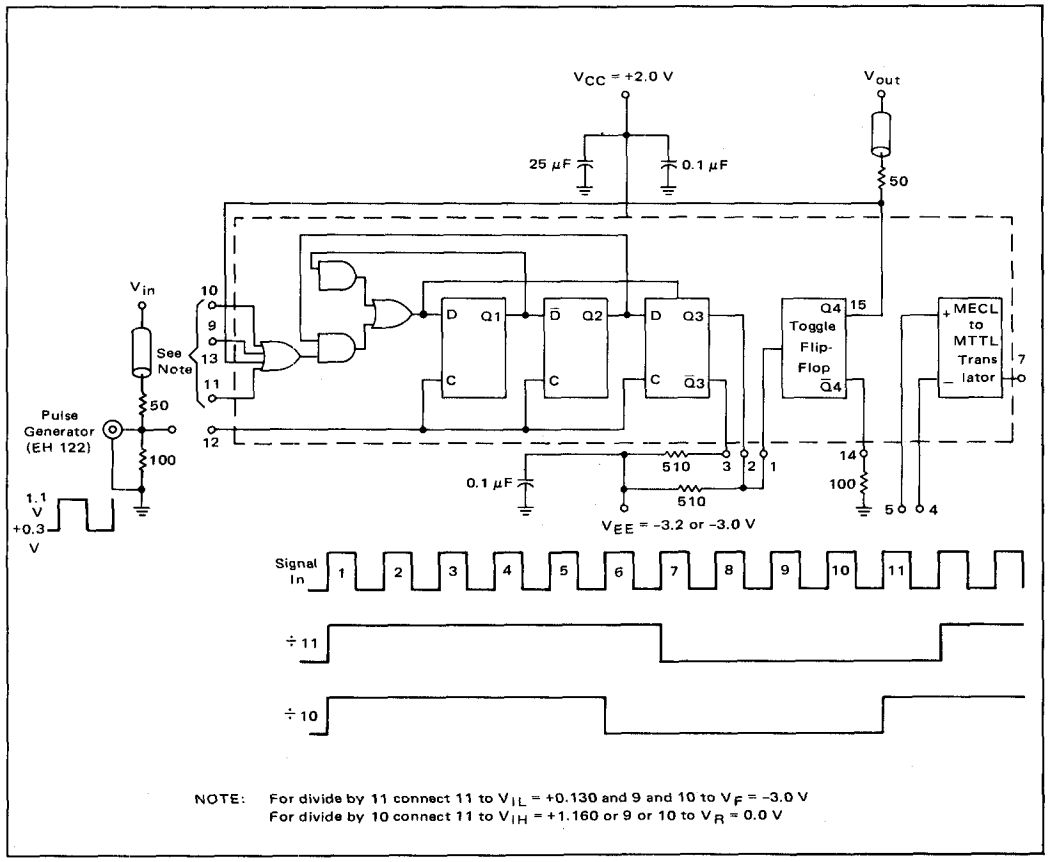
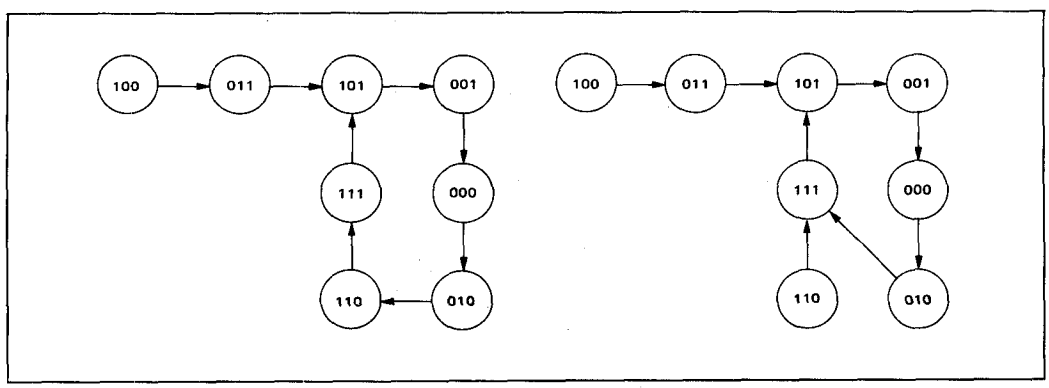
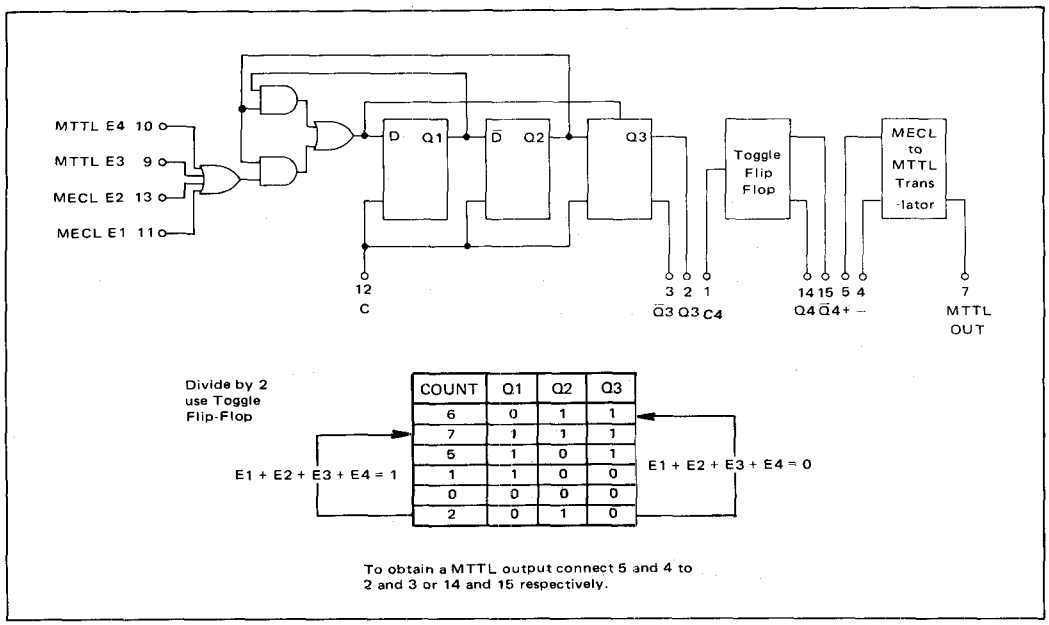


FIGURE 8 – STATE DIAGRAMS



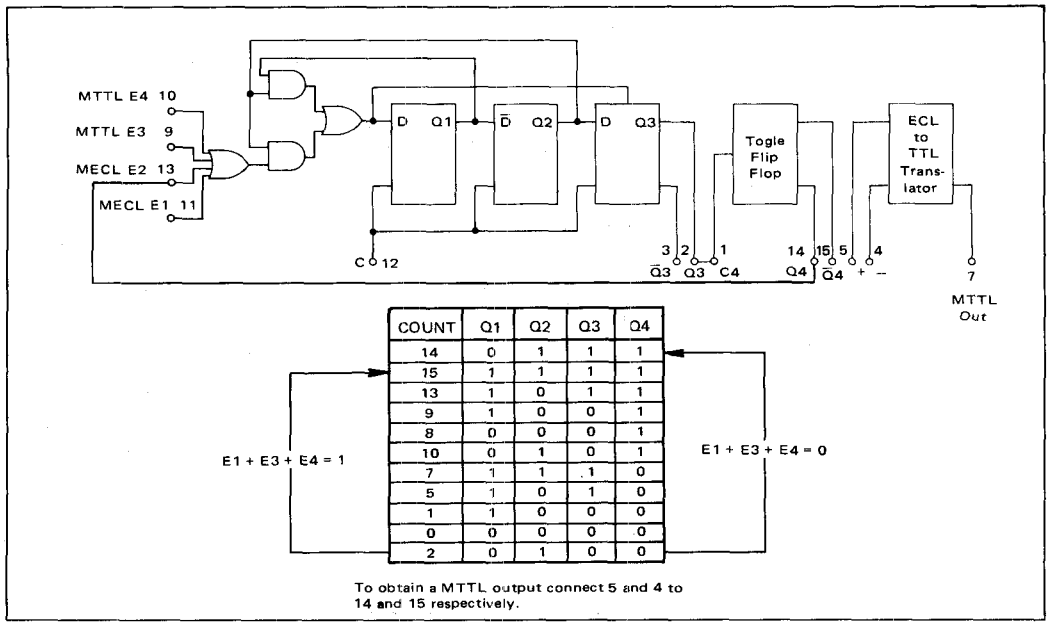
6

FIGURE 9 – ÷5/6



COUNT	Q1	Q2	Q3
6	0	1	1
7	1	1	1
5	1	0	1
1	1	0	0
0	0	0	0
2	0	1	0

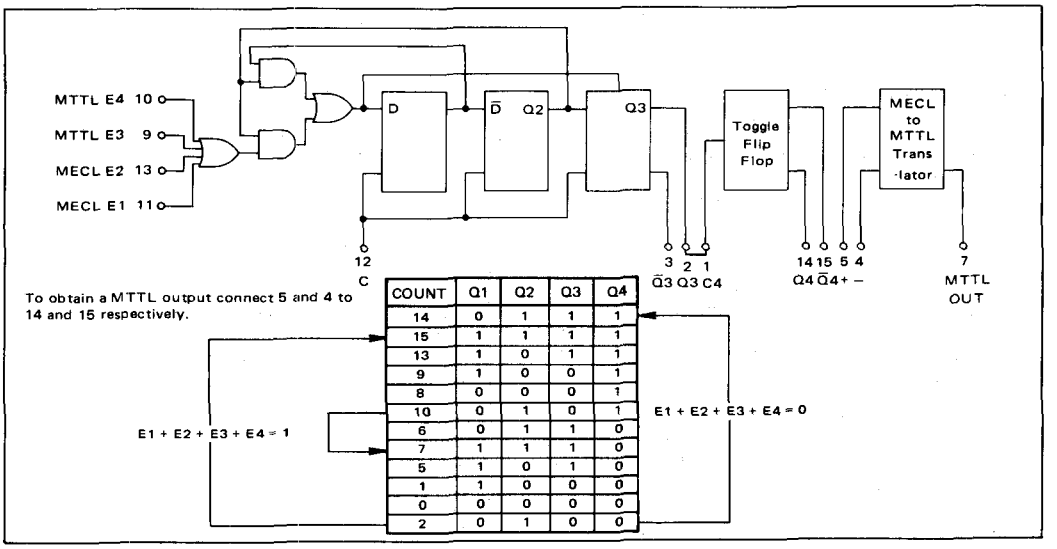
FIGURE 10 – ÷10/11



COUNT	Q1	Q2	Q3	Q4
14	0	1	1	1
15	1	1	1	1
13	1	0	1	1
9	1	0	0	1
8	0	0	0	1
10	0	1	0	1
7	1	1	1	0
5	1	0	1	0
1	1	0	0	0
0	0	0	0	0
2	0	1	0	0

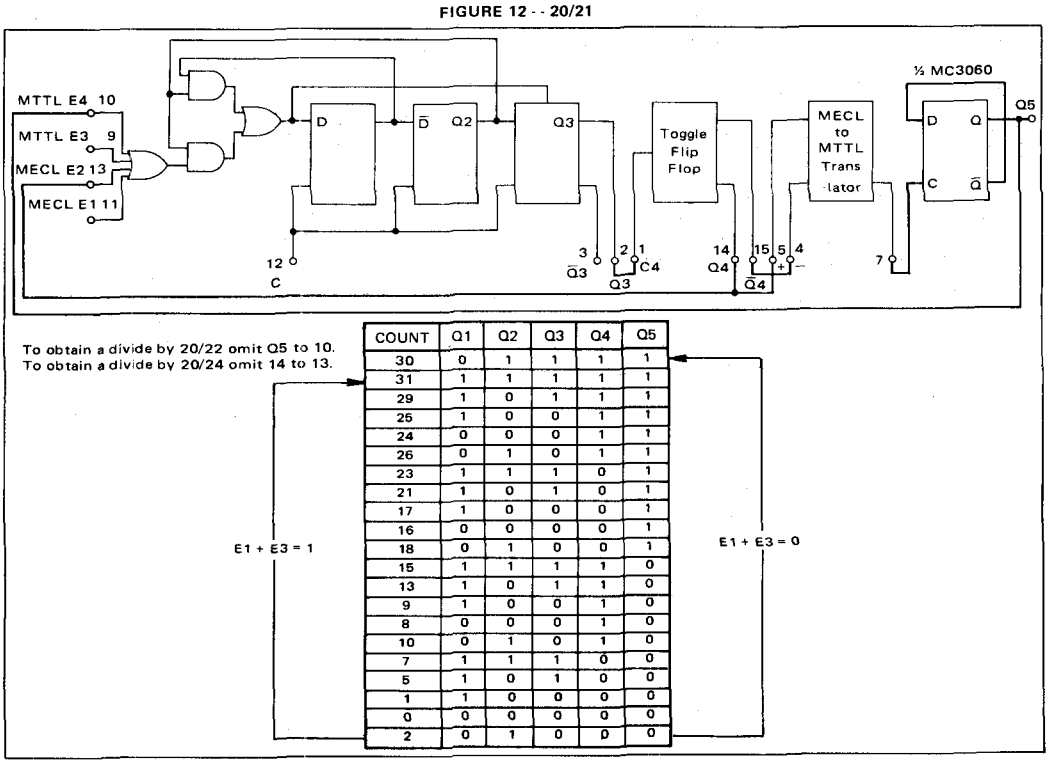
6

FIGURE 11 – – – 10/12



COUNT	Q1	Q2	Q3	Q4
14	0	1	1	1
15	1	1	1	1
13	1	0	1	1
9	1	0	0	1
8	0	0	0	1
10	0	1	0	1
6	0	1	1	0
7	1	1	1	0
5	1	0	1	0
1	1	0	0	0
0	0	0	0	0
2	0	1	0	0

FIGURE 12 - - 20/21



COUNT	Q1	Q2	Q3	Q4	Q5
30	0	1	1	1	1
31	1	1	1	1	1
29	1	0	1	1	1
25	1	0	0	1	1
24	0	0	0	1	1
26	0	1	0	1	1
23	1	1	1	0	1
21	1	0	1	0	1
17	1	0	0	0	1
16	0	0	0	0	1
18	0	1	0	0	1
15	1	1	1	1	0
13	1	0	1	1	0
9	1	0	0	1	0
8	0	0	0	1	0
10	0	1	0	1	0
7	1	1	1	0	0
5	1	0	1	0	0
1	1	0	0	0	0
0	0	0	0	0	0
2	0	1	0	0	0

FUNCTION DESCRIPTION

INTRODUCTION

The MC12012 is one part of a variable modulus (divisor) prescaling subsystem used in certain Digital Phase-Locked Loops (PLL).

More often than not, the feedback loop of any PLL contains a counter-divider. Many methods are available for building a divider, but not all are simple, economical, or convenient in a particular application.

The technique and system described here offer a new approach to the construction of a phase-locked loop divider. In addition to using the MC12012 variable modulus prescaler, this system requires an MC12014 Counter Control Logic function, together with suitable programmable counters (e.g. MC4016s). Data sheets for these additional devices should be consulted for their particular functional descriptions.

THE MC12012 TWO MODULUS PRESCALER

Three functional blocks are contained in the MC12012 variable modulus prescaler: 1) a controllable ÷5/÷6 prescaler; 2) a ÷ 2 prescaler; and 3) an ECL to TTL translator (for single power supply operation).

Selection of division by 5 or by 6 is made by inputs to E1 through E4. If all E inputs are low before the transition of the clock pulse driving Q3 high, Q3 will stay high for 3 clock pulses, then will go low for 3 clock pulses. This provides a divide by 6 function.

On the other hand, if any one or all of the E inputs are high prior to the positive transition of the clock pulse driving Q3 high, Q3 will stay high for only 2 clock pulses, then will go low for 3 clock pulses. The result is division by 5.

For the ÷5 operation, at least one of the E inputs must go high sometime before the clock pulse. This time is referred to as the "setup time." Specifications for setup time are given in the electrical characteristics table: t_{setup1} and t_{setup2} for E1 and E2 (MECL inputs), and E3 and E4 (MTTL inputs).

For the divide by 6 operation all E inputs must be low for some time prior to the clock pulse. This time is referred to as the "release time." Data for release time is given in the electrical characteristics table; t_{re1} and t_{re2} for E1, E2, E3, E4.

The data given in the tables for setup and release times are referenced to the positive transition of the clock pulse causing Q3 to go high. If it is necessary to reference the setup and release times to the positive transition of Q3, add t++ (specified for Q3) to the setup/release times given. It should be noted that the logic states for the enable inputs are important only for only one clock pulse which causes Q3 to go high (within the limits specified by setup and release times).

The ÷ 5/÷ 6 prescaler may be connected externally to the ÷ 2 prescaler to form a ÷ 10/÷ 11 prescaler (Figure 10) or a ÷ 10/÷ 12 prescaler (Figure 11).

By way of an example showing how a ÷ 10/÷ 11 prescaler operates, note that if E1, E3, and E4 (Figure 10) are held in a low state, the counter divides by 11. To do this, a feedback connection is established from Q4 to E2 (or to E1). With this feedback, the ÷ 5/÷ 6 prescaler divides by 5 when Q4 is high, and by 6 when Q4 is low.

Since Q4 changes state with each positive transition of Q3, the prescaler alternates between ÷ 5 and ÷ 6 resulting in a ÷ 11 at Q4.

If any one or all of the E inputs are high (Figure 10), the 5/6 prescaler always divides by 5 and a divide by 10 results at Q4.

With the addition of external flip-flops and counters (MECL or MTTL) various other modulus prescalers may be produced (20/21, 20/22, 20/24, 40/41, 50/51, 100/101, etc.).

THE TECHNIQUE OF DIRECT PROGRAMMING BY UTILIZING A TWO MODULUS PRESCALER (MC12012)

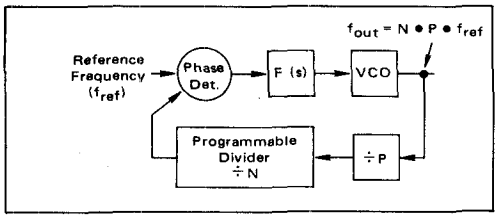
The disadvantage of using a fixed modulus (÷ P) for frequency division in high frequency phase-locked loops (PLL) is that it requires dividing the desired reference frequency by P also (desired reference frequency equals channel spacing.)

The MC12012 is specially designed for use with a technique called "variable modulus prescaling". This technique allows a simple MECL two-modulus prescaler (MC12012) to be controlled by a relatively slow MTTL programmable counter. The use of this technique permits direct high-frequency prescaling without any sacrifice in resolution since it is no longer necessary to divide the reference frequency by the modulus of the high frequency prescaler.

The theory of "variable modulus prescaling" may be explained by considering the system shown in Figure 13. For the loop shown:

$$f_{out} = N \bullet P \bullet f_{ref} \quad (1)$$

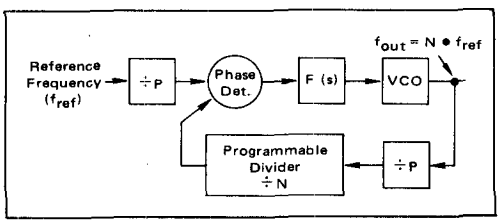
FIGURE 13 – FREQUENCY SYNTHESIS BY PRESCALING



where P is fixed and N is variable. For a change of 1 in N, the output frequency changes by $P \bullet f_{ref}$. If f_{ref} equals the desired channel spacing, then only every P channel may be programmed using this method. A problem remains: how to program intermediate channels.

One solution to this problem is shown in Figure 14.

FIGURE 14 – FREQUENCY SYNTHESIS BY PRESCALING



A ÷ P is placed in series with the desired channel spacing (frequency) to give a new reference frequency: channel spacing/P.

Another solution is found by considering the defining equation (1) for f_{out} of Figure 13. From the equation it may be seen that only every P channel can be programmed simply, because N is always an integer. To obtain intermediate channels, P must be multiplied by an integer plus a fraction. This fraction would be of the form: A/P. If N is defined to be an integer number, Np, plus a fraction, A/P, N may be expressed as:

$$N = Np + A/P.$$

Substituting this expression for N in equation 1 gives:

$$f_{out} = (Np + A/P) \bullet P \bullet f_{ref} \quad (2)$$

or:

$$f_{out} = (Np\ P + A) \bullet f_{ref} \quad (3)$$

$$f_{out} = Np \bullet P \bullet f_{ref} + A \bullet f_{ref}. \quad (4)$$

Equation 4 shows that all channels can be obtained directly if N can take on fractional values. Since it is difficult to multiply by a fractional number, equation 4 must be synthesized by some other means.

Taking equation 3 and adding ±AP to the coefficient of f_{ref}, the equation becomes:

$$f_{out} = (Np \bullet P + A + A \bullet P - A \bullet P)\ f_{ref}. \quad (5)$$

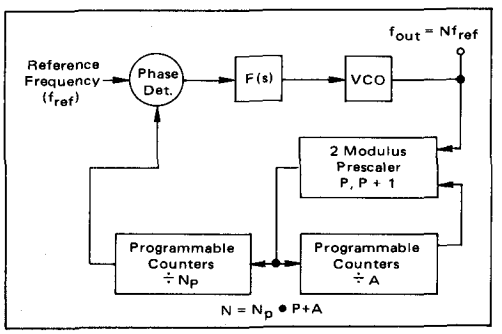
Collecting terms and factoring gives:

$$f_{out} = [(Np - A)\ P + A\ (P + 1)]\ f_{ref} \quad (6)$$

From equation 6 it becomes apparent that the fractional part of N can be synthesized by using a two-modulus counter (P and P + 1) and dividing by the upper modulus, A times, and the lower modulus (Np - A) times.

This equation (6) suggests the circuit configuration in Figure 15. The A counter shown must be the type that

FIGURE 15 – FREQUENCY SYNTHESIS BY TWO MODULUS PRESCALING



counts from the programmed state (A) to the enable state, and remains in this state until divide by Np is completed in the programmable counter.

In operation, the prescaler divides by P + 1, A times. For every P + 1 pulse into the prescaler, both the A counter and Np counter are decremented by 1. The prescaler divides by P + 1 until the A counter reaches the zero state. At the end of (P + 1) • A pulses, the state of the Np counter equals (Np - A). The modulus of the prescaler then changes to P. The variable modulus counter divides by P until the remaining count, (Np - A) in the Np counter, is decremented to zero. Finally, when this is completed, the A and Np counters are reset and the cycle repeats.

To further understand this prescaling technique, consider the case with P = 10. Equation 6 becomes:

$$f_{out} = (A + 10\ Np) \bullet f_{ref} \quad (7)$$

If Np consists of 2 decades of counters then:

$$Np = 10\ Np_1 + Np_0$$

(Np_1 is the most significant digit),

and equation 7 becomes:

FIGURE 16 – DIRECT PROGRAMMING UTILIZING TWO-MODULUS PRESCALER

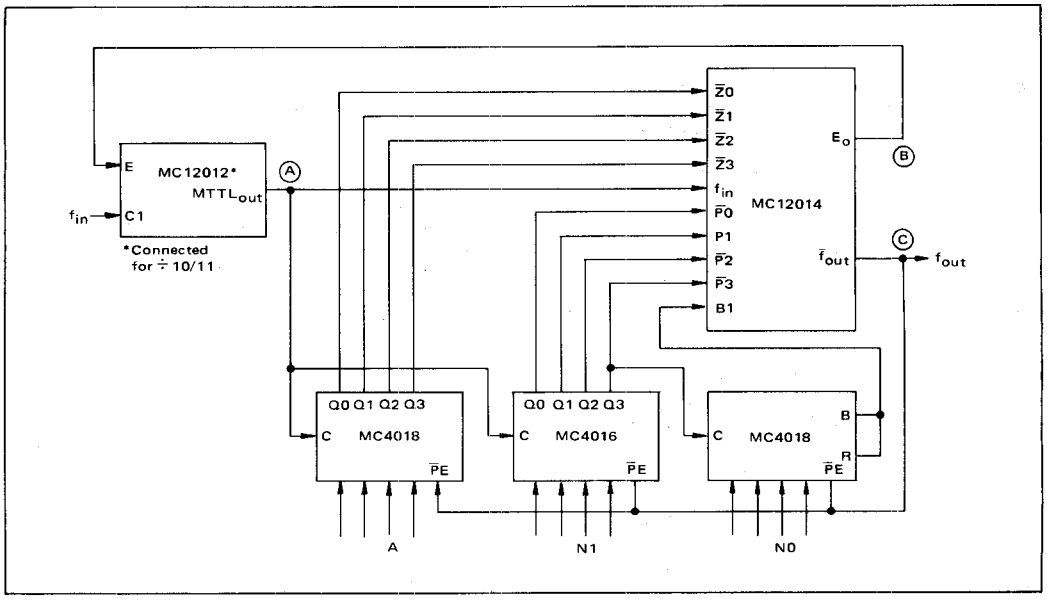


FIGURE 17 – WAVEFORMS FOR DIVIDE BY 43

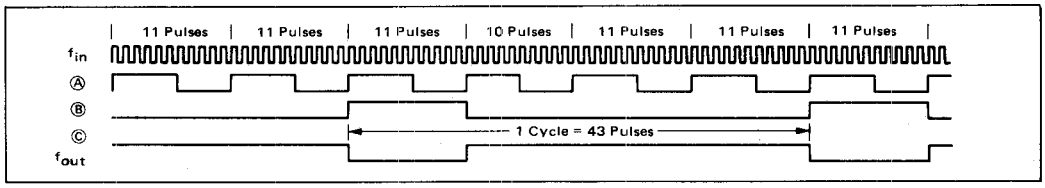


FIGURE 18 – WAVEFORMS FOR DIVIDE BY 42

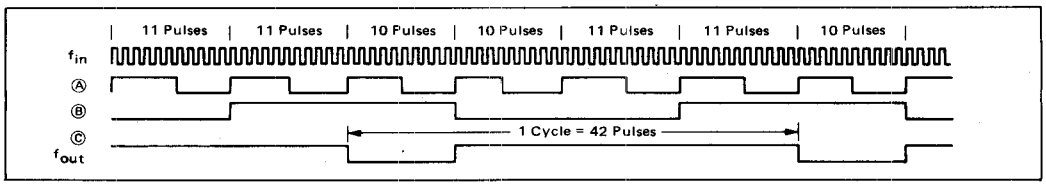
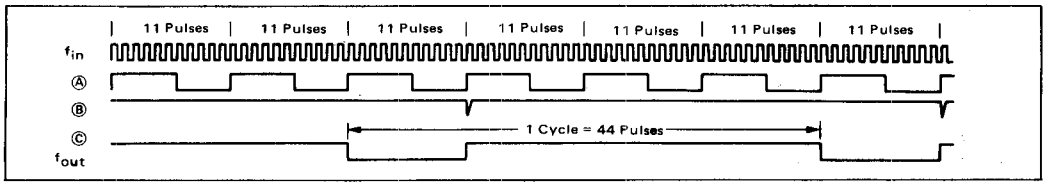


FIGURE 19 – WAVEFORMS FOR DIVIDE BY 44



6

$$f_{out} = (100\,N_{P1} + 10\,N_{P0} + A)\,f_{ref}.$$

To do variable modulus prescaling using the MC12012 and programmable divide by N counters (MC4016, MC4018, one additional part is required: the MC12014 (Counter Control Logic).

In variable modulus prescaling the MC12014 serves a dual purpose: it detects the terminal (zero) count of the A counter, to switch the modulus of the MC12012; and it extends the maximum operating frequency of the programmable counters to above 25 MHz. (See the MC12014 data sheet for a detailed description of the Counter Control Logic).

Figure 16 shows the method of interconnecting the MC12012, MC12014, and MC4016 (or MC4018) for variable modulus prescaling. To understand the operation of the circuit shown in Figure 16, consider division by 43. Division by 43 is done by programming $N_{P1} = 0$, $N_{P0} = 4$, and $A = 3$.

Waveforms for various points in the circuit are shown in Figure 17 for this division. From the waveforms it may be seen that the two-modulus prescaler starts in the divide by 11 mode, and the first input pulse causes point A to go high. This positive transition decrements the Np counter to 3, and counter A to 2.

After 11 pulses, point Ⓐ again goes high; the Np counter decrements to 2 and the A counter to 1. The "2" contained in the Np counter enables the inputs to the frequency extender portion of the MC12014. After 11 more pulses point Ⓐ goes high again.

With this position transition at Ⓐ, the output (f_{out}) of the MC12014 goes low, the Np counter goes to 1, and the A counter goes to 0. The zero state of the A counter is detected by the MC12014, causing point Ⓑ to go to 1 and changing the modulus of the MC12012 to 10 at the start of the cycle.

When f_{out} goes low, the programmable counters are reset to the programmed number. After 11 pulses (the enable went high after the start of the cycle and therefore doesn't change the modulus until the next cycle), point Ⓐ makes another positive transition. This positive transition causes f_{out} to return high, release the preset on the counter, and generates a pulse to clear the latch (return point Ⓑ to 0).

After 10 pulses the cycle begins again (point Ⓑ was high prior to point Ⓐ going high). The number of input pulses that have occured during this entire operation is: 11 + 11 + 11 + 10 = 43. Figures 18 and 19 show the waveforms for divide by 42 and divide by 44 respectively.

The variable modulus prescaling technique may be used in any application as long as the number in the Np counter is greater than or equal to the number in the A counter. Failure to observe this rule will result in erroneous results. (For example, for the system shown in Figure 16 if the number 45 is programmed, the circuit actually will divide by 44. This is not a serious restriction since Np is greater than A in most applications).

It is important to note that the A counter has been composed of only one counter for discussion only; where required, the A counter may be made as large as needed by cascading several programmable counters. Figure 20 shows the method of interconnecting counters. Operation is previously described. The number of stages in the A counter should not exceed the number of stages for the

FIGURE 20 – METHOD OF INTERCONNECTING COUNTERS

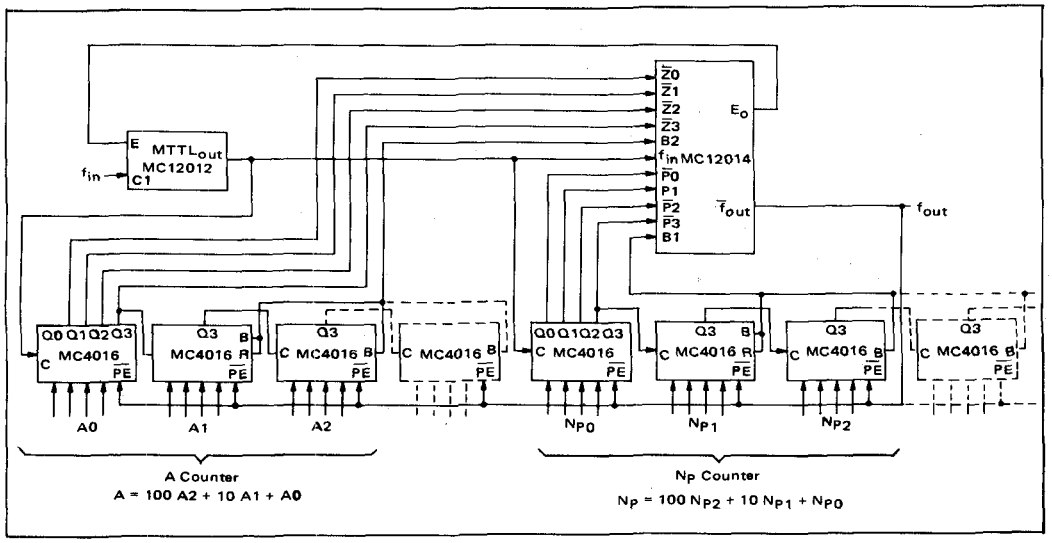


FIGURE 21 – DIRECT PROGRAMMING 100-200 MHz SYNTHESIZER IN 50 kHz STEPS

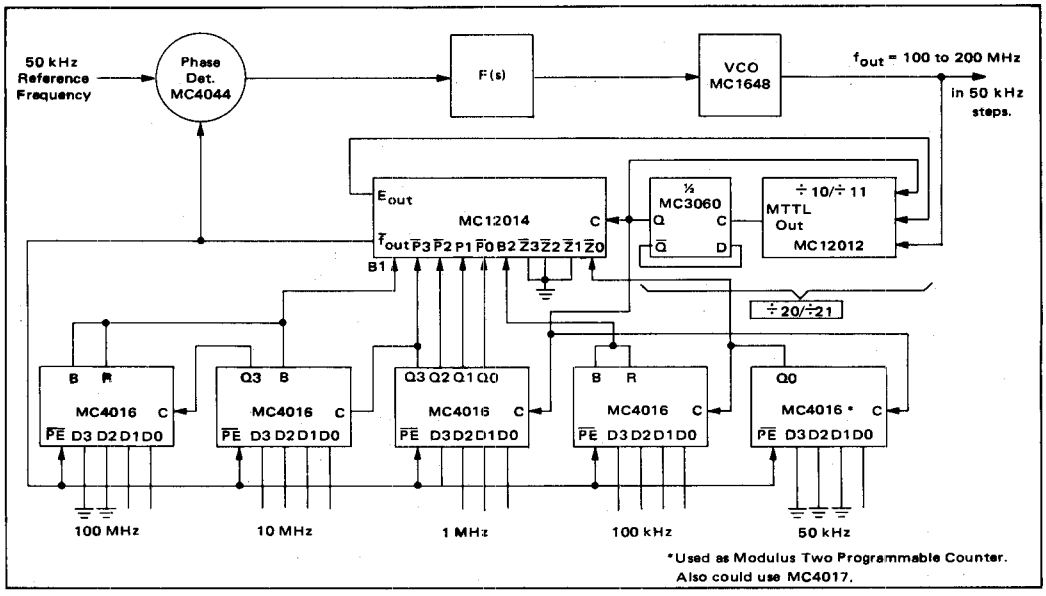
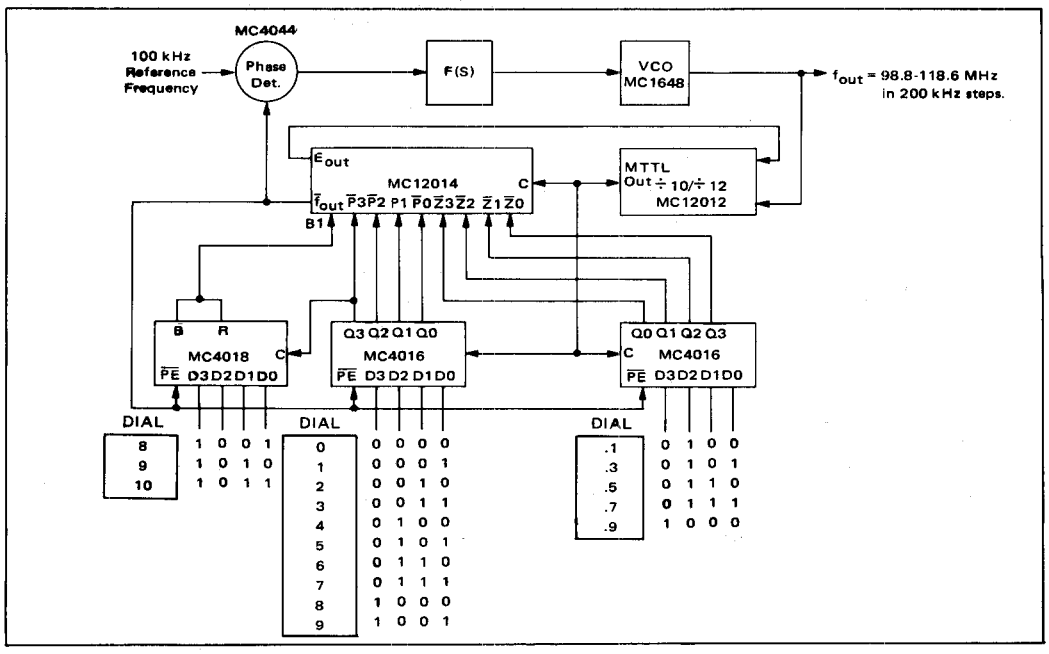


FIGURE 22 – FM BAND SYNTHESIZER WITH 10.7 MHz I.F. OFFSET



Np counters. As many counters as desired may be cascaded, as long as fan-in and fan-out rules for each part are observed.

The theory of "variable modulus prescaling" developed above, examined a case in which the upper modulus of the two-modulus prescaler was 1 greater than the lower modulus. However, the technique described is by no means limited to this one special case. There are applications in which it is desirable to use moduli other than P/(P + 1).

It can be shown that for a general case in which the moduli of the two-modulus prescaler are P and P + M, equation 6 becomes:

$$f_{out} = [(Np - A)\,P + A\,(P + M)] \bullet f_{ref}$$

or

$$f_{out} = [Np \bullet P + M \bullet A] \bullet f_{ref}. \qquad (8)$$

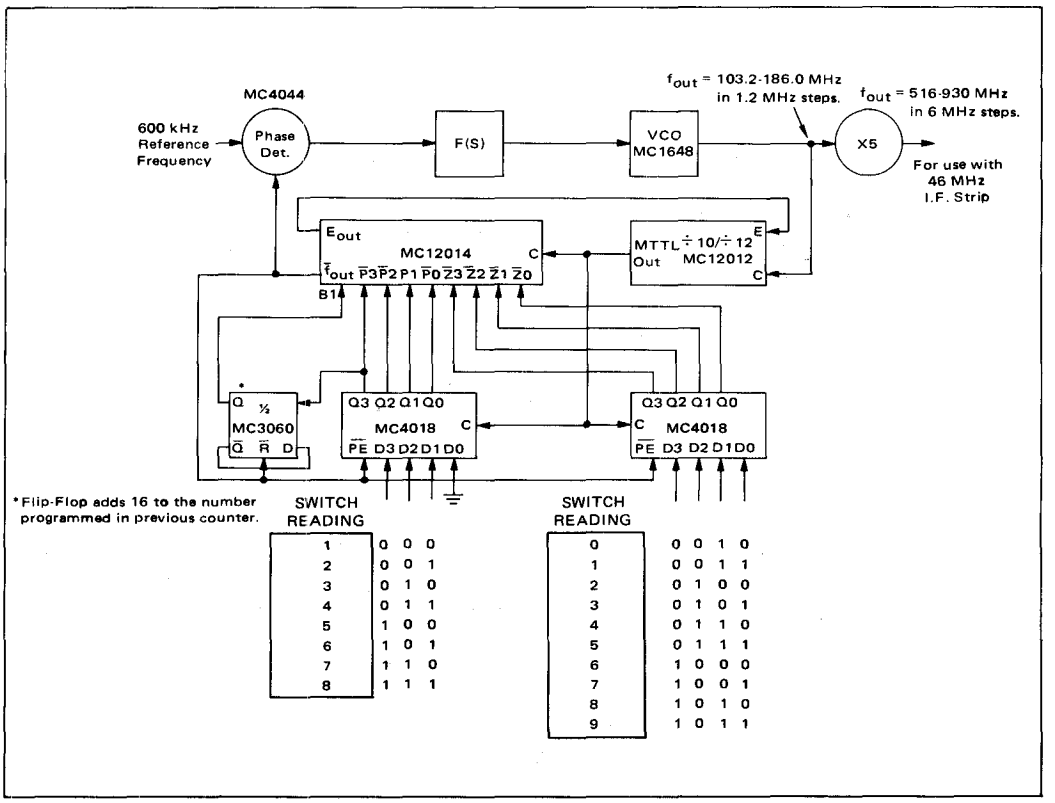
From equation 8 it may be seen that the upper modulus of the two-modulus prescaler has no effect on the Np counter, and that the number programmed in the A counter is simply multiplied by M.

APPLICATIONS

There is no one procedure which will always yield the best counter configuration for all possible MC12012 applications. Each designer will develop his own special design for the counter portion of his PLL system.

An insight into some of the various possible counter schemes may be obtained by considering the various PLL systems shown in Figures 21, 22, and 23. These examples were chosen to show some of the moduli that may be obtained by using the MC12012.

FIGURE 23 – UHF SYNTHESIZER USING 10/12 COUNTER



SWITCH READING				
1	0	0	0	
2	0	0	1	
3	0	1	0	
4	0	1	1	
5	1	0	0	
6	1	0	1	
7	1	1	0	
8	1	1	1	

SWITCH READING				
0	0	0	1	0
1	0	0	1	1
2	0	1	0	0
3	0	1	0	1
4	0	1	1	0
5	0	1	1	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1