



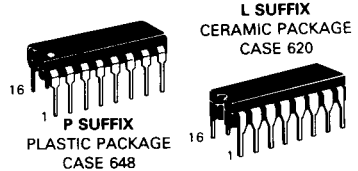
# MC12060 MC12061

## CRYSTAL OSCILLATOR

The MC12060 and MC12061 are for use with an external crystal to form a crystal controlled oscillator. In addition to the fundamental series mode crystal, two bypass capacitors are required (plus usual power supply pin bypass capacitors). Translators are provided internally for MECL and TTL outputs.

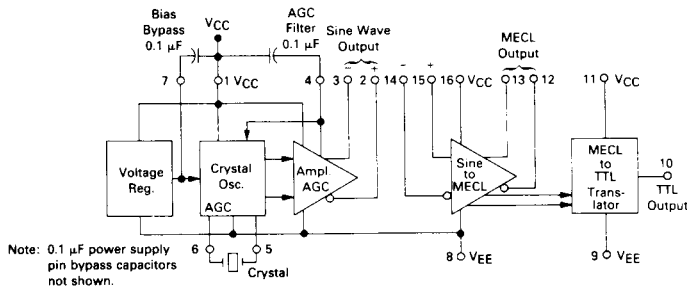
- Frequency Range = 100 kHz to 2.0 MHz for MC12060  
2.0 MHz to 20 MHz for MC12061
- Temperature Range = 0°C to +70°C for MC12060/061
- Single Supply Operation: +5.0 Vdc or -5.2 Vdc
- Three Outputs Available:
  1. Complementary Sine Wave (600 mVp-p typ)
  2. Complementary MECL
  3. Single Ended TTL

## CRYSTAL OSCILLATOR

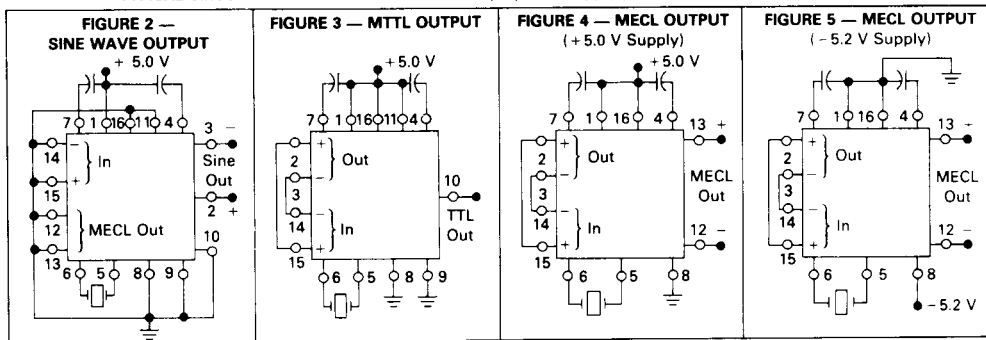


MC12060/MC12061 ONLY

FIGURE 1—BLOCK DIAGRAM



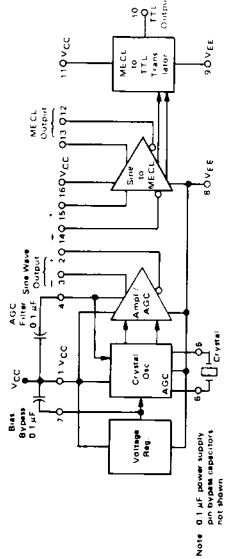
TYPICAL CIRCUIT CONFIGURATIONS Note: 0.1  $\mu$ F power supply pin bypass capacitors not shown.



### CRYSTAL REQUIREMENTS

Note: Start-up stabilization time is a function of crystal series resistance. The lower the resistance, the faster the circuit stabilizes.

Characteristic	MC12060	MC12061
Mode of Operation	Fundamental Series Resonance	
Frequency Range	100 kHz - 2.0 MHz	2.0 MHz - 20 MHz
Series Resistance, R1	Minimum at Fundamental	
Maximum Effective Resistance $R_{E(max)}$	4k ohms	155 ohms



**TEST VOLTAGE/CURRENT VALUES**

Volts										mA		
V <sub>IHmax</sub>	V <sub>IHmin</sub>	V <sub>IAmix</sub>	V <sub>IHT</sub>	V <sub>CC1</sub>	V <sub>CC</sub>	V <sub>CC2</sub>	V <sub>CC3</sub>	V <sub>CC4</sub>	V <sub>CC5</sub>	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>L</sub>
4.16	3.19	3.86	3.51	4.0	4.75	5.0	5.25	16	-0.4	-2.5		
4.19	3.21	3.9	3.52	4.0	4.75	5.0	5.25	16	-0.4	-2.5		
4.28	3.23	3.96	3.55	4.0	4.75	5.0	5.25	16	-0.4	-2.5		

**TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW**

Characteristic	Symbol	Pin Under Test	0°C			+25°C			+75°C			Unit	Gnd
			Min	Max	Typ	Min	Max	Min	Max				
Power Supply Drain Current MC12060 MC12061	I <sub>CC</sub>	1	—	—	13	16	19	—	—	—	—	mAdc	8
		11	—	—	18	23	28	—	—	—	—	—	8
		16	—	—	13	16	19	—	—	—	—	—	8,9
Input Current	I <sub>INH</sub>	14	—	—	—	—	250	—	—	—	—	µAdc	8
		15	—	—	—	—	250	—	—	—	—	µAdc	8
		14	—	—	—	—	1.0	—	—	—	—	µAdc	8,14
Differential Offset Voltage MC12061 MC12060	ΔV	4 to 7 2 to 3	—	—	40	—	325	—	—	—	—	mVdc	8
		2 to 3	—	—	-200	0	+200	—	—	—	—	—	—
		2 to 3	—	—	-300	—	+300	—	—	—	—	—	—
Output Voltage Level	V <sub>out</sub>	2	—	—	—	3.5	—	—	—	—	—	Vdc	8
		3	—	—	—	3.5	—	—	—	—	—	Vdc	8
		12	4.0	4.16	4.04	—	4.19	4.1	4.28	Vdc	12	8	
Logic "1" Output Voltage	V <sub>OH1*</sub>	13	4.0	4.16	4.04	—	4.19	4.1	4.28	Vdc	13	8	
		10	2.4	—	2.4	—	—	2.4	—	Vdc	10	8,9	
		12	2.98	3.43	3.0	—	3.44	3.02	3.47	Vdc	12	8	
Logic "0" Output Voltage	V <sub>OL1*</sub>	13	2.98	3.43	3.0	—	3.44	3.02	3.47	Vdc	13	8	
		10	—	—	—	—	—	—	—	Vdc	10	8,9	
		12	—	—	—	—	—	—	—	Vdc	12	8	
Logic "1" Threshold Voltage	V <sub>OHA</sub>	13	3.98	—	4.02	—	—	—	—	Vdc	13	8	
		10	—	—	—	—	—	—	—	Vdc	10	8,9	
		12	—	—	—	—	—	—	—	Vdc	12	8	
Logic "0" Threshold Voltage	V <sub>OLA</sub>	13	—	—	—	—	—	—	—	Vdc	13	8	
		10	—	—	—	—	—	—	—	Vdc	10	8,9	
		12	—	—	—	—	—	—	—	Vdc	12	8	
Output Short-Circuit Current	I <sub>OS</sub>	10	20	60	20	—	60	20	—	mAdc	—	—	
		13	—	—	—	—	—	—	—	mAdc	—	—	
		12	—	—	—	—	—	—	—	mAdc	—	—	

**ELECTRICAL CHARACTERISTICS**

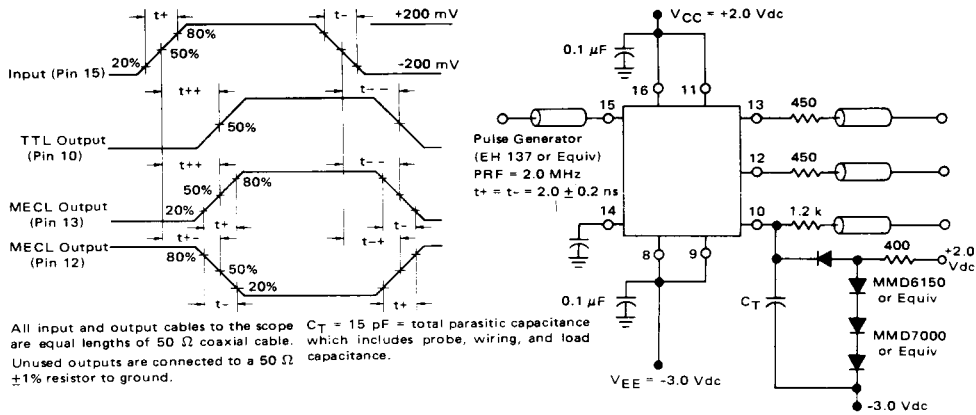
**TEST VOLTAGE/CURRENT VALUES**

Volts										mA		
V <sub>IHmax</sub>	V <sub>IHmin</sub>	V <sub>IAmix</sub>	V <sub>IHT</sub>	V <sub>CC1</sub>	V <sub>CC</sub>	V <sub>CC2</sub>	V <sub>CC3</sub>	V <sub>CC4</sub>	V <sub>CC5</sub>	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>L</sub>
4.16	3.19	3.86	3.51	4.0	4.75	5.0	5.25	16	-0.4	-2.5		
4.19	3.21	3.9	3.52	4.0	4.75	5.0	5.25	16	-0.4	-2.5		
4.28	3.23	3.96	3.55	4.0	4.75	5.0	5.25	16	-0.4	-2.5		

\*Devices will meet standard MECL logic levels using V<sub>EE</sub> = -5.2 Vdc and V<sub>CC</sub> = 0.

MC12060 • MC12061

FIGURE 6 — AC CHARACTERISTICS — MECL AND TTL OUTPUTS



Characteristic	Symbol	Pin Under Test	Test Limits				TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW:								
			0°C		+25°C		+75°C		Unit	Pulse In	Pulse Out	+2.0 Vdc	-3.0 Vdc	Gnd	
			Min	Max	Min	Typ	Max	Min							Max
Propagation Delay	$t_{15+10+}$	10	—	22	—	17	25	—	27	ns	15	10	11,16	8,9	14
	$t_{15-10-}$	10	—	19	—	12	18	—	18						
	$t_{15+12-}$	12	—	5.2	—	4.3	5.5	—	5.8						
	$t_{15-12+}$	12	—	5.0	—	3.7	5.2	—	5.2						
	$t_{15+13+}$	13	—	4.8	—	4.0	5.0	—	5.2						
	$t_{15-13-}$	13	—	4.8	—	4.0	5.0	—	5.1						
Rise Time	$t_{12+}$	12	—	4.0	—	3.0	4.0	—	4.4	ns	15	12	11,16	8,9	14
	$t_{13+}$	13	—	4.0	—	3.0	4.0	—	4.4	ns	15	13	11,16	8,9	14
Fall Time	$t_{12-}$	12	—	4.0	—	3.0	4.0	—	4.0	ns	15	12	11,16	8,9	14
	$t_{13-}$	13	—	4.0	—	3.0	4.0	—	4.0	ns	15	13	11,16	8,9	14

Characteristic	Pin Under Test	+25°C		Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW	
		Min	Typ		+2.0 Vdc	-3.0 Vdc
		Sine Wave Amplitude				
MC12060	2	500	650	mVp-p	1	8.9
	3	500	650			
MC12061	2	650	750			
	3	650	750			

FIGURE 7 — AC TEST CIRCUIT — SINE WAVE OUTPUT

All output cables to the scope are equal lengths of 50  $\Omega$  coaxial cable. All unused cables must be terminated with a 50  $\Omega$   $\pm 1\%$  resistor to ground.

450  $\Omega$  resistor and the scope termination impedance constitute a 10:1 attenuator probe.

Crystal — Reeves Hoffman Series Mode,

Series Resistance Minimum at Fundamental

MC12060 MC12061

$f = 500$  kHz  $f = 10$  MHz

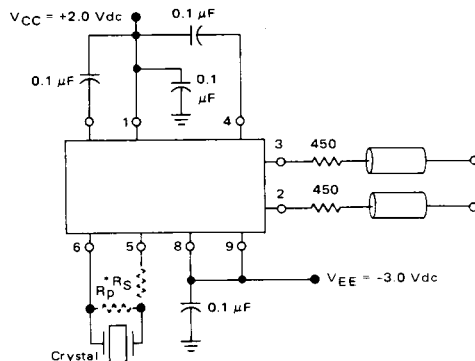
$R_E = 1$  k $\Omega$   $R_E = 5$   $\Omega$

\* $R_S$  MC12060 = 3 k $\Omega$

MC12061 = 15 k $\Omega$  is inserted only for test purposes. When used with the above specified crystal, it guarantees oscillation with any crystal which has an equivalent series resistance

$\leq 155$   $\Omega$  for MC12061 and  $\leq 4$  k $\Omega$  for MC12060

$R_p$ : will improve start up problems value: 200–500  $\Omega$



## OPERATING CHARACTERISTICS

The MC12061 and MC12060 consist of three basic sections: an oscillator with AGC and two translators (Figure 1). Buffered complementary sine wave outputs are available from the oscillator section. The translators convert these sine wave outputs to levels compatible with MECL and/or TTL.

Series mode crystals should be used with the oscillator. If it is necessary or desirable to adjust the crystal frequency, a reactive element can be inserted in series with the crystal — an inductor to lower the frequency or a capacitor to raise it. When such an adjustment is necessary, it is recommended that the crystal be specified slightly lower in frequency and a series trimmer capacitor be added to bring the oscillator back on frequency. As the oscillator frequency is changed from the natural resonance of the crystal, more and more dependence is placed on the external reactance, and temperature drift of the trimming components then affects overall oscillator performance.

The MC12061 and MC12060 are designed to operate from a single supply — either +5.0 Vdc or -5.2 Vdc. Although each translator has separate  $V_{CC}$  and  $V_{EE}$  supply pins, the circuit is NOT designed to operate from both voltage levels at the same time. The separate  $V_{EE}$  pin from the TTL translator helps minimize transient disturbance. If neither translator is being used, all unused pins (9 thru 16) should be connected to  $V_{EE}$  (pin 8). With the translators not powered, supply current drain is typically reduced from 42 mA to 23 mA for the MC12061, and 35 mA to 16 mA for the MC12060.

## Frequency Stability

Output frequency of different oscillator circuits (of a given device type number) will vary somewhat when used with a given test setup, however the variation should be within approximately  $\pm 0.001\%$  from unit to unit.

Frequency variations with temperature (independent of the crystal, which is held at 25°C) are small — about  $-0.08$  ppm/°C for MC12061 operating at 8.0 MHz, and about  $-0.16$  ppm/°C for MC12060 operating at 1.0 MHz (see Figure 8).

## Signal Characteristics

The sine wave outputs at either pin 2 or pin 3 will typically range from 800 mVp-p (no load) to 500 mVp-p (120 ohm ac load). Approximately 500 mVp-p can be provided across 50 ohms by slightly increasing the dc current in the output buffer by the addition of an external resistor (680 ohms) from pin 2 or 3 to ground, as shown in Figure 9. Frequency drift is typically less than 0.0003% when going from a high-impedance load (1 megohm, 15 pF) to the 50 ohm load of Figure 9. The dc voltage level at pin 2 or 3 is nominally 3.5 Vdc with  $V_{CC} = +5.0$  Vdc.

Harmonic distortion content in the sine wave outputs is crystal as well as circuit dependent. The largest harmonic (third) will usually be at least 15 dB down from the fundamental. The harmonic content is approxi-

mately load independent except that the higher harmonic levels (greater than the fifth) are increased when the MECL translator is being driven.

Typically, the MECL outputs (pins 12 and 13) will drive up to five gates, as defined in Figure 10, and the TTL output (pin 10) will drive up to ten gates, as defined in Figure 11.

## Noise Characteristics

Noise level evaluation of the sine wave outputs using the circuit of Figure 12, with operation at 1.0 MHz for MC12060 or 9.0 MHz for MC12061, indicates the following characteristics:

- Noise floor (200 kHz from oscillator center frequency) is approximately  $-122$  dB when referenced to a 1.0 Hz bandwidth. Noise floor is not sensitive to load conditions and/or translator operation.
- Close-in noise (100 Hz from oscillator center frequency) is approximately  $-88$  dB when referenced to a 1.0 Hz bandwidth.

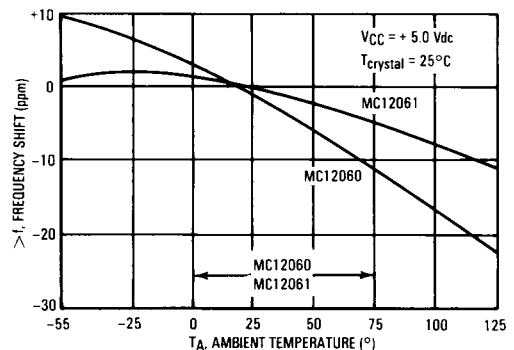


FIGURE 9 — DRIVING LOW-IMPEDANCE LOADS

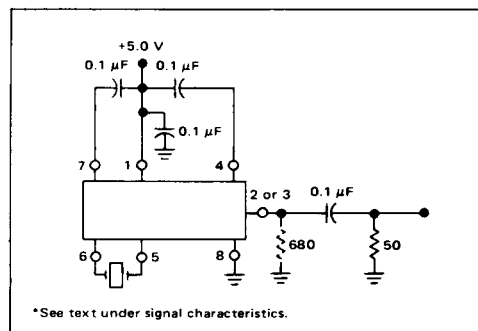


FIGURE 10 — MECL TRANSLATOR LOAD CAPABILITY

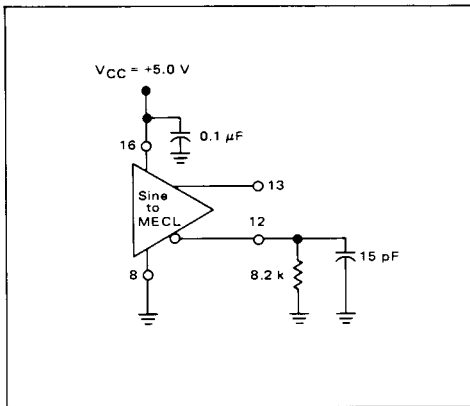


FIGURE 11 — TTL TRANSLATOR LOAD CAPABILITY

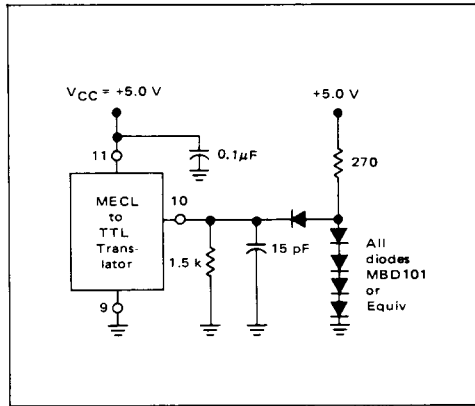
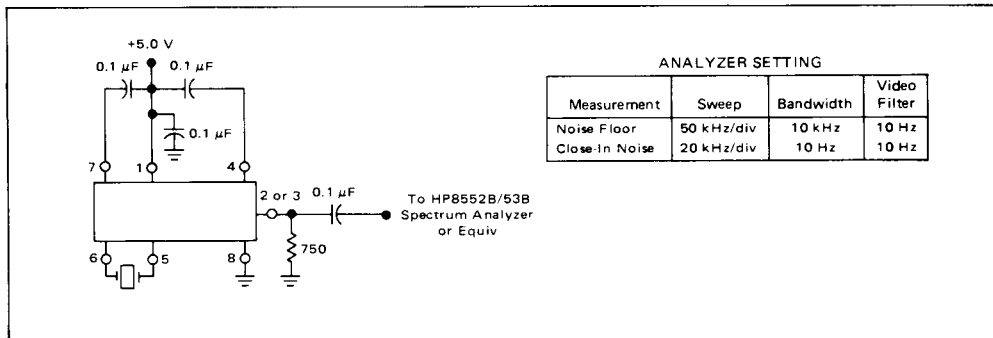
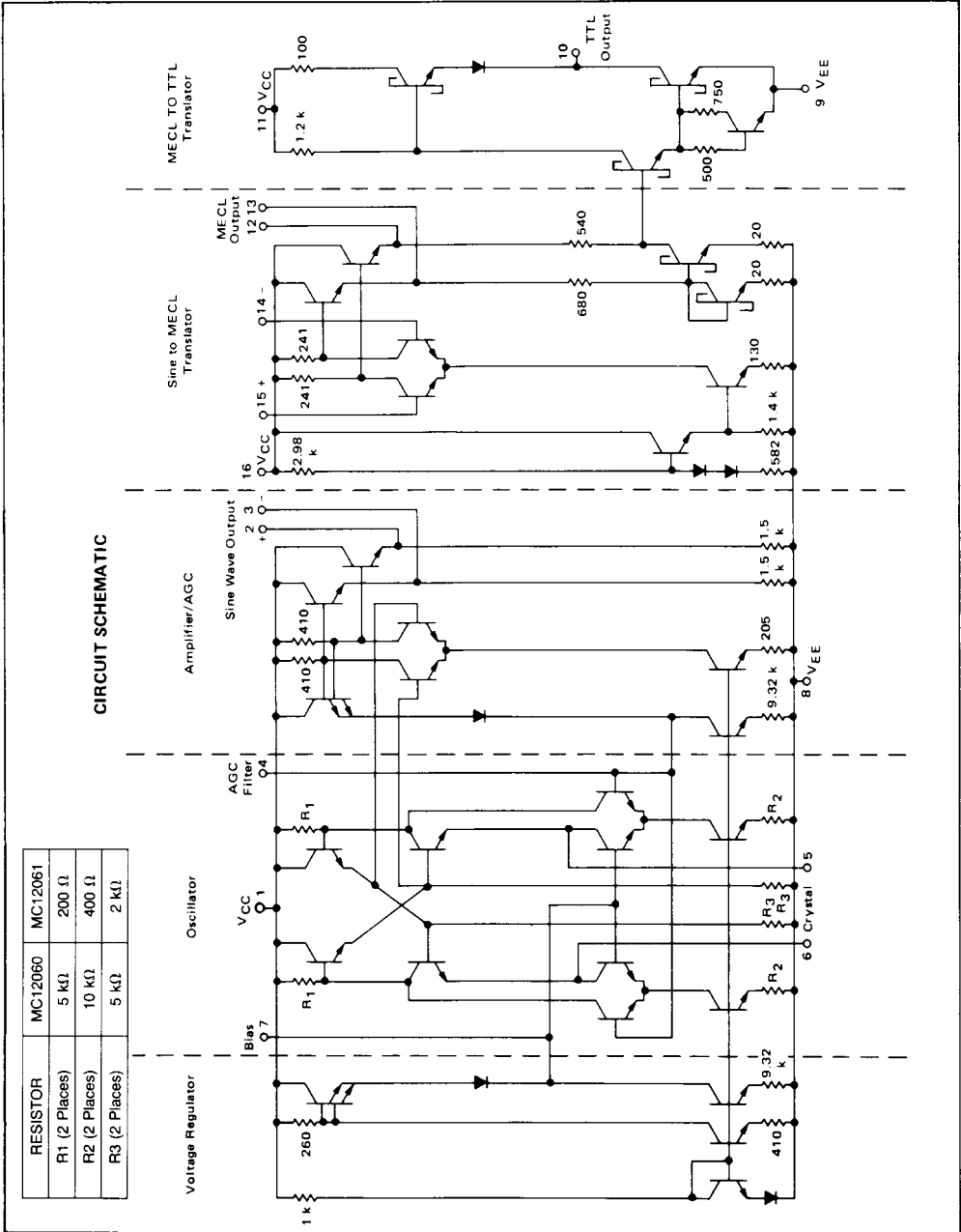


FIGURE 12 — NOISE MEASUREMENT TEST CIRCUIT



MC12060 • MC12061

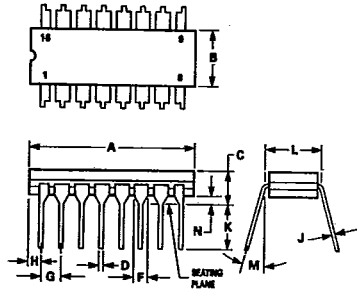


# PACKAGE OUTLINE DIMENSIONS

www.DataSheet4U.com

A letter suffix to the MECL logic function part number is used to specify the package style (see drawings below). See appropriate selector guide for specific packaging available for a given device type.

## L SUFFIX CERAMIC PACKAGE CASE 620-09

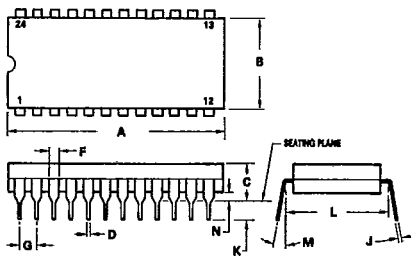


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.08	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC			
H	0.81	1.14	0.030	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.08	0.125	0.160
L	7.37	7.87	0.290	0.310
M	— 15° — 15°			
N	0.81	1.02	0.030	0.040

- NOTES:
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  - PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
  - DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

## L SUFFIX CERAMIC PACKAGE CASE 623-05

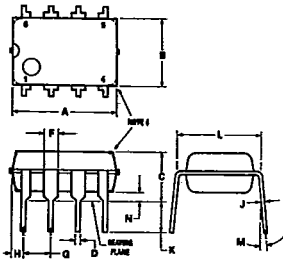
(LW SUFFIX  
FOR  
MC10H181  
ONLY)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.08	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.77	1.52	0.069	0.060
G	2.54 BSC			
J	0.20	0.30	0.008	0.012
K	3.18	4.08	0.125	0.160
L	15.24	BSC	0.600	BSC
M	0° 15° 0° 15°			
N	0.81	1.27	0.030	0.050

- NOTES:
- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  - LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

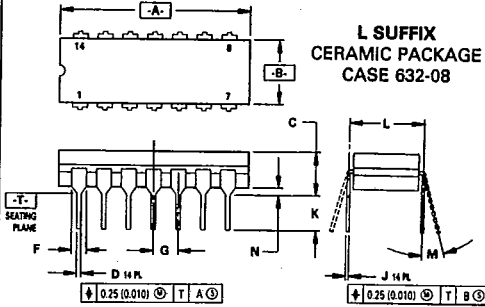
## P SUFFIX PLASTIC PACKAGE CASE 626-04



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC			
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC			
M	— 10° — 10°			
N	0.81	0.76	0.030	0.030

- NOTES:
- LEAD POSITIONAL TOLERANCE:  
 $\pm 0.13 (0.005) \text{ (M)} \text{ T A } \text{ (M)} \text{ B } \text{ (M)}$
  - DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  - PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
  - DIMENSIONS A AND B ARE DATUMS.
  - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

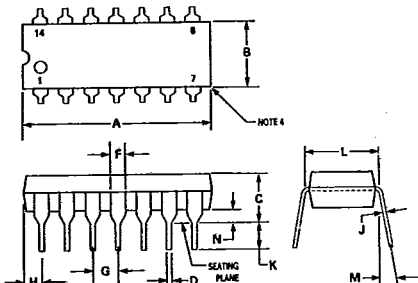
## L SUFFIX CERAMIC PACKAGE CASE 632-08



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.22	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.38	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC			
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC			
M	0° 15° 0° 15° 15° 15°			
N	0.81	1.01	0.030	0.040

- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH.
  - DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  - DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

### P SUFFIX PLASTIC PACKAGE CASE 646-06

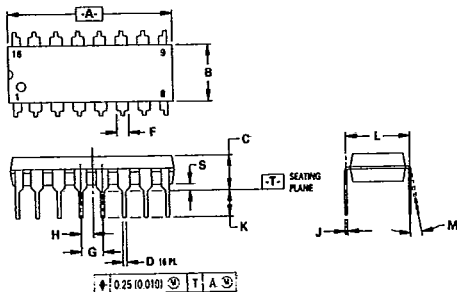


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

## NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

### P SUFFIX PLASTIC PACKAGE CASE 648-08



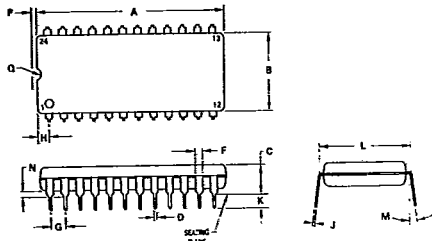
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC	0.050 BSC		
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

## NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

### P SUFFIX PLASTIC PACKAGE CASE 649-03

### (PW SUFFIX FOR MC10H181 ONLY)

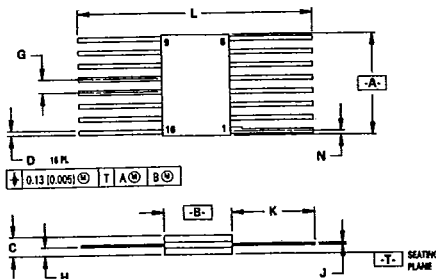


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.32	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.85	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

## NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

### F SUFFIX CERAMIC PACKAGE CASE 650-05



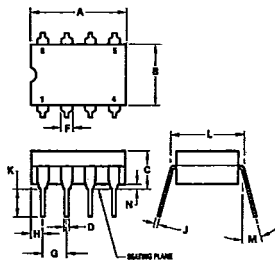
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	9.90	0.370	0.390
B	6.23	6.60	0.245	0.260
C	1.53	2.15	0.060	0.085
D	0.38	0.48	0.014	0.019
G	1.27 BSC		0.050 BSC	
H	0.64	0.01	0.025	0.040
J	0.11	0.17	0.004	0.007
K	6.35	9.39	0.250	0.370
L	18.93	—	0.745	—
N	—	0.50	—	0.020

## NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION "A" AND "B" ALLOW FOR LID MISALIGNMENT, AND GLASS MENISCUS.
- DIMENSION "H" SHALL BE MEASURED AT THE POINT OF EXIT OF THE LEAD FROM THE BODY.
- LEAD NUMBER 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
- FINISH.
- LEAD NUMBERS SHOWN FOR REFERENCE ONLY.



### L SUFFIX CERAMIC PACKAGE CASE 693-02

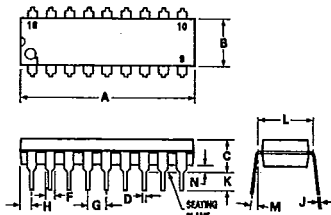


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	— 15°		— 15°	
N	0.51	1.02	0.020	0.040

## NOTES:

- LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

### P SUFFIX PLASTIC PACKAGE CASE 707-02

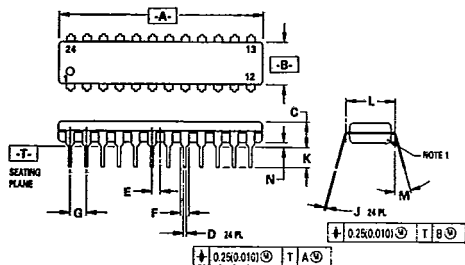


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0° 15°		0° 15°	
N	0.51	1.02	0.020	0.040

## NOTES:

- POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.

### P SUFFIX PLASTIC PACKAGE CASE 724-03

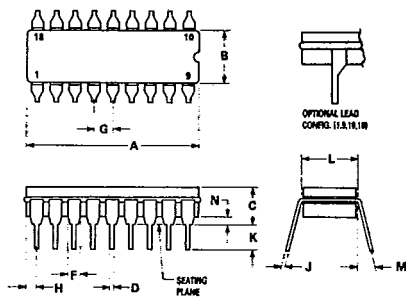


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.86	0.250	0.270
C	3.69	4.64	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0° 15°		0° 15°	
N	0.51	1.01	0.020	0.040

## NOTES:

- CHAMFERED CONTOUR OPTIONAL.
- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.

### L SUFFIX CERAMIC PACKAGE CASE 726-04

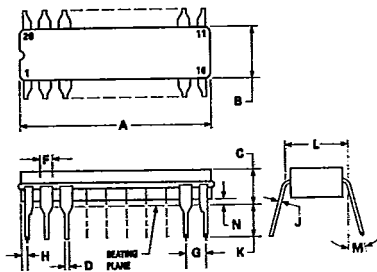


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0° 15°		0° 15°	
N	0.51	1.02	0.020	0.040

## NOTES:

- LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIM "A" & "B" INCLUDES MENISCUS.
- "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

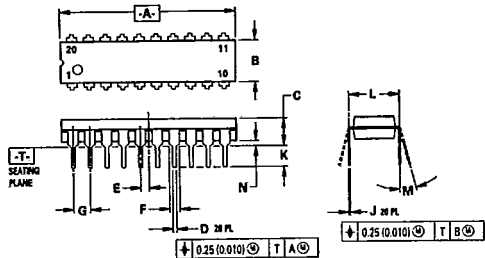
**L SUFFIX  
CERAMIC PACKAGE  
CASE 732-03**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.50	7.49	0.250	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.55	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

- NOTES:
- LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
  - DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  - DIM A AND B INCLUDES MENISCUS.

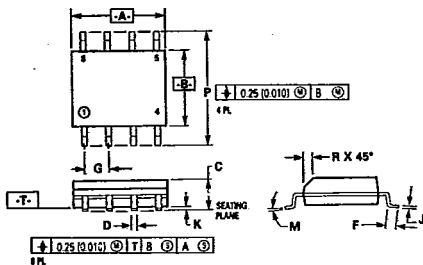
**P SUFFIX  
PLASTIC PACKAGE  
CASE 738-03**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.56	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.89	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.52	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH.
  - DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
  - DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

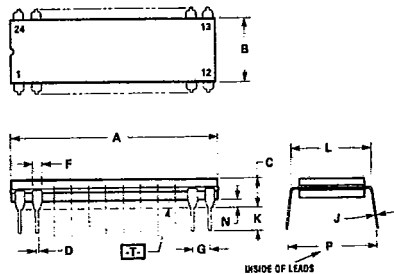
**D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751-03**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.90	4.00	0.152	0.157
C	1.35	1.75	0.054	0.069
D	0.35	0.48	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
H	0.18	0.25	0.007	0.009
J	0.10	0.25	0.004	0.009
K	5.90	6.20	0.232	0.244
M	0°	7°	0°	7°
N	0.25	0.50	0.010	0.019

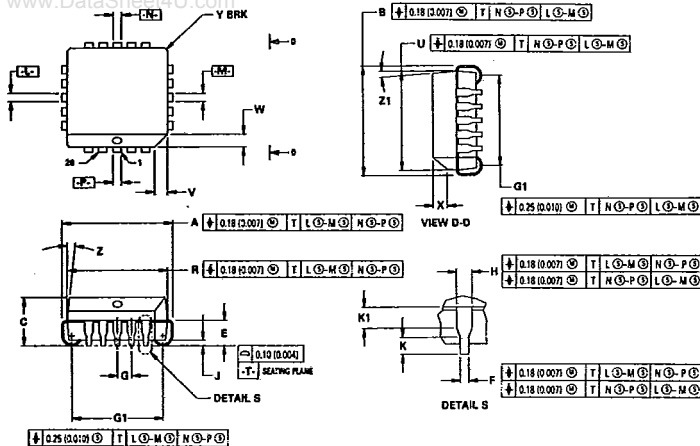
- NOTES:
- DIMENSIONING "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
  - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIM: MILLIMETER.
  - DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION.
  - MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

**L SUFFIX  
CERAMIC PACKAGE  
CASE 758-01**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.64	1.240	1.285
B	7.24	7.75	0.285	0.305
C	3.68	4.44	0.145	0.175
D	0.38	0.53	0.015	0.021
F	1.14	1.57	0.045	0.062
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	7.62	7.87	0.300	0.310
N	0.51	1.27	0.020	0.050
P	9.14	10.16	0.360	0.400

- NOTES:
- DIMENSION A IS DATUM.
  - POSITIONAL TOLERANCE FOR LEADS: 24 PLACES
  - CONTROLLING DIMENSION: INCH.
  - DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  - DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.



**FN SUFFIX  
PLASTIC PACKAGE  
CASE 775-02**

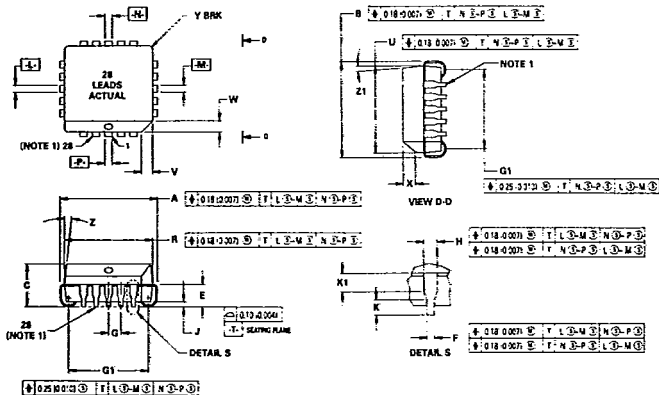
**NOTES:**

1. DATUMS - L, M, N, AND P - DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM - T, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.78	10.03	0.385	0.395
B	9.78	10.03	0.385	0.395
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	8.89	9.04	0.350	0.356
U	8.89	9.04	0.350	0.356
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	7.88	8.38	0.310	0.330
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

**NOTES:**

1. DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.
2. DATUMS - L, M, N, AND P - DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM - T, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.



**FN SUFFIX  
PLASTIC PACKAGE  
CASE 776-02**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	10.12	10.92	0.400	0.430
Z1	2°	10°	2°	10°

# MECL Logic Surface Mount

www.DataSheet4U.com

## WHY SURFACE MOUNT?

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of Insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the State-of-the-Art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance have been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board, contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and offer increased functions with the same size product.

## MECL AVAILABILITY IN SURFACE MOUNT

Motorola is now offering MECL 10K and MECL 10KH in the PLCC (Plastic Leaded Chip Carrier) packages.

MECL in PLCC may be ordered in conventional plastic rails or on Tape and Reel. Refer to the Tape and Reel section for ordering details.

## TAPE AND REEL

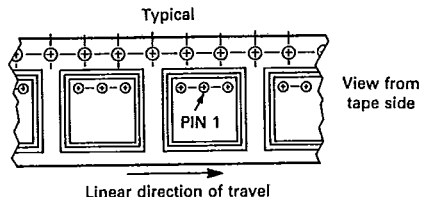
Motorola has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. The packaging fully conforms to

the latest EIA RS-481A specification. The antistatic embossed tape provides a secure cavity sealed with a peel-back cover tape.

## GENERAL INFORMATION

- Reel Size 13 inch (330 mm) Suffix: R2
- Tape Width 16 mm
- Units/Reel 1000

## MECHANICAL POLARIZATION



## ORDERING INFORMATION

- Minimum Lot Size/Device Type = 3000 Pieces.
- No Partial Reel Counts Available.
- To order devices which are to be delivered in Tape and Reel, add the appropriate suffix to the device number being ordered.

## EXAMPLE:

### ORDERING CODE

MC10100FN  
MC10100FNR2  
MC10H100FN  
MC10H100FNR2  
MC12015D  
MC12015DR2

### SHIPMENT METHOD

Magazines (Rails)  
13 inch Tape and Reel  
Magazines (Rails)  
13 inch Tape and Reel  
Magazines (Rails)  
13 inch Tape and Reel

## DUAL-IN-LINE PACKAGE TO PLCC PIN CONVERSION DATA

The following tables give the equivalent I/O pinouts of Dual-In-Line (DIL) packages and Plastic Leaded Chip Carrier (PLCC) packages.

## Conversion Tables

16 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
20 PIN PLCC	2	3	4	5	6	7	8	9	10	12	13	14	15	17	18	19	20

20 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
20 PIN PLCC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

24 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
28 PIN PLCC	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	22	23	24	25	26	27	28