MOTOROLA

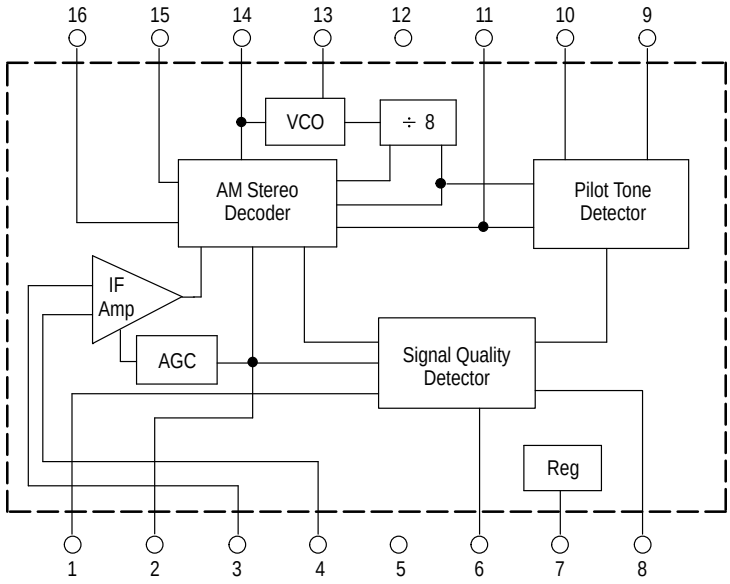
MC13028A

Advanced Wide Voltage IF and C-QUAM® AM Stereo Decoder

The MC13028A is a third generation C–QUAM stereo decoder targeted for use in low voltage, low cost AM/FM E.T.R. radio applications. Advanced features include a signal quality detector that analyzes signal strength, signal to noise ratio, and stereo pilot tone before switching to the stereo mode. A “blend function” much like FM stereo has been added to improve the transition from mono to stereo. The audio output level is adjustable to allow easy interface with a variety of AM/FM tuner chips. The external components have been minimized to keep the total system cost low.

- Adjustable Audio Output Level
- Stereo Blend Function
- Stereo Threshold Adjustment
- Operation from 2.2 V to 12 V Supply
- Precision Pilot Tone Detector
- Forced Mono Function
- Single Pinout VCO
- IF Amplifier with IF AGC Circuit
- VCO Shutdown Mode at Weak Signal Condition

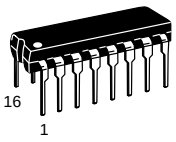
Representative Block Diagram



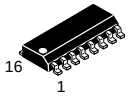
This device contains 679 active transistors.

C–QUAM AM STEREO ADVANCED WIDE VOLTAGE IF and DECODER for E.T.R. RADIOS

SEMICONDUCTOR TECHNICAL DATA

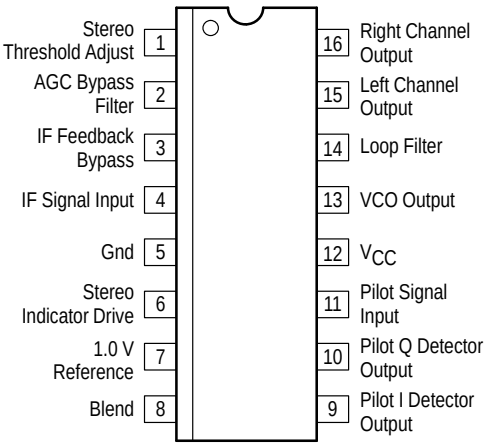


P SUFFIX
PLASTIC PACKAGE
CASE 648



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13028AD	T_A = –25° to +70°C	SO–16
MC13028AP		DIP–16

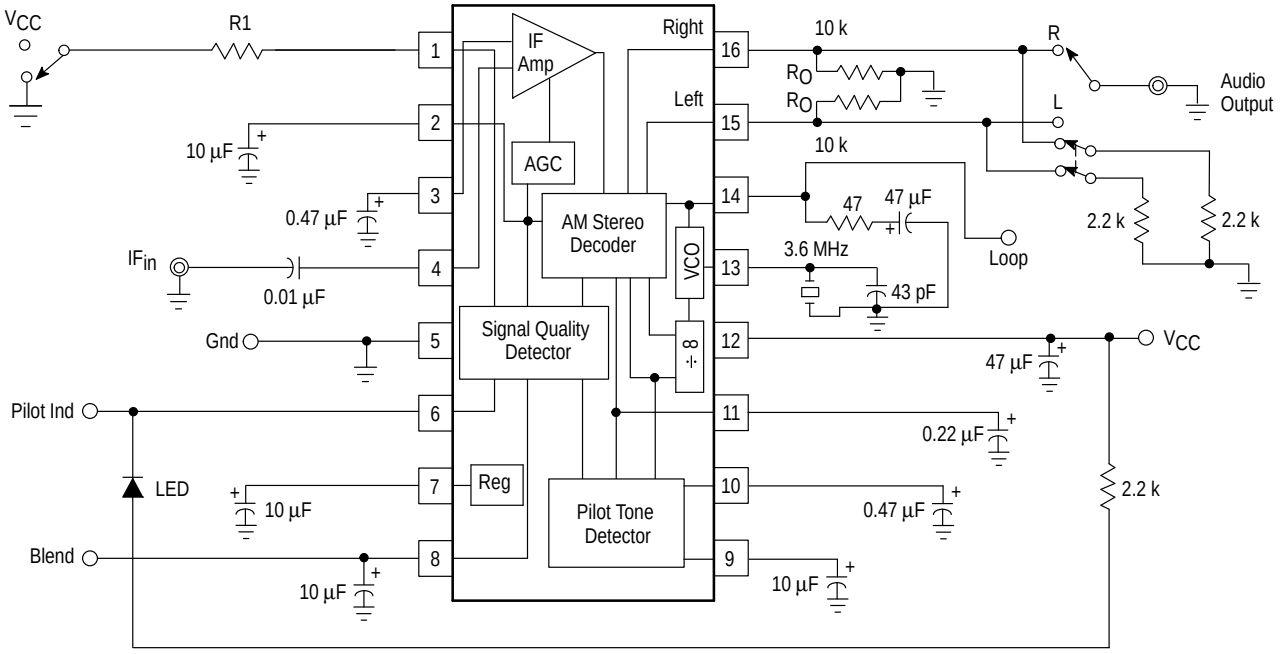
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	14	Vdc
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	–25 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
LED Indicator Current	I_{LED}	10	mA

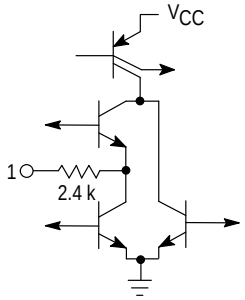
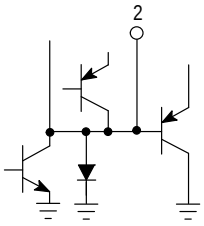
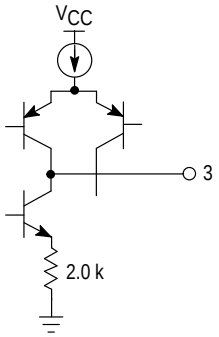
ELECTRICAL CHARACTERISTICS (V_{CC} = 8.0 Vdc, T_A = 25°C, Input Signal Level = 74 dBµV, Modulation = 1.0 kHz @ 50% Modulation, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current Drain	I_{CC}				mA
V_{CC} = 2.2 V		–	9.0	11	
V_{CC} = 8.0 V		–	11	–	
Audio Output Level, L+R, Mono Modulation	V_{out}				mVrms
R_O = 1.8 k, V_{CC} = 2.2 V, Input 55 dBµV		22	33	44	
R_O = 10 k, V_{CC} = 8.0 V, Input 50 dBµV		150	200	250	
Input 40 dBµV		80	130	180	
Input 31 dBµV		–	50	–	
Audio Output Level, L or R Only, Stereo Modulation	V_{out}				mVrms
R_O = 1.8 k, V_{CC} = 2.2 V, 55 dBµV Input		35	80	106	
R_O = 10 k, V_{CC} = 8.0 V		340	460	580	
Output THD					%
50% Stereo, L or R Only	THD1	–	0.6	1.8	
50% Mono, L+R	THD2	–	0.3	0.6	
90% Mono, L+R, Input 86 dBµV	THD3	–	–	1.5	
Channel Separation	L or R	23	35	–	dB
50% L or R Only					
Decoder Input Sensitivity	V_{in}	–	33	–	dBµV
V_{out} = –10 dB					
Force to Mono Mode, (Pin 10)	–	0.25	0.3	–	Vdc
Stereo Threshold Adjust (Pin 1)	S_{TA}				dBµV
Pin 1 Open		–	50	55	
R1 = 15 k (Gnd)		–	55	–	
R1 = 680 k (V_{CC})		–	48	–	
Signal to Noise Ratio, R_O = 10 k	S/N				dB
50% Stereo, L or R Only		40	62	–	
50% Mono, L+R		40	59	–	
Input Impedance	R_{in}	–	10	–	kΩ
(Reference Specification)	C_{in}	–	8.0	–	pF
Maximum Input Signal Level for THD ≤ 1.5%	–	–	–	86	dBµV
Blend Voltage	BI				Vdc
Mono Mode		0.7	–	0.9	
Stereo Mode		1.20	1.30	1.35	
Out of Lock		–	0.12	0.2	
VCO Lock Range	OSC_{tun}	–	±2.5	–	kHz
AGC Range	AGC_{rng}	–	44	–	dB
Channel Balance	C–B	–1.0	–	1.0	dB
Pilot Sensitivity	–	–	2.5	4.0	%

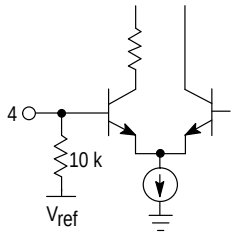
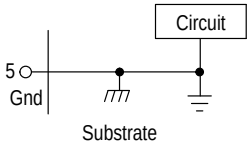
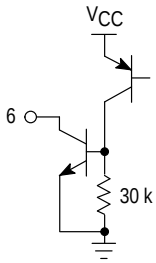
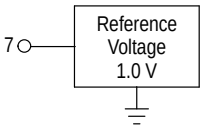
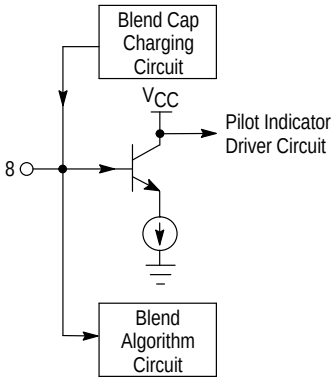
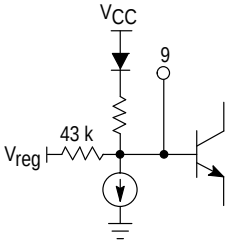
Standard Test Circuit



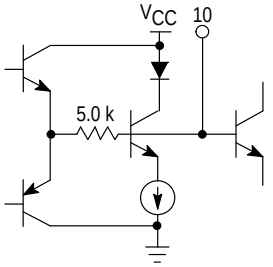
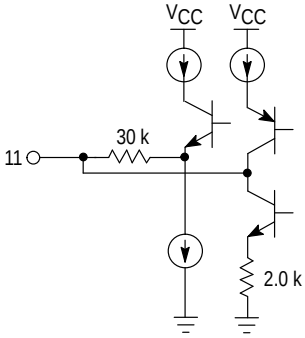
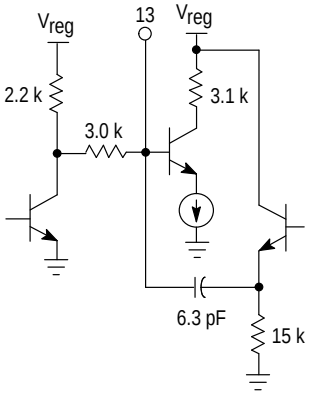
PIN FUNCTION DESCRIPTION

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
1	S_{TA}		**Stereo Threshold Adjustment Pin** The function of this circuit is to provide the freedom to achieve a desired value of incoming IF signal level which will cause full stereo operation of the decoder. The level can be determined by the value of R1, a resistor from Pin 1 that can be connected to either V_{CC} or to ground. This resistor may also be omitted in some designs (Pin 1 left open). The approximate dc level with the pin left open is 0.6 Vdc.
2	AGC_{cap}		**AGC Filter Bypass Capacitor** An electrolytic capacitor is used as a bypass filter and it sets the time constant for the AGC circuit action. The recommended capacitor value is 10 µF from Pin 2 to ground. The dc level at this pin varies as shown in the curve in Figure 13, AGC Voltage versus Input Level.
3	IF_{FBcap}		**IF Amplifier Feedback Capacitor** A capacitor which is specified to have a low ESR at 450 kHz is normally used at Pin 3. The value recommended for this capacitor is 0.47 µF from Pin 3 to ground. This component forms a low pass filter which has a corner frequency around 30 kHz.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
4	IF_{in}		**IF Amplifier Input** Pin 4 is the IF input pin. The typical input impedance at this pin is 10 k. The input should be ac coupled through a 0.01 μF capacitor.
5	Gnd		**Supply Ground** In the PCB layout, the ground pin should be connected to the chassis ground directly. This pin is the internal circuit ground and the silicon substrate ground.
6	S_{IND}		**Stereo Indicator Driver** This driver circuit is intended to light an LED or other indicator when the decoder receives the proper input signals and switches into the stereo mode. The maximum amount of current that the circuit can sink is 10 mA. A current limiting resistor is applied externally to control LED brightness versus total power supply current.
7	V_{Ref}		**Regulated Voltage, 1.0 V** An electrolytic capacitor used as a bypass filter is recommended from Pin 7 to ground. The capacitor value should be 10 μF.
8	CAP_{Blend}		**Blend Capacitor** The value of the capacitor on this pin will effect the time constant of the decoder blend function. The recommended value is 10 μF from Pin 8 to ground. The dc level at Pin 8 is internally generated in response to input signal level and signal quality. This pin is a key indicator of the operational state of the IC (see text Functional Description). It is recommended to discharge the blend capacitor externally when changing stations.
9	I_{Pilot}		**Pilot I Detector Output** The Pilot I Detector output requires a 10 μF electrolytic capacitor to ground. The value of this capacitor sets the pilot acquisition time. The dc level at Pin 9 is approximately 1.0 Vdc, unlocked, and 1.1 to 2.4 Vdc in the locked condition.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
10	Q_{Pilot}		**Pilot Q Detector Output** This pin is connected to the Pilot Q detector and requires a 0.47 μF capacitor to ground to filter the error line voltage at the PLL pilot tone detector. If the value of this capacitor is made too large, the decoder may be prevented from coming back into stereo after a signal drop out has been experienced in the field. The force to mono function is also accomplished at this pin by pulling the dc voltage level at the pin below 1.0 V.
11	$PILOT_{fil}$		**Pilot Signal Input** A capacitor to ground forms a filter for the pilot input signal. The recommended value of the capacitor is 0.22 μF. The dc level at Pin 11 is approximately 1.0 Vdc.
12	V_{CC}		**Supply Voltage (V_{CC})** The operating supply voltage range is from 1.8 Vdc to 12 Vdc.
13	OSC_{in}		**Oscillator Input** The oscillator pin requires a ceramic resonator and parallel capacitor connected to ground. The recommended source for the ceramic resonator is Murata, part number CSA 3.60MGF108. A 43 pF NPO capacitor is in parallel with the resonator. The dc level at Pin 13 is approximately 1.1 Vdc.

PIN FUNCTION DESCRIPTION

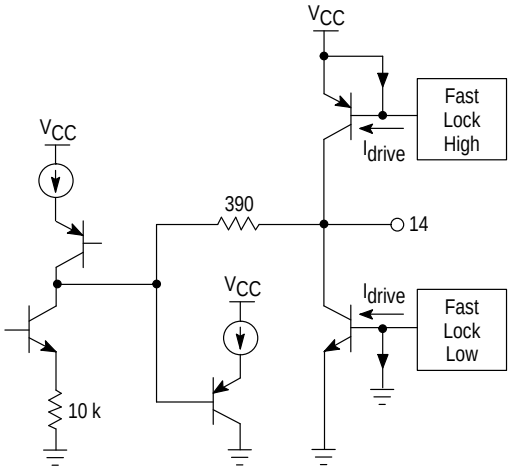
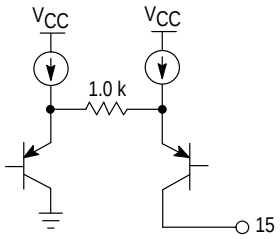
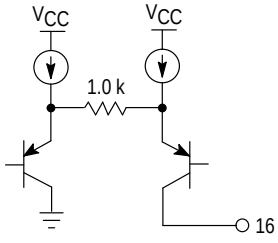
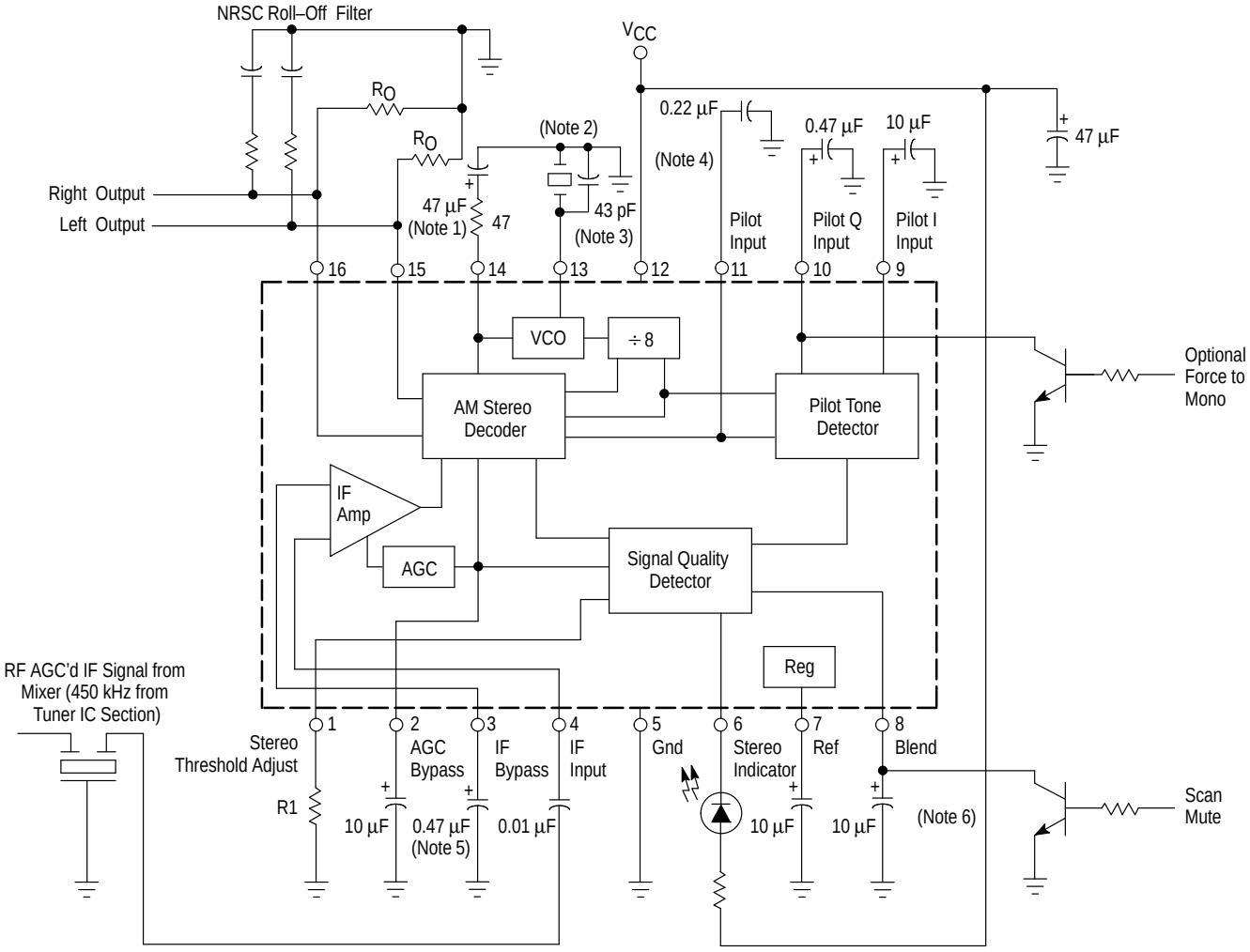
Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
14	$LOOP_{Filter}$		**Loop Filter** A capacitor which forms the loop filter is connected from Pin 14 to ground. The recommended value is 47 µF in series with 47 Ω. This capacitor should be of good construction quality so it will have a very low specification for leakage current in order to prevent stereo distortion. The 47 Ω resistor in series with the capacitor controls the PLL corner frequency response, keeping the response shape critically damped and not peaked up. The dc level at Pin 14 is approximately 0.6 Vdc in the locked condition.
15	$LEFT_{out}$		**Left Channel Audio Output** This is the left channel audio output pin from which the IC can provide 1.3 μA_{pp} drive current for each percent of mono modulation. A resistor to ground sets the level of the audio output. For example, *100%* (mono mod) x 1.3 μA_{pp} (IC drive per % mod) = 130 μA_{pp} flowing through the load resistor. (For a 2.2 k load, 286 mV_{pp} is then the output signal voltage.) When dealing with stereo signals, multiply the mod level by 2; i.e. *50%* (left only mod) x 2 (stereo factor) x 1.3 μA_{pp} (IC drive per % mod) = 130 μA_{pp} flowing through the load resistor.
16	$RIGHT_{out}$		**Right Channel Audio Output** This is the right channel audio output pin. A resistor to ground sets the level of the audio output. See the explanation under the Left Channel Audio Output description above.

Figure 1. Typical Circuit for E.T.R. Applications



NOTES: 1. The 47 µF capacitor is recommended to be a low leakage type capacitor. Leakage current due to this capacitor causes increase in stereo distortion and decreased separation performance.
2. The recommended source for this part is Murata Products. CSA3.60MGF108. The location of this part should be carefully considered during the layout of the decoder circuit. This part should not be near the audio signal paths, the 25 Hz pilot filter lines, or the V_{CC} high current lines, and the ceramic element ground line should be direct to the chassis ground lead in order to avoid any oscillator inter–modulation.
3. The 43 pF capacitor is recommended to be a NPO type ceramic part. Changing the value of this capacitor alters the lock range of the decoder PLL.
4. The tolerance on the value of the 0.22 µF capacitor should be within ±20% for the full design temperature range of operation. Any reduction in the value of this capacitor due to temperature excursions will reduce the pilot tone circuit sensitivity.
5. The 0.47 µF capacitor is recommended to be a low ESR type capacitor, (less than 1.5 Ω) in order to avoid increased audio output distortions under weak input signal conditions with higher modulation levels.
6. The scan/mute function is located on the Blend pin at Pin 8. To provide this function, Pin 8 should be pulled down below 0.3 V until the decoder and the synthesizer have both locked to a new station.

FUNCTIONAL DESCRIPTION

Introduction

The MC13028A is designed as a low voltage, low cost decoder for the C–QUAM AM Stereo technology and is completely compatible with existing monaural AM transmissions. The IC requires relatively few, inexpensive external parts to produce a full featured C–QUAM AM Stereo implementation. The layout is straightforward and should produce excellent stereo performance. This device performs the function of IF amplification, AGC, modulation detection, pilot tone detection, signal quality inspection, and left and right audio output matrix operation. The IC is targeted for use in portable and home AM Stereo radio applications.

A simple overview follows which traces the path of the input signal information to the MC13028A all the way to the audio output pins of the decoder IC.

From the appropriate pin of an AM IC, the IF amplifier circuit of the MC13028A receives its input at Pin 4 as a 450 kHz, typically modulated C–QUAM signal. The input signal level for stereo operation can vary from 47 dBμV to about 90 dBμV. A specific threshold level between these limits can be designed into a receiver by the choice of the resistor value for R1 connected to Pin 1. This IC design incorporates feedback in the IF circuit section which provides excellent dc balance in the IF amplifier. This balanced condition also guarantees excellent monophonic performance from the decoder. An IF feedback filter at Pin 3 is formed by a 0.47 μF low leakage capacitor. It is used to filter out the unwanted audio which is present on the IF amplifier feedback line at higher modulation levels under weak input RF signal conditions. Elimination of the unwanted signal helps to decrease the amount of distortion in the audio output of the stereo decoder under these particular input conditions. An AGC circuit controls the level of IF signal which is subsequently fed to the detector circuits. An AGC bypass capacitor is connected to Pin 2 and forms a single pole low pass filter. The value of this part also sets the time constant for the AGC circuit action.

The amplified C–QUAM IF signal is fed simultaneously to the envelope detector circuit, and to a C–QUAM converter circuit. The envelope detector provides the L+R (mono) signal output which is fed to the stereo matrix. In the converter circuit, the C–QUAM signal is restored to a Quam signal. This is accomplished by dividing the C–QUAM IF signal by the demodulated cos ϕ term. The cos ϕ term is derived from the phase modulated IF signal in an active feedback loop. Cosine ϕ is detected by comparing the envelope detector and the in–phase detector outputs in the high speed comparator/feedback loop. Cosine ϕ is extracted from the I detector output and is actively transferred through feedback to the output of the comparator. The output of the comparator is in turn fed to the control input of the divider, thus closing the feedback loop of the converter circuit. In this process, the cos ϕ term is removed from the divider IF output, thus allowing direct detection of the L–R by the quadrature detector. The audio outputs from both the envelope and the L–R detectors are first filtered to minimize the second harmonic of the IF signal. Then they are fed into a matrix circuit where the Left channel and the Right channel outputs can be extracted at Pins 15 and 16. (The outputs from the I and Q detectors are also filtered similarly.) At this time, a stereo indicator driver circuit, which can sink up to 10 mA, is also enabled. The stereo output will occur if the input IF signal is: larger than the stereo threshold level, not too noisy, and if a proper pilot tone is present. If these three conditions are not met, the blend circuit will begin to force monaural operation at that time.

A blend circuit is included in this design because conditions occur during field use that can cause input signal strength fluctuation, strong unwanted co–channel or power line interference, and/or multi–path or re–radiation. When these aberrant conditions occur, rapid switching between stereo and mono might occur, or the stereo quality might be degraded enough to sound displeasing. Since these conditions could be annoying to the normal listener, the stereo information is blended towards a monaural output. This circuit action creates a condition for listening where these aberrant effects are better tolerated by the consumer.

Intentional mono operation is a feature sometimes required in receiver designs. There are several ways in which to accomplish this feat. First, a resistor from Pin 10 to ground can be switched into the circuit. A value of 1.0 k is adequate as is shown in the schematic in Figure 18. A second method to force the decoder into mono is simply to shunt Pin 10 to ground through an NPN transistor (collector to Pin 10, emitter to ground), where the base lead is held electrically “high” to initiate the action.

A third method to force a mono condition upon the decoder is to shunt Pin 8 of the decoder to ground through an NPN transistor as described above. Effectively, this operation discharges the blend capacitor (10 μF), and the blend function takes over internally forcing the decoder into mono. This third method does not necessarily require extra specific parts for the forced mono function as the first two examples do. The reason for this is that most electronically tuned receiver designs require an audio muting function during turn on/turn off, tuning/scanning, or band switching (FM to AM). When the muting function is designed into an AM Stereo receiver, it also should include a blend capacitor reset (discharge) function which is accomplished in this case by the use of an NPN transistor shunting Pin 8 to ground, (thus making the addition of a forced mono function almost “free”). The purpose of the blend reset during muting is to re–initialize the decoder back into the “fast lock” mode from which stereo operation can be attained much quicker after any of the interruptive activities mentioned earlier, (i.e. turn on, tuning, etc.).

The VCO in this IC is a phase shift oscillator type design that operates with a ceramic resonator at eight times the IF frequency, or 3.60 MHz. With IF input levels below the stereo threshold level, the oscillator is not operational. This feature helps to eliminate audio tweets under low level, noisy input conditions.

The phase locked loop (PLL) in the MC13028A is locked to the L–R signal. This insures good stereo distortion performance at the higher levels of left only or right only modulations. Under normal operating conditions, the PLL remains locked because of the current flow capability of the loop driver circuit. This high gain, high impedance circuit performs optimally when the current flow is balanced. The balanced condition is enhanced by the loop driver filter circuit connected between Pin 14 and ground. The filter circuit consists of a 47 Ω resistor in series with a 47 μF capacitor. The 47 Ω resistor is to set the Fast Lock rate. It is recommended that the capacitor be a very low leakage type electrolytic, or a tantalum composition part because any significant amount of leakage current flowing through the capacitor will unbalance the loop driver circuit and result in less than optimum stereo performance, see Figures 10 and 11.

The pilot tone detector circuit is fed internally from the Q detector output signal. The circuit input employs a low pass filter at Pin 11 that is designed to prevent the pilot tone detector input from being overloaded by higher levels of L–R modulation. The filter is formed by a 0.22 μF capacitor and the input impedance of the first amplifier. A pilot I detector circuit employs a capacitor to ground at Pin 9 to operate in conjunction with an internal resistor to create an RC integration time. The value of the capacitor determines the amount of time required to produce a stereo indication. This amount must include the time it takes to check for the presence of detector falsing due to noise or interference, station retuning by the customer, and pilot dropout in the presence of heavy interference. The pilot Q detector utilizes a filter on its pilot tone PLL error line at Pin 10. This capacitor to ground (usually 0.47 μF) is present to filter any low frequency L–R information that may be present on the error line. If the value of this capacitor is allowed to be too small, L–R modulation ripple on the error line may get large enough to cause stereo dropout. If the capacitor value is made too large, the pilot tone may be prevented from being reacquired if it is somehow lost due to fluctuating field conditions.

A 1.0 V reference level is created internally from the V_{CC} source to the IC. This regulated line is used extensively by circuits throughout the MC13028A design. An electrolytic capacitor from Pin 7 to ground is used as a filter for the reference voltage.

DISCUSSION OF GRAPHS AND FIGURES

If the general recommendations put forth in this application guide are followed, excellent stereo performance should result.

The curves in Figures 2 through 7 depict the separation and the distortion performance in stereo for 30%, 50%, and 65% single channel modulations respectively. The data for these figures were collected under the conditions of V_{CC} = 8.0 V and R_O = 10 k in both the left and the right channels as applied to the application circuit of Figure 1. A very precise laboratory generator was used to produce the AM Stereo test signal of 450 kHz at 70 dBμV fed to Pin 4. An NRSC post detection filter was not present at the time of these measurements. The audio separation shows an average performance at 30% and 50% modulations of –45 dB in the frequency range of 2.0 kHz to 5.0 kHz. The corresponding audio distortions under these conditions are about 0.28% at 30% modulation, and about 0.41% at 50% modulation.

Figure 6 shows that the typical separation at 65% modulation in the 2.0 kHz to 5.0 kHz region is about –37 dB, and the corresponding audio distortion shown in Figure 7 is about 1.0%. The performance level of these sinusoidal signals is somewhat less than those discussed in the previous paragraph due to the internal operation of the clamping circuits. In the field, the transmitters at AM Stereo radio stations are not usually permitted to modulate single channel levels past 70%. Therefore these conditions do not occur very often during normal broadcast material.

The roll–off at both the low and high frequencies of the 30% single channel driven responses is due to the fact that a post detection bandpass filter of 60 Hz to 10 kHz was used in the measurement of the data, while a post detection filter of 2.0 Hz to 20 kHz was used for the collection of data in the 50% and 65% modulation examples. The tighter bandwidth was used while collecting the performance data at 30% modulation levels in order to assure that the distortion measurement was indicative of the true distortion products measured near the noise floor and thus not encumbered by residual noise and hum levels which would erroneously add to the magnitude of the harmonic distortion data. Note in Figure 8 the traces of noise response for the four different bandwidths of post detection filtering. It can be seen that the noise floors improve steadily with increasing levels of incoming 450 kHz as the value of the lower corner frequency of the filter is increased. Data for the stereo noise floors was collected with the decoder in the forced stereo mode.

Figure 2. Single Channel Separation at 30% Modulation

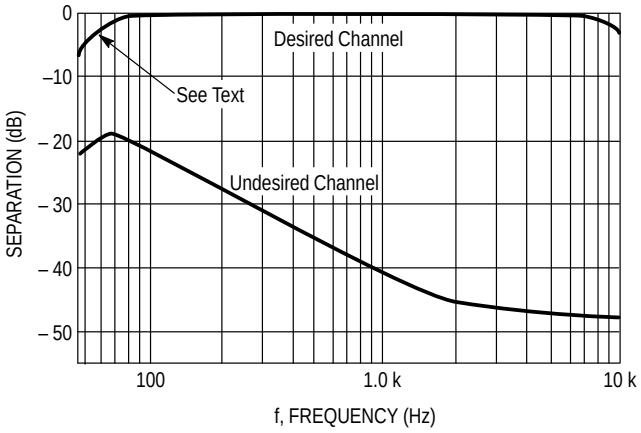


Figure 3. Single Channel Distortion at 30% Modulation

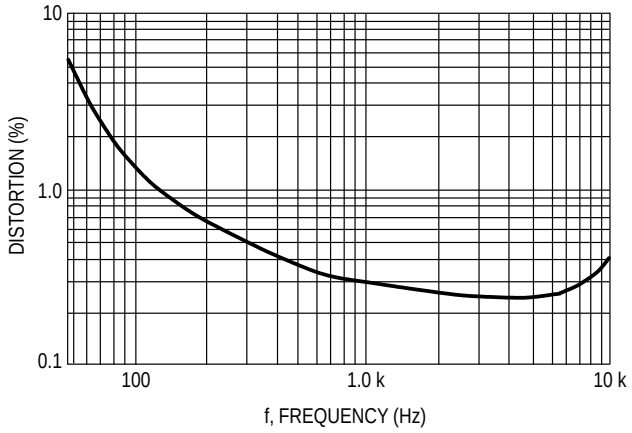


Figure 4. Single Channel Separation at 50% Modulation

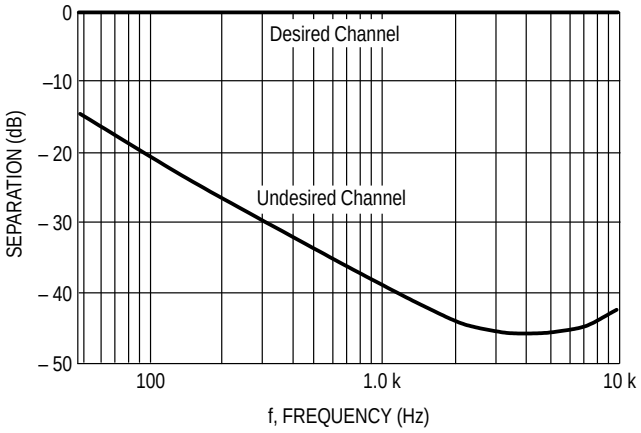


Figure 5. Single Channel Distortion at 50% Modulation

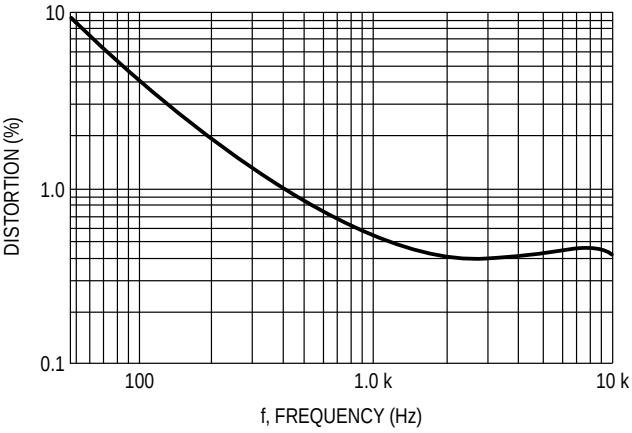


Figure 6. Single Channel Separation at 65% Modulation

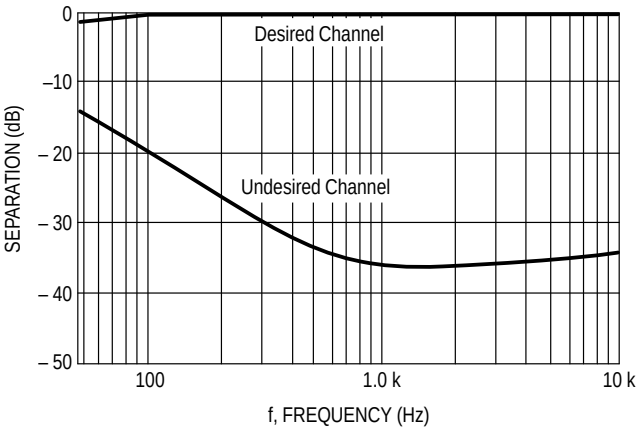


Figure 7. Single Channel Distortion at 65% Modulation

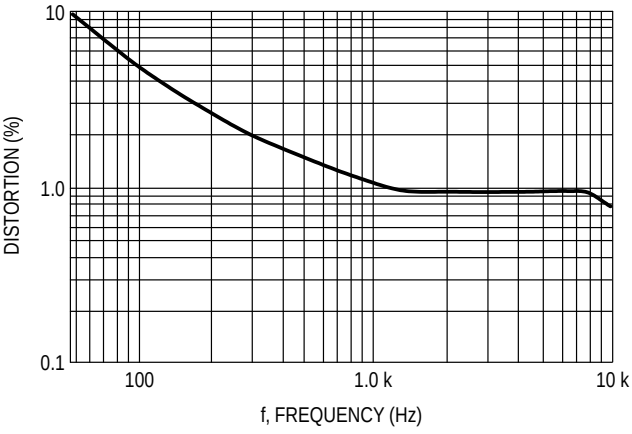


Figure 8. Stereo Noise and Stereo Composite Distortion when Mono Transmitted

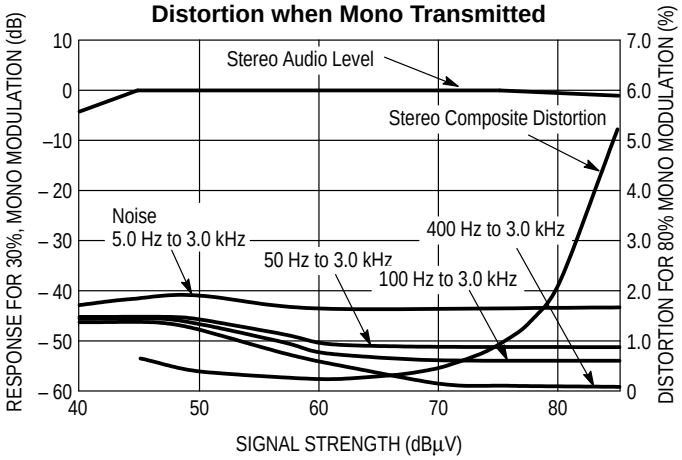


Figure 9. R1 versus Stereo Threshold Point

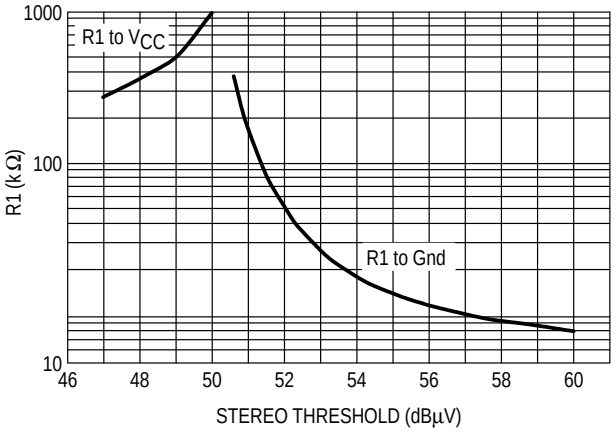


Figure 10. Decoder Separation versus Filter Capacitor (Pin 14) Leakage Current

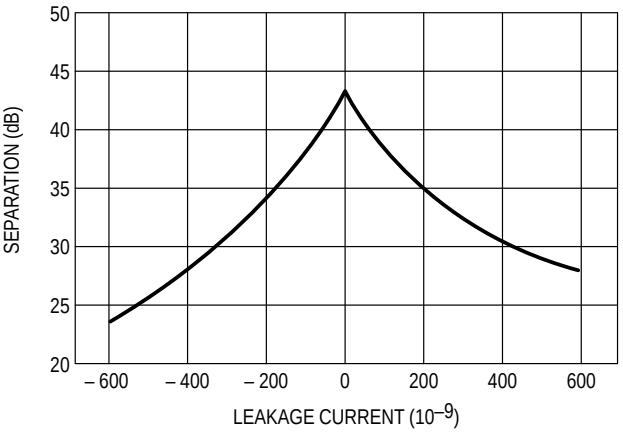


Figure 11. Decoder Distortion versus Filter Capacitor (Pin 14) Leakage Current

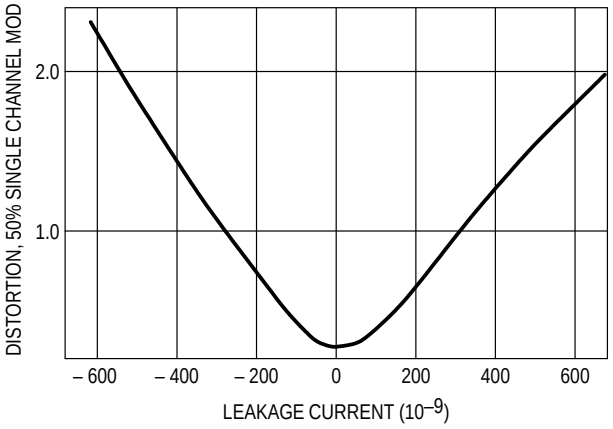


Figure 12. Low Frequency Corner of PLL Response

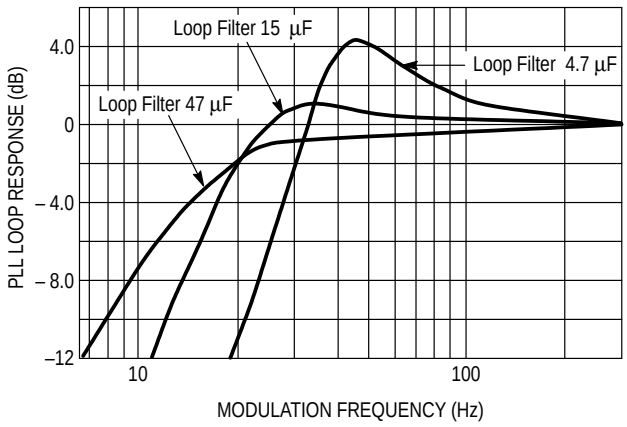


Figure 13. AGC Voltage versus Input Signal Level

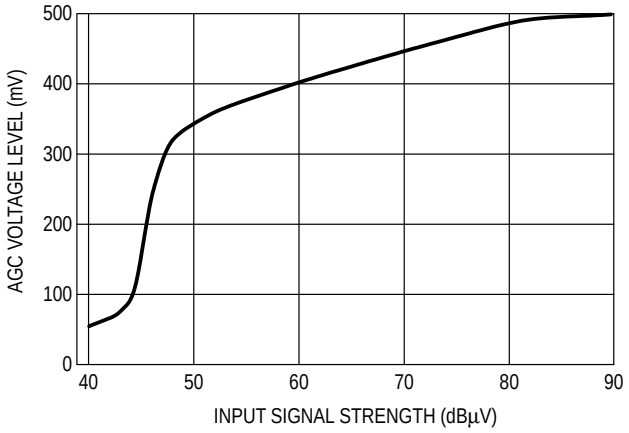


Figure 9 presents more detailed information with respect to the value of resistor R1 at Pin 1 versus the desired incoming signal level for stereo threshold.

Figures 10 and 11, discussed briefly in the Pin Function Description Section, show the importance of using a quality component at Pin 14 to ground. It can be seen that an electrolytic capacitor leakage current of 600 nA can unbalance the PLL to the point where stereo performance may degrade to only 25 dB of separation with a corresponding 2.0% distortion at 50% modulation levels.

The value of the capacitor connected to Pin 14 (47 μF) is also a factor in the determination of the low frequency corner of the PLL circuit response. Three traces of PLL response appear in Figure 12 where they have been plotted for three different values of loop filter capacitor. The recommended value of 47 μF provides the best response shape in this particular circuit set–up where a Murata Products CSA3.60MGF108 part is used.

Figure 13 presents the response of the AGC voltage versus decoder input signal level. This is a typical response when the IC is used as shown in the application schematic of Figure 1. The trace begins approximately at the point of decoder sensitivity, and rises rapidly until reaching the area of stereo sensitivity, approximately 50 dBμV. Thereafter, the circuit responds in a linear fashion for the next 30 dB of input signal increase.

Figures 14 through 17 inclusively depict the V_{CC} ripple rejection performance for the MC13028A under mono and stereo conditions for nominal and for low values of V_{CC}. It should be noted that this data was collected without any V_{CC} filtering. As one might expect, the ripple rejection is better in mono than in stereo. When the decoder operates in stereo, the VCO is functional, thus the decoder becomes more susceptible to audio ripple on the V_{CC} line. Under normal operating conditions, with the recommended value of 47 μF at Pin 12 and 10 μF at Pin 7, a V_{CC} ripple reading will be virtually the same as measuring the noise floor of the IC.

AM STEREO TUNER / FM STEREO IF

Description of Application

This application combines a Sanyo LA1832M with the Motorola MC13028A AM Stereo decoder IC. The LA1832 provides an FM IF, FM multiplex detection, AM tuning, and the AM IF functions. The MC13028A provides the AM Stereo detection as well as Left and Right audio outputs. An MC145151 synthesizer provides the frequency control of the local oscillator contained within the LA1832. Frequency selection is by means of a switch array attached to the synthesizer. The application circuit is shown in Figure 18.

Circuit Board Description

The copper side layout and the component locations are shown in Figure 19. The view is from the plating side of the board, with the components shown in hidden view. Several jumper wires are placed on the component side of the board to complete the circuit. Posts are provided for electrical connections to the circuit. The circuit board has been scaled to fit the page, however, the dimensions provide the true size.

Circuit Description

The Sanyo data sheet for the LA1832 should be consulted for an understanding of the FM detection and multiplex decoding.

Special Parts

The following information provides circuit function, part number, and the manufacturer's name for special parts identified by their schematic symbol. Where the part is not limited to a single source, a description sufficient to select a part is given.

U1 IC – AM Stereo Decoder
MC13028AD by Motorola

U2 IC – AM/FM IF and Multiplex Tuner
LA1832M by Sanyo

U3 IC – Frequency Synthesizer
MC145151DW2 by Motorola

T1 AM IF Coil
A7NRES–11148N by TOKO

F1 AM IF Ceramic Filter
SFG450F by Murata

F2 FM IF Detector Resonator
CDA10.7MG46A by Murata

F3 FM Multiplex Decoder Resonator
CSB456F15 by Murata

F4 AM Tuner Block
BL–70 by Korin Giken

X1 10.24 MHz Crystal, Fundamental Mode,
AT Cut, 18 pF Load Cap, 35 Ω maximum series R.
HC–18/U Holder

X2 3.6 MHz AM Stereo Decoder Resonator
CSA3.60MGF108 by Murata

S5 8 SPST DIP Switch

Figure 14. Mono V_{CC} Ripple Rejection

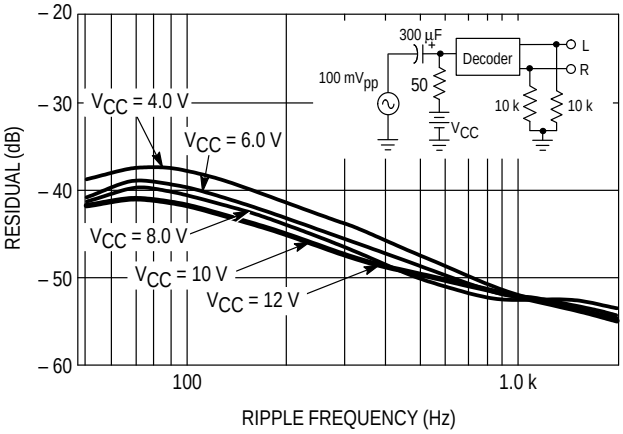


Figure 15. Mono Low Voltage V_{CC} Ripple Rejection

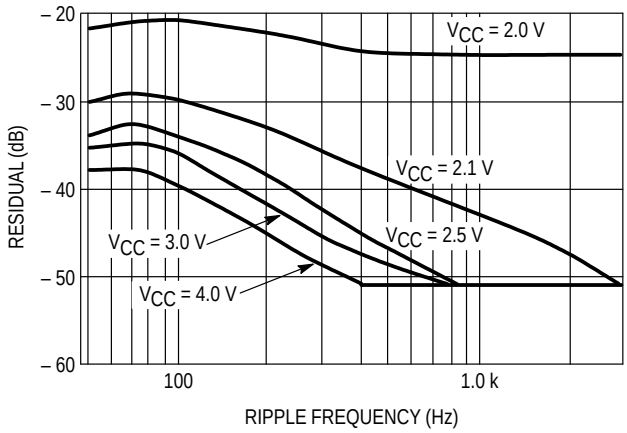


Figure 16. Stereo V_{CC} Ripple Rejection

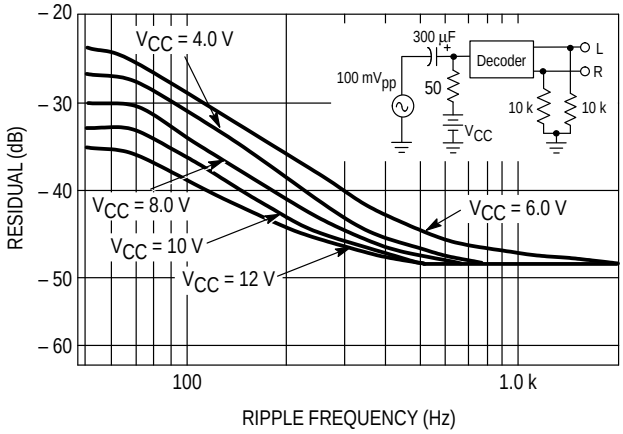


Figure 17. Stereo Low Voltage V_{CC} Ripple Rejection

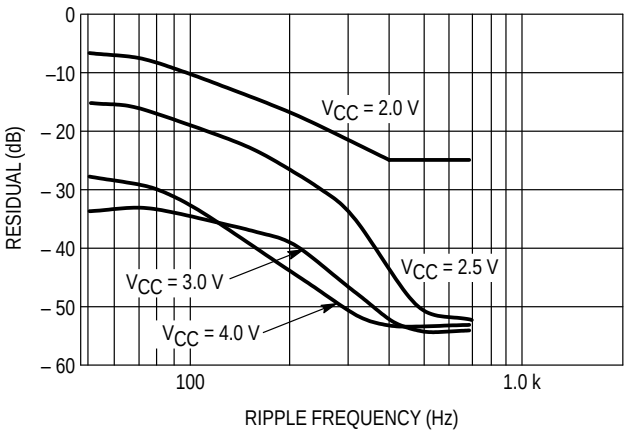


Figure 18. MC13028A Decoder IC Application

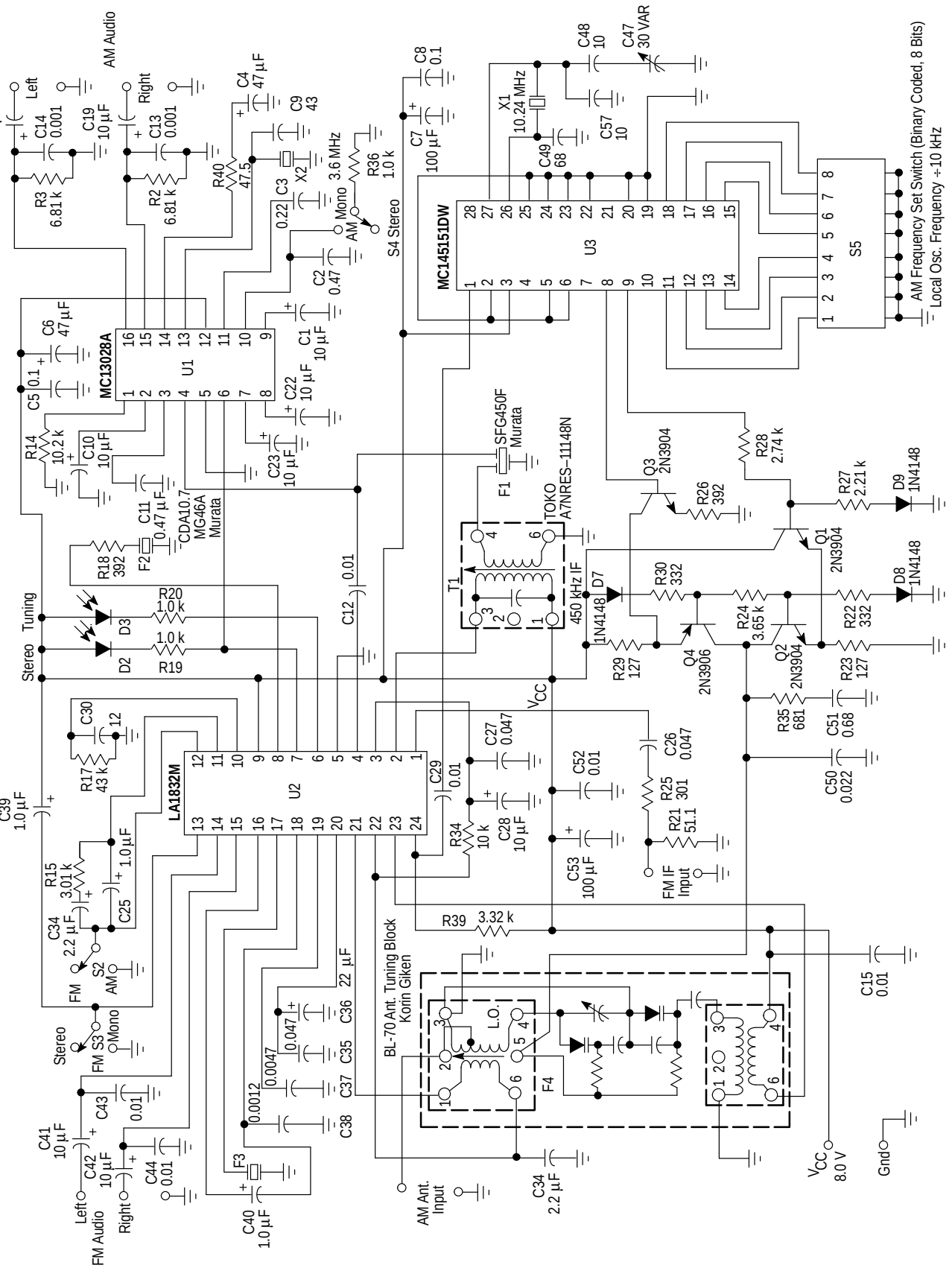
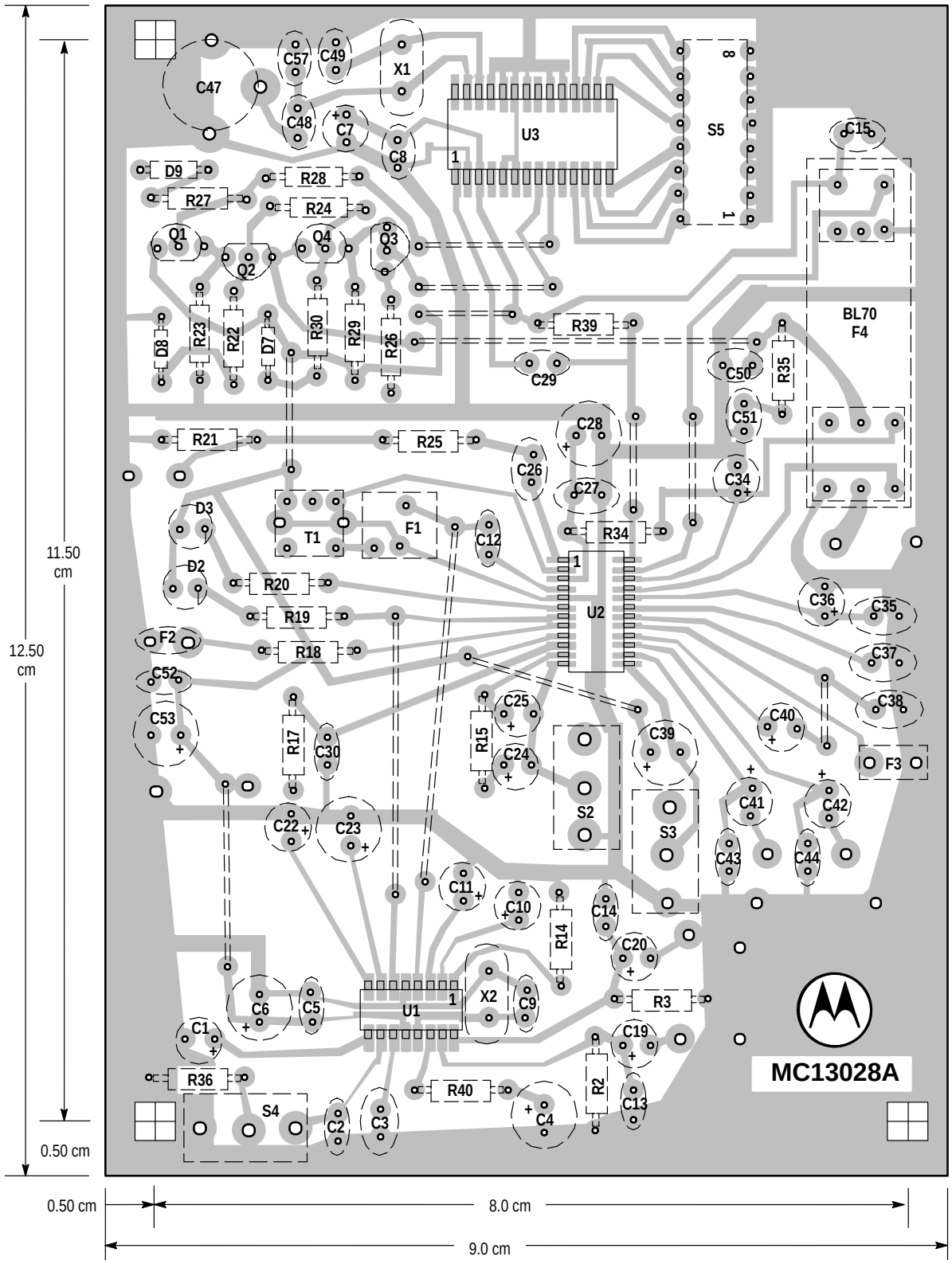


Figure 19. MC13028A Decoder IC Application Circuit Board



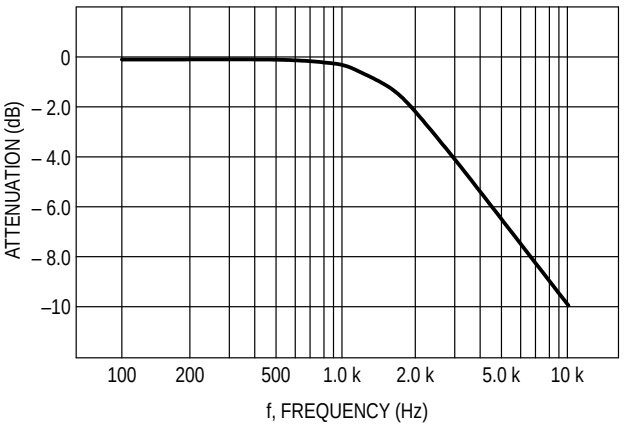
The LA1832 tuner IC (U2) is set for AM operation by switch S2 connecting Pin 12 to ground. An AM Stereo signal source is applied to Pin 2 of the RF coil contained within the BL–70 tuning block. That coil applies the signal to Pin 21 of U2. The L.O. coil is connected from Pin 23 to V_{CC}. The secondary is tuned by a varactor which is controlled by a dc voltage output from the synthesizer circuit. The reactance of this oscillator tank is coupled back to Pin 23. It is through this reactance that the frequency of the L.O. is determined. A buffered output from the L.O. emerges at Pin 24. This signal is routed to Pin 1 of the synthesizer (U3), thus completing the frequency control loop.

The mixer output at Pin 2 is applied to the IF coil T1. Coil T1 provides the correct impedance to drive the ceramic bandpass filter F1. The IF signal returns to U2 through Pin 4, and also to the input, Pin 4 of the AM Stereo decoder (U1). The ceramic filter F1 is designed to operate into a load resistance of 2.0 kΩ. This load is provided at Pin 4 of U2.

The stereo outputs exit from Pins 15 and 16 of U1. The design amplitudes of the audio outputs will vary according to the values used for the resistors to ground at Pins 15 and 16 of the decoder, (labeled R_O in the Electrical Characteristics Table and the Test Circuit on page 2 and 3, and in Figure 1, and called R2 and R3 in Figure 18). While the values chosen for R_O are left to the discretion of the designer, the numbers chosen in this data sheet are reflective of those required to set the general industry standard levels of audio outputs in receiver designs.

Pins 15 and 16 are also good locations for the insertion of simple RC filters that are used to comply with the United States NRSC requirement for the shape of the overall receiver audio response. The following curve, Figure 20, shows the response of this U.S. standard.

Figure 20. NRSC De–Emphasis Curve for the United States



There are many design factors that affect the shape of the receiver response, and they must all be considered when trying to approximate the NRSC de–emphasis response. The mixer output transformer (IF coil, T1), and ceramic filter probably have the greatest contribution to the frequency response. The ceramic filter can be tailored from its rated response by the choice of transformer impedance and bandwidth. When designing an overall audio response shape, the response of the speakers or earphones should also be considered.

Component Values.

The Pin Function Description table gives specific information on the choice of components to be used at each pin of U1. A similar section in the Sanyo LA1832 data sheet should be consulted as to the components to be used with U2.

Tuning

The frequency to which the test circuit will tune is set by the eight binary switches contained in the S5 assembly, numbered from 1 to 8. Number 1 connects to Pin 11 of U3 and number 8 connects to Pin 18. The other switches connect to the pins in between and in order. Each individual switch is a SPST type.

To tune to a specific RF frequency, a computation must be made in order to ascertain the divide ratio to input to the synthesizer via the switch array. The divide ratio is simply the eight digit binary equivalent number for the local oscillator frequency divided by 10 kHz. The local oscillator frequency is the desired RF frequency plus 450 kHz, the IF frequency. Any local oscillator value within the AM band can be represented by a binary number. Each binary bit represents a switch setting where a “1” is an open switch and a “0” is a closed switch. The most significant bit represents switch 8 which is connected to Pin 18.

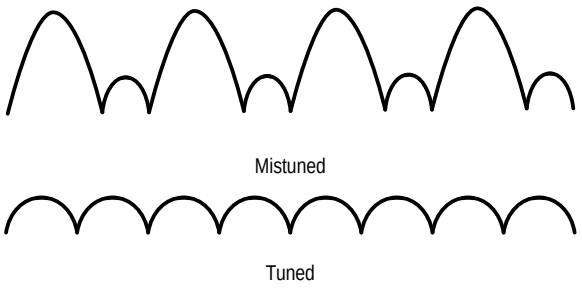
To illustrate, consider the setting for an input frequency of 1070 kHz. (This frequency was used to test the circuit board as described further on.) The local oscillator frequency is 1070 kHz plus 450 kHz which equals 1520 kHz. Dividing by 10 kHz yields the number 152. The binary number for 152 is 10011000. Thus the switches are set to:

Switch	Position	Number
8	Open	1
7	Closed	0
6	Closed	0
5	Open	1
4	Open	1
3	Closed	0
2	Closed	0
1	Closed	0

Circuit Adjustments

The FM circuit requires no adjustment. The AM L.O. must be able to tune from 980 to 2150 kHz to cover the broadcast range. Adjust the core of the L.O. coil if needed in order to be able to cover this range. The AM RF coil and trimmer can be adjusted for best signal after connection to the loop antenna. The coil is adjusted near the low end of the band, and the trimmer is adjusted at the top of the band. The IF coil, T1, is first adjusted for maximum signal out of the filter, F1. This is a “coarse” adjustment. The final “fine tune” adjustment occurs after the following conditions are met. From an AM Stereo generator with the pilot tone off, feed the decoder an input signal of approximately 70 dBμV that is modulated with an 80% L–R audio signal at 3.0 kHz. While monitoring either the left or the right output from the decoder on an oscilloscope, precisely fine tune the IF coil for a minimum residual signal, see the following diagram. If there is no sideband tilt in the system, this adjustment should hold for both channels. Otherwise, the best compromise adjustment for both channels should be used.

Figure 21. Decoder Signal Output for Mistuned and Tuned Condition with Input Signal of 80% L–R at 3.0 kHz



AM Circuit Test

The connections for test are as shown in Figure 22. A 50 Ω resistor is placed on the AM antenna input. The AM Stereo generator is connected to the AM antenna input. Measurements of audio level in mono mode are made with an audio voltmeter connected through a FET probe (pilot signal “off”). Measurements of audio level and distortion in stereo mode (pilot signal “on”) are made using a pilot rejection filter ahead of the distortion analyzer or the audio meter. The pilot rejection filter has a rejection ratio that should exceed 20 to 25 dB. Typical data is shown in Figures 23–26. Figures 23 and 24 were read on the left channel in mono mode. Figures 25–26 were in stereo mode.

Figure 22. MC13028A/LA1832 Application Circuit Board Test Setup

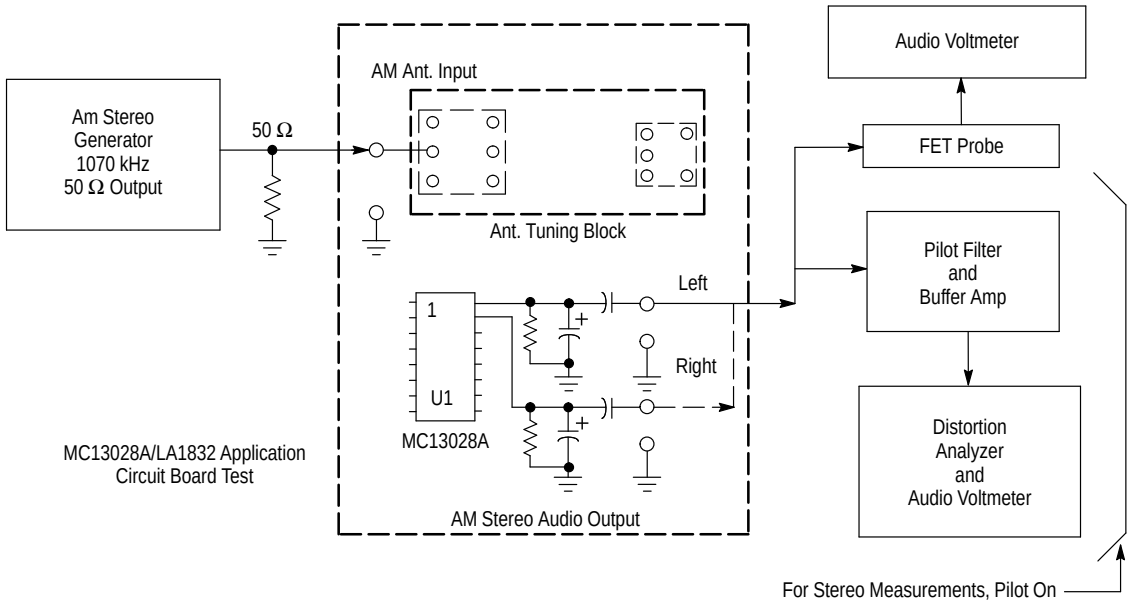


Figure 23. Left AM Output at 30% Modulation

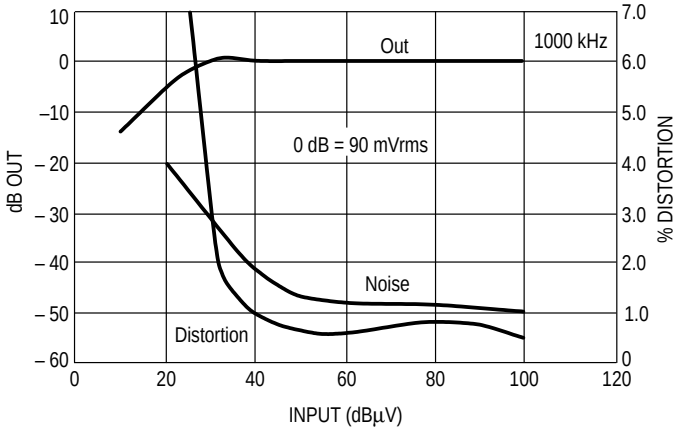


Figure 24. Left AM Output at 80% Modulation

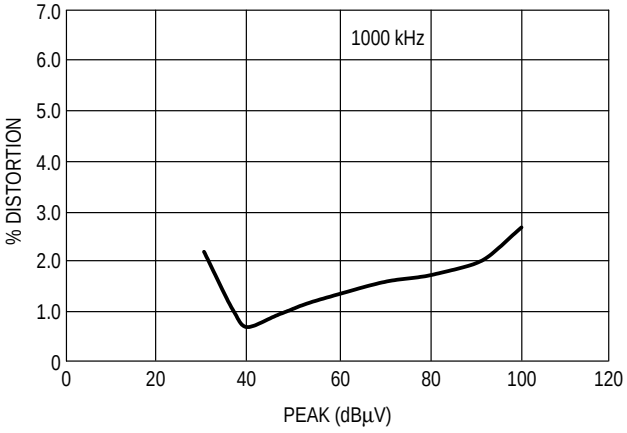


Figure 25. AM Output Right Channel Only Modulated at 50%

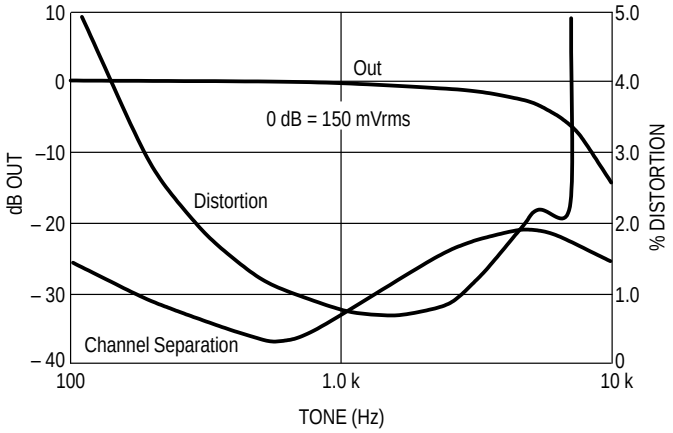
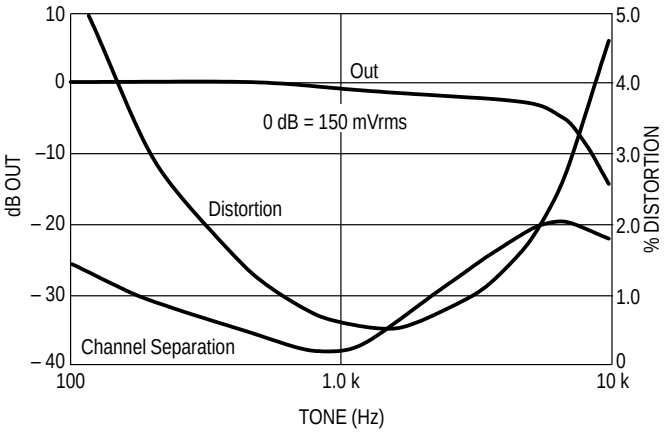
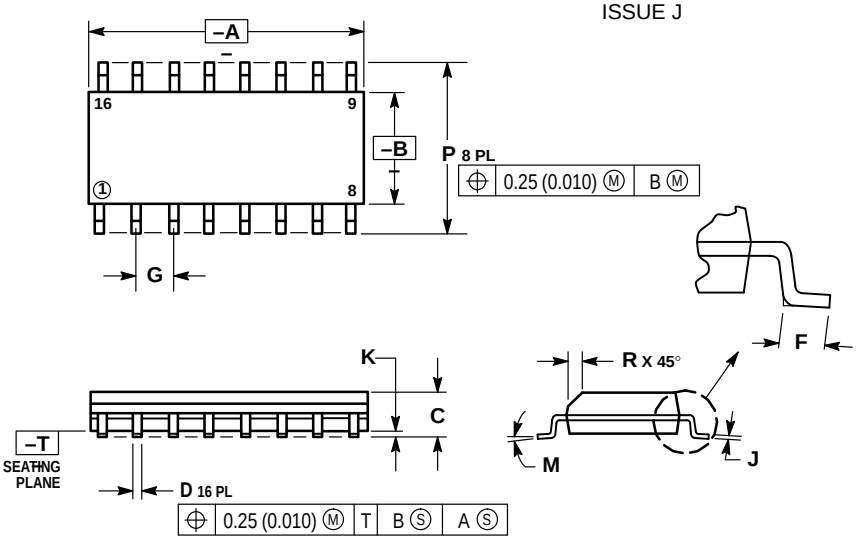


Figure 26. AM Output Left Channel Only Modulated at 50%



OUTLINE DIMENSIONS

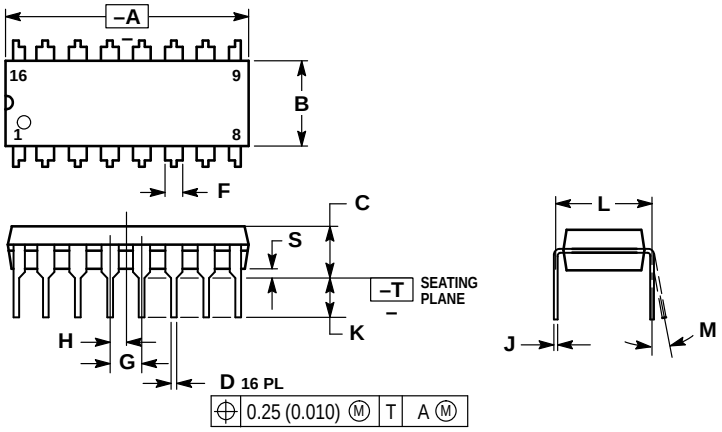
D SUFFIX
PLASTIC PACKAGE
CASE 751B–05
(SO–16)
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

P SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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