MOTOROLA

MC13144

Advance Information

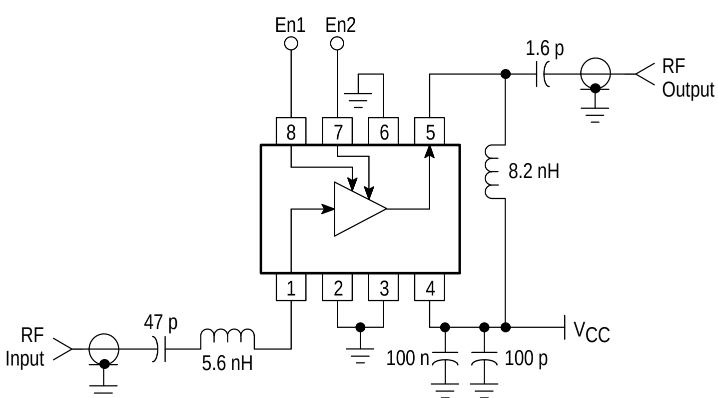
VHF - 2.0 GHz Low Noise Amplifier with Programmable Bias

The MC13144 is designed in the Motorola High Frequency Bipolar MOSIAC V™ wafer process to provide excellent performance in analog and digital communication systems. It includes a cascoded LNA usable up to 2.0 GHz and at 1.8 Vdc, with 2 bit digital programming of the LNA bias. Targeted applications are in the UHF Family Radio Services, UHF and 800 MHz Special Mobile Radio, 800 MHz Cellular and GSM, PCS, DECT and PHS at 1.8 to 2.0 GHz and Cordless Telephones in the 902 to 928 MHz band covered by FCC Title 47; Part 15. The MC13144 offers the following features:

- 17 dB Gain at 900 MHz
- 1.4 dB Noise Figure at 900 MHz
- 1.0 dB Compression Point of –7.0 dBm; Input Third Order Intercept Point of –5.0 dBm
- Low Operating Supply Voltage (1.8 to 6.0 Vdc)
- Programmable Bias with Enable 1 and Enable 2
- Enable 1 and Enable 2 Programmed High for Optimal Noise Figure and Gain Associated with NF
- Can Override Enable and Externally Program In Up to 15 mA

MOSAIC V is a trademark of Motorola, Inc.

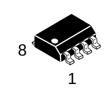
Typical Application as 900 MHz Low Noise Amplifier



This device contains 67 active transistors.

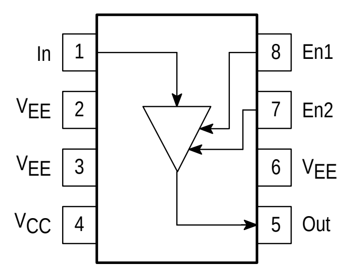
VHF – 2.0 GHz LOW NOISE AMPLIFIER WITH PROGRAMMABLE BIAS

SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13144D	T_A = – 40° to +85°C	SO–8

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}(max)$	7.0	Vdc
Junction Temperature	T_{Jmax}	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTES: 1. Devices should not be operated at or outside these values. The “Recommended Operating Conditions” provide for actual device operation.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	1.8	–	6.0	Vdc

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.0 Vdc; f_{RF} = 1.0 GHz; Pin = –25 dBm)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (Power Down) (En1 = En2 = Low)	I_{CC0}	–	0.0001	20	µA
Supply Current (Power Up) (En1 = High; En2 = Low)	I_{CC1}	–	1.2	2.0	mA
Supply Current (Power Up) (En1 = High; En2 = Low)	I_{CC2}	–	3.4	5.0	mA
Supply Current (Power Up) (En1 = High; En2 = Low)	I_{CC3}	–	8.2	12	mA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 3.0 Vdc; f_{RF} = 1.0 GHz; Pin = –25 dBm)

Characteristic	Symbol	Min	Typ	Max	Unit
Amplifier Gain (50 Ω Insertion Gain) (En1 = En2 = High)	S_{21}^2	–	12	–	dB
Amplifier Reverse Isolation (En1 = En2 = High)	S12	–	–35	–	dB
Amplifier Input Return Loss (En1 = En2 = High)	Γin_{amp}	–	–10	–	dB
Amplifier Output Return Loss (En1 = En2 = High)	Γout_{amp}	–	–15	–	dB
Input 3rd Order Intercept Point (En1 = En2 = High)	IIP3				dBm
df = 100 kHz		–	–11	–	
df = 1.0 MHz		–	–5.0	–	
Amplifier Noise Figure (Figure 1; En1 = En2 = High)	NF	–	1.4	2.0	dB
Amplifier Gain @ NF (Figure 1; En1 = En2 = High)	G_{NF}	–	17	–	dB
Amplifier Gain (En1 = En2 = High)	G_{ain3}	14	17	–	dB
Amplifier Gain (En1 = High; En2 = Low)	G_{ain2}	10	13.3	–	dB
Amplifier Gain (En1 = High; En2 = Low)	G_{ain1}	6.0	9.2	–	dB

CIRCUIT DESCRIPTION

General

The MC13144 is a low noise amplifier with programmable bias. This device is designated for use in the front end section in analog and digital FM systems such as Wireless Local Area Network (LAN), Digital European Cordless Telephone (DECT), PHS, PCS, GPS, Cellular, UHF and 800 MHz Special Mobile Radio (SMR), UHF Family Radio Services and 902 to 928 MHz cordless telephones.

Current Regulation/Enable

Temperature compensating voltage independent current regulation is digitally controlled by a 2 bit programmable bias/enable circuit.

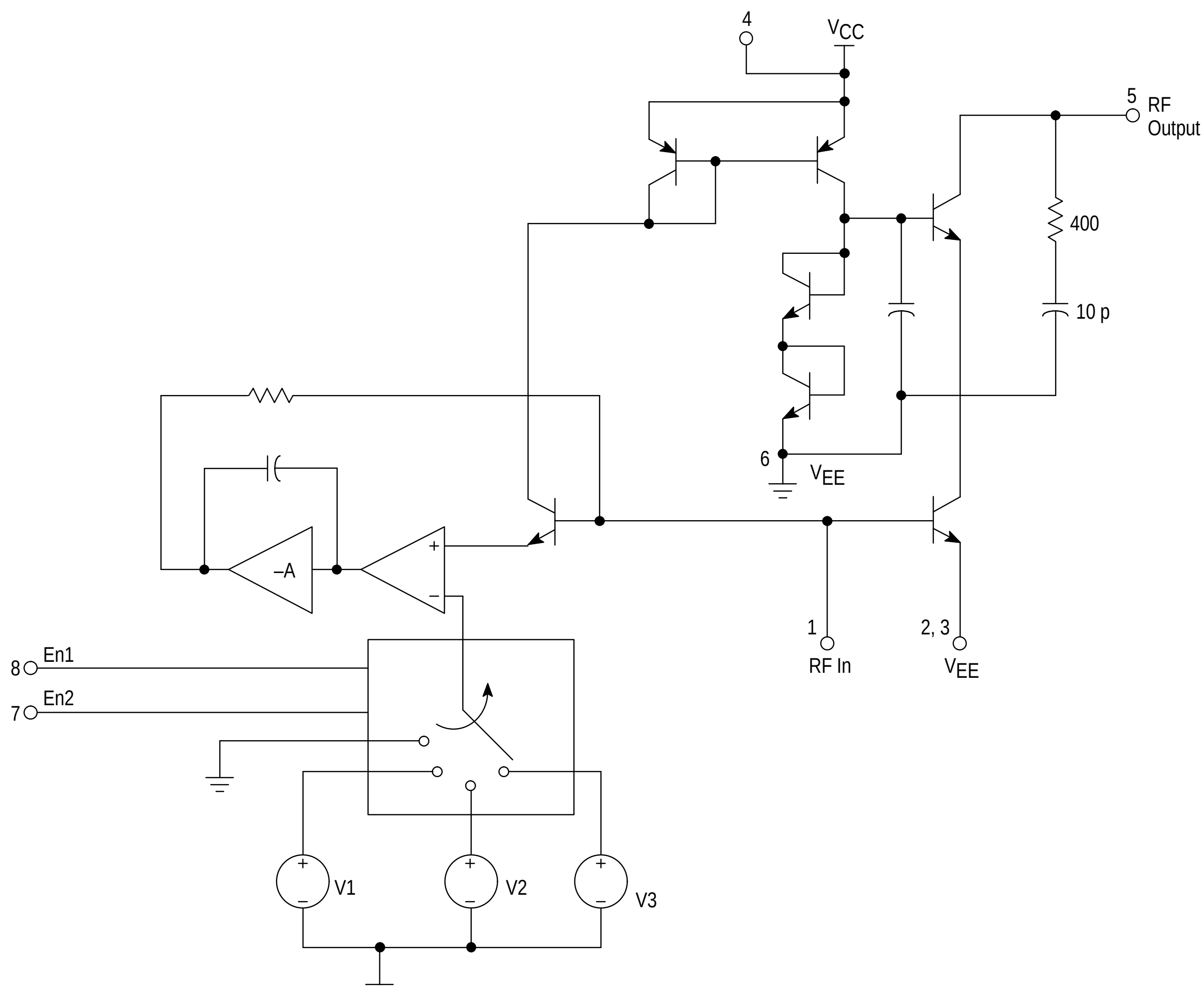
LNA

The LNA is a unique and patented cascode amplifier with digitally (2 bit) programmable bias (see Internal Circuit Schematic). Typical gain of the LNA is 17 dB for minimum noise figure of 1.4 dB at 900 MHz.

Programmable Bias/Enable Circuit

This unique circuit allows for 3 bias levels and a standby mode in which the LNA can be externally biased as desired.

Figure 1. MC13144 Internal Circuit*



NOTE: * The MC13144 uses a unique and patent pending circuit topology.

APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The PC board layout accommodates all SMT components on the circuit side (see Circuit Side Component Placement View).

Component Selection

The evaluation PC board is laid out for the 4DFA (2 pole SMD Type) and 4DFB (3 pole SMD Type) filters which are available for applications in Cellular and GSM, GPS (1.2 to 1.5 GHz), DECT, PHS and PCS (1.8 to 2.0 GHz) and ISM Bands (902 to 928 MHz and 2.4 to 2.5 GHz). In the 926.5 MHz Application Circuit, a ceramic deielectric filter is used (Toko part # 4DFA–926A10).

LNA Input/Output

The LNA input impedance is the base of a common emitter cascode amplifier. The LNA output is the collector of the cascode stage and it is loaded with a series resistor of 400 Ω and a capacitor of 10 pF to provide stability.

Digitally Programmable Bias/Enable

The LNA is enabled by a 2 bit (En1 and En2) programmable bias circuit. The internal circuit shows the comparator circuit which programs the internal regulator. The logic table below shows the bias and typical performance.

f = 900 mHz

I_{CC}/Gain	En2 Low	En2 High
En1 Low	0 mA/–22 dB	1.2 mA/9.2 dB
En1 High	3.4 mA/13 dB	9.4 mA/17 dB

f = 1900 mHz

I_{CC}/Gain	En2 Low	En2 High
En1 Low	0 mA/–22 dB	1.2 mA/7.5 dB
En1 High	3.4 mA/10 dB	8.2 mA/13 dB

Input/Output Matching

A typical application at 900 MHz yields 17 dB gain and 1.4 dB noise figure. In this circuit a series inductor of 5.6 nH is used to match the input and a shunt inductor of 8.2 nH which also serves as an RFC and a series capacitor of 0.9 p is used to match the LNA output to 50 Ω load impedance.

It may be desirable to use a RF ceramic or SAW filter after the LNA when driving a mixer to provide image frequency rejection. The image filter is selected based on cost, size and performance tradeoffs. Typical RF filters have 3.0 to 5.0 dB insertion loss. Interface matching between the RF input, RF filter and the mixer is shown in Application Circuit and the Component Placement View.

A typical application at 1900 MHz yields 13 dB gain and 2.7 dB noise figure. In this circuit a series inductor of 5.6 nH and a series capacitor of 1.0 pF are used to match the input and a shut inductor of 2.0 nH and a series capacitor of 2.0 pF are used to match the LNA output to 50 Ω load impedance.

Figure 2. MC13144D Application Circuit
(926.5 MHz)

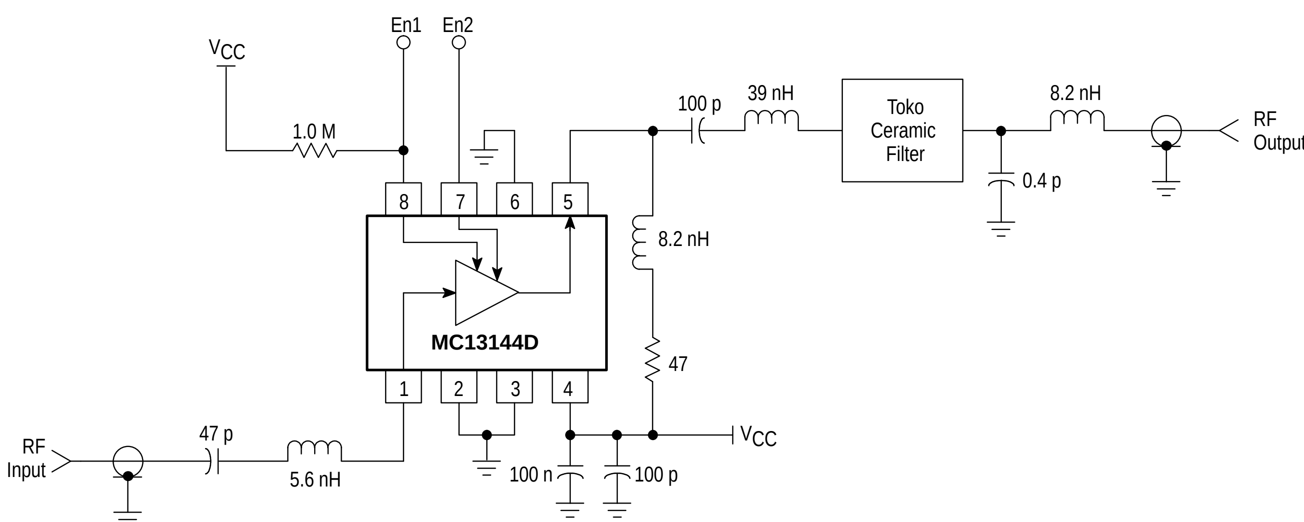


Figure 3. Typical S–Parameters VCC = 3.0 Vdc; En1 = En2 =1

Freq (MHz)	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
100	0.91	–11	4.2	143	0.00028	24	0.80	–10
125	0.92	–14	4.2	136	0.00033	71	0.79	–10
150	0.90	–16	4.2	127	0.0006	60	0.79	–11
175	0.89	–19	4.2	118	0.0011	80	0.78	–12
200	0.89	–22	4.0	108	0.0014	35	0.78	–13
250	0.88	–26	3.8	97	0.0015	39	0.78	–14
300	0.86	–32	4.1	77	0.0022	52	0.78	–17
350	0.85	–36	3.5	59	0.0017	65	.078	–19
400	0.84	–41	3.7	50	0.0024	68	0.79	–21
450	0.83	–46	3.7	26	0.0021	63	0.79	–24
500	0.81	–50	3.2	15	0.0028	56	0.79	–26
550	0.80	–55	3.5	–3.0	0.0027	51	0.80	–29
600	0.79	–59	3.1	–22	0.0038	46	0.81	–32
650	0.77	–63	3.0	–36	0.0057	30	0.82	–35
700	0.77	–67	2.8	–52	0.0067	32	0.83	–39
750	0.77	–72	2.5	–68	0.0095	26	0.83	–43
800	0.76	–77	2.2	–77	0.014	13	0.80	–49
850	0.74	–82	2.2	–86	0.019	12	0.75	–51
900	0.71	–85	2.3	–100	0.020	38	0.73	–51
950	0.69	–88	2.3	–117	0.021	55	0.74	–51
1000	0.67	–91	2.3	–132	0.020	72	0.76	–54
1100	0.67	–98	2.2	–163	0.022	87	0.76	–59
1200	0.66	–106	2.1	168	0.026	107	0.79	–65
1300	0.79	–72	1.9	136	0.030	134	0.64	–73
1400	0.64	–121	1.9	100	0.038	150	0.80	–80
1500	0.62	–128	1.9	74	0.053	170	0.81	–87
1600	0.61	–135	1.7	40	0.068	157	0.82	–96
1700	0.59	–145	1.5	7.0	0.076	120	0.81	–105
1800	0.58	–152	1.4	–24	0.092	97	0.80	–115
1900	0.54	–125	1.2	–57	0.11	59	0.74	–125
2000	0.47	–130	1.0	–79	0.093	195	0.68	–130

Figure 4. Circuit Side Component Placement View

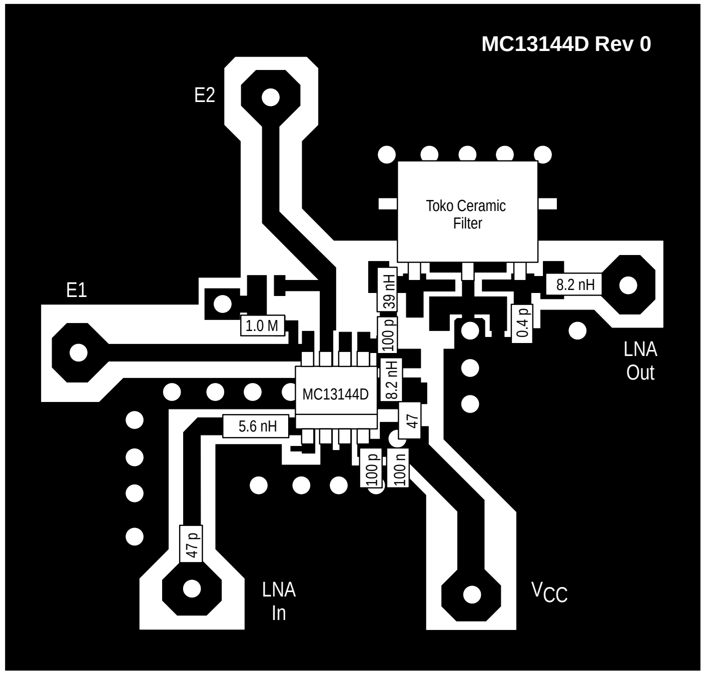
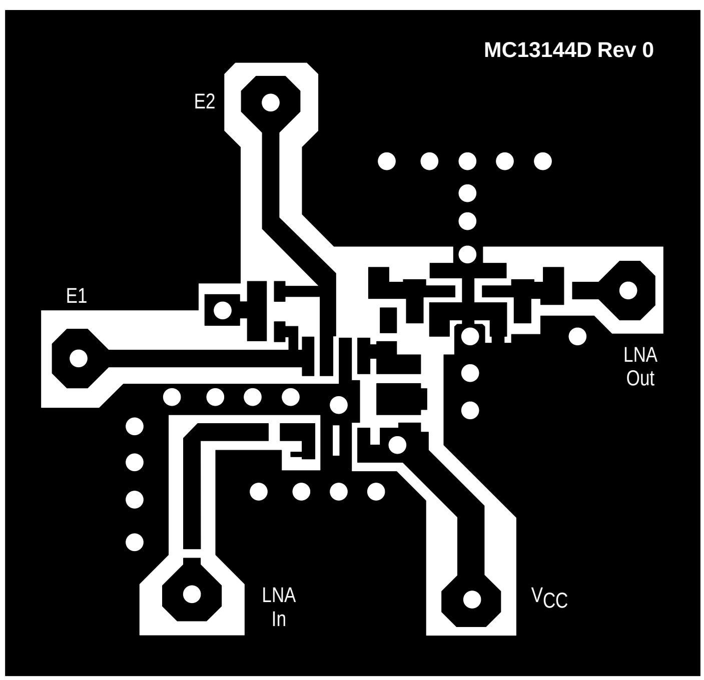
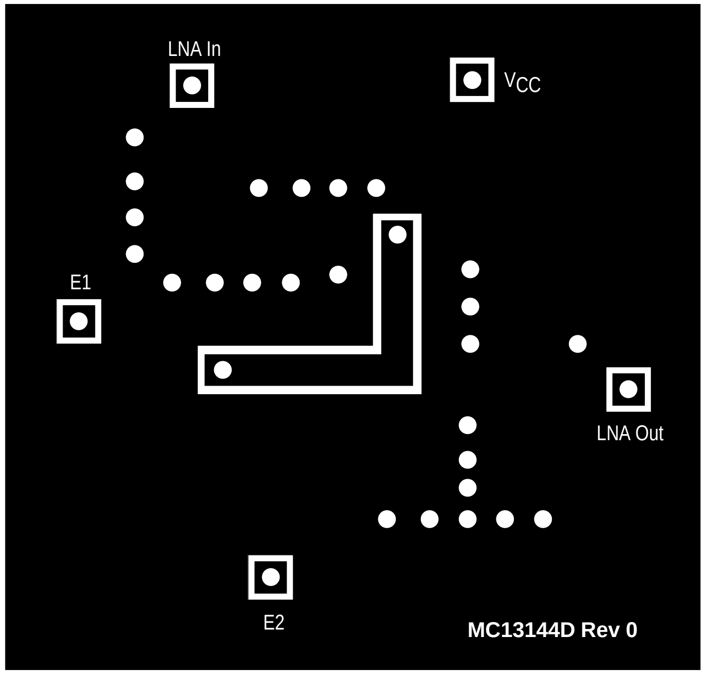


Figure 5. Circuit Side View



NOTES: Critical dimensions are 50 MIL centers lead to lead in SO–8 footprint.
Also line widths to labeled ports excluding V_{CC}, E1 and E2 are 50 MIL (0.050 inch).
FR4 PCB, 1/32 inch.

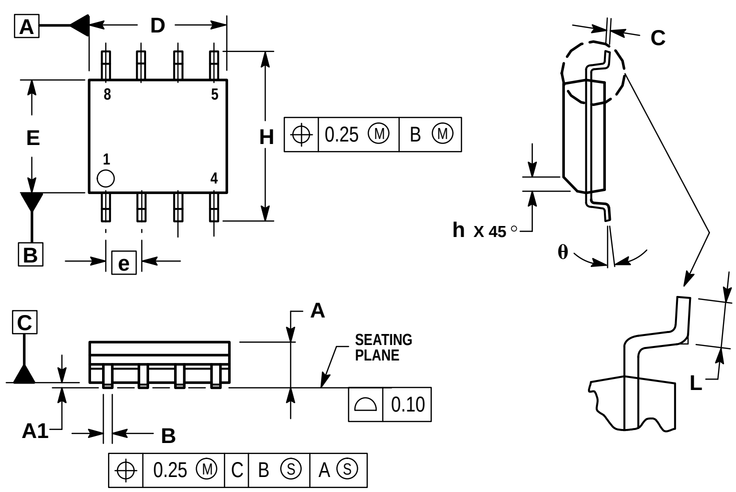
Figure 6. Ground Side View



NOTES: FR4 PCB, 1/32 inch.

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC PACKAGE
CASE 751–06
(SO–8)
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

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