Freescale Semiconductor
Advance Information

Document Number: MC13242
Rev. 0.3, 03/23/12

MC13242

Package Information
Plastic Package
Case 2258-01
MLGA-32

Ordering Information

Device	Device Marking	Package
MC13242[1]	13242	MLGA-32

[1] See Table 1 for more details

MC13242

2.4 GHz Low Power Transceiver for the IEEE® 802.15.4 Standard

1 Introduction

The MC13242 is a 2.4 GHz Industrial, Scientific, and Medical (ISM) and Medical Body Area Network (MBAN) transceiver intended for the IEEE® 802.15.4 Standard. The MC13242 device is a standalone transceiver that is normally combined with a software stack and a Freescale Kinetis MCU to implement an IEEE 802.15.4 Standard platform solution.

The MC13242 contains a complete 802.15.4 physical layer (PHY) modem designed for the IEEE® 802.15.4 Standard which supports peer-to-peer, star, and mesh networking. When combined with an appropriate microcontroller (MCU), the MC13242 provides a cost-effective solution for short-range data links and networks. Interface with the MCU is accomplished using a four wire serial peripheral interface (SPI) connection and an interrupt request output, which allows for the use of a variety of processors. The software and processor can be scaled to fit applications ranging from simple point-to-point systems, to complete ZigBee networks.

The MC13242 provides the IEEE 802.15.4 Standard PHY/MAC for use with the Freescale Kinetis family of MCUs. Freescale's software stack solutions are based on its IEEE 802.15.4 MAC and include BeeStack and BeeStack Consumer codebases for ZigBee® compliant applications.

NOTE

For more detailed applications information, refer to the MC13242 Reference Manual (RM).

1.1 Ordering information

Table 1. Orderable parts details

Device	Operating Temp Range (T_A)	Package
MC13242C	–40° to 125° C	MLGA-32
MC13242CR2	–40° to 125° C	MLGA-32 Tape and Reel

2 Features

This section provides a simplified block diagram and highlights MC13242 features.

2.1 Block diagram

Figure 1 shows a simplified block diagram of the MC13242, which is an IEEE®802.15.4 standard compatible transceiver.

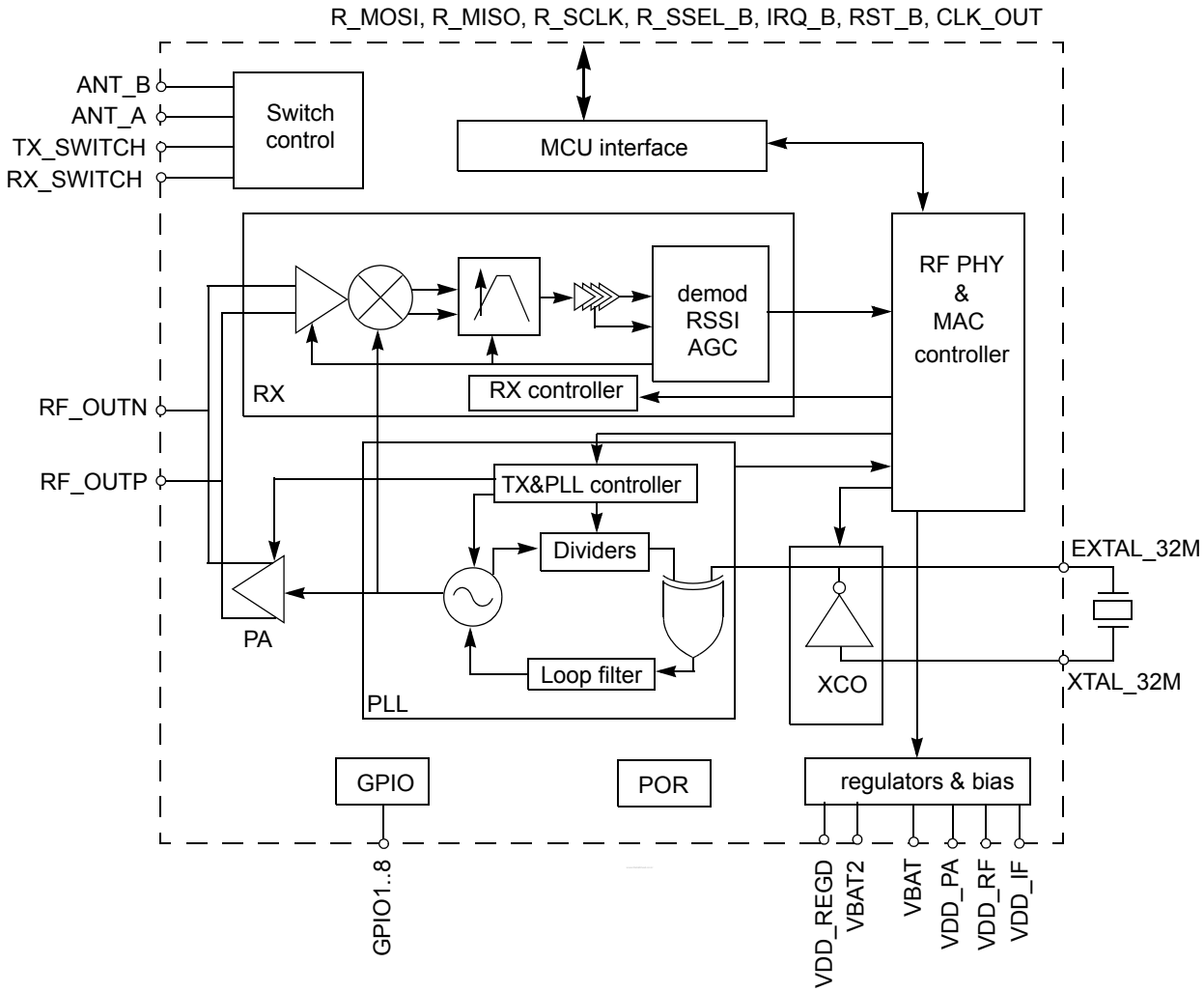


Figure 1. MC13240 simplified block diagram

When the MC13242 is used in concert with a host MCU, the interface between the devices is accomplished through a 4-wire SPI port and interrupt request line. The Media Access Control (MAC), drivers, and network and application software (as required) reside on the host processor. The transceiver / MCU interface is described in Section 6.4.1, “Serial peripheral interface (SPI)”.

2.2 Features summary

The transceiver has the following features:

- Fully compliant IEEE 802.15.4 Standard 2006 transceiver supports 250 kbps O-QPSK data in 5.0 MHz channels and full spread-spectrum encode and decode.
  - 2.4 GHz frequency band of operation (ISM).
  - 250 kbps data rate with O-QPSK modulation in 5.0 MHz channels with direct sequence spread spectrum (DSSS) encode and decode.
  - Operates on one of 16 selectable ISM channels per IEEE 802.15.4 specification.

  - Programmable output power.
  - Supports 2.36 GHz to 2.40 GHz medical band (MBAN) frequencies with IEEE 802.15.4j channel, spacing and modulation requirements.
- Small RF foot print
  - Differential input/output port used with external balun for single port operation.
  - Supports diversity antenna operation with external front end (FE).
  - Low external component count.
- Hardware acceleration for IEEE® 802.15.4 Standard
  - Complete 802.15.4 on board modem
  - IEEE 802.15.4 Standard 2006 packet processor/sequencer with receiver frame filtering
  - Advanced security module (ASM) with support for 128-bit AES encryption.
  - Random number generator
  - Support for dual PAN mode
  - Internal event timer block with four comparators to assist sequencer and provide timer capability
- 32 MHz crystal reference oscillator with on board trim capability to supplement external load capacitors
- Programmable frequency clock output (CLK_OUT) for use by MCU
- SPI command channel and interface — 4-wire SPI slave port with burst mode operation
- Interrupt request output (IRQ) — provides interrupt request capability to MCU
- Bit stream mode (BSM) to monitor packet data with synchronization clock
- 128-byte RAM data buffer to store 802.15.4 packet contents for transceiver sequences
- Eight (8) software programmable GPIOs
- Low-power operating modes with single SPI command device wake-up (SPI communication is enabled in LP mode)
- 1.8 V to 3.6 V operating voltage with on chip voltage regulators
- –40°C to +125°C operational temperature range
- RoHS compliant, 5 mm x 5 mm, 32-pin MLGA package

2.3 Software Solutions

Freescale provides a powerful software environment called the Freescale BeeKit Wireless Connectivity Toolkit. BeeKit is a comprehensive codebase of wireless networking libraries, application templates, and sample applications. The BeeKit Graphical User Interface (GUI), part of the BeeKit Wireless Connectivity Toolkit, allows users to create, modify, and update various wireless networking implementations. A wide range of software functionality is available to complement the MC13242 and these are provided as codebases within BeeKit. The following sections describe the available tools.

2.3.1 Simplified media access controller (SMAC)

The Freescale simplified media access controller (SMAC) is a simple ANSI C based code stack available as sample source code. The SMAC can be used for developing proprietary RF transceiver applications using the MC13242.

- Supports point-to-point and star network configurations
- Proprietary networks
- Source code and application examples provided

2.3.2 IEEE® 802.15.4 2006 Standard-Compliant MAC

The Freescale 802.15.4 Standard-Compliant MAC is a code stack available as object code. The 802.15.4 MAC can be used for developing MC13240 networking applications based on the full IEEE® 802.15.4 Standard that use custom Network Layer and application software.

- Supports star, mesh and cluster tree topologies
- Supports beaconed networks
- Supports GTS for low latency
- Multiple power saving modes
- AES-128 Security module
- 802.15.4 Sequence support
- 802.15.4 Receiver Frame filtering

2.3.3 SynkroRF Platform

The SynkroRF Network is a general-purpose, proprietary networking layer that sits on top of the IEEE® 802.15.4 MAC and PHY layers. It is designed for wireless personal area networks (WPANs) and conveys information over short distances among the participants in the network. It enables small, power efficient, inexpensive solutions to be implemented for a wide range of applications. Some key characteristics of an SynkroRF Network are:

- An over-the-air data rate of 250 kbps in the 2.4 GHz band
- 3 independent communication channels in the 2.4 GHz band (15, 20, and 25)
- 2 network node types, controller and controlled nodes
- Channel agility mechanism
- Low latency Tx mode automatically enabled in conditions of radio interference
- Fragmented mode transmission and reception, automatically enabled in conditions of radio interference
- Robustness and ease of use
- Essential functionality to build and support a CE network

The SynkroRF Network layer uses components from the standard HC(S)08 Freescale platform, which is also used by the Freescale's implementations of 802.15.4. MAC and ZigBee™ layers. For more details about the platform components, see the *Freescale Platform Reference Manual*.

2.3.4 BeeStack Consumer

Freescale's ZigBee RF4CE stack, called BeeStack Consumer, is a networking layer that sits on top of the IEEE® 802.15.4 MAC and PHY layers. It is designed for standards-based wireless personal area networks (WPANs) of home entertainment products and conveys information over short distances among the participants in the network. It enables small, power efficient, inexpensive solutions to be implemented for a wide range of applications. Targeted applications include DTV, set top box, A/V receivers, DVD players, security, and other consumer products.

Some key characteristics of a BeeStack Consumer network are:

- An over-the-air data rate of 250 kbps in the 2.4 GHz band
- 3 independent communication channels in the 2.4 GHz band
- 2 network node types, controller node and target node
- Channel agility mechanism
- Provides robustness and ease of use
- Includes essential functionality to build and support a CE network

The BeeStack Consumer layer uses components from the standard HCS08 Freescale platform, which is also used by the Freescale implementations of 802.15.4. MAC or ZigBee™ layers. For more details about the platform components, see the *Freescale Platform Reference Manual*.

2.3.5 ZigBee-compliant network stack

Freescale's BeeStack architecture builds on the ZigBee protocol stack. Based on the OSI Seven-Layer model, the ZigBee stack ensures inter-operability among networked devices. The physical (PHY), media access control (MAC), and network (NWK) layers create the foundation for the application (APL) layers. BeeStack defines additional services to improve the communication between layers of the protocol stack.

At the application layer, the application support layer (ASL) facilitates information exchange between the application support sub-layer (APS) and application objects. Finally, ZigBee device objects (ZDO), in addition to other manufacturer-designed applications, allow for a wide range of useful tasks applicable to home and industrial automation.

BeeStack uses the IEEE 802.15.4-compliant MAC/PHY layer that is not part of ZigBee itself. The NWK layer defines routing, network creation and configuration, and device synchronization. The application framework (AF) supports a rich array of services that define ZigBee functionality. ZigBee device objects (ZDO) implement application-level services in all nodes via profiles. A security service provider (SSP) is available to the layers that use encryption (NWK and APS); i.e., advanced encryption standard (AES) 128-bit security.

The complete Freescale BeeStack protocol stack includes the following components:

- ZigBee device objects (ZDO) and ZigBee device profile (ZDP)
- Application support sub-layer (APS)
- Application framework (AF)
- Network (NWK) layer

- Security service provider (SSP)
- IEEE 802.15.4-compliant MAC and physical (PHY) layer

3 Transceiver description and RF/modem interface

3.1 Key specifications

MC13242 meets or exceeds all IEEE 802.15.4 performance specifications applicable to 2.4 GHz ISM and MBAN (Medical Band Area Network) bands. Key specifications for MC13242 are:

- ISM band:
  - RF operating frequency: 2405 MHz to 2480 MHz (center frequency range)
  - ISM Channel numbering: Fc = 2405 + 5 (k – 11) in MHz, k = 11, 12, …, 26.
- MBAN band:
  - RF operating frequency: 2360 MHz to 2400 MHz (center frequency range)
  - MBANS channel page 9 is (2360 MHz–2390 MHz band)
  - Fc = 2363.0 + 1.0 * k in MHz for k = 0.....26
  - MBANS channel page 10 is (2390 MHz–2400 MHz band)
  - Fc = 2390.0 + 1.0 * k in MHz for k = 0.....8
- IEEE 802.15.4 Standard 2.4 GHz modulation scheme
  - Chip rate: 2000 kbps
  - Data rate: 250 kbps
  - Symbol rate: 62.5 kbps
  - Modulation: OQPSK
- Receiver sensitivity: –102 dBm, typical (@1% PER for 20 byte payload packet)
- Differential bidirectional RF input/output port with integrated transmit/receive switch
- Programmable output power from –30 dBm to +10 dBm.

3.2 RF and modem interface

3.2.1 RF interface and usage

The MC13242 RF output ports are bidirectional (diplexed between receive/transmit modes) and differential enabling interfaces with numerous off-chip devices such as a balun. When using a balun, this device provides an interface to directly connect between a single-ended antenna with MC13242 RF ports. In addition, MC13242 provides four output driver ports that can have both drive strength and slew rate configured to control external peripheral devices. These signals designated ANT_A, ANT_B, RX_SWITCH, and TX_SWITCH when enabled are switched via an internal hardware state machine. These ports provide control features for peripheral devices such as:

- Antenna diversity modules
- External PAs

- External LNAs
- T/R switched

3.2.2 Radio to MCU interface

An array of MCUs can be supported through use of dedicated I/Os that route from the 32-pin MLGA package.

The MCU interface consists of:

- SPI interface
- IRQ management
- Registers (direct and indirect access)
- Clock out feature
- 128-byte packet buffer

NOTE

MC13242 supports independent transmit, receive, or CCA/ED (energy detection) modes of operation and combinations as described in Section 3.3.4, “Clear channel assessment (CCA), energy detection (ED), and link quality indicator (LQI)”.

Figure 2 shows the interconnection of MC13242 and a generic MCU. The reference manual (RM) will provide more detailed information describing functionality, connections between the radio and MCU, etc.

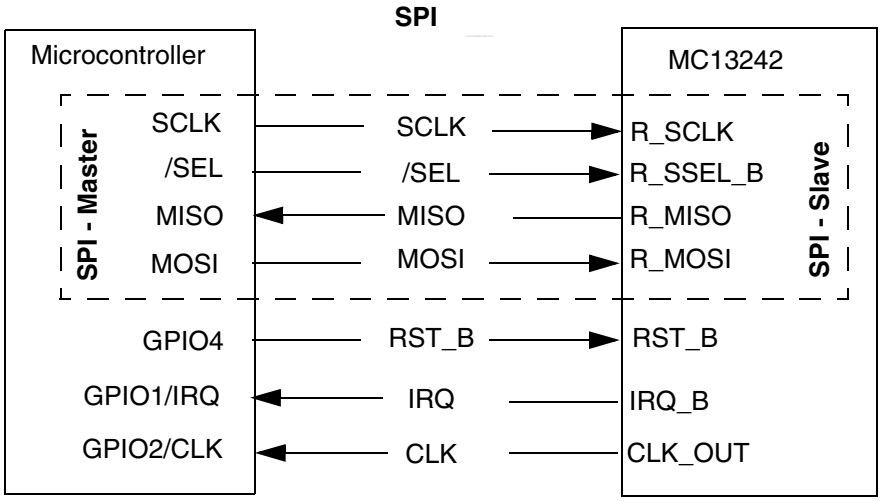


Figure 2. MCU to MC13242 block diagram

3.2.2.1 SPI interface

MCU communication with MC13242 is via a 4-wire serial peripheral interface (SPI). Exclusive access to MC13242’s register set and packet buffer is provided by the SPI. For more specific SPI interface information refer to Section 6.4.1, “Serial peripheral interface (SPI)”.

3.2.2.2 IRQ management

MC13242 has up to 14 individual sources of interrupt request to the MCU (see Table 2). These are all capable of individual control, and are logically OR-combined to drive a single, active low, interrupt request pin (IRQ_B) to the external MCU. Features supported are:

- The IRQ_B pin can be configured as actively-driven high or open-drain.
- Each interrupt source has its own interrupt status bit in MC13242's Direct Register space.
- Each interrupt can be individually controlled by an interrupt mask — The IRQ is issued when the mask is cleared to 0.
- There is also a global interrupt mask, TRCV_MSK, which can enable/disable all IRQ_B assertions by programming a single masking bit.
- All status bits use a write-1-to-clear protocol — interrupt status bits are not affected by reads.
- IRQ_B will remain asserted until all active interrupt sources are cleared or masked.

Table 2. IRQ sources

MC13242 interrupt sources
SEQIRQ
TXIRQ
RXIRQ
CCAIRQ
RXWTRMRKIRQ
FILTERFAIL_IRQ
PLL_UNLOCK_IRQ
WAKE_IRQ
PB_ERR_IRQ
AES_IRQ
TMR1IRQ
TMR2IRQ
TMR3IRQ
TMR4IRQ

Any or all of the interrupt sources, can be enabled to cause an assertion on IRQ_B.

3.2.2.3 Memory map and registers

Numerous register bits are provided to control interrupt behavior within the MC13242. Detailed information for memory map and registers is located in the MC13242 Reference Manual (RM).

3.2.2.4 Clock output feature

The CLK_OUT digital output can be enabled to drive the system clock to the MCU. This provides a highly accurate clock source based on the transceiver reference oscillator. The clock is programmable over a wide range of frequencies divided down from the reference 32 MHz (see Table 3).The CLK_OUT pin will be enabled upon POR. The frequency CLK_OUT will be determined by the state of the GPIO5/BOPT pin. If this pin is low upon POR, then the frequency will be 4 MHz (32 MHz/8). If this pin is high upon POR (upon POR GPIO5 has a pullup resistor) then the frequency will be 32.78689 kHz (32 MHz/976).

3.3 Transceiver functions

3.3.1 Receive path

The receive path has the functionality to operate in run state or operate in a low power run state (LPRS) that can be considered as a partial power down mode. The radio receiver path is based upon a near zero IF (NZIF) architecture incorporating front end amplification, one(1) mixed signal down conversion to IF that is programmably filtered, demodulated and digitally processed. The RF front end (FE) input port is differential that shares the same off chip matching network with the transmit path.

3.3.2 Transmit path

MC13242 transmits OQPSK modulation having power and channel selection adjustment per user application. After the channel of operation is determined, coarse and fine tuning is executed within the Frac-N PLL to engage signal lock. After signal lock is established, the modulated buffered signal is then routed to a multi-stage amplifier for transmission. The differential signals at the output of the PA (RFOUTP, RFOUTN) are converted as single ended (SE) signals with off chip components as required.

3.3.3 Low Power Run State (LPRS)

The MC13242 provides a unique low power run state (LPRS) in the receive mode operation. A summary of this mode of operation when selected is described below:

- Whenever a receive cycle is initiated, the receiver is not turned fully on to save current until receive energy of a preset level is detected.
- The receiver will turn fully on only when triggered by energy at a pre-determined preset level thus enabling reception of the expected frame. Afterwards, the receiver will begin operating in the full-on state that is considered to be the same as the standard receive state
- The preset level can be programmed for various RX input power levels

Use of the LPRS mode provides two distinct advantages:

- Reduced “listen” mode current — The receive current is significantly reduced while waiting for a frame. If a node is a coordinator, router, or gateway and it spends a significant percentage of its RF-active time waiting for incoming frames from clients or other devices, the net power savings can be significant.
- Reduced sensitivity as a desired effect — The LPRS mode provides different levels of reduced sensitivity. If a node operates in a densely populated area, it may be desirable to de-sensitize the

receiver such that the device does not respond to incoming frames with an energy level below the desired threshold. This could be useful for security, net efficiency, reduced noise triggering, and many other purposes.

3.3.4 Clear channel assessment (CCA), energy detection (ED), and link quality indicator (LQI)

MC13242 supports three clear channel assessment (CCA) modes of operation to include energy detection (ED) and link quality indicator (LQI). Functionality for each of these modes is provided in the sections that follow.

3.3.4.1 CCA mode 1

CCA mode 1 has two functions:

- To estimate the energy in the received baseband signal.This energy is estimated based on receiver signal strength indicator (RSSI).
- To determine whether the energy is greater than a threshold.

The estimate of the energy can also be used as the Link Quality metric. In CCA Mode 1, MC13242 warms up from Idle to Receive mode where RSSI (Receiver Signal Strength Indicator) averaging takes place right after 170µs of receiver warm-up.

3.3.4.2 CCA mode 2

CCA mode 2 detects whether there is any 802.15.4 signal transmitting at the frequency band that an 802.15.4 transmitter intends to transmit. From the definition of CCA mode 2 in the 802.15.4 standard, the requirement is to detect an 802.15.4 complied signal. Whether the detected energy is strong or not is not important for CCA mode 2.

3.3.4.3 CCA mode 3

CCA mode 3 as defined by 802.15.4 standard is implemented using a logical combination of CCA mode 1 and CCA mode 2. Specifically, CCA mode 3 operates in one of two operating modes:

- CCA mode 3 is asserted if both CCA mode 1 and CCA mode 2 are asserted.
- CCA mode 3 is asserted if either CCA mode 1 or CCA mode 2 is asserted.

This mode setting is available through a programmable register.

3.3.4.4 Energy detection (ED)

Energy detection (ED) is based on receiver signal strength indicator (RSSI) and correlator output for the 802.15.4 standard. energy detect (ED) is an average value of signal strength. The magnitude from this measurement is calculated from the digital RSSI value that is averaged over an 128 µs duration.

3.3.4.5 Link quality indicator (LQI)

Link quality indicator (LQI), is based on receiver signal strength indicator (RSSI) or correlator output for the 802.15.4 standard. In this mode, RSSI measurement is done during normal packet reception. LQI computations for MC13242 are based on either digital RSSI or correlator peak values. This setting is executed through a register bit where the final LQI value is available 64 µs after preamble is detected. If a continuous update of LQI based on RSSI throughout the packet is desired, it can be read in a separate 8-bit register by enabling continuous update in a register bit.

3.4 IEEE 802.15.4 acceleration hardware

The 802.15.4 transceiver integrates (as listed below) hardware features that reduce the software stack size, off-loads functions from the CPU, supports security and improves performance:

- Complete IEEE®802.15 modem.
- 2006 packet processor/sequencer
- Advanced security module (ASM) with support for AES-128 encryption
- Internal event timer block with four comparators to assist sequencer and provide timer capability.

3.4.1 Packet processor

The MC13242 packet processor performs sophisticated hardware filtering of the incoming received packet, to determine whether the packet is both PHY- and MAC-compliant, whether the packet is addressed to this device, and if the device is a PAN coordinator, whether a message is pending for the sending device. The packet processor greatly reduces the packet filtering burden on software, allowing software to tend to higher-layer tasks with a lower latency and smaller software footprint.

3.4.1.1 Features

- Aggressive packet filtering to enable long, uninterrupted MCU sleep periods
- Fully compliant with both 2003 and 2006 versions of the 802.15.4 wireless standard
- Supports all frame types, including reserved types
- Supports all valid 802.15.4 frame lengths
- Enables auto-Tx acknowledge frames (no MCU intervention) by parsing of frame control field and sequence number
- Supports all source and destination address modes, and also PAN ID compression
- Supports broadcast address for PAN ID and short address mode
- Supports “promiscuous” mode, to receive all packets regardless of address- and rules-checking
- Allows frame type-specific filtering (e.g., reject all but beacon frames)
- Supports SLOTTED and non-SLOTTED modes
- Includes special filtering rules for PAN coordinator devices
- Enables minimum-turnaround Tx-acknowledge frames for data-polling requests by automatically determining message-pending status
- Assists MCU in locating pending messages in its indirect queue for data-polling end devices

- Makes available to MCU detailed status of frames that fail address- or rules-checking.
- Supports Dual PAN mode, allowing the device to exist on 2 PAN's simultaneously
- Supports 2 IEEE addresses for the device
- Supports active promiscuous mode

3.4.2 Packet buffering

The packet buffer is a 128-byte random access memory (RAM) dedicated to the storage of 802.15.4 packet contents for both TX and RX sequences. For TX sequences, software stores the contents of the packet buffer starting with the frame length byte at packet buffer address 0, followed by the packet contents at the subsequent packet buffer addresses. For RX sequences the incoming packet's frame length is stored in a register, external to the packet buffer. Software will read this register to determine the number of bytes of packet buffer to read. This facilitates DMA transfer through the SPI. For receive packets, an LQI byte is stored at the byte immediately following the last byte of the packet (frame length +1). Usage of the packet buffer for RX and TX sequences is on a time-shared basis; receive packet data will overwrite the contents of the packet buffer. Software can inhibit receive-packet overwriting of the packet buffer contents by setting the PB_PROTECT bit. This will block RX packet overwriting, but will not inhibit TX content loading of the packet buffer via the SPI.

3.4.2.1 Features

- 128 byte buffer stores maximum length 802.15.4 packets
- Same buffer serves both TX and RX sequences
- The entire Packet Buffer can be uploaded or downloaded in a single SPI burst.
- Automatic address auto-incrementing for burst accesses
- Single-byte access mode supported.
- Entire packet buffer can be accessed in hibernate mode
- Under-run error interrupt supported

3.4.3 Advanced Security Module (ASM)

The ASM engine encrypts using the advanced encryption standard (AES). It can perform counter (CTR), cipher block chaining (CBC), and plain AES mode encryption. The combination of CTR and CBC modes of encryption is known as CCM mode encryption. CCM is short for counter with CBC-MAC. CCM is a generic authenticate and encrypt block cipher mode. CCM is defined for use only with 128 bit block ciphers, such as AES.

The ASM has the following features:

- CTR encryption in 11 bus clock cycles.
- CBC encryption in 11 bus clock cycles.
- AES encryption in 11 bus clock cycles.
- Encrypts 128 bits as a unit.

The ASM is designed to be loaded with data and then started with a self-clearing start bit. Sixteen 8-bit registers of a key plus sixteen 8-bit registers of a counter plus sixteen 8 bit registers of text are necessary for counter mode encryption. Cipher block chaining (CBC) mode needs only a key field and a text field programmed. Typically, only the text fields and counter fields need to be continuously written because the key field won't change.A simple block diagram of the ASM module is shown in Figure 3.

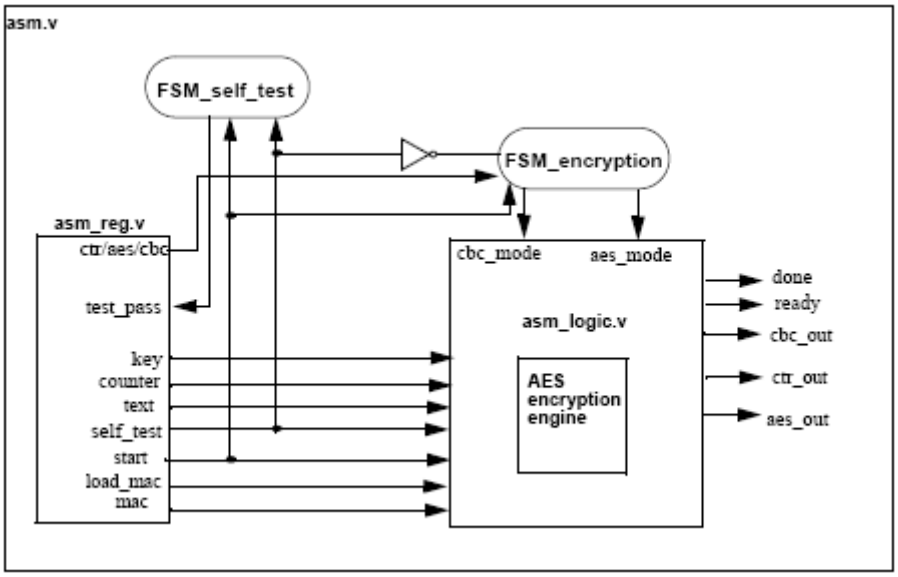


Figure 3. ASM block diagram

3.4.4 Event timer

MC13242 features a 24-bit event timer that can be used in conjunction with the sequencer to provide protocol control as well as timing interrupts. The event timer consists of a continuously running counter and 4 separate 24-bit comparators:

- The event timer counter runs at the 802.15.4 bit rate of 250 kHz (programmable).
- Each comparator has an individual interrupt request capability — the compare status is set when there is a match between the comparator and the timer counter. Each status can be enabled to generate an IRQ.
- In addition, a separate 16-bit T2PRIMECMP comparator is provided, which uses only the *lower 16 bits* of event timer, rather than a require a full 24-bit compare.

For each timer compare enable, if the bit is set, a match on the respective 24-bit compare value to the event timer, will cause the corresponding interrupt status bit to become set. If the compare enable is low, event timer matches won't cause the corresponding interrupt status bit to become set.

4 System clocks

The primary system reference frequency is a 32 MHz crystal oscillator. The crystal requirements for the oscillator and oscillator performance must support a ±40 ppm frequency accuracy to meet the IEEE® 802.15.4 Standard requirements. All system clocks are generated from this source. Features of the clock system include:

- The 32 MHz reference oscillator with onboard programmable capacitive loading that allows software tuning of frequency accuracy. Modes of operation supported are:
  - Off mode
  - RFoff mode (low power consumption)
  - RF mode (high power consumption)
  - Bypass mode
- CPU clock output as high as 32 MHz (see Table 3)

5 System and power management

MC13242 is a low power device that also supports extensive system control and power management modes to maximize battery life and provide system protection.

5.1 Modes of operation

The MC13242 modes of operation include:

- Idle mode — In this mode the XTAL is on and analog regulator disabled. The timer is “on”, registers normal operation, XTAL_out programmable, REGD on, POR on, and SPI on.
- Doze mode — In this mode the XTAL is on and VREGA disabled. The timer can either be “on or off”, registers retained, XTAL_out programmable, digital regulator on in low power mode, POR off, and SPI on.
- Low power (LP) / hibernate mode — In this mode both the XTAL and VREGA are disabled, timer is off, registers retained, XTAL_out off, digital regulator on in low power mode, POR off and SPI on.
- Reset / powerdown mode — In this mode the XTAL is off and VREGA disabled, timer is off, registers reset, XTAL_out off, digital regulator off, POR off, and SPI off.
- Run mode — In this mode the XTAL is on and VREGA on. The timer is “on”, registers normal operation, XTAL_out programmable, digital regulator on, POR on, and SPI on.

5.2 Power management

The MC13242 power management is controlled through programming the modes of operation. Different modes allow for different levels of power-down and RUN operation. These programmable modes also include features:

- Receiver modes of operation:
  - RX preamble search

— RX Preamble search sniff
— X FAD Preamble search
— RX packet decoding

- The RF section of the radio only powered-up as required to do a TX, RX, or CCA/ED operation.

6 Peripherals

The MC13242 provides a set of I/O pins useful for suppling a system clock to the MCU, controlling external RF modules/circuitry, and GPIO. In addition, there is a special option for streaming the digital packet data for external monitoring (BSM).

6.1 Clock output (CLK_OUT)

MC13242 integrates a programmable clock to source numerous frequencies for connection with various MCUs. Package pin # 16 can be used to provide this clock source as required allowing the user to make adjustments per their application requirement.

Care must be taken that the clock output signal does not “talk” or interfere with the reference oscillator or the radio. Additional functionality this feature supports is:

• 3 clock domains (XTAL, SCLK, SDM_CK).

• Built in synchronization at all clock domain crossings.

• Aggressive clock gating in the XTAL domain to minimize dynamic current consumption based on the power mode selected.

• XTAL domain can be completely gated off (hibernate mode)

• SPI communication allowed in hibernate

• Single-clock domain in scan mode

Table 3. CLK_OUT table

CLK_OUT_DIV [2:0]	CLK_OUT frequency	Comments
0	32 MHz	
1	16 MHz	
2	8 MHz	
3	4 MHz	DEFAULT if GPIO5/BOPT=0
4	2 MHz	
5	1 MHz	
6	62.5 kHz	
7	32.786 kHz	DEFAULT if GPIO5/BOPT=1

There is an enable and disable bit for CLK_OUT. When disabling, the clock output will optionally continue to run for 128 clock cycles after disablement. There will also be one (1) bit available to adjust the CLK_OUT I/O pad drive strength.

6.2 RESET_B (RST_B)

RST_B when asserted low will turn the device off by shutting down all regulators in addition to memory/registers not maintaining their prior state. When in RESET, this state is MC13242's minimum power state where the intention is for the host MCU to drive RST_B.

6.3 Bit streaming mode (BSM)

Another peripheral option is bit streaming mode that when activated allows all 802.15.4 packet data, received or transmitted, to be serialized and shifted out to external hardware for further processing. A simple development system can be crafted to consume the BSM outputs and generate packet trace data for all 802.15.4 traffic appearing on a network within the range of the MC13242 device allowing for PAN-level monitoring and debugging.

BSM uses a simple synchronous 3-wire interface consisting of BSM_CLK, BSM_DATA, and BSM_FRAME outputs. Packet data is shifted out serially at the 802.15.4 bit rate (250 kHz). Signaling is provided on BSM_FRAME to indicate start-of-packet and end-of-packet and to discriminate between TX and RX packet types. BSM_DATA and BSM_FRAME are synchronous to BSM_CLK. BSM_DATA and BSM_FRAME are shifted out on the falling BSM_CLK and intended to be captured on rising BSM_CLK.

A single shift register control bit activates or deactivates BSM. Aside from controlling this bit, BSM requires no software support while the mode is engaged. BSM outputs are multiplexed with GPIO, so that the pins are available for general-purpose use when BSM is disabled. BSM does not interfere with packet processing or transmit data handling in any way, it is merely a monitoring tool. BSM when engaged will not measurably increase current consumption because the hardware (including the external I/O) operates at the 250 kHz rate.

6.4 General-purpose input output (GPIO)

MC13242 supports 8 GPIO pins where all I/O pins will have the same supply voltage, which depending on the battery can vary from 1.8 V up to 3.6 V. When a die pin is configured as a general-purpose output or for peripheral use, there will be specific settings required per use case. Pin configuration will be executed by software to adjust input/output direction and drive strength, capability. When a die pin is configured as a general-purpose input or for peripheral use, software (see Table 4) can enable a pull-up or pull-down device. Immediately after reset, all pins are configured as high-impedance general-purpose inputs with "internal pull-up or pull-down devices enabled".

Features for these pins include:

- Programmable output drive strength
- Programmable output slew rate
- Hi-Z mode
- Programmable as outputs or inputs (default)
- Pins shared with BSM mode outputs

Table 4. Pin configuration summary

Pin function configuration	Details	Tolerance			Units
		Min.	Typ.	Max.	
I/O buffer full drive mode[1]	Source or sink	—	±10	—	mA
I/O buffer partial drive mode[2]	Source or sink	—	±2	—	mA
I/O buffer high impedance[3]	Off state	—	—	10	nA
No slew, full drive	Rise and fall time[4]	2	4	6	ns
No slew, partial drive	Rise and fall time	2	4	6	ns
Slew, full drive	Rise and fall time	6	12	24	ns
Slew, partial drive	Rise and fall time	6	12	24	ns
Propagation delay[5], no slew	Full drive[6]	—	—	11	ns
Propagation delay, no slew	Partial drive[7]	—	—	11	ns
Propagation delay, slew	Full drive	—	—	50	ns
Propagation delay, slew	Partial drive	—	—	50	ns

1 For this drive condition, the output voltage will not deviate more than 0.5 V from the rail reference VOH or VOL.

2 For this drive condition, the output voltage will not deviate more than 0.5 V from the rail reference VOH or VOL.

3 Leakage current applies for the full range of possible input voltage conditions.

4 Rise and fall time values in reference to 20% and 80%

5 Propagation Delay measured from/to 50% voltage point.

6 Full drive values provided are in reference to a 75 pF load.

7 Partial drive values provided are in reference to a 15 pF load.

6.4.1 Serial peripheral interface (SPI)

MC13242's SPI interface allows an MCU to communicate with MC13242's register set and packet buffer. The SPI is a slave-only interface; the MCU must drive R_SSEL_B, R_SCLK and R_MOSI. Write and read access to both direct and indirect registers is supported, and transfer length can be single-byte, or bursts of unlimited length. Write and read access to the Packet buffer can also be single-byte, or a burst mode of unlimited length. The SPI interface is asynchronous to the rest of the IC. No relationship between R_SCLK and MC13242's internal oscillator is assumed. And no relationship between R_SCLK and the CLK_OUT pin is assumed. All synchronization of the SPI interface to the IC takes place inside the SPI module. SPI synchronization takes place in both directions: SPI-to-IC (register writes), and IC-to-SPI (register reads). The SPI is capable of operation in all power modes, except Reset. Operation in hibernate mode allows most MC13242 registers and the complete packet buffer to be accessed in the lowest-power operating state enabling minimal power consumption, especially during the register-initialization phase of the IC. The SPI design features a compact, single-byte control word, reducing SPI access latency to a minimum. Most SPI access types require only a single-byte control word, with the address embedded in the control word. During control word transfer (the first byte of any SPI access), the contents of the IRQSTS1 register (MC13242's highest-priority status register) are always shifted out, so that the MCU gets access to IRQSTS1, with the minimum possible latency, on every SPI access.

6.4.1.1 Features

- 4-wire industry standard interface, supported by all MCUs
- SPI R_SCLK maximum frequency 16 MHz (for SPI write accesses).
- SPI R_SCLK maximum frequency 9 MHz (for SPI read accesses).
- Write and read access to all Coconino registers (direct and indirect)
- Write and read access to packet buffer
- SPI accesses can be single-byte or burst.
- Automatic address auto-incrementing for burst accesses
- The entire packet buffer can be uploaded or downloaded in a single SPI burst.
- Entire packet buffer, and most registers, can be accessed in hibernate mode
- Built-in synchronization inside the SPI module to/from the rest of the IC.
- R_MISO can be tristated when SPI inactive, enabling multi-slave configurations

6.4.2 Antenna diversity

To improve the reliability of RF connectivity to long range applications, the antenna diversity feature is supported without using the MCU through use of four dedicated control pins (package pins 23, 24, 25, and 26) by direct register antenna selection. The digital regulator supplies bias to analog switches that can be programmed to sink and source current or operate in a high impedance mode.

Fast antenna diversity (FAD) mode supports this radio feature and, when enabled, will allow the choice of selection between two antennas during the preamble phase. By continually monitoring the received signal, the FAD block will select the first antenna on which the received signal has a correlation factor above a predefined progammable threshold. The FAD accomplishes the antenna selection by sequentially switching between the two antennas testing for the presence of a suitably strong signals/symbols where the first antenna to reach this condition is then selected for the reception of the packet.

The first antenna is monitored for a period equal to 1 symbol, t_s = 16 µs, then antenna monitoring is switched to the second antenna, t_a = 8 µs. The period t_a is required to allow for the external module control circuitry to turn on/off to select the antenna. $t_s + t_a$ = 24 µs that will allow enough time to test both antennas within the first 4 preamble symbols, $t_{fad} = 3 \times t_a + 2 \times t_s$ = 56 µs, thus $t_{fad} < 4 \times t_s < 64$ µs. Operationally, FAD will continue to switch between the two antennas until one is found that has a sufficiently strong detected signal. FAD's operation covers less than four s0 symbols before the antenna that is selected allowing the symbol demodulator to detect at least four s0 symbols before declaring "Preamble Detect".

7 Pin assignment and connections

7.1 Package pin designations

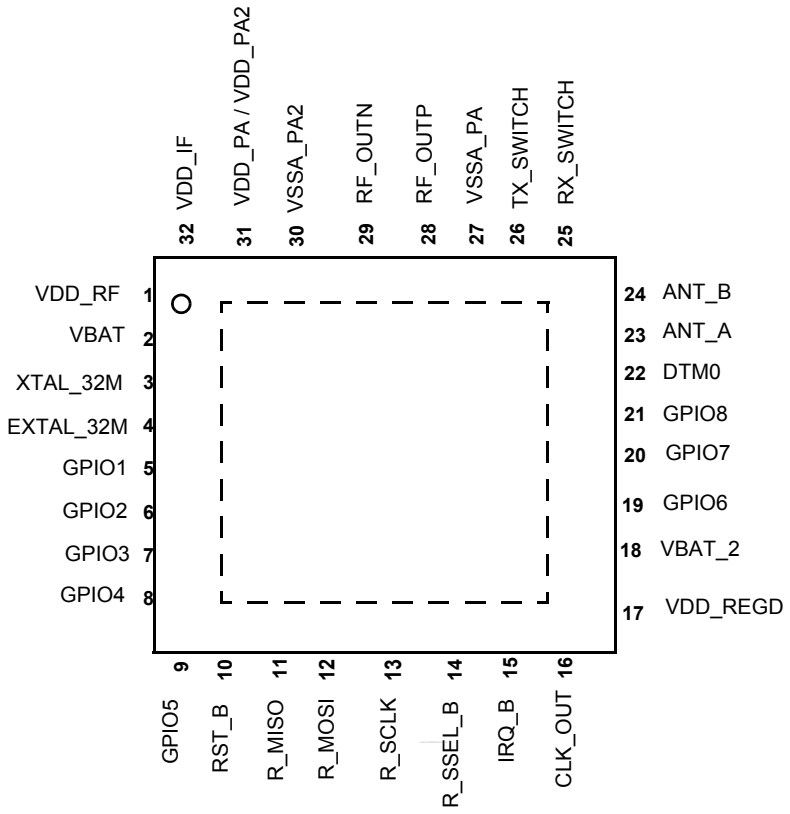


Figure 4. MC13242 package pin assignment

7.2 Pin definitions

Table 5 details the MC13242 pin assignment functionality.

Table 5. Pin function description

Pin number	Pin name	Type	Primary function	Secondary function	Description
1	VDD_RF	Analog Power Input	Analog Voltage		Analog 1.8 Vdc Input
2	VBAT	Power Input	Battery Voltage		Connect to system VDD supply
3	XTAL_32M	Analog Output	RF		32 MHz reference oscillator output
4	EXTAL_32M	Analog Input	RF		32 MHz references oscillator input
5	GPIO1	Digital Input/Output	General-Purpose IO		
6	GPIO2	Digital Input/Output	General-Purpose IO		
7	GPIO3	Digital Input/Output	General-Purpose IO	BSM_FRAME	Bit stream mode frame output
8	GPIO4	Digital Input/Output	General-Purpose IO	BSM_DATA	Bit stream mode data
9	GPIO5	Digital Input/Output	General-Purpose IO	BSM_CLK/BOPT	Bit stream mode clock / CLK_OUT default state select
10	RST_B	Digital Input/Output	Digital		Device asynchronous hardware reset. Active low.
11	R_MISO	Digital Input/Output	Digital		SPI MISO
12	R_MOSI	Digital Input/Output	Digital		SPI MOSI
13	R_SCLK	Digital Input/Output	Digital		SPI clock
14	R_SSEL_B	Digital Input/Output	Digital		SPI slave select
15	IRQ_B	Digital Input/Output	Digital		Interrupt command signal
16	CLK_OUT	Digital Output	RF		Programmable clock source
17	VDD_REGD	Digital Power Input	Digital Voltage		Digital 1.8 Vdc input
18	VBAT2	Power Input	Battery Voltage		Connect to system VDDint
19	GPIO6	Digital Input/Output	General-Purpose IO		
20	GPIO7	Digital Input/Output	General-Purpose IO		
21	GPIO8	Digital Input/Output	General-Purpose IO		
22	DTM0	Digital Input/Output	Digital Test		Digital test mux input/output
23	ANT_A	Digital Input/Output	Antenna Diversity		Programmable sink and source current output with selectable high impedance state.
24	ANT_B	Digital Input/Output	Antenna Diversity		Programmable sink and source current output with selectable high impedance state.
25	RX_SWITCH	Digital Input/Output	Control Switch		Programmable sink and source current output with selectable high impedance state.
26	TX_SWITCH	Digital Input/Output	Control Switch		Programmable sink and source current output with selectable high impedance state.

Table 5. Pin function description (continued)

Pin number	Pin name	Type	Primary function	Secondary function	Description
27	VSSA_PA	Power Input	Gnd		RF ground
28	RF_OUTP	RFInput/Output	RF		Bidirectional RF input/output positive
29	RF_OUTN	RFInput/Output	RF		Bidirectional RF input/output negative
30	VSSA_PA2	Power Input	Gnd		RFground
31	VDD_PA / VDD_PA2	Analog Power Input	Analog Voltage		Analog 1.8 Vdc input
32	VDD_IF	Analog Power Input	Analog Voltage		Analog 1.8 Vdc input

8 Functional description

The following sections provide a detailed description of the MC13242 functionality including the operating modes and Serial Peripheral Interface (SPI).

8.1 MC13242 operating modes

The MC13242 has 6 operating modes:

- Reset / power down
- Low power (LP) / hibernate
- Doze (low power with reference oscillator active)
- Idle
- Receive
- Transmit

Table 6 lists and describes these modes.

Table 6. MC13242 mode definitions and transition times

Mode	Definition	Current consumption[1]	Transition time to or from idle
Reset / powerdown	All IC functions off, leakage only. $\overline{\text{RST}}$ asserted.	< 30 nA	TBD
Low power / hibernate	Crystal reference oscillator off. (SPI is functional.)	< 1 μA	TBD
Doze	Crystal reference oscillator on but CLK_OUT output available only if selected.	600 uμA (no clockout)	TBD
Idle	Crystal reference oscillator on with CLK_OUT output available.	700 μA (no clockout)	TBD
Receive	Crystal reference oscillator on. Receiver on.	15 mA [2]	TBD
Transmit	Crystal reference oscillator on. Transmitter on.	15 mA [3]	TBD

1 Conditions: VBAT and VBAT_2 = 2.7 V, nominal process @ 25°C

2 Signal sensitivity = –102 dBm

3 RF output = 0 dBm

8.2 Serial peripheral interface (SPI)

The host microcontroller directs the MC13242, checks its status, and reads/writes data to the device through the 4-wire SPI port. The transceiver operates as a SPI slave device only. A transaction between the host and the MC13242 occurs as multiple 8-bit bursts on the SPI. The SPI signals are:

- Slave select (R_SSEL_B) — A transaction on the SPI port is framed by the active low R_SSEL_B input signal.

- SPI clock (R_SCLK) — The host drives the SPICLK input to the MC13242. Data is clocked into the master or slave on the leading (rising) edge of the return-to-zero SPICLK and data out changes state on the trailing (falling) edge of SPICLK.

NOTE

For Freescale microcontrollers, the SPI clock format is the clock phase control bit CPHA=0 and the clock polarity control bit CPOL=0.

- Master out/slave in (MOSI) — Incoming data from the host is presented on the MOSI input.
- Master in/slave out (MISO) — The MC13242 presents data to the master on the MISO output.

The SPI interface is capable of operating with either the crystal oscillator ON (synchronous mode), or OFF (asynchronous mode; i.e., hibernate).

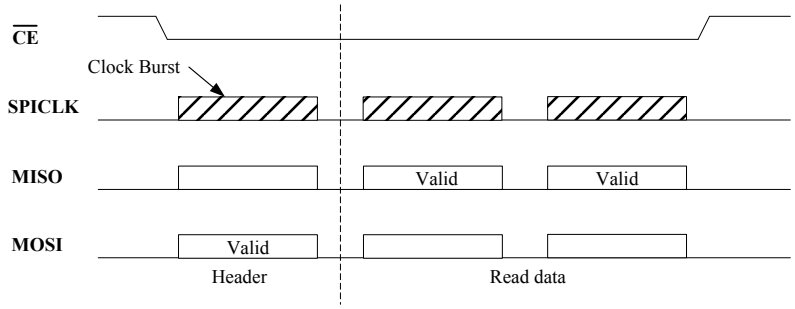


Figure 5. SPI read transaction diagram

8.2.1 SPI transfer protocol

Coconino's SPI is a slave-only interface, and follows a CPHA=0 and CPOL=0 protocol. Taken together, CPHA and CPOL determine the clock polarity and clock edge used to transfer data between the SPI master and slave, in both communication directions. CPHA=0 (clock phase) indicates that data is captured on the leading edge of SCK and changed on the following edge. CPOL=0 (clock polarity) indicates that the inactive state value of R_SCLK is low. All data is transferred MSB-first. The following diagram depicts the transfer protocol of the Coconino SPI.

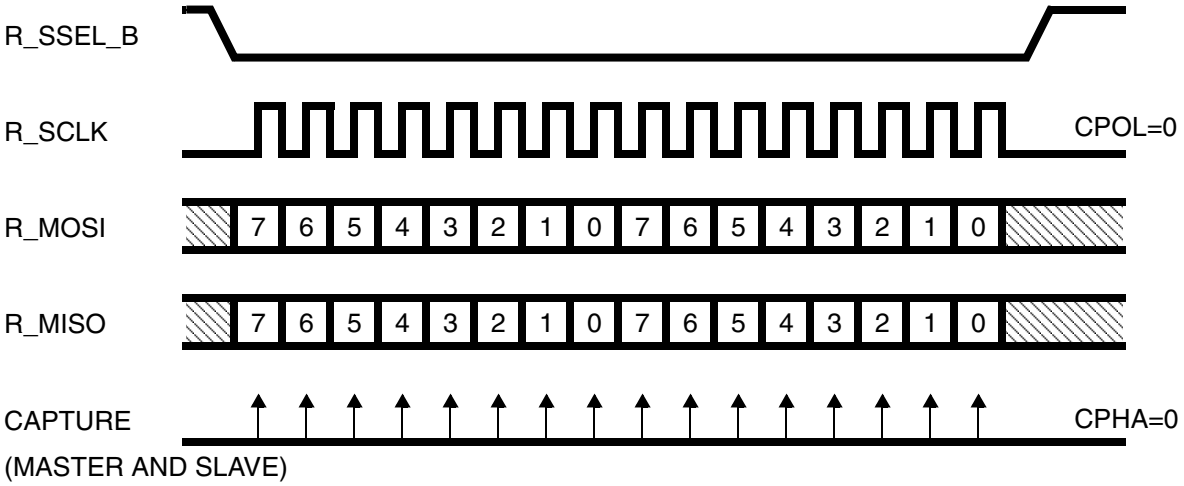


Figure 6. SPI transfer protocol

8.2.2 SPI control word

Every SPI transaction begins with one single-byte control word. The control word consists of the address, direction (write or read), transaction target (register or packet buffer), and for the packet buffer, the access mode (burst or byte). For most transactions, data transfer follows immediately after the control word. However, for indirect access register transactions, and for packet buffer byte-mode transactions, an additional address byte follows the control word, before data transfer begins. Bit 7 of the control word selects the transfer direction (1=READ, 0=WRITE). Bit 6 selects the transfer target (1=PACKET BUFFER, 0=REGISTER). For register accesses, the remaining bits select the register address. For packet buffer access, bit 5 selects the access mode (1=BYTE, 0=BURST). For packet buffer access, the remaining bits in the control word are reserved and ignored by Coconino. Details and examples of control word usage appear in the following sections. The following table depicts an overview of the control word.

Table 7. Contol word overview

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access Mode	Access Type
1	0	Register address [5:0]						Register access	Read
0	0	Register address [5:0]							Write
1	1	0	Reserved					Packet buffer burst access	Read
0	1	0	Reserved						Write
1	1	1	Reserved					Packet bugger byte access	Read
0	1	1	Reserved						Write

9 Electrical characteristics

9.1 Maximum ratings

Table 8. Maximum ratings

Requirement	Description	Symbol	Rating level	Unit
Power Supply Voltage		VBAT, VBAT2	–0.3 to 3.6	Vdc
Digital Input Voltage		Vin	–0.3 to (VDDINT + 0.3)	Vdc
RF Input Power		Pmax	+10	dBm
ESD[1]	Human Body Model	HBM	±2000	Vdc
	Machine Model	MM	±200	Vdc
	Charged Device Model	CDM	±750	Vdc
EMC[2]	Power Electro-Static Discharge / Direct Contact	PESD	No damage / latch up to ±4000	Vdc
			No soft failure / reset to ±1000	
	Power Electro-Static Discharge / Indirect Contact		No damage / latch up to ±6000	Vdc
			No soft failure / reset to ±1000	
	Langer IC / EFT / P201	EFT (Electro Magnetic Fast Transient)	No damage / latch up to ±5	Vdc
			No soft failure / reset to ±5	
	Langer IC / EFT / P201		No damage / latch up to ±300	Vdc
			No soft failure / reset to ±150	
Junction Temperature		T_J	+150	°C
Storage Temperature Range		T_{stg}	–65 to +165	°C

NOTE

Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the electrical characteristics or recommended operating conditions tables.

1 Electrostatic discharge on all device pads meet this requirement

2 Electromagnetic compatibility for this product is low stress rating level

9.2 Recommended operating conditions

Table 9. Recommended operating conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (V_{BATT} = VDD_{INT})	V_{BATT}, VDD_{INT}	1.8	2.7	3.6	Vdc
Input Frequency	fin	2.360	—	2.480	GHz
Ambient Temperature Range	TA	–40	25	125	°C
Logic Input Voltage Low	VIL	0	—	30% VDDINT	V
Logic Input Voltage High	VIH	70% VDDINT	—	VDDINT	V
SPI Clock Rate	f_{SPI}	—	—	16.0	MHz
RF Input Power	Pmax	—	—	10	dBm
Crystal Reference Oscillator Frequency (±40 ppm over operating conditions to meet the 802.15.4 Standard.)	fref	32 MHz only			

9.3 DC electrical characteristics

Table 10. DC electrical characteristics
(VBATT, VDDINT = 2.7 V, T_A=25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Current (VBATT + VDDINT)					
Reset / power down[1]	$I_{leakage}$	—	<30	—	nA
Hibernate[1]	I_{CCH}	—	<1	—	µA
Doze (No CLK_OUT)	I_{CCD}	—	600	—	µA
Idle (No CLK_OUT)	I_{CCI}	—	700	—	µA
Transmit mode (0 dBm nominal output power)	I_{CCT}	—	15	18	mA
Receive mode	I_{CCR}	—	15	18	mA
Input current (VIN = 0 V or VDDINT) (All digital inputs)	IIN	—	—	±1	µA
Input low voltage (all digital inputs)	VIL	0	—	30% VDDINT	V
Input high voltage (all digital inputs)	VIH	70% VDDINT	—	VDDINT	V
Output high voltage (IOH = -1 mA) (all digital outputs)	VOH	80% VDDINT	—	VDDINT	V
Output low voltage (IOL = 1 mA) (all digital outputs)	VOL	0	—	20% VDDINT	V

[1] To attain specified low power current, all GPIO and other digital IO must be handled properly.

9.4 AC electrical characteristics

Table 11. Receiver AC electrical characteristics
(VBATT, VDDINT=2.7 V, T_A=25 °C, fref=32 MHz, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Sensitivity for 1% packet error rate (PER) (–40 to +125 °C)	SENSper	—	–99	–97	dBm
Sensitivity for 1% packet error rate (PER) (+25 °C)	SENSper	—	–102		dBm
Saturation (maximum input level)	SENSmax	—	+10	—	dBm
Channel rejection for dual port mode (1% PER and desired signal –82 dBm) +5 MHz (adjacent channel) –5 MHz (adjacent channel) +10 MHz (alternate channel) –10 MHz (alternate channel) >= 15 MHz		 — — — — —	 38 34 47 47 55	 — — — — —	 dB dB dB dB dB
Frequency error tolerance		—	—	200	kHz
Symbol rate error tolerance		80	—	—	ppm

Table 12. Transmitter AC electrical characteristics
(VBATT, VDDINT=2.7 V, T_A=25°C, fref=32 MHz, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power spectral density[1], absolute limit from –40°C to +125°C		–30	—	—	dBm
Power Spectral Density[2], Relative limit from –40°C to +125°C		–20	—	—	dB
Nominal output power	Pout	–0.5	0	0.5	dBm
Maximum output power		—	10	—	dBm
Error vector magnitude	EVM	—	8	13	%
Output power control range[3]		—	40	—	dB
Over the air data rate		—	250	—	kbps
2nd harmonic[4]		—	<-50	<-40	dBm
3rd harmonic [4]		—	<-50	<-40	dBm

1 [f-fc] > 3.5 MHz, average spectral power is measured in 100 kHz resolution BW.

2 For the relative limit, the reference level is the highest reference power measured within ± 1 MHz of the carrier frequency

3 Measurement is at the package pin on the output of the Tx/Rx switch. It does not degrade more than ±2 dB across temperature and an additional ±1 dB across all processes. Power adjustment will span nominally from –30 dBm to +10 dBm in 21 steps @ 2 dBm / step.

4 Measured with output power set to nominal (0 dBm) and temperature @ 25°C. If trap filter is needed must meet reference board size requirements.

9.4.1 SPI timing: R_SSEL_B to R_SCLK

The following diagram describes timing constraints that must be guaranteed by the system designer.

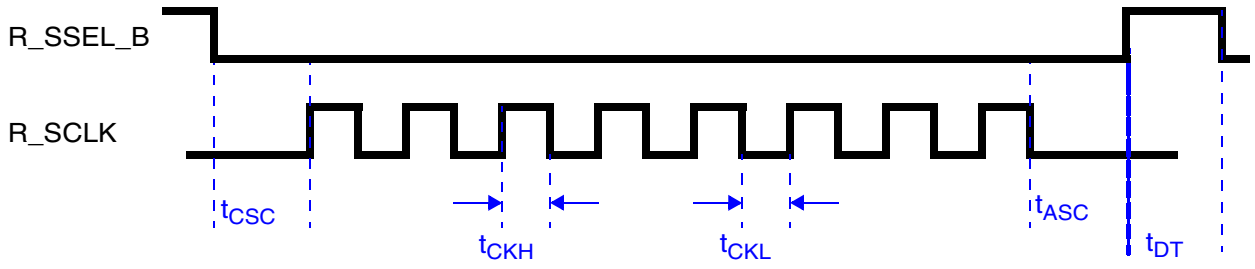


Figure 7. SPI timing: R_SSEL_B to R_SCLK

t_{CSC} (CS-to-SCK delay): 31.25 ns

t_{ASC} (After SCK delay): 31.25 ns

t_{DT} (Minimum CS idle time): 62.5 ns

t_{CKH} (Minimum R_SCLK high time): 31.25 ns (for SPI writes); 55.55 ns (for SPI reads)

t_{CKL} (Minimum R_SCLK low time): 31.25 ns (for SPI writes); 55.55 ns (for SPI reads)

NOTE

The SPI master device deasserts R_SSEL_B only on byte boundaries, and only after guaranteeing the t_{ASC} constraint shown above.

9.4.2 SPI timing: R_SCLK to R_MOSI and R_MISO

The following diagram describes timing constraints that must be guaranteed by the system designer. These constraints apply to the Master SPI (R_MOSI), and are guaranteed by the Coconino SPI (R_MISO).

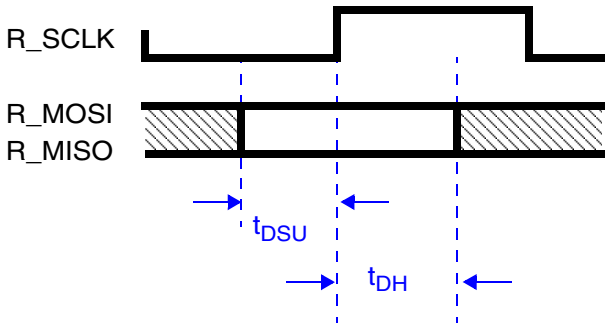


Figure 8. SPI timing: R_SCLK to R_MOSI and R_MISO

t_{DSU} (data-to-SCK setup): 10 ns

t_{DH} (SCK-to-data hold): 10 ns

Table 13. RF port impedance

Characteristic	Symbol	Typ	Unit
RFIN Pins for internal T/R switch configuration, TX mode 2.360 GHz 2.420 GHz 2.480 GHz	Zin	TBD	Ω
RFIN Pins for internal or external T/R switch configuration, RX mode 2.360 GHz 2.420 GHz 2.480 GHz	Zin	TBD	Ω
PAO Pins for external T/R switch configuration, TX mode 2.360 GHz 2.420 GHz 2.480 GHz	Zin	TBD	Ω

10 Crystal oscillator reference frequency

This section provides application specific information regarding crystal oscillator reference design and recommended crystal usage.

10.1 Crystal oscillator design considerations

The IEEE ® 802.15.4 Standard requires that frequency tolerance be kept within ±40 ppm accuracy. This means that a total offset up to 80 ppm between transmitter and receiver will still result in acceptable performance. The MC13242 transceiver provides on board crystal trim capacitors to assist in meeting this performance, while the bulk of the crystal load capacitance is external.

10.2 Crystal requirements

The suggested crystal specification for the MC13242 is shown in Table 14. A number of the stated parameters are related to desired package, desired temperature range and use of crystal capacitive load trimming.

Table 14. MC13242 crystal specifications

Parameter	Value	Unit	Condition
Frequency	32	MHz	
Frequency tolerance (cut tolerance)	±10	ppm	at 25°C
Frequency stability (temperature)	±25	ppm	Over desired temperature range
Aging[1]	±2	ppm	max
Equivalent series resistance	60	Ω	max
Load capacitance	5–9	pF	

Table 14. MC13242 crystal specifications (continued)

Parameter	Value	Unit	Condition
Shunt capacitance	<2	pF	max
Mode of oscillation			fundamental

[1] A wider aging tolerance may be acceptable if application uses trimming at production final test.

11 Reference circuit

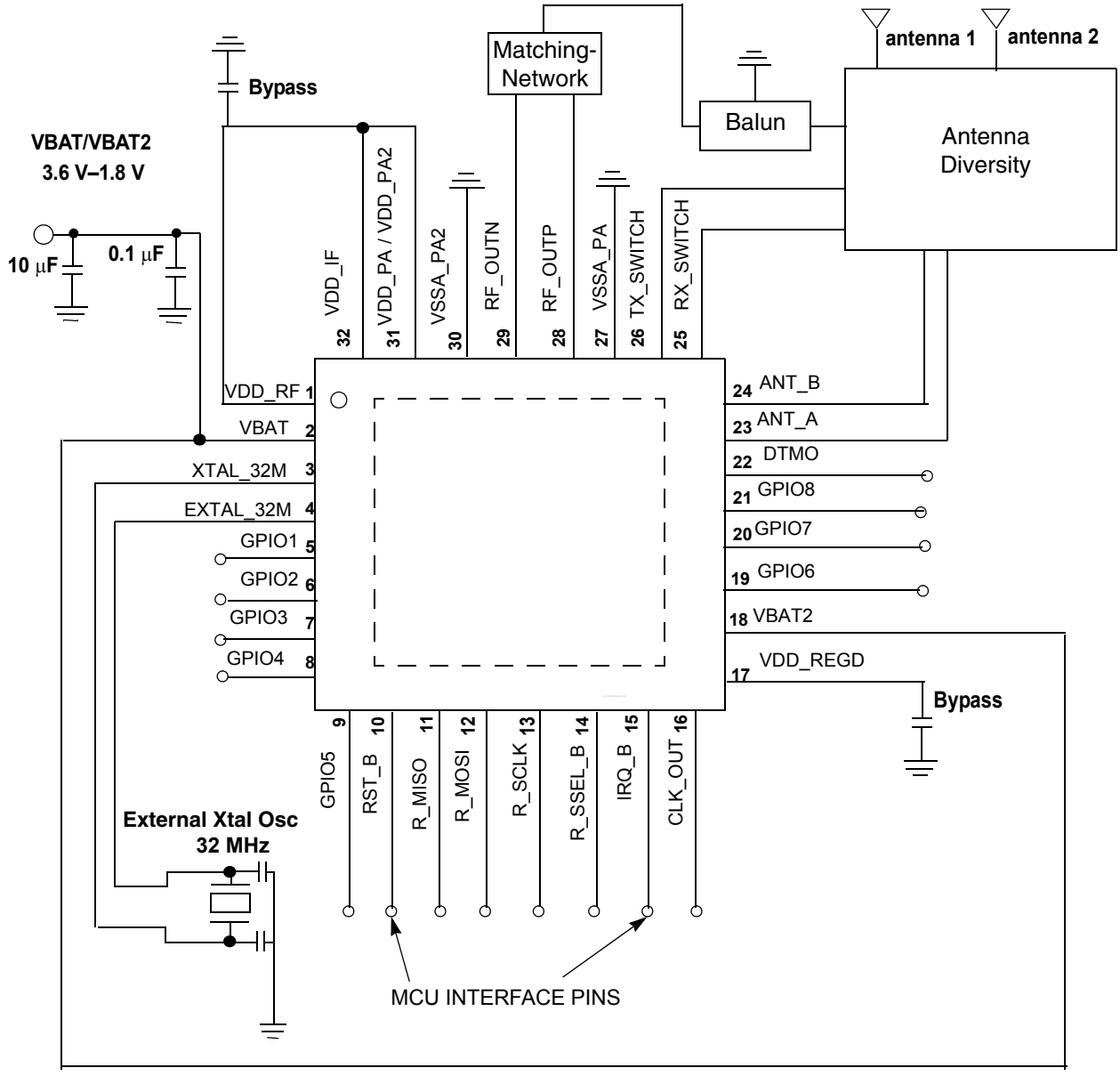


Figure 9. Use case block diagram for antenna diversity

12 Packaging information

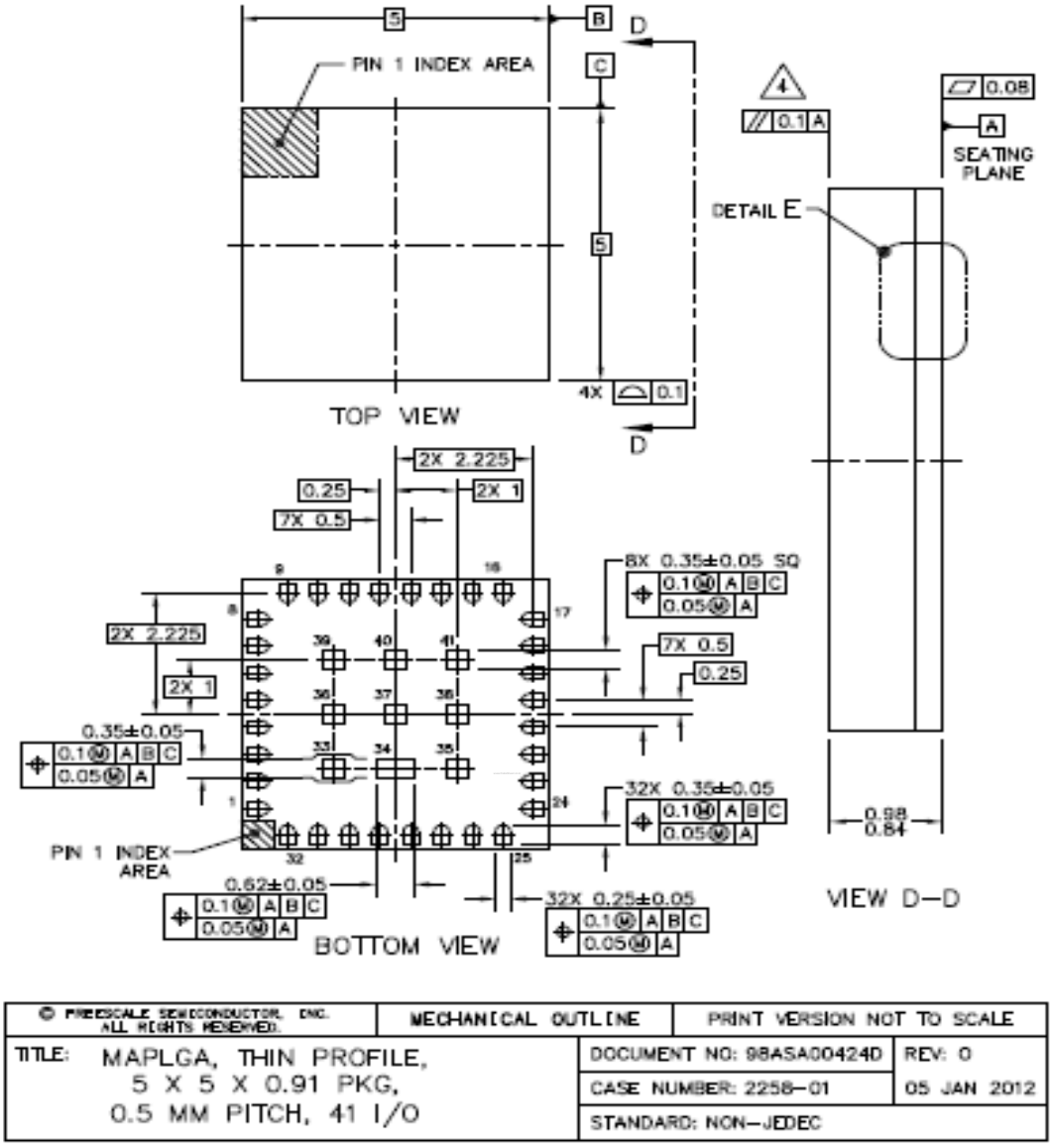
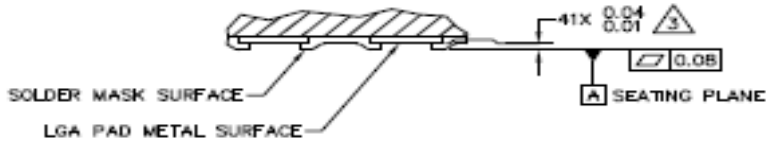


Figure 10. Outline Dimensions for MLGA-32, 5x5 mm (Case 2258-01, Rev. 0)



DETAIL E
VIEW ROTATED 90° CW

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: MAPLGA, THIN PROFILE, 5 X 5 X 0.91 PKG, 0.5 MM PITCH, 41 I/O	DOCUMENT NO: 98ASA00424D	REV: O
	CASE NUMBER: 2258–01	05 JAN 2012
	STANDARD: NON–JEDEC	

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DIMENSION APPLIES TO ALL LEADS.
4. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 11. Solder Mask /Package attach drawing

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

***For Literature Requests Only*:**
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-521-6274 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: MC13242
Rev. 0.2
03/23/12

freescale™
semiconductor