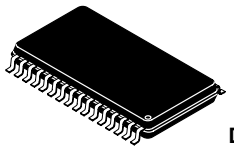
MC143120B1

Neuron® Chip Distributed Communications and Control Processor



DW SUFFIX
SOG PACKAGE
CASE 1116-0

ORDERING INFORMATION

MC143120B1DW	SOG Package

The MC143120 is a communications and control processor which enables the development of interoperable products. It provides systems designers with many features to accelerate product development for distributed sense and control applications. Services at every layer of the OSI networking model are implemented in the included LonTalk® firmware-based protocol and are easily and optionally invoked. In addition, 34 I/O models are integrated with hardware to provide simplified sense and control device interfacing.

The MC143120 is designed for maximum clock operation of 10 MHz over a temperature range of – 40 to + 85°C including EEPROM writes.

- Three 8-Bit Pipelined Processors for Concurrent Processing of Application Code and Network Packets
- 11-Pin I/O Port Programmable in 34 Modes for Fast Application Program Development
- Two 16-Bit Timer/Counters for Measuring and Generating I/O Device Waveforms
- 5-Pin Communications Port That Supports Direct Connect and Network Transceiver Interface
- 1024 Bytes of Static RAM for Buffering Network and Application Data
- 512 bytes of EEPROM with On-Chip Charge Pump for Address, Binding Data, and Application Code
- Programmable Pull-Ups on IO4 – IO7 and 20 mA Sink Current on IO0 – IO3
- Unique 48-Bit ID Number Redundantly Stored in Every Device
- 10 Kbyte ROM
- 32-Pin SOG Package
- Low Operating Current 15 mA (typical) at 10 MHz Frequency
  3 mA (typical) at 625 kHz Frequency
- Sleep Mode Operation Reduced Current Consumption (15 μA Typical)
- 0.8μ Manufacturing Process
- Redundant 48-Bit ID for Longer Reliability

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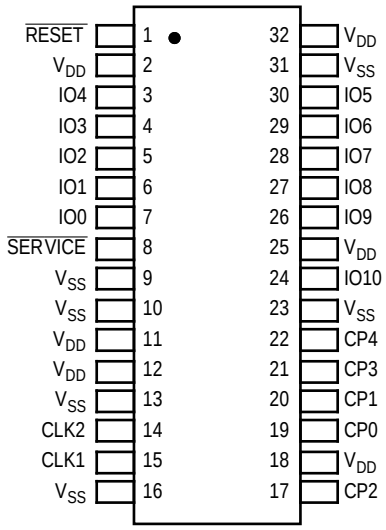
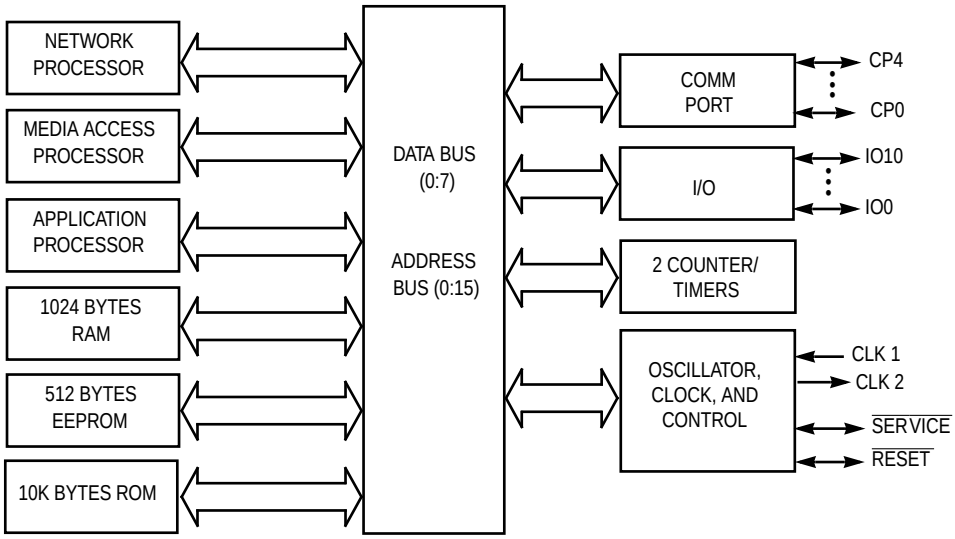
PIN ASSIGNMENT

32-LEAD SOG



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage Range (Referenced to V_{SS})	V_{DD}	– 0.3 to 7.0 V	V
Input Voltage Range (Referenced to V_{SS})	V_{in}	– 0.3 to V_{DD} + 0.3	V
Maximum Drain Current	I_{DD}	200	mA
Maximum Source Current	I_{SS}	300	mA
Maximum Power Dissipation	P_D	800	mW
Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	4.5	5.5	V
TTL Low-Level Input Voltage	V_{IL}	V_{SS}	0.8	V
TTL High-Level Input Voltage	V_{IH}	2.0	V_{DD}	V
CMOS Low-Level Input Voltage	V_{IL}	V_{SS}	0.8	V
CMOS High-Level Input Voltage	V_{IH}	V_{DD} – 0.8	V_{DD}	V
Operating Free-Air Temperature	T_A	–40*	+ 85	°C

* Writes to EEPROM are guaranteed down to –40°C for all Neuron Chip devices.

ELECTRICAL CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}				V
IO0 – IO10, D0 – D7, CP0, CP3, CP4, $\overline{\text{SERVICE}}$		—	—	0.8	
CP0, CP1 (Differential)		—	—	Programmable	
Reset				0.3 V_{DD}	
Input High Voltage	V_{IH}				V
IO0 – IO10, D0 – D7, CP0, CP3, CP4, service pin		2.0	—	—	
CP0, CP1 (Differential)		Programmable	—	—	
Reset				V_{DD} – 0.7	
Low-Level Output Voltage	V_{OL}				V
Standard Outputs (I_{OL} = 1.4 mA) (Note 1)		—	—	0.4	
High Sink (IO0 – IO3), $\overline{\text{SERVICE}}$, $\overline{\text{RESET}}$ (I_{OL}= 20 mA)		—	—	0.8	
High Sink (IO0 – IO3), $\overline{\text{SERVICE}}$, $\overline{\text{RESET}}$ (I_{OL}= 10 mA)		—	—	0.4	
Maximum Sink (CP2, CP3) (I_{OL}= 40 mA)		—	—	1.0	
Maximum Sink (CP2, CP3) (I_{OL}= 15 mA)		—	—	0.4	
High-Level Output Voltage	V_{OH}				V
Standard Outputs (I_{OH} = –1.4 mA) (Note 1)		V_{DD} – 0.4	—	—	
High Sink (IO0 – IO3), $\overline{\text{SERVICE}}$ (I_{OH} = – 1.4 mA)		V_{DD} – 0.4	—	—	
Maximum Source (CP2, CP3) (I_{OH} = – 40 mA)		V_{DD} – 1.0	—	—	
Maximum Source (CP2, CP3) (I_{OH} = – 15 mA)		V_{DD} – 0.4	—	—	
Hysteresis (Excluding CLK1, $\overline{\text{RESET}}$)	V_{hys}	175	—	—	mV
Input Current (Excluding pullups) (V_{SS} to V_{DD}) (Note 2)	I_{in}	– 10	—	10	μA
Pullup Source Current (V_{out} = 0 V, Output = High-Z) (Note 2)	I_{pu}	60	—	260	μA
Operating Mode Supply Current (Notes 3, 4, and 5)					mA
10 MHz Clock		—	14	25	
5 MHz Clock		—	7.5	13	
2.5 MHz Clock		—	4.5	7	
1.25 MHz Clock		—	3.2	4.2	
0.625 MHz Clock		—	1.6	2.5	
Sleep Mode Supply Current (Note 3,4)		—	9	100	μA

NOTES:

1. Standard outputs are A0 – A15, D0 – D7, IO4 – IO10, CP0, CP1, CP4, $\overline{\text{E}}$, and R/$\overline{\text{W}}$. ($\overline{\text{RESET}}$ is a CMOS open drain input/output. CLK2 must have ≤ 15 pF.)
2. IO4 – IO7 and $\overline{\text{SERVICE}}$ have configurable pullups. $\overline{\text{RESET}}$ has a permanent pullup.
3. Supply current measurement conditions: all outputs under no-load conditions, all inputs ≤ 0.2 V or ≥ (V_{DD} – 0.2 V), configurable pullups off, crystal oscillator clock input, differential receiver disabled. The differential receiver adds approximately 200 μA typical and 600 μA maximum when enabled. It is enabled on either of the following conditions:
   - Neuron Chip in Operating mode **and** Comm Port in Differential mode.
   - Neuron Chip in Sleep mode **and** Comm Port in Differential mode **and** Comm Port Wakeup not masked.
4. Typical values are at midpoint of voltage range and 25°C only.

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RESET TRIP POINT (V_{DD})

Part Number	Min	Typ	Max	Unit
MC143120B1	2.1	3.3	4.4	V

Table 1. Pin Descriptions

Pin Name	I/O	Pin Function	DW Suffix Pin Number
CLK1	Input	Oscillator connection or external clock input.	15
CLK2	Output	Oscillator connection. Leave open when external clock is input to CLK1. One Load.	14
$\overline{\text{RESET}}$	I/O (Built-In Configurable Pullup)	Reset pin (active low).	1
$\overline{\text{SERVICE}}$	I/O (Built-In Configurable Pullup)	Service pin. Indicator output during operation.	8
IO0 – IO3	I/O	Large current-sink capacity (20 mA). General I/O port.	7, 6, 5, 4
IO4 – IO7	I/O (Built-In Configurable Pullup)	General I/O port. One of IO4 to IO7 can be specified as No. 1 timer/counter input with IO0 as output. IO4 can be used as the No. 2 timer/counter input with IO1 as output.	3, 30, 29, 28
IO8 – IO10	I/O	General I/O port. Can be used for serial communication with other devices.	27, 26, 24
D0 – D7	I/O	Memory data bus.	N/A
R/$\overline{\text{W}}$	Output	Read/write control output port for external memory.	N/A
$\overline{\text{E}}$	Output	Control output port for external memory.	N/A
A15 – A0	Output	Address output port.	N/A
V_{DD}	Input	Power input (5 V nom). All V_{DD} pins must be connected together externally.	2, 11, 12, 18, 25, 32
V_{SS}	Input	Power input (0 V, GND). All V_{SS} pins must be connected together externally.	9, 10, 13, 16, 23, 31
CP0 – CP4	Communication Network Interface	Bidirectional port that supports communications protocols by specifying mode.	19, 20, 17, 21, 22
NC	N/A	No internal connection. Leave open.	N/A

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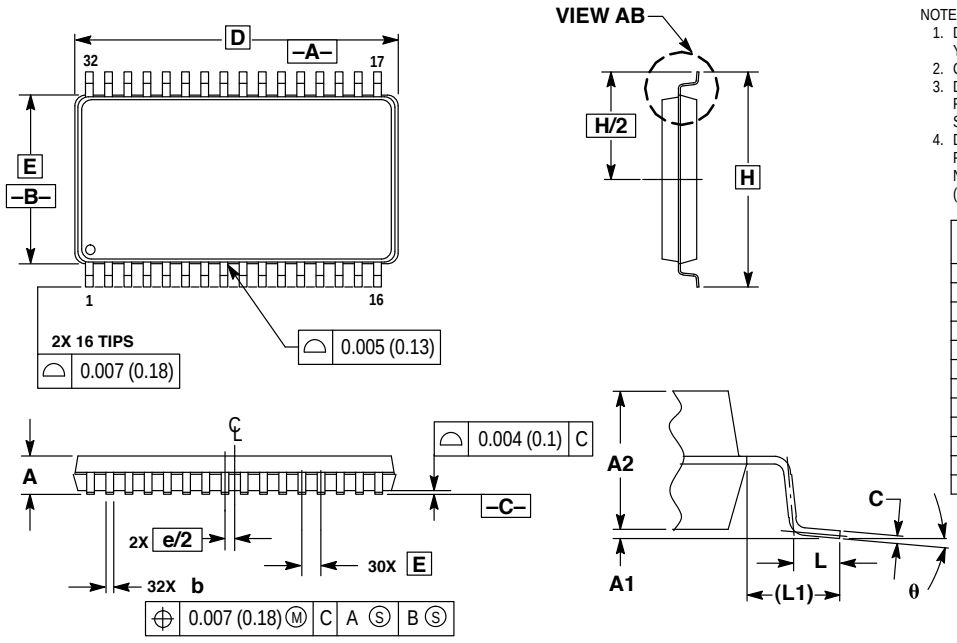
DW SUFFIX
SOG PACKAGE
CASE 1116-01



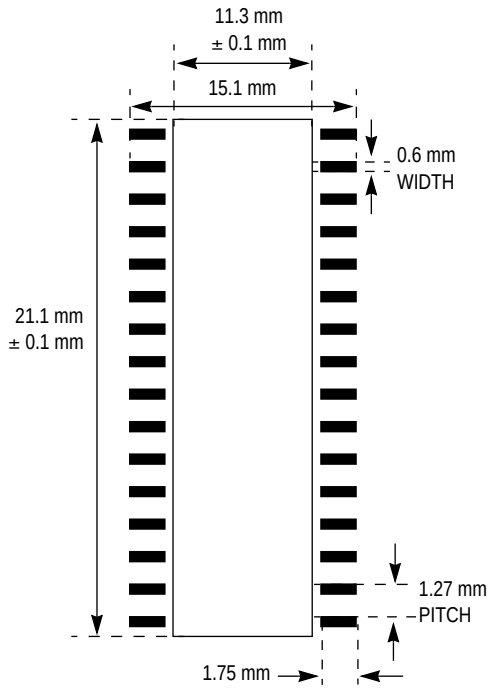
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSIONS SHALL NOT EXCEED 0.006 (0.15) PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.026 (0.65).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.090	0.100	2.29	2.54
A1	0.004	0.010	0.10	0.25
A2	0.086	0.090	2.18	2.29
b	0.014	0.020	0.35	0.51
C	0.004	0.009	0.10	0.22
D	0.825 BSC		20.96 BSC	
E	0.430 BSC		10.92 BSC	
e	0.050 BSC		1.27 BSC	
H	0.560 BSC		14.22 BSC	
L	0.021	0.041	0.33	1.04
L1	0.120 REF		3.048 REF	
θ	0 °	8 °	0 °	8 °

VIEW AB

MC143120 PAD LAYOUT

DW SUFFIX
32-LEAD SOG



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