

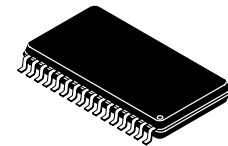
MC143120B1

Neuron[®] Chip Distributed Communications and Control Processor

The MC143120 is a communications and control processor which enables the development of interoperable products. It provides systems designers with many features to accelerate product development for distributed sense and control applications. Services at every layer of the OSI networking model are implemented in the included LonTalk[®] firmware-based protocol and are easily and optionally invoked. In addition, 34 I/O models are integrated with hardware to provide simplified sense and control device interfacing.

The MC143120 is designed for maximum clock operation of 10 MHz over a temperature range of - 40 to + 85°C including EEPROM writes.

- Three 8-Bit Pipelined Processors for Concurrent Processing of Application Code and Network Packets
- 11-Pin I/O Port Programmable in 34 Modes for Fast Application Program Development
- Two 16-Bit Timer/Counters for Measuring and Generating I/O Device Waveforms
- 5-Pin Communications Port That Supports Direct Connect and Network Transceiver Interface
- 1024 Bytes of Static RAM for Buffering Network and Application Data
- 512 bytes of EEPROM with On-Chip Charge Pump for Address, Binding Data, and Application Code
- Programmable Pull-Ups on IO4 – IO7 and 20 mA Sink Current on IO0 – IO3
- Unique 48-Bit ID Number Redundantly Stored in Every Device
- 10 Kbyte ROM
- 32-Pin SOG Package
- Low Operating Current 15 mA (typical) at 10 MHz Frequency
 3 mA (typical) at 625 kHz Frequency
- Sleep Mode Operation Reduced Current Consumption (15 μ A Typical)
- 0.8 μ Manufacturing Process
- Redundant 48-Bit ID for Longer Reliability



DW SUFFIX
SOG PACKAGE
CASE 1116-0

ORDERING INFORMATION
MC143120B1DW SOG Package

ARCHIVE INFORMATION

ARCHIVE INFORMATION

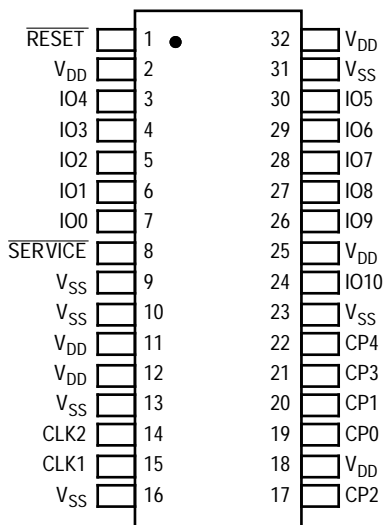
Echelon, LON, LonBuilder, LonManager, LonTalk, LonUsers, LONWORKS, Neuron, 3120, 3150, and NodeBuilder are registered trademarks of Echelon Corporation.

LonLink, LonMaker, LONMARK, LONews, and LonSupport are trademarks of Echelon Corporation.

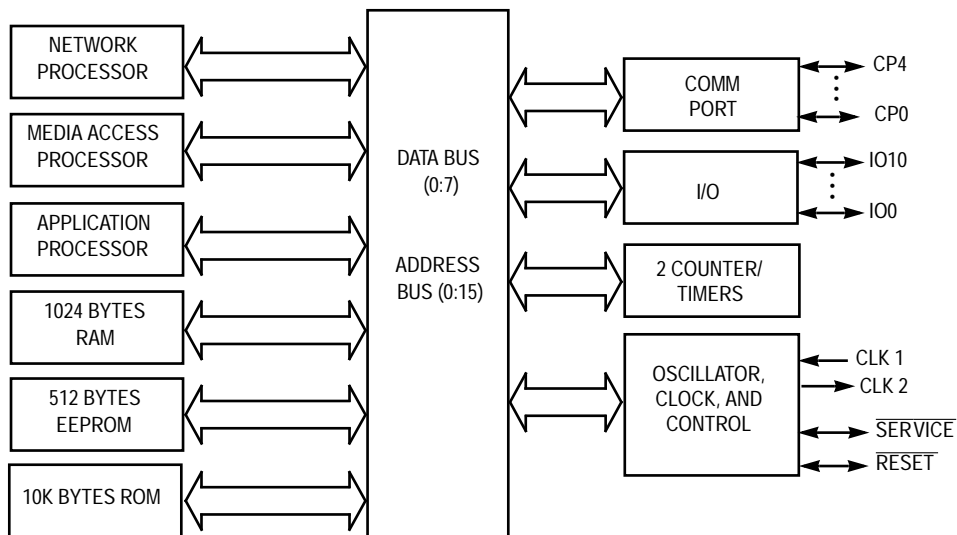


PIN ASSIGNMENT

32-LEAD SOG



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage Range (Referenced to V_{SS})	V_{DD}	- 0.3 to 7.0 V	V
Input Voltage Range (Referenced to V_{SS})	V_{in}	- 0.3 to $V_{DD} + 0.3$	V
Maximum Drain Current	I_{DD}	200	mA
Maximum Source Current	I_{SS}	300	mA
Maximum Power Dissipation	P_D	800	mW
Operating Temperature	T_A	- 40 to + 85	°C
Storage Temperature Range	T_{stg}	- 65 to + 150	°C

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} , $T_A = -40$ to + 85°C)

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	4.5	5.5	V
TTL Low-Level Input Voltage	V_{IL}	V_{SS}	0.8	V
TTL High-Level Input Voltage	V_{IH}	2.0	V_{DD}	V
CMOS Low-Level Input Voltage	V_{IL}	V_{SS}	0.8	V
CMOS High-Level Input Voltage	V_{IH}	$V_{DD} - 0.8$	V_{DD}	V
Operating Free-Air Temperature	T_A	-40*	+ 85	°C

* Writes to EEPROM are guaranteed down to -40°C for all Neuron Chip devices.

ELECTRICAL CHARACTERISTICS ($V_{DD} = 4.5$ to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage IO0 – IO10, D0 – D7, CP0, CP3, CP4, SERVICE CP0, CP1 (Differential) Reset	V_{IL}	—	—	0.8 Programmable 0.3 V_{DD}	V
Input High Voltage IO0 – IO10, D0 – D7, CP0, CP3, CP4, service pin CP0, CP1 (Differential) Reset	V_{IH}	2.0 Programmable	—	— — $V_{DD} - 0.7$	V
Low-Level Output Voltage Standard Outputs ($I_{OL} = 1.4$ mA) (Note 1) High Sink (IO0 – IO3), SERVICE, RESET ($I_{OL} = 20$ mA) High Sink (IO0 – IO3), SERVICE, RESET ($I_{OL} = 10$ mA) Maximum Sink (CP2, CP3) ($I_{OL} = 40$ mA) Maximum Sink (CP2, CP3) ($I_{OL} = 15$ mA)	V_{OL}	—	—	0.4 0.8 0.4 1.0 0.4	V
High-Level Output Voltage Standard Outputs ($I_{OH} = -1.4$ mA) (Note 1) High Sink (IO0 – IO3), SERVICE ($I_{OH} = -1.4$ mA) Maximum Source (CP2, CP3) ($I_{OH} = -40$ mA) Maximum Source (CP2, CP3) ($I_{OH} = -15$ mA)	V_{OH}	$V_{DD} - 0.4$ $V_{DD} - 0.4$ $V_{DD} - 1.0$ $V_{DD} - 0.4$	—	— — — —	V
Hysteresis (Excluding CLK1, RESET)	V_{hys}	175	—	—	mV
Input Current (Excluding pullups) (V_{SS} to V_{DD}) (Note 2)	I_{in}	- 10	—	10	μ A
Pullup Source Current ($V_{out} = 0$ V, Output = High-Z) (Note 2)	I_{pu}	60	—	260	μ A
Operating Mode Supply Current (Notes 3, 4, and 5)					mA
10 MHz Clock		—	14	25	
5 MHz Clock		—	7.5	13	
2.5 MHz Clock		—	4.5	7	
1.25 MHz Clock		—	3.2	4.2	
0.625 MHz Clock		—	1.6	2.5	
Sleep Mode Supply Current (Note 3,4)		—	9	100	μ A

NOTES:

- Standard outputs are A0 – A15, D0 – D7, IO4 – IO10, CP0, CP1, CP4, \bar{E} , and R/W. ($\overline{\text{RESET}}$ is a CMOS open drain input/output. CLK2 must have ≤ 15 pF.)
- IO4 – IO7 and SERVICE have configurable pullups. $\overline{\text{RESET}}$ has a permanent pullup.
- Supply current measurement conditions: all outputs under no-load conditions, all inputs ≤ 0.2 V or $\geq (V_{DD} - 0.2)$ V, configurable pullups off, crystal oscillator clock input, differential receiver disabled. The differential receiver adds approximately 200 μ A typical and 600 μ A maximum when enabled. It is enabled on either of the following conditions:
 - Neuron Chip in Operating mode **and** Comm Port in Differential mode.
 - Neuron Chip in Sleep mode **and** Comm Port in Differential mode **and** Comm Port Wakeup not masked.
- Typical values are at midpoint of voltage range and 25°C only.

RESET TRIP POINT (V_{DD})

Part Number	Min	Typ	Max	Unit
MC143120B1	2.1	3.3	4.4	V

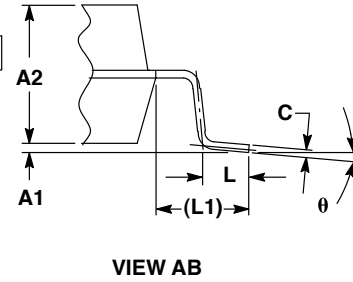
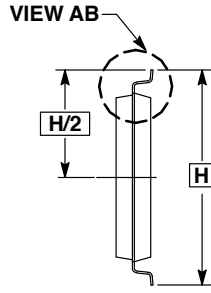
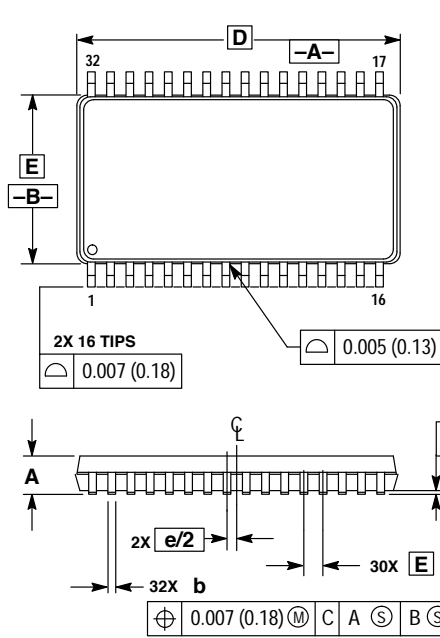
Table 1. Pin Descriptions

Pin Name	I/O	Pin Function	DW Suffix Pin Number
CLK1	Input	Oscillator connection or external clock input.	15
CLK2	Output	Oscillator connection. Leave open when external clock is input to CLK1. One Load.	14
RESET	I/O (Built-In Configurable Pullup)	Reset pin (active low).	1
SERVICE	I/O (Built-In Configurable Pullup)	Service pin. Indicator output during operation.	8
IO0 – IO3	I/O	Large current-sink capacity (20 mA). General I/O port.	7, 6, 5, 4
IO4 – IO7	I/O (Built-In Configurable Pullup)	General I/O port. One of IO4 to IO7 can be specified as No. 1 timer/counter input with IO0 as output. IO4 can be used as the No. 2 timer/counter input with IO1 as output.	3, 30, 29, 28
IO8 – IO10	I/O	General I/O port. Can be used for serial communication with other devices.	27, 26, 24
D0 – D7	I/O	Memory data bus.	N/A
R/W	Output	Read/write control output port for external memory.	N/A
\bar{E}	Output	Control output port for external memory.	N/A
A15 – A0	Output	Address output port.	N/A
V_{DD}	Input	Power input (5 V nom). All V_{DD} pins must be connected together externally.	2, 11, 12, 18, 25, 32
V_{SS}	Input	Power input (0 V, GND). All V_{SS} pins must be connected together externally.	9, 10, 13, 16, 23, 31
CP0 – CP4	Communication Network Interface	Bidirectional port that supports communications protocols by specifying mode.	19, 20, 17, 21, 22
NC	N/A	No internal connection. Leave open.	N/A

ARCHIVE INFORMATION

ARCHIVE INFORMATION

**DW SUFFIX
SOG PACKAGE
CASE 1116-01**

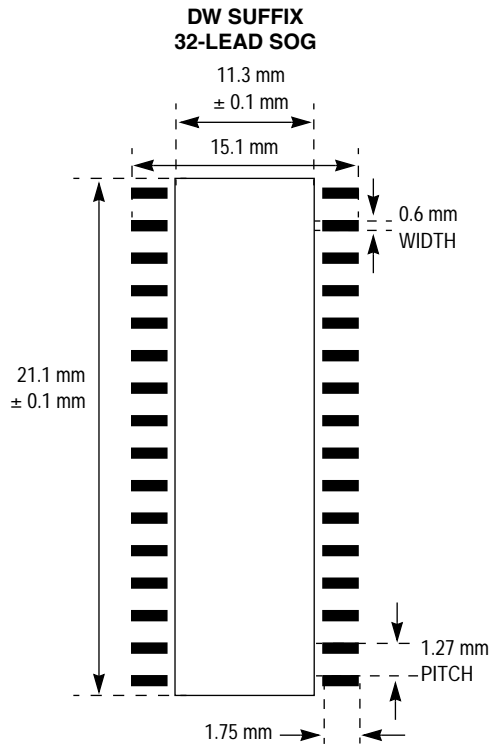


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSIONS SHALL NOT EXCEED 0.006 (0.15) PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.026 (0.65).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.090	0.100	2.29	2.54
A1	0.004	0.010	0.10	0.25
A2	0.086	0.090	2.18	2.29
b	0.014	0.020	0.35	0.51
C	0.004	0.009	0.10	0.22
D	0.825 BSC		20.96 BSC	
E	0.430 BSC		10.92 BSC	
e	0.050 BSC		1.27 BSC	
H	0.560 BSC		14.22 BSC	
L	0.021	0.041	0.33	1.04
L1	0.120 REF		3.048 REF	
θ	0°	8°	0°	8°

MC143120 PAD LAYOUT



This page intentionally left blank.


ARCHIVE INFORMATION

ARCHIVE INFORMATION

This page intentionally left blank.

ARCHIVE INFORMATION

ARCHIVE INFORMATION

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution:
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447 OR 602-303-5454

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244-6609
INTERNET: <http://www.mot.com/SPS/>

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 81-3-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

**MOTOROLA**