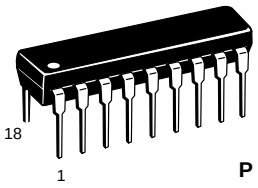
MC144144

Advance Information

Enhanced Closed-Caption Decoder
CMOS

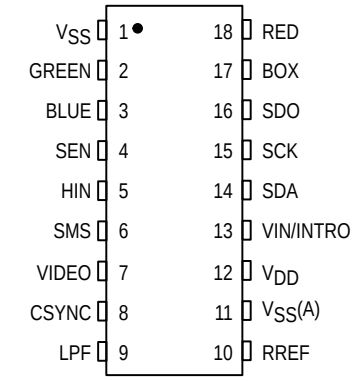


P SUFFIX
PLASTIC DIP
CASE 707

ORDERING INFORMATION

MC144144P Plastic DIP

PIN ASSIGNMENT



The MC144144 is a Line 21 closed–caption decoder for use in television receivers or set–top decoders conforming to the NTSC standard. Capability for processing and displaying all of the latest standard Line 21 closed–caption format transmissions is included. The device requires a closed–caption encoded composite video signal, a horizontal sync signal, and an external keyer to produce captioned video. RGB and box signal outputs are provided, which along with the mode select, allow simple interfacing to either color or black–and–white TV receivers.

Display storage is accomplished with an on–chip RAM. A modified ASCII character set, which includes several non–English characters, is decoded by an on–chip ROM. An on–screen character appears as a white or colored dot matrix on a black background.

Captions (video–related information) can be up to four rows appearing anywhere on the screen and can be displayed in two modes: roll–up, paint–on, or pop–on. With rollup captions, the row scrolls up and new information appears at the bottom row each time a carriage return is received. Pop–on captions work with two memories. One memory is displayed while the other is used to accumulate new data. A special command causes the information to be exchanged in the two memories, thus causing the entire caption to appear at once.

When text (non–video related information) is displayed, the rows contain a maximum of 32 characters over a black box which overwrites the screen. Fifteen rows of characters are displayed in the text mode.

An on–chip processor controls the manipulation of data for storage and display. Also controlled are the loading, addressing, and clearing of the display RAM. The processor transfers the data received to the RAM during scan lines 21 through 42. The operation of the display RAM, character ROM, and output logic circuits are controlled during scan lines 43 through 237. The functions of the MC144144 are controlled via a serial port which may be configured to be either I^2C or SPI.

- Conforms to FCC Report and Order as Amended by the Petition for Reconsideration on Gen. Doc. 91–1
- Conforms to EIA–608 for XDS Data Structure
- Supports Four Different Data Channels for Field 1 and Five Different Data Channels for Field 2, Time Multiplexed within the Line 21 Data Stream: Captions Utilizing Languages 1 and 2, Text Utilizing Languages 1 and 2 and XDS Support
- Output Logic Provides Hardware Underline Control and Italics Slant Generation
- Single Supply, Operating Voltage Range: 4.75 to 5.25 V
- Supply Current: 20 mA (Preliminary)
- Operating Temperature Range: 0 to 70°C
- Composite Video Input Range: 0.7 to 1.4 V p–p
- Horizontal Input Polarity: Either Positive or Negative
- Internal Timing and Sync Signals Derived from On–Chip VCO

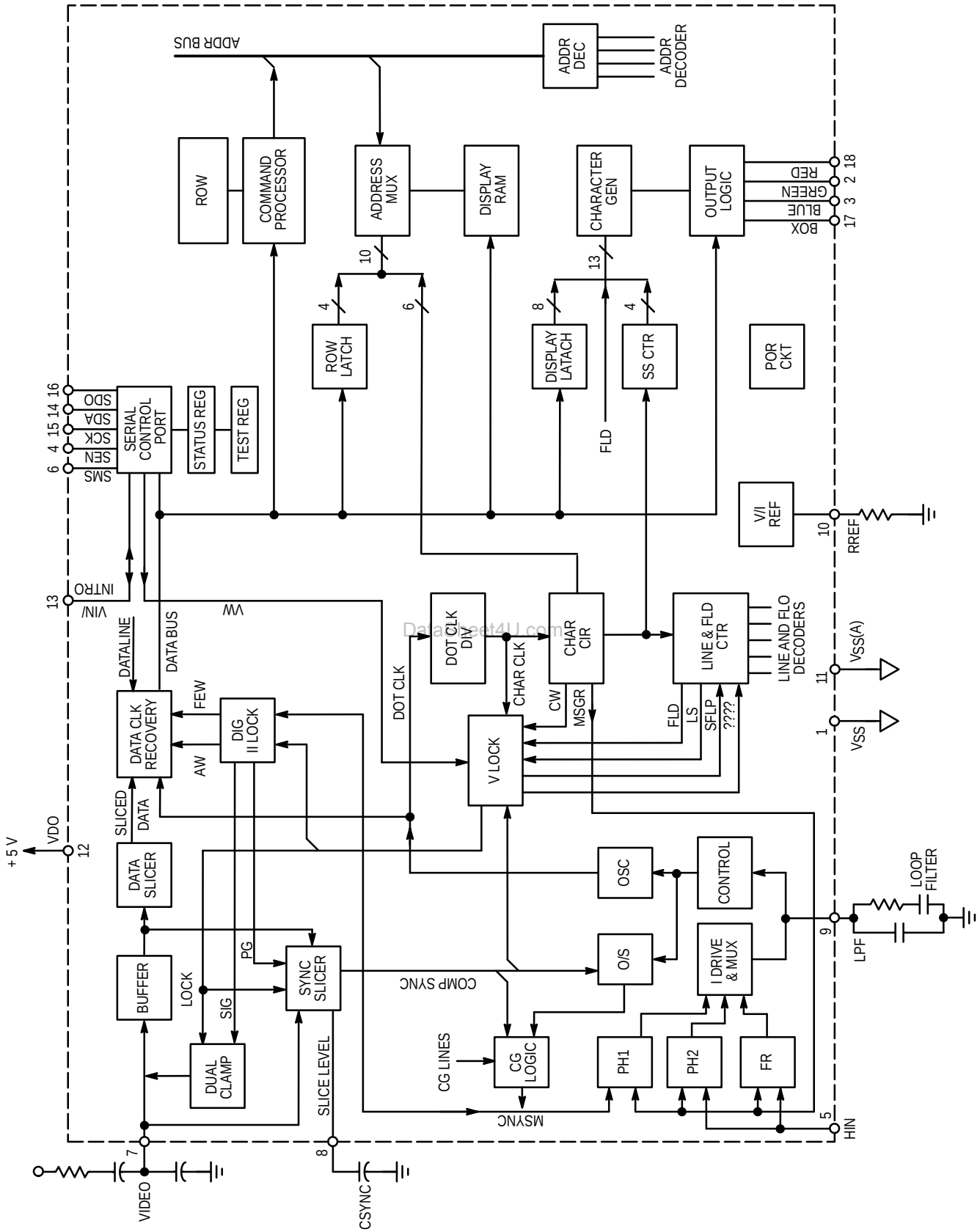
In this document, the term ‘user’ refers to the television or VCR designer. The user may choose to make certain optional features selectable by the viewer. These features then become viewer options.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
11/95

MOTOROLA

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS* (Voltages referenced to $V_{SS(A)}$ and $V_{SS(D)}$)

Symbol	Parameter	Value	Unit
$V_{DD}(A)$	Analog DC Supply Voltage	– 0.5 to 6.0	V
$V_{DD}(D)$	Digital DC Supply Voltage	– 0.5 to 6.0	V
V_{in}	DC Input Voltage Analog Section	– 0.5 to $V_{DD}(A)$ + 0.5	V
	Digital Section	– 0.5 to $V_{DD}(D)$ + 0.5	
V_{out}	DC Output Voltage, Digital Section	– 0.5 to $V_{DD}(D)$ + 0.5	V
I_{in}	DC Input Current, per Pin	+ 10	mA
I_{out}	DC Output Current, per Pin	+ 20	mA
I_{DD}	DC Supply Current	+ 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC ELECTRICAL CHARACTERISTICS

($V_{DD}(A) = V_{DD}(D)$ = 4.75 to 5.25 V, T_A = 0 to 70°C, Voltages Referenced to $V_{SS}(D)$ Unless Otherwise Indicated)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IL}	Input Voltage Low		0	0.2 V_{CC}	V
V_{IH}	Input Voltage High		0.7 V_{CC}	V_{CC}	V
V_{OL}	Output Voltage Low	I_{OL} = 1.0 mA	—	0.4	V
V_{OH}	Output Voltage High	I_{OH} = 0.75 mA	V_{CC} – 0.4	—	V
I_{IL}	Input Leakage	0 V, V_{CC}	– 3.0	3.0	μA
I_{CC}	Supply Current	Estimated	—	20	mA
$K\phi$	VCO Gain		—	TBD	MHz/V
I_{LP}	Loop Filter Current		—	TBD	mA

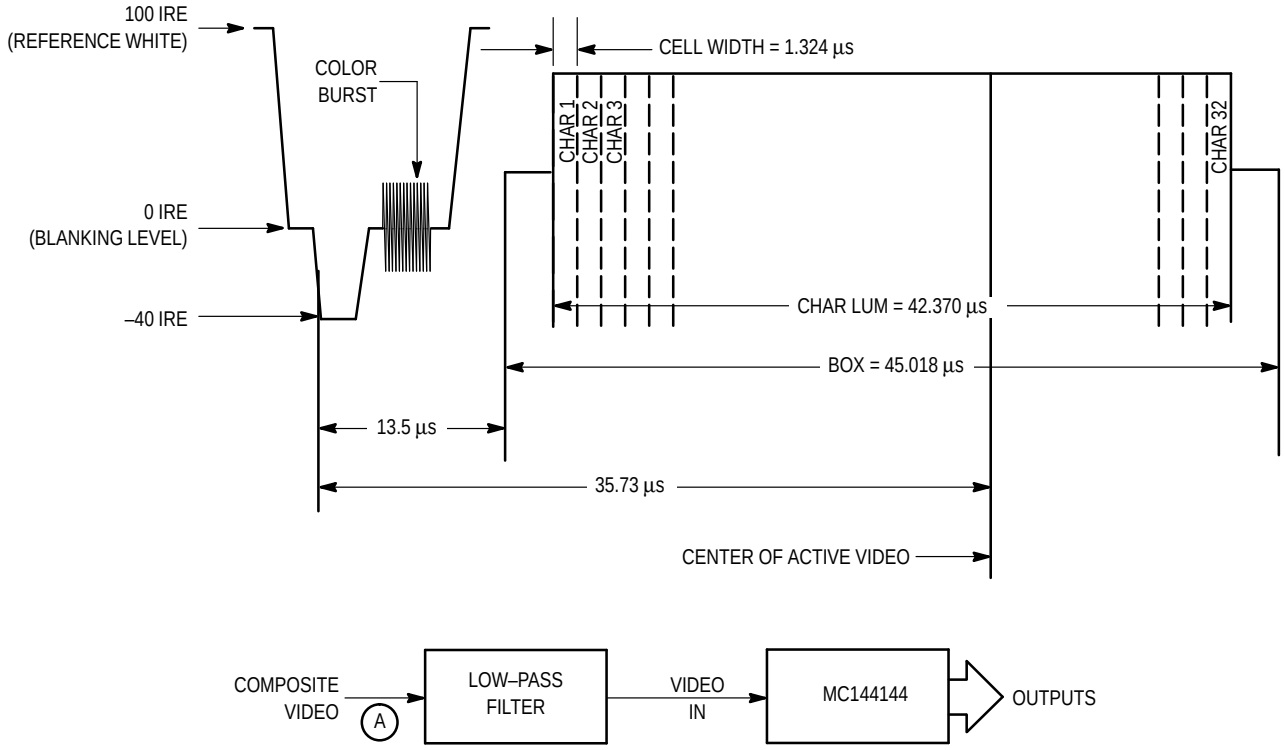
* The estimated value is 20 mA; this is not guaranteed.

AC AND TIMING CHARACTERISTICS

Parameter	Conditions
Composite Video Input	
Amplitude:	1.0 Vp–p, ± 3 dB
Polarity:	Sync tips negative
Bandwidth:	600 kHz
Signal Type:	Interlaced
Max Input R:	470 Ω
DC Offset:	Signal to be ac coupled with a minimum series capacitance of 0.1 μF.
Non–Standard Video Signals Must Have the Following Characteristics	
Sync Amplitude:	200 mV min
Vert Pulse Width:	3H ± 0.5H
Vert Pulse Tilt:	20 mV max
H Timing:	Phase Step (head switch) ± 10 μs max F_h Deviation (long term) ± 0.5% max F_h p–p Deviation (short term) ± 0.3% max
Horizontal Signal Input (Preferably H Flyback)	
Amplitude:	CMOS level signal, low ≤ 0.2 V_{CC}, high ≥ 0.7 V_{CC}
Video Lock Mode: Polarity: Frequency:	 Any 15,734.263 Hz, ± 3%
HIN Lock Mode: Polarity: Frequency:	 Any Display HFB pulse
Line 21 Input Parameters (at 1.0 Vp–p) (Line 21 must be in its proper position to the leading edge of the vertical sync signal.)	
Code Amplitude:	50 IRE ± 10 IRE
Code Zero Level:	– 5 IRE, + 15 IRE relative to back porch
Bit Rate:	32 x F_h
Start of Code:	10.5 ± 1.0 μs (Measured from the midpoint of the leading edge of video H pulse to the midpoint of the rising edge of the first clock run–in cycle.)
Start of Data:	3.972 μs, – 0.00 μs, + 0.30 μs (Measured from the midpoint of the falling edge of the last clock run–in cycle to the midpoint of the rising edge of the start bit.)
Input Signal–to–Random Noise Performance	
Unit will function down to a 25 dB ratio (CCIR weighted	One error per row or better at that level.
Internal Sync Circuits	
The internal sync circuits will lock to all 525 line or 625 line signals having a vertical sync pulse.	It is at least 2 H long. It starts at the proper 2 H boundary for its field. If equalizing pulse serrations are present they must be less than 0.125 H in width.
Timing Signals	
Dot Clock:	768 x F_H = 12.0839 MHz
Dot Period:	82.75 ns
Character Cell Width:	1.324 μs (t_H ÷ 48)
Width of Row (Box):	45.018 μs (34 chars = 17/24 x t_H)
Width of Row (Char):	42.370 μs (32 chars = 2/3 x t_H)

AC AND TIMING CHARACTERISTICS (continued)

Parameter	Conditions
Horizontal Timing	
The timing of the ouput signals box and RGB have been set to make a centered display.	The positioning of these outputs can be adjusted in 330 ns increments by writing a new value to the H Position Register.
Control Port Signals – Two–Wire Serial Mode (SMS = LOW, SEN = HIGH) (See Figure 10)	
Clock and Data Transitions: The SCK and SDA bus lines are normally pulled high with a resistor. Data on the SDA bus may only change during SCK low time periods. Data changes during SCK high periods will indicate a start or stop condition.	Start Condition: A high–to–low transition of SDA with SCK high is a start condition which must precede any other command. Stop Condition: A low–to–high transition of SDA with SCK high is a stop condition which terminates all communications.
Acknowledge: All address and data words are serially transmitted to and from the MC144144 in eight bit words. A ninth bit time is used for the acknowledge.	The acknowledging device does so by pulling the SDA bus low during the ninth bit.
Control Port Signals – Three–Wire Serial Mode (SMS = HIGH) (See Figure 11)	
Three–wire bus with Clock signal on SCK pin, Serial Data Input on SDA pin and Serial Data Output on SDO pin.	SEN pin LOW disabled the port, placing SDO in three–state. Signal transitions on SCK and SDA are ignored. SEN pin HIGH enables the port for operation. SEN and SMS pins LOW is a hardware reset for the part. These pins must be held low for at least 100 ns. Serial synchronization can be established by clocking in the minimum required SSR string of FFh, FFh, FEh. More than two bytes of FFh may be input but the string must end with FEh.



NOTES:

1. Timing parameters derived from the *NAB Engineering Handbook*, 7th Edition, page 5.4–75.
2. Dot period = 82.76 ns.
3. An assumption is made that the delay through the low–pass filter is 220 ns. Therefore, the timing of the output signals is normally set so that the start of the leading box preceding the first displayable character cell occurs at 13.4 to 13.7 µs after the midpoint of the leading edge of the horizontal sync pulse at Point A. The 13.4 to 13.7 µs value may be altered via a mask option; contact your Motorola representative.

Figure 1. Timing of Output Signals Relative to Composite Video at Point A

INTRODUCTION

THE MC144144 DECODER

The MC144144 is a stand alone integrated circuit, capable of processing VBI data from both fields of the video when the data conforms to the transmission format defined in the Television Decoder Circuits Act of 1990 and in accordance with the EIA–608.

The Line 21 data stream can consist of data from several data channels multiplexed together. Field 1 has four data channels, two Captions and two Text. Field 2 has five additional data channels, two Captions, two Text, and Extended Data Services (XDS). The XDS data structure is defined in EIA–608.

In this document, the term “user” refers to the television or VCR designer. The user may choose to make certain optional features selectable by the viewer. These features then become viewer options.

DATA TRANSMISSION FORMAT

The composite data signal contained within the active portion of the VBI line consists of a seven–cycle sine–wave clock run–in burst, a start bit, and 16 bits of data. These 16 bits consist of two 7–bit characters and control codes, with odd parity, that conform to the FCC closed caption decoder requirements and EIA–608. The clock rate is 0.5035 MHz which is 32 x F_H. The clock burst and data packet are 50 IRE units peak–to–peak and are filtered to a “2T” response. Data is sent with the least significant bit (bit b0) being sent first and the most significant bit (bit b7, the parity bit) being sent last.

MC144144 FEATURE SUMMARY

The primary features of the MC144144 are briefly described below.

VBI Data Processing

The MC144144 extracts the data in Line 21 of the incoming video. All data channels in both fields are handled. Specifically, the MC144144 can:

- Process data from both fields of Line 21 simultaneously.
- Display data from any data channel.
- Output XDS data through the serial port while displaying selected data.
- Output XDS data raw or filtered.
- XDS filter parameters user selectable from a list of pre–programmed values.
- NTSC or PAL operation selectable.

Video Data Display Modes

The data extracted from the incoming video may be displayed in different ways, according to the user selection and the type of data. The display features available are:

- Ten different data display modes, CC1–CC4, T1–T4, and two XDS displays.
- Pop–on, Paint–on, and Roll–up CAPTION displays.
- TEXT display default is a full–screen, 15–row display.
- User able to vertically reduce and reposition the TEXT display as desired.
- Color or Monochrome display mode selectable.
- XDSG Display Mode (channel grazing):
  Network Name, Call Letters,
  Program Name,
  Program Length, Time In Show
- XDSF Display Mode (full information):
  XDSG Display Mode information plus:
  Program Type (only basic types),
  Program Description.

Control Port Data Display Modes

In addition to displaying data extracted from Line 21 of the incoming video, the MC144144 can display information supplied through its serial port. This is referred to as the on–screen display (OSD) mode. This mode provides:

- OSD display can use all Video Data Display modes and features.
- Additional graphics features available.
- Double high and double wide characters available.
- Information may be placed anywhere on the screen.
- OSD display can be locked to an external V signal, if desired, to provide an OSD display when no video is present.

Character Set

The MC144144 has a new character set with extended features. For example:

- New font with lowercase letters having descenders.
- Optional display mode using drop shadow.
- EIA–608 extended characters.
- EIA–608 background and foreground attributes.
- Special framing and graphics for OSD display.
- Double high and double wide character display for OSD.
- Fifteen scan lines per character row for OSD and TEXT.

Serial Communications Interface

Communications and control of the MC144144 are through a serial control interface. Two serial control modes are available with the MC144144 performing as a slave device. These modes are:

- A two–wire, I^2C interface.
- A three–wire, serial peripheral interface (SPI).

Five pins are dedicated to the control port function and one pin can be configured to provide an interrupt output. These pins are designated as:

SMS = Serial mode select.
SCK = Serial port clock for either serial mode.
SDA = Serial port data for I^2C mode and data In for SPI mode.
SDO = Serial data out for SPI mode. Not used in I^2C mode.
SEN = SPI mode enable signal. Must be HIGH for I^2C mode.
VIN/INTRO = INTRO mode = Interrupt output on selected event (when used).

I^2C Mode

- I^2C mode is selected by bringing the SMS pin LOW and SEN pin HIGH.
- Acts as a slave device.
- SDA and SCK pins are the data and clock lines of this port.

- When used, INTRO can be enabled to interrupt on selected events.
- When SEN pin is made LOW the part will be reset.

SPI Mode

- SPI mode is selected by making the SMS pin HIGH.
- Acts as a slave device.
- All communications are clocked in and out as 8–bit bytes.
- SCK is the serial clock (input), SDA is Data In, and SDO is data out.
- SEN pin enables communication. When it is LOW the SDO pin is three–state.
- When SEN is brought HIGH the part will be synchronized and waiting for a command.
- If SEN is tied HIGH, the part can be synchronized by a command string.
- When used, INTRO can be enabled to interrupt on selected events.
- When SEN and SMS pins are made LOW the part will be reset.

Setup and Operational Control

User Selectable Displays are:

Captions, Language I, Field 1 (CC1)
Captions, Language II, Field 1 (CC2)

Captions, Language I, Field 2 (CC3)
Captions, Language II, Field 2 (CC4)

Text, Language I, Field 1 (T1)
Text, Language II, Field 1 (T2)

Text, Language I, Field 2 (T3)
Text, Language II, Field 2 (T4)

XDSG Display Mode
XDSF Display Mode

OSD mode (through the serial port)

User Controlled Features are:

Decoder ON/OFF

Color or Monochrome Output

EIA–608 Extended Attributes ON/OFF

OSD Drop Shadow ON/OFF

Text box size, Number of rows = x

Text box position, Base row = y

TV lines per character row, 13 or 15

Erase Timer (16 s) ON/OFF

Data Output Modes (through the serial port)

XDS Data Output, Raw or Filtered
Selected Channel and XDS Activity Indicators
Video Lock Indicator

Setup Options:

Horizontal timing of BOX

NTSC or PAL H lock source, Video or EXT HIN

V lock source, Video or EXT VIN

Default Condition Following Reset

Display Channel = CC1

Decoder = OFF

TEXT Size = 15 Rows

Lines/Row = 13

Background = BOX

Extended Attrib = ON

Data Outputs = OFF

NTSC operation

VCO Lock = Video

BOX Timing = 13.5 μs

Vert Lock = Video

VIN/INTRO = INTRO and Disabled

Horiz Lock = Video

Color/Mono = Color

OSD Display = Drop Shadow

OSD Display = 15 Lines/Row

OVERVIEW OF THE LINE 21 CLOSED CAPTION SYSTEM

THE LINE 21 CLOSED–CAPTIONING SYSTEM

The Line 21 closed–captioning system provides for the transmission of caption information and other text material as an encoded composite data signal during the unblanked portion of Line 21, field 1 of the standard NTSC video signal. In addition, a framing code is transmitted during the first half of Line 21, field 2.

The encoded composite video signal for Line 21, fields 1 and 2 is shown in Figure 5. The video signal conforms to the standard synchronizing waveform for color transmission given in Sub–part E, Part 73 of the FCC Rules and Regulations.

Multiplexed Data Channels

The Line 21, field 1 closed–caption system defines four different data channels which can be time multiplexed within the Line 21 data stream. They are Captions — Language 1, Captions — Language 2, Text — Language 1, and Text — Language 2. Both languages may be English in either case.

Field 2 has five additional data channels, two Captions, two Text, and Extended Data Services (XDS). The XDS data structure is defined in EIA–608.

DATA FORMAT

The composite data signal contained within the active portion of the VBI line consists of a seven–cycle sine–wave clock run–in burst, a start bit, and 16 bits of data. These 16 bits consist of two 8–bit alphanumeric characters formulated according to the USA Standard Code for Information Interchange (USASCII;x3.4–1967) with odd parity. The clock rate is 0.5035 MHz which is 32 x F_H. The clock burst and data packet are 50 IRE units peak–to–peak and are filtered to a “2T” response. Data is sent with the least significant bit (bit b0) being sent first and the most significant bit (bit b7, the parity bit) being sent last.

The data channels for each field are transmitted in Line 21 of that field as a time multiplexed data stream. The start of a particular channel's data stream is identified by the occurrence of one of its unique command codes. Once a unique command code is received, all subsequent data is considered to belong to that data channel until a unique command code is received for another data channel.

The 7–bit ASCII table defines two types of information: printing and non–printing. Printable data are data bytes having values between x0100000 ($20) and x1111111 ($7F), where x represents the parity bit. Data bytes having values between x0000000 ($00) and x0011111 ($1F) are called non–printing characters, because they have no displayable character font in the standard ASCII table.

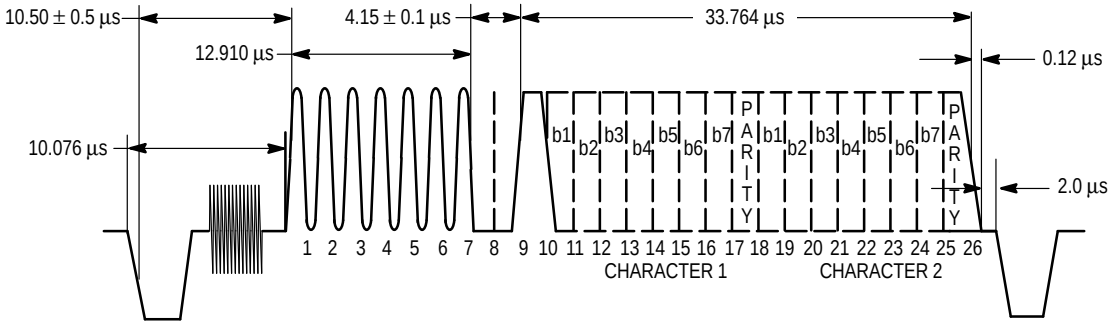


Figure 2. Encoded Composite Video Signal

Displayable Character Set

The specifications define a modified ASCII table character set where eight of the alphanumeric characters have been changed to provide some non–English characters. Also, 15 additional characters are defined by special character commands. The changes in the ASCII table characters are shown in Table 1.

Table 1. Modifications to the ASCII Characters

Hex Code	ASCII Character	Line-21 Character
2A	*	a′
5C	\	e′
5E	^	i′
5F	_	o′
60	‘	u′
7B	{	ç
7D	}	Ñ
7E	~	ñ

Fifteen additional displayable characters are sent by transmitting a two–byte code. The sixteenth code provides a transparent space. The byte pair has a non–printing character followed by a printing character, where the non–printing character is $11 for Language 1 and $19 for Language 2. The printing character determines the special character font that is displayed according to Table 2.

Commands and Special Information

Data channel commands and special information are transmitted as two–byte pairs consisting of a non–printing character followed by a printing character. The two bytes of the pair must be transmitted in the same field, and the pair is transmitted twice in successive frames. This redundancy provides some immunity to noise errors for control information.

Throughout the Line 21 system, bit 4 of the non–printing character identifies the language. Bit b4 = 0 signifies Language 1 commands and b4 = 1 signifies Language 2. The non–printing characters used in the Line 21 system are $10 through $17 for Language 1 and $18 through $1F for Language 2.

Table 2. Additions to the ASCII Characters

Print	Character
30	®
31	°
32	1/2
33	¿
34	™
35	¢
36	£
37	“1/8 note” music symbol
38	à
39	“Transparent Space”
3A	è
3B	â
3C	ê
3D	î
3E	ô
3F	û

OPERATING CHARACTERISTICS

DECODER OPERATION

The MC144144 provides full function NTSC, Line 21 performance. Input commands are included to enable the decoder to process and display any of the eight caption/text data channels (CC1, CC2, CC3, CC4, T1, T2, T3, or T4) contained in Line 21 of either field of the incoming video. XDS displays can also be selected. ON/OFF commands control the screen displays. When switched to the decoder off (TV) state, incoming data in the selected channel will still be processed but not displayed.

The MC144144 can also be configured to operate with PAL video signals. It will decode information encoded into its VBI in Line 22. The encoded data must conform to the waveform and command structure defined for NTSC, Line 21 operation.

DECODER SET–UP

VCO Lock

The design includes a VCO with stable gain characteristics and good power supply rejection. The internal horizontal and vertical synchronizing circuits provide a high degree of noise immunity. There are options for both horizontal and vertical lock. The VCO can be phase locked either to the horizontal signal derived from the video input signal (VIDEO) or to the externally supplied HIN signal, typically horizontal flyback.

HIN lock is used to provide a display having a minimum of observable jitter. This requires an HIN signal derived from the TV display and of the proper polarity. Such a signal is readily available in a television receiver. VIDEO lock mode enables the VCO to lock in phase to the incoming video signal, thus providing good operation in an application where no display related HIN signal is available, such as in a VCR.

Timing

Timing signals are derived from the VCO for use in the line counting and display circuits. Line counting requires proper identification of the input signal's vertical pulse. Default operation uses the vertical sync signal derived from the video input signal as the source for vertical lock. This method results in locking characteristics having good performance and good noise immunity.

In the event that OSD operation is required under conditions when no input video is present, it would be necessary to set the MC144144 for VIN lock. In this mode, the vertical timing will be determined from the vertical pulse signal supplied to the VIN pin.

The horizontal position of the caption display is determined by the internal timing circuits. A default condition has been established that should result in a well centered display in a typical application. However, since signal delays through video processing circuits can vary between designs, the MC144144 provides the user with the ability to change the default timing. No matter which of the horizontal lock modes is selected, the display horizontal position on the screen can be adjusted in quarter character (330 ns) steps by serial port commands.

DISPLAY FORMATS

Normal Mode

Characters are displayed as white or colored, dot–matrix characters on an opaque background. The box is normally black but the MC144144 can be set to blue by a serial command. The characters are described by a 12–by–18 dot pattern within a character cell which is 16 dots wide by 26 dots high per frame. The location of the character luminance within the character cell varies from character to character to allow for the display of lower case letters with descenders. All characters have at least a one dot border of black around each character. Underline is also provided.

The character ROM consists of a 12–by–18 dot–matrix pattern per character. Figure 3 shows the character font. Alternate rows and columns are read out of each field to produce an interleaved and rounded character. A display row contains a maximum of 32 characters plus a leading and trailing blank box, each a character cell in width, making the overall width of a display row 34 x 8 = 272 dots. Successive display rows are butted together, so that the total display is 195 dots high.

The black box (34 character cells wide by 195 dots high) results in a box size of 45.018 μs in width by 195 scan lines in height. Box starts in scan line 43 and extends to scan line 237. Theoretically, the display will be horizontally centered in the video display when box starts 13.2 μs after the leading edge of H. The default setting of the MC144144 places the center of the box at about 13.5 μs to allow for some delay in the normal video path. However, the box horizontal position can be adjusted by the user in 330 ns increments. The display will be approximately within the safe title area for NTSC receivers. Character width is 42.37 μs, also centered on the screen, resulting in a leading and trailing 1.32 μs black border.

An optional caption display mode, drop shadow, can be selected by the user through the serial port. This display mode eliminates the black box around the characters and places a two–dot black shadow to the right and below the character luminance dots when in the 15 scan line per row mode. This display mode is usable in captions, text, and OSD displays. Figure 4 shows the characters with shadowing added.

Extended Features

EIA–608 defined new extended features such as optional background and foreground display attributes and optional extended characters. The MC144144 will always respond to the extended characters but the extended background/foreground response can be controlled by the user. The background and foreground attributes add codes for background colors, black foreground as well as transparent, opaque, and semi–transparent background. The BOX signal output pin will be set into a three–state condition whenever one of the semi–transparent attribute codes is active. The external keying circuits can then use this condition to implement the intended video display.

The font for the extended characters is shown in Figure 5. The accented capital letters have been implemented by placing the accent marks above the character cell. When selected, this mode will result in the accent marks being written into the character cell space of the row above. In some operating modes we will expand the size of the overall box height by adding two additional scan lines at the top and one additional line at the bottom. This will make room for the accent marks in the topmost row and add a black line below the descenders of any lowercase characters in the last row.

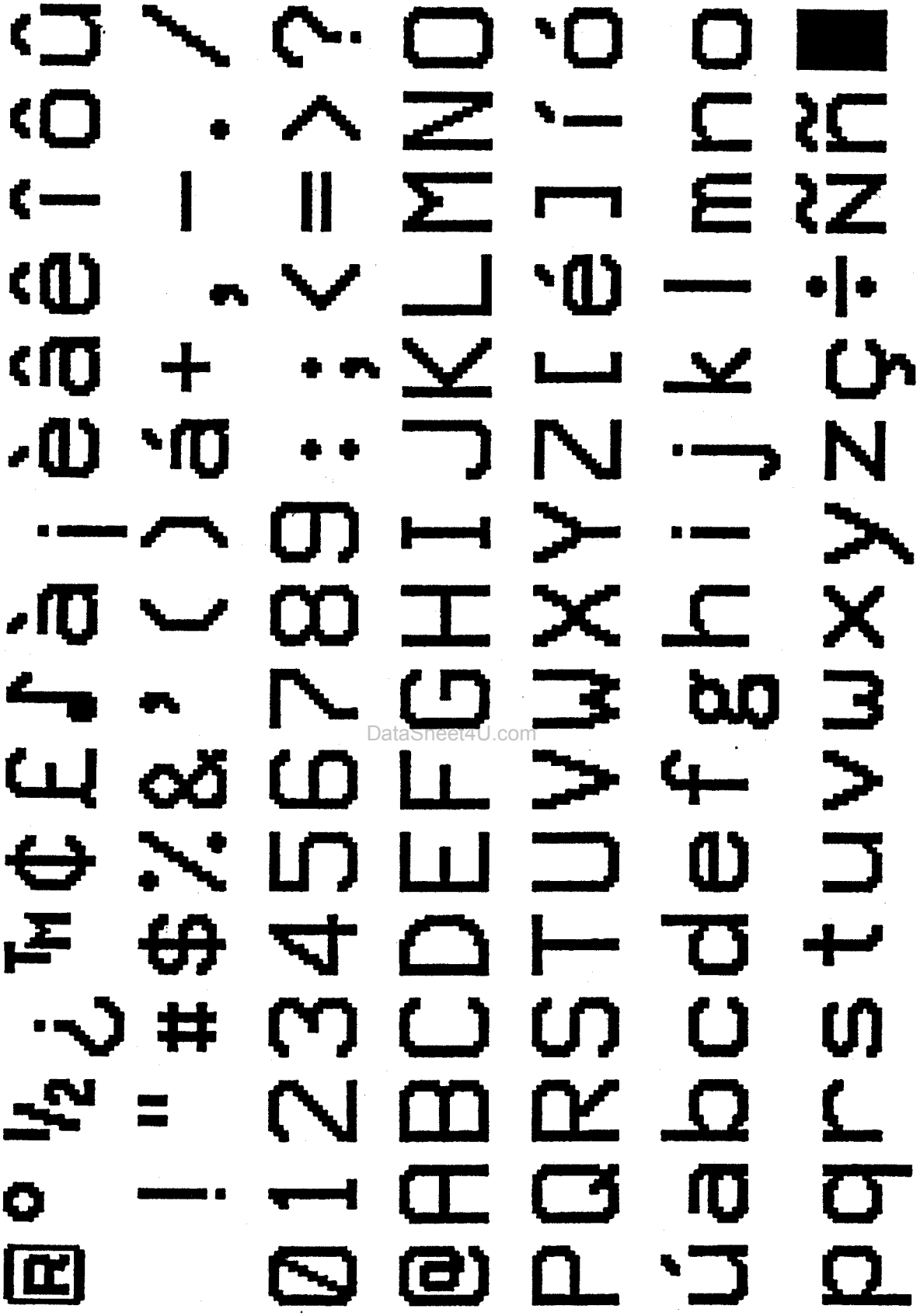


Figure 3. Display Character Font

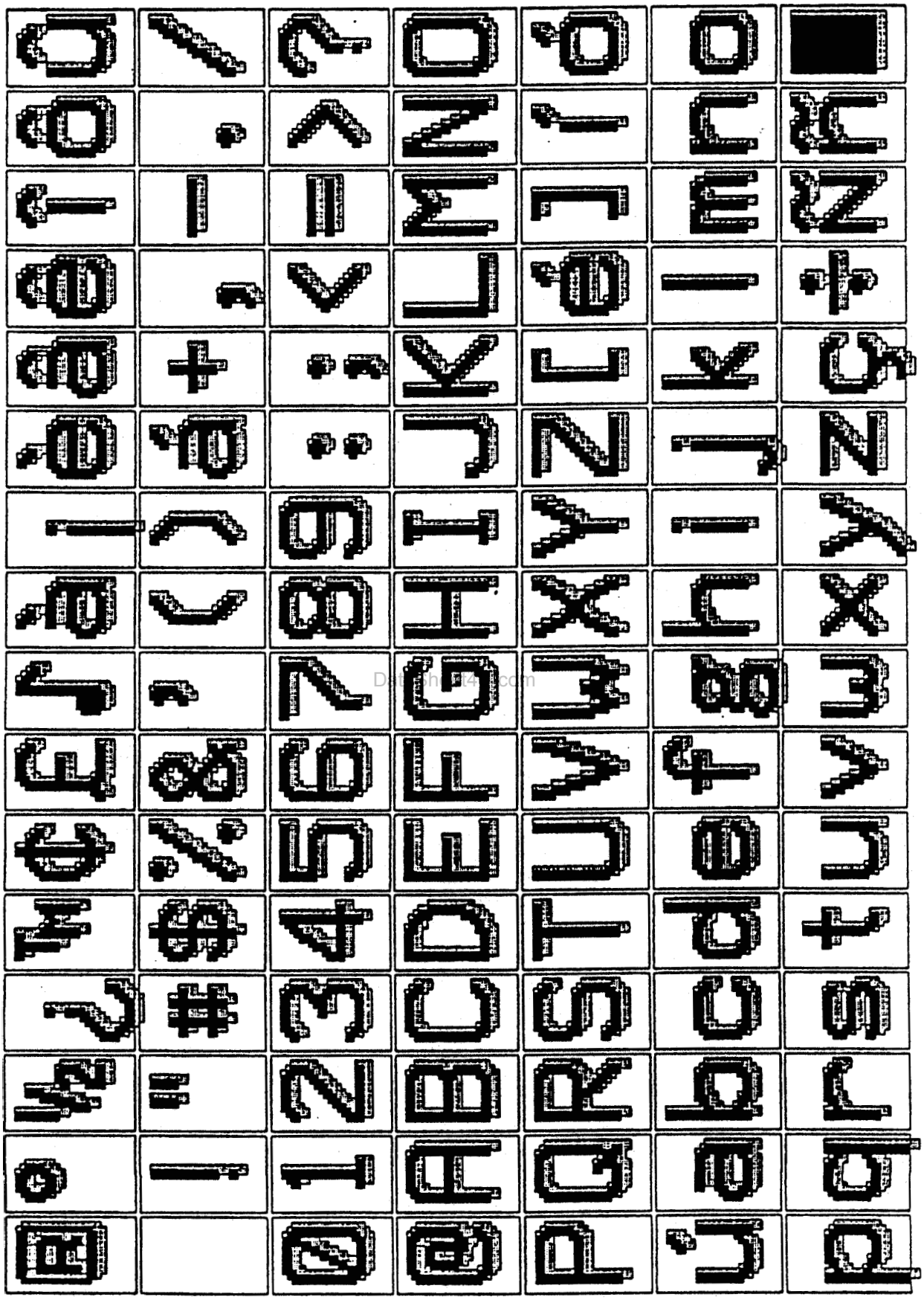


Figure 4. Display Character Font with Shadowing Added

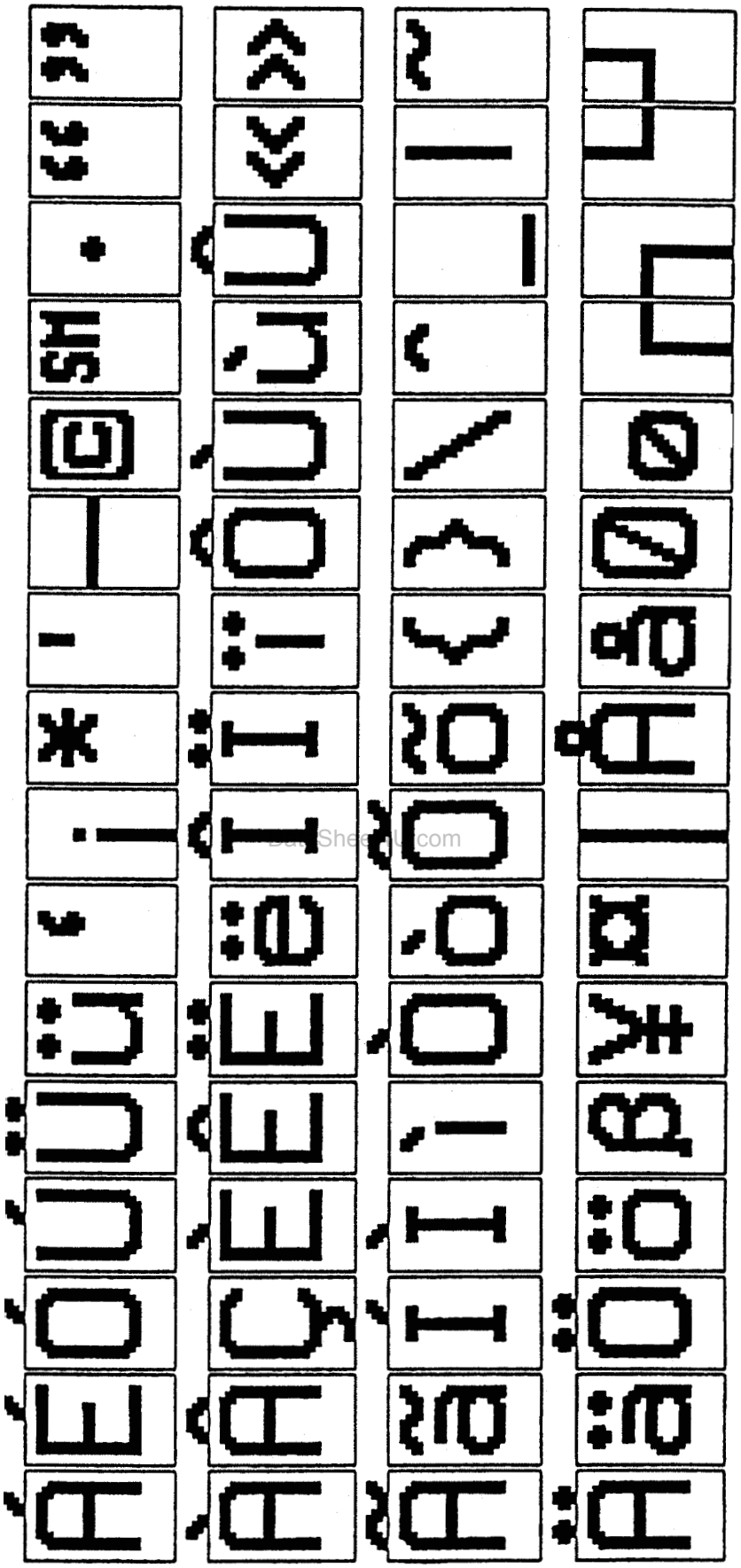


Figure 5. Display Character Font Extended Characters

This approach was used because shrinking the capitals to make room for the accent mark within the character cell makes poor quality characters and in some cases there would be no differentiation between the capital and lower case letter. It also has the advantage of minimizing the ROM size and providing a good readable font that closely matches what is normally seen in print.

In the unlikely case of a conflict between an accented capital letter in one row and a lowercase descender in the same character position in the row above, the descender is given priority. It is believed that the improved readability of our approach over shrunk capital letters far outweighs this potential conflict and results in a cost effective compromise for providing a full, extended features implementation.

The extended characters share their address space with the ODS graphics characters. When a BOX display is used the extended character set is in force. However, if a drop shadow display is used the graphics characters are in force. For caption and text display modes, if drop shadow is set, the user must also command the MC144144 to switch back to extended characters.

Text Mode Display

When TEXT mode is selected normally, a black box will be displayed as long as valid Line 21 code in the field selected is being detected. The MC144144 provides the option to make the box blue instead of black. This option will hold for captions as well as text.

The default TEXT display mode uses a 15 row by 34 character black box. TEXT characters will be displayed as they are received starting in the top row. Successive carriage returns will move the display down successive rows until all 15 rows have been displayed. Thereafter, the text will scroll up as new characters are added to the bottom row.

If the data for the selected channel is interrupted by a command for another channel, data processing stops but the display will remain. When a resume text command is received, data processing will resume and the new characters will be added starting at the position that the display row/column pointer was in at the interruption of data processing. If a start text command is received, the display will be cleared and new characters will be displayed starting in row 1, column 1 (left side).

The number of display rows and the location (base row) of the TEXT box can be altered by the user. In this way, the user can decide how much of the screen can be covered when displaying non–program related information.

When scrolling, the display will shift one scan line per frame until a complete row has been scrolled. If a carriage return is received before scrolling is complete, the display will immediately complete the “scroll” by jumping up the remaining scan lines and starts displaying the new text.

Caption Mode Display

According to the FCC specifications, caption data can appear in any of the 15 display rows but a single caption may consist of no more than four rows. The form of the caption display depends on the caption mode indicated by the transmitted caption command, pop–on, paint–on, or roll–up. The MC144144 can display a single caption having as many as eight rows. When any of the CAPTION display modes have been selected, the screen will be transparent (display box is only present when a caption is being displayed).

Pop–on captions work with two caption memories. One of them is normally displayed while the other is being used to accumulate new caption data. A new caption is popped–on by swapping the two memories with the end of caption (EOC) command. When the on–screen memory is erased, the screen is blank (transparent) and the memory will default to the row/column pointer at row 1, column 1 and monochrome non–underlined.

When caption mode is selected, the decoder will process any data following the resume caption loading (RCL) command (or the EOC). Normally, this command will be followed by a preamble address code (PAC) to indicate the row, column, and character attributes to be used with the following data. If no PAC is received the data will be added to the location last indicated by the row/column pointer prior to the receipt of the RCL command.

Paint–on caption mode is essentially equivalent to the pop–on mode except that the data received after the resume direct captioning (RDC) command is written to the on–screen memory rather than the off–screen memory. All the rules for PACs, midcodes, etc., are otherwise the same.

Roll–up caption mode presents a “text” like display that is limited to two, three, or four rows, depending on the resume roll–up (RUn) command used. The PAC following the RUn command is used as the BASE ROW for the ROLL–UP display. The BASE ROW will be the “bottom” row of the ROLL–UP display. In this case black box does not appear until characters are being displayed and box is only wide enough to provide a leading and trailing box in each line. The new data appears in the bottom row and as each carriage return is received, the row scrolls up and the new data added to the bottom. When the number of rows indicated by the resume command has been reached, the data in the top row scrolls off as new data is added to the bottom.

The TAB (INDENT) PAC permits placing captions starting at four character boundaries in any caption row. The TAB OFFSET command provides the means for adjusting the starting position for a caption at any column position in the current row.

XDS Mode Display

Two XDS display modes are provided. One provides information about the current program that would be of interest for “channel grazing”. The second display shows the grazing packets plus additional XDS packets which will inform the viewer about the program content. Information will be displayed as it is received. The display uses the drop shadow mode with 15 scan lines per row.

The XDSG mode is the GRAZE (channel grazing) display. The display contains three rows of information at the top of the screen, formatted for easy reading. They will contain the following XDS packet information:

Row 1, Grn – **Network Name – Call Letters**
Row 2, Ital, Und – **Program Name (title)**
Row 3, Cyan – **Program Length – Time In Show**

The XDSF mode is the FULL (information) display. This display shows the same information as the GRAZE display and adds the program type as well the first four program description rows (if transmitted). Although XDS defines eight program description rows, the first four are identified as containing the most important information and are the ones most

likely to be sent. Since 15 scan lines per row mode is being used, rows 10 – 13 will appear at the bottom of the screen.

Row 1, Grn – **Network Name – Call Letters**
Row 2, Ital, Und – **Program Name (title)**
Row 3, Cyan – **Program Length – Program Type – Time In Show**
Row 10, Yel – **Program Description Row 1 (if sent)**
Row 11, Yel – **Program Description Row 2 (if sent)**
Row 12, Yel – **Program Description Row 3 (if sent)**
Row 13, Yel – **Program Description Row 4 (if sent)**

When an XDS display mode has been selected the information will be displayed as the appropriate packets are received. The display will remain on–screen as long as valid XDS data continues to be received. If the 16–second erase timer is enabled (the default condition), the XDS display will be erased when no valid XDS data has been received for 16 seconds. If subsequent XDS data is received with displayable packets, that information will reappear on the screen. XDS data recovery can be active in the XDS display mode.

The XDS display mode is turned off by selecting a different display mode.

DISPLAY ERASE AND AUTOBLANKING

The display is erased in the TEXT mode by the start text command (but box is maintained) and in the CAPTION mode by the erase displayed memory (EDM) command. The non–displayed memory can be erased by the erase non–displayed memory (ENM) command.

Four other events can also cause the display to be erased. First, changing the display mode, such as from CC1 to T1, CC1 to XDSF, and so forth, will clear the memory and hence the display. Second, a loss of video lock, such as on a channel change, will cause the screen to be cleared. The currently active display mode will not be changed.

The third action that will clear the displayed memory is when the autoblanking circuit is activated. The autoblanking circuit monitors the presence of a Line 21 waveform in the field corresponding to the data channel selected for display. The decoder is held in the decoder OFF (TV) state until a Line 21 waveform is continuously detected for a period of 0.5 s. Once the decision has been made, and assuming that the user has selected the decoder ON state, the normal display for the data channel selected will be presented.

The autoblanking circuit will not be activated again until a Line 21 waveform has been lost for 1.5 s. Any data received during the 1.5 s period will reset the counter so that autoblanking will only be activated on continuous loss of the Line 21 waveform for 1.5 s.

The fourth method of clearing the screen is by the action of the 16 s erase timer. This function is only active when a CAPTION or XDS display mode has been selected. If no data is received for the display channel selected for a 16 s period, the on–screen memory will be erased. The decoder will still be in the selected channel with the decoder ON, so that when data for the selected channels resumes, it will be displayed.

SERIAL COMMUNICATIONS INTERFACE

Commands and data are sent to and from the MC144144 through its serial communications interface. Two Serial Control Modes are available. One mode is a two–wire I^2C bus interface (Figure 6). The other serial mode is a three–wire (Figure 7), synchronous serial peripheral interface (SPI). In both cases the MC144144 acts as a slave device.

This port is the path for setting the configuration and operational modes of the device. It is also the port for outputing the recovered XDS data and for inputing the OSD data for display.

Five pins are dedicated to the control port function and one pin can be configured to provide an interrupt output. These pins are designated as:

SCK = serial clock line in either serial mode.

SDA = serial data (bidirectional) line in I^2C mode and data in for SPI mode.

SDO = serial data out for SPI mode. Not used in I^2C mode.

SEN = SPI mode enable signal. Must be HIGH for I^2C mode.

SMS = serial mode select.

VIN/INTRO = Interrupt output on selected event when used.

When the vertical lock = VIDEO, the VIN/INTRO pin is set as an output, providing the INTRO signal. This interrupt operation is available in either serial control mode.

The MC144144 will be able to interrupt on the occurrence of any of several events. The master device will clear the interrupt by writing to the interrupt request register.

I^2C Bus Operation

The serial control mode (Figure 6) in use is selected by the state of the SMS pin. When SMS is set LOW, the MC144144 will be in the I^2C mode. In this mode, the MC144144 supports a bidirectional two–wire bus and data transmission protocol. The bus is controlled by the master device, which generates the serial clock (SCK), controls the bus access, and generates the start and stop conditions. The SDA pin is the bidirectional data line. In this mode the SDO output is not used and the pin will be in its high impedance state.

The MC144144 is a slave device having a slave address of 0010100. The MC144144 can receive or transmit data under control of the master device.

When the SMS and SEN pins are both LOW, the part will be in the RESET state. Therefore the SEN pin can be used to reset the part while in the I^2C mode. The SEN pin may be tied to an NRESET signal or tied HIGH if no reset is desired.

The bus protocol requires:

- Data transfer may only be started when the bus is not busy.
- During data transfer, data transitions must not occur while the clock is HIGH.

Bus conditions are defined as:

Not Busy – data and clock lines both HIGH.

Start – A HIGH to LOW transition of SDA line while SCK line is HIGH.

Stop – A LOW to HIGH transition of SDA line while SCK line is HIGH.

Acknowledge – When addressed, the receiving device must output an acknowledge after the reception of each byte. The

master device must generate the clock for the acknowledge bit. Acknowledge is SDA = LOW.

Data – The data (SDA) is output by the transmitting device on the falling edge of SCK, MSB first. The receiving device will read the data, MSB first on the rising edge of SCK.

TWO WIRE SERIAL MODE REQUIREMENTS

Symbol	Parameter	Min	Max	Unit
f_{SCK}	Clock Frequency	—	100	kHz
t_{LOW}	Clock Pulse Width Low	4.7	—	µs
t_{HIGH}	Clock Pulse Width High	4.0	—	µs
t_r	SDA and SCL Rise Time	—	1.0	µs
t_f	SDA and SCL Fall Time	—	300	ns
t_{AA}	Clock Low to Data Out Valid	0.1	3.5	µs
t_{BUF}	Bus Free Time	4.7	—	µs
$t_{HD.STA}$	Start Hold Time	4.0	—	µs
$t_{SU.STA}$	Start Setup Time	4.7	—	µs
$t_{HD.DAT}$	Data In Hold Time	0	—	µs
$t_{SU.DAT}$	Data In Setup Time	250	—	ns
$t_{SU.STO}$	Stop Setup Time	4.7	—	µs
t_{DH}	Data Out Hold Time	100	—	ns
t_I	Input Filter TC	—	100	ns

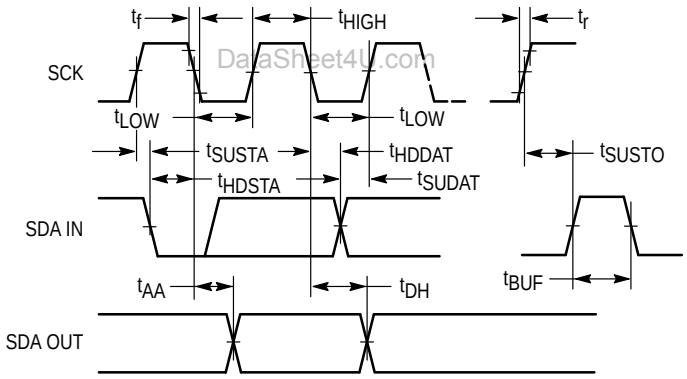


Figure 6. Two–Wire Serial Mode

Communication with the MC144144 is initiated when the master device sends the MC144144 slave address following the start condition. The MC144144 has a preset, single, seven–bit slave address. The MC144144 will respond with an acknowledge. The eighth bit of the slave address is driven high for read operations and low for write operations.

Writing to the I²C Bus

All write commands are either one or two byte commands. The number of data bytes to be received by the MC144144 is inherent in the command and the MC144144 will respond with the acknowledge signal only for the number of bytes expected. If the master writes more bytes than expected, there will be no acknowledge for the extra bytes.

The MC144144 is enabled when a start condition followed by its slave address byte is received. It will be disabled once it deems the command to have been completed or by a stop condition. A new start condition without a stop condition will begin a new sequence. Therefore, successive commands may be executed by successive strings of “start – slave address – command” sequences without any intervening stop condition being sent.

A write to the MC144144 should always be preceded by executing a status read to verify that the MC144144 is not busy. The status register data is output immediately following the reception of the slave address with the read bit set. If the RDY bit is set, the master device can initiate its write sequence, always beginning with the start condition. The first byte of a two byte command is written first.

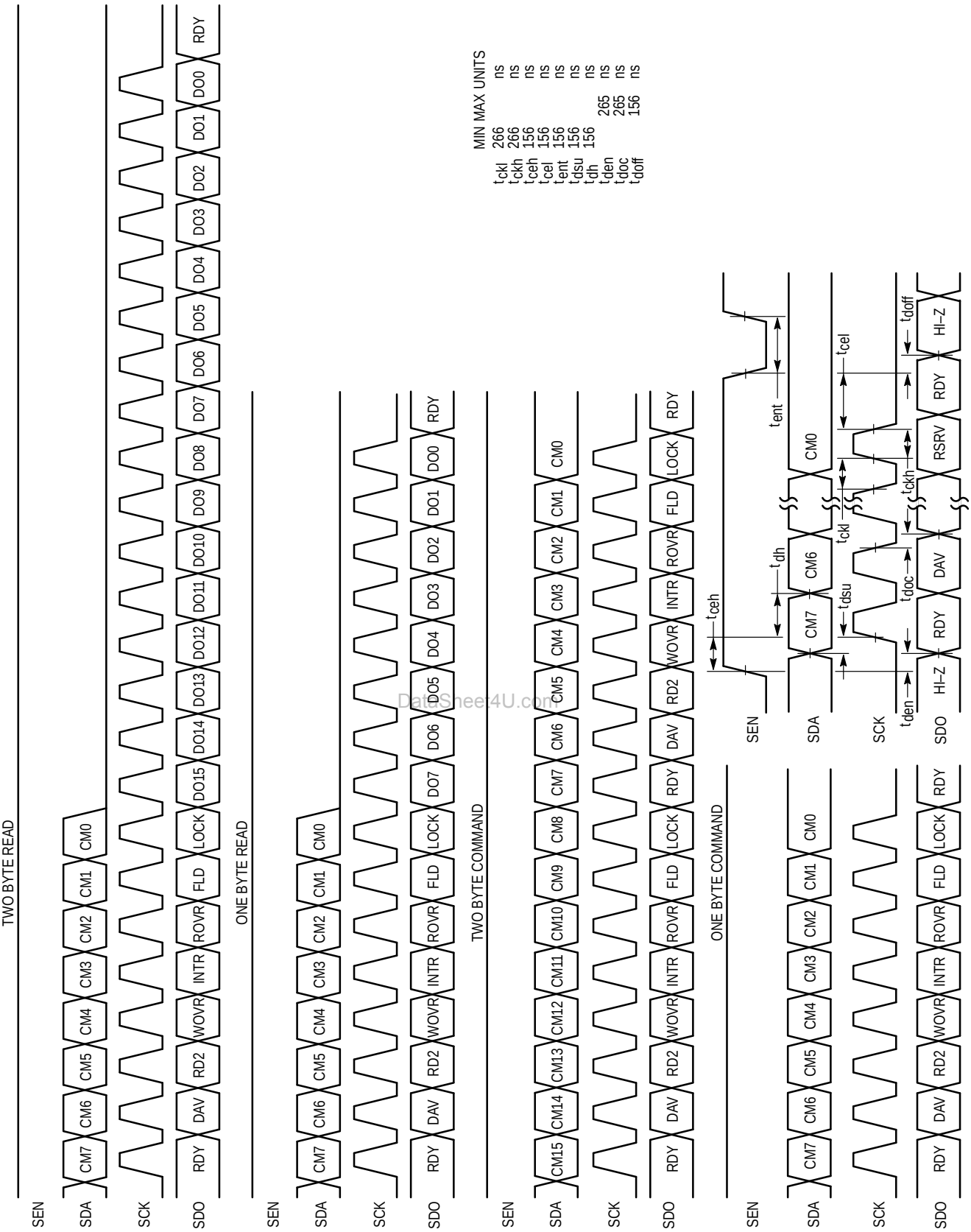


Figure 7. Three–Wire Serial Mode

Reading Data Using the I2C Bus

With the exception of the serial status (SS) register, which may be read at any time, each read operation must be set up before the data can be read from the serial output registers of the MC144144. Data is set up for a read operation either automatically or manually. XDS data reads are set up automatically upon recovery by setting a valid XDS FILTER register selection. All other data read operations must be set up manually using the READ SELECT commands RDS1 and RDS2. These commands load the selected data byte or pair of bytes into the serial output register(s), set the SS register RD2 bit according to the number of data bytes requested and set the SS register DAV bit to indicate availability of data.

The MC144144 I2C bus supports one, two, and three byte read sequences. All read sequences output the SS register as the first output byte. If the serial status DAV bit is set, one or two data bytes should also be read. If the DAV bit is not set, the I2C master device should end the read sequence by failing to acknowledge the received byte.

The number of data bytes available is indicated by the state of the RD2 bit of the serial status. In a typical read operation the status byte is read and the DAV and RD2 bits are examined. If one or two data bytes are available they are read in sequence separated by acknowledges. The last byte read should not be acknowledged by the master. It is necessary to read all available data in a read operation to clear the DAV bit and permit subsequent reads. All data is output MSB first.

SPI Bus Operation

When the SMS pin is HIGH, the MC144144 will be in the SPI serial control mode (Figure 7). The clock line should be tied to the SCK pin. The DATA IN signal and DATA OUT signal from the master device should be connected to the SDA and SDO pins, respectively. The SEN pin is used to select the MC144144 when there are multiple peripherals on the bus.

As noted above, when both the SMS and SEN pins are LOW, the part is in the RESET state. When the SPI bus is used in a dedicated fashion between the master and the MC144144, both the SEN and SMS pins would be tied HIGH. The RESET function would require that both of these pins be tied to the NRESET signal. To ensure synchronization, the master should send the serial synchronization signal after the reset is released.

When the SPI mode is used in a multiple peripheral environment, the SEN pin is used as the MC144144 enable signal. SMS could then be used for the NRESET signal as long as reset was only applied while SEN was LOW. In this case, there would be no need for the master to send a serial synchronization string after reset if there was at least 100 ns between the end of reset and the start of port enable.

A command string can be interrupted at any time and the port resynchronized by sending the serial sync signal or by the rising edge of SEN.

The SPI bus is a three–wire bus when used in a dedicated manner between the MC144144 and the master device. If other peripherals are connected to the bus, then the SEN pin must be used to place this device on the bus at the appropriate time. When SEN is LOW, the SDO pin will be three–state and transitions on the SCK and SDA pins will be ignored.

If data output is not required from the MC144144, then control can be accomplished using only the SCK and SDA pins. Since this type of operation precludes the ability to check the RDY bit, it is very important that commands be spaced by at least two frames (133 ms) to ensure that one command has been executed before initiating another.

The bus is controlled by the master device, which generates the serial clock (SCK) and initiates all actions. Clocking data in on SDA will simultaneously produce data out on SDO. The master should always check for the appropriate handshake signal before executing any command, other than NOP.

Writing to the part requires that the RDY bit be set while reading from the part requires checking the SS register to see if the DAV bit is set. Both of these bits are contained in the serial status (SS) register. Writing to the MC144144 will concurrently output the contents of the SS register, MSB first, unless other data is being output as a result of one of the READ commands. If it is desired to read the SS without executing a command, the NOP command can be written at any time, even if the serial status RDY bit is not set.

The RDY status bit is driven onto the SDO pin between command transmissions. The controlling MCU can test the state of this pin without clocking in order to determine if subsequent serial transfers are possible. The DAV bit can only be checked by outputing the contents of the SS register.

Writing to the SPI Bus

All write commands are either one or two byte commands. The number of data bytes to be received by the MC144144 is inherent in the command. If the master writes more bytes than expected, the command may be overwritten or corrupted by the extraneous bytes.

A write to the MC144144 should always be preceded by executing a status read to verify that the device is ready. The serial status is output by the device concurrent with the input of any command byte. If the RDY bit of the serial status register is set, the master device can write a new command.

The command and data bytes are written MSB first. The first byte of a two byte command is sent first. The bits are clocked into the MC144144 by placing the data on the SDA input and bringing SCK high.

Reading Data Using the SPI Bus

With the exception of the SS read, each read operation must be set up before the data can actually be read from the serial output registers of the device. Data is set up for a read operation either automatically or manually. XDS data is set up for READ automatically upon recovery by setting a valid XDS FILTER register selection. All other data read operations must be set up manually, using the READ SELECT commands RDS1 and RDS2. These commands load the selected data byte or pair of bytes into the serial output registers, set the SS register RD2 bit according to the number of data bytes requested, and set the serial status DAV bit to indicate availability of data.

The MC144144 SPI bus supports two and three byte read sequences. In SPI mode, the SS must be read before a read sequence is started so that the DAV and RD2 bits can be checked. The number of data bytes available is indicated by the state of the RD2 bit. The special command READ1 or READ2 is then used to read the one or two available data bytes. The serial status is clocked out during the write of the

READ1 or READ2 command. The data byte or bytes are then clocked out in sequence, MSB first, while NOP commands are written into the device. Data bits are clocked out on the rising edge of SCK. All available data bytes must be read to clear the DAV bit and permit subsequent reads.

The first bit of the first output byte is driven out on SDO following the rising edge of SCK on the last bit (LSB) of the READ1 or READ2 command.

COMMANDS AND REGISTERS

Serial Port Commands

Most of the MC144144 commands are common to both the I^2C and SPI modes. Some commands, such as NOP and the SPI read commands, are unique to SPI mode operation. In the I^2C mode, the commands must be contained within the start – slave address – etc., sequence. In the following command descriptions, the letter "h" following a command code designates hexadecimal notation.

RESET

RST = FBh, FCh, 00h — A three byte command sequence in SPI or I^2C mode.

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
1	1	1	1	1	0	1	X

The RESET command sequence will establish all the default settings but will not reset the serial port itself. This sequence can be entered without RDY being set.

NO OPERATION

NOP = 00h — A one byte command for use in SPI or I^2C mode.

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
0	0	0	0	0	0	0	X

The NOP command does not affect the status of the RDY bit in the serial status (SS) register and can be executed independent of the RDY status.

SERIAL SYNC BYTES

SSB = FFh, … **FFh, FEh —** Used in SPI mode.

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
1	1	1	1	1	1	1	X

SPI mode communications can be synchronized by sending a synchronizing data string to the part. This string should consist of at least two SSB bytes of FFh followed by one SSB byte of FEh. At the end of the FEh byte the port is ready for use.

CAPTION/TEXT DISPLAY MODE COMMANDS

CPTX = 10h – 1Fh — Caption and text display commands are one byte commands.

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
0	0	0	1	FLD	LANG	CPTX	DONOF

A data channel can be selected for display with the display either enabled (DEC ON) or disabled (DEC OFF). These commands will turn off an active XDS display mode.

CMD Byte	Data Channel and DEC ON	CMD Byte	Data Channel and DEC OFF
17	CC1	16	CC1
15	CC2	14	CC2
1F	CC3	1E	CC3
1D	CC4	1C	CC4
13	T1	12	T1
11	T2	10	T2
1B	T3	1A	T3
19	T4	18	T4

XDS AND MISCELLANEOUS DISPLAY MODE COMMANDS

DISP = 20h – 28h — XDS display commands are one byte commands.

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
0	0	1	0	0	AUTO	DISP	DONOF

These commands control the XDS display modes and the state of the 16 second erase timer. The 16 second erase timer is active only for both the caption and XDS display modes but not for text display mode.

CMD Byte	XDS Disp	16 Sec Timer
23	XDSG	ON
27	XDSG	OFF
21	XDSF	ON
25	XDSF	OFF
20	*	ON
24	*	OFF

* Does not affect the display mode currently in operation.

READ AND WRITE COMMANDS

Read Selects

RDS1 = 40h – 47h

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
0	1	0	AD4	AD3	AD2	AD1	AD0

A one byte command which is used to initiate a one byte read sequence by moving the contents of the register identified by the address field of the command, to the output register. Only addresses 0 – 7 are valid.

RDS2 = 60h – 66h

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
0	1	1	AD4	AD3	AD2	AD1	AD0

A one byte command which is used to initiate a two byte read sequence by moving the contents of the two consecutive registers, starting with the one identified by the address portion of the command, to the output registers and setting the RD2 bit in the SS register. Only addresses 0 – 6 are valid.

NOTE: For XDS data recovery, when the XDS filter register (see **Internal Register** section) is enabled for the desired packets, the internal program will automatically establish the two byte recovery mode and move the recovered data bytes to the output register.

Reads

READ1 = F8h — Command to read one byte in the SPI mode.

READ2 = F9h — Command to read two bytes in the SPI mode.

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
1	1	1	1	1	0	0	RD2

The READx commands do not affect the status of the RDY bit in the serial status (SS) register and can be executed independent of the RDY status.

In both serial communications modes, the DAV bit in the SS register indicates when data is available. When the RD2 bit is LOW, DAV is cleared on the rising edge of SCK at the LSB of the first data byte. When the RD2 bit is HIGH, DAV is cleared on the rising edge of SCK at the LSB of the second data byte. The RD2 bit is only valid if DAV is HIGH.

Reading in the I^2C mode is selected by the R/NW bit in the slave address byte. The first byte after the slave address byte will be SS followed by the data in output buffers A and B. If the instruction being executed is a one byte read, then the contents of buffer B will be all ones.

Write

WRx = C0h–DFh

CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
1	1	0	AD4	AD3	AD2	AD1	AD0

The WRITE commands require two bytes to execute. The first byte is the write command and includes the address being written to. The second byte will be the data byte.

OSD DISPLAY MODE COMMANDS

OSD commands are one and two byte commands. They are used to control the loading of data for OSD display and their presentation to the screen. Normally OSD display mode uses 15 TV lines per display row to enhance the screen appearance.

The one–byte commands are:

CMD Byte		Function
30h	(RETURN)	Carriage return for OSD when in TEXTSET mode.
31h	(CLRE)	OSD equivalent to delete to end of row (DER).
32h	(TEXTSET)	Establishes a text type of OSD display.
33h	(POPSET)	Establishes a pop–on type of OSD display.
36h	(FLIP)	OSD equivalent of pop–on caption end of caption (EOC).
37h	(OEDM)	OSD equivalent to erase displayed memory.
38h	(OENM)	OSD equivalent to erase non–displayed memory.

The two–byte commands are:

A0h rr POP ROW SEL	Sets display row and moves cursor to char column 1. The low order nibble of rr designates the display row. Bit 5 of rr specifies a double high row. For example: rr = 0Eh would select display row 14. rr = 23h would select display row three, double high.
A1h rr PHY ROW SEL	Sets the physical row, where the low order nibble of rr designates the physical row. rr can be any value from 00h to 0Fh.
A2h cc CURSOR SET	Places the cursor at the character position designated by cc, which can be any value from 00h to 20h (column 0 – 32). Zero is the PAC space.
A3h dd WRITE CHAR	Writes the data byte dd to the current cursor location and then increments the cursor.
A4h rr WRITE MAP	Maps the current physical row to the display row designated by the low nibble of the rr byte. Bit 4 of rr = 1 enables display of the row. Bit 5 of rr = 1 indicates a double high row.
A5h dd WRITE CHARD	Same as A3 command but specifies a double wide character.
A6h nn WAIT	Sets the RDY bit of SS and then suspends serial command execution for approximately the number of frames designated by the nn byte.

Figure 9 shows the two different character sets, graphics or extended, that share the address space C0h – FFh. The graphics character set is in force when the OSD display is in drop shadow mode (the default condition). The following two byte commands can be used to switch from the graphics characters to the extended characters and vice versa. An OSD screen can only use one set at a time.

84h 30h GRAPHICS	Sets the graphics character set in force.
8Ch 30h EXTENDED	Sets the extended character set in force.

INTERNAL REGISTERS

Information controlling the setup and operation of the MC144144 are maintained in several registers. The user may read or alter the contents of these registers as required.

Serial Status (SS) Register — Address = Not Required (see **Serial Communications Interface** section)

D7	D6	D5	D4	D3	D2	D1	D0
RDY	DAV	RD2	WOVR	INTR	ROVR	FLD	LOCK

D7 – RDY — Active HIGH, indicating that the port input buffer is empty. Only the NOP, RESET, and READ instructions may be sent if RDY is LOW.

D6 – DAV — Active HIGH, indicating that data is available to be read out.

D5 – RD2 — Signals the number of bytes available for output. LOW = 1 byte, HIGH = 2 bytes.

D4 – WOVR — Active HIGH, indicating a serial input data overrun.

D3 – INTR — Active HIGH, indicating that an interrupt other than DAV is pending.

D2 – ROVR — Active HIGH, indicating that the data available in the output buffer has not been read out and new data has been written over it.

D1 – FLD — Signals the current video field. LOW = Field 2, HIGH = Field 1.

D0 – LOCK — Active HIGH, indicating that the internal sync circuits are locked. Maybe used as an indication of the presence of a video signal.

Configuration Register — Address = 00h

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	VLK	HLK	MONO	TVS

D0 – TVS — Selects the television standard. HIGH selects PAL and LOW selects NTSC. The default is NTSC. When PAL is selected the display defaults to 15 TV lines per display row.

D1 – MONO — Selects monochrome operation. Active HIGH, indicating that character luminance will be output on the color pins. Default is LOW, selecting COLOR operation.

D2 – HLK — Selects the horizontal signal source to be used to lock the VCO. LOW = internal, HIGH = HIN. The default is internal.

D3 – VLK — Selects the vertical signal source to be used to establish vertical sync lock. LOW = internal, HIGH = VIN. The default is internal. When internal lock is enabled the VIN/INTRO pin will default to the INTRO output mode. Interrupts should not be selected in the interrupt mask register if VLK mode is used.

D4 – D7 — Reserved

Display Register — Address = 01h

D7	D6	D5	D4	D3	D2	D1	D0
O15	ODRP	CENH	C15	CDRP	TENH	T15	TDRP

D0 – TDRP — Selects drop shadow or full box in TEXT mode. HIGH = DROP SHADOW and LOW = BOX. The default is LOW.

D1 – T15 — Selects the number of TV lines per character row in a TEXT display. HIGH = 15 lines/row and LOW = 13 lines/row. The default is LOW.

D2 – TENH — Enables enhanced attributes for a TEXT display. HIGH = disabled, LOW = enabled. The default is LOW.

D3 – CDRP — Selects drop shadow or full box in CAPTION mode. High = DROP SHADOW and LOW = BOX. The default is LOW.

D4 – C15 — Selects the number of TV lines per character row in a CAPTION display. HIGH = 15 lines/row and LOW = 13 lines/row. The default is LOW.

D5 – CENH — Enables enhanced attributes for a CAPTION display. HIGH = disabled, LOW = enabled. The default is LOW.

D6 – ODRP — Selects drop shadow or full box in the OSD and XDS display modes. High = DROP SHADOW and LOW = BOX. The default is HIGH.

D7 – O15 — Selects the number of TV lines per character row in the OSD and XDS display modes. HIGH = 15 lines/row and LOW = 13 lines/row. The default is HIGH.

NOTE: OSD and XDS display modes always have enhanced attributes enabled.

H Position Register — Address = 02h

D7	D6	D5	D4	D3	D2	D1	D0
BLBX	HPOL	h5	h4	h3	h2	h1	h0

D0 – D5 = h0 – h5
Used to set the horizontal timing of the display. The default value in this register is 26h. Each count change represents a timing change of 330 ns. Lower numbers move the display to the RIGHT. Conversely, larger numbers move the display to the LEFT.

D6 – HPOL — Set the polarity to be used for locking to the HIN signal when in the EXT HLK mode. LOW = rising edge, HIGH = falling edge. The default is LOW.

D7 – BLBX — Designates color of BOX. HIGH = blue box and LOW = black box. The default is LOW.

Text Position Register — Address = 03h

D7	D6	D5	D4	D3	D2	D1	D0
y3	y2	y1	y0	x3	x2	x1	x0

D0 – D3 = x0 – x3
Sets the number of rows in the TEXT display. The default is 15 rows.

D4 – D7 = y0 – y3
Sets the base row of the TEXT display.

The default value in this register is set to FFh, which produces a 15 row display with base row 15. Entering a new value in this register can alter the size and placement of the TEXT display. For example, to produce an 8 row TEXT display with a base row of 12, this register should be set to 8Ch. If the value of the x and y bits result in a display where TEXT rows are off the top of the screen, then the first row of the TEXT display will start in row 1 and have the number of rows determined by the x value.

Line 21 Activity Register — Address = 04h

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	XDS	SCH

D0 – SCH — Indicates data being processed in the data channel selected for display. Will become inactive if no data is received for the selected channel within the previous 16 sec. HIGH = active, LOW = inactive. The reset state is LOW.

D1 – XDS— Indicates XDS data is being processed. Will become inactive if no XDS data is received within the previous 16 seconds. HIGH = active, LOW = inactive. The reset state is LOW.

XDS Filter Register — Address = 05h

D7	D6	D5	D4	D3	D2	D1	D0
s2	s1	s0	PUBL	MISC	CHAN	FUTR	CURR

D0 – CURR — Selects current class packets for output through the serial control port when XDS recovery has been enabled.

D1 – FUTR — Selects future class packets for output through the serial control port when XDS recovery has been enabled.

D2 – CHAN — Selects channel information class packets for output through the serial control port when XDS recovery has been enabled.

D3 – MISC — Selects miscellaneous class packets for output through the serial control port when XDS recovery has been enabled.

D4 – PUBL — Selects public service class packets for output through the serial control port when XDS recovery has been enabled.

D5 – D7 = s0 – s2 — Selects a set of secondary parameters, tabulated below, to be used in filtering the XDS data when XDS recovery has been enabled.

s2	s1	s0	Secondary Filter
0	0	0	All
0	0	1	Time Information Only
0	1	0	In Band Only
0	1	1	Out of Band Only
1	0	0	VCR Information
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Setting this register to 00h turns XDS data recovery off. Setting bits D0 through D4 enables XDS data recovery for the classes selected as qualified by the secondary filter action specified by bits D5 – D7. If Bits D0 – D4 are all set to 1, all classes of XDS data will be output (even reserved and undefined).

The time information only selection includes the time of day (TOD) and local time zone (LTZ) packets.

VCR information will select TOD, LTZ, net ID, local call letters, impulse capture, tape delay, composite 2, and out of band channel number packets for recovery.

Interrupt Request Register — Address = 06h

D7	D6	D5	D4	D3	D2	D1	D0
dTXT	dCAP	dXDS	dSCH	dLOK	EOF	DLE	res

D0 – res — Reserved.

D1 – DLE — Active HIGH, indicating that the data line has ended. This bit will clear in each field, a few lines after row 15.

D2 – EOF — Active HIGH, indicating that the video signal is currently at the end of a field. This bit will clear in each field, a few lines after row 15.

D3 – dLOK — Active HIGH, indicating that the state of the LOCK signal has changed. The SS register must be read to determine the current state.

D4 – dSCH — Active HIGH, indicating that a change in selected channel activity has occurred. The Line 21 activity register must be read in order to determine if the selected data channel is active.

D5 – dXDS — Active HIGH, indicating that a change in XDS activity has occurred. The Line 21 activity register must be read to determine if XDS data is active.

D6 – dCAP — Active HIGH, indicating that a change in a caption data channel activity has occurred. The caption activity register must be read to determine which caption data channels are active.

D7 – dTXT — Active HIGH, indicating that a change in a text data channel activity has occurred. The caption activity register must be read to determine which text data channels are active.

Except as noted for the case of bits D1 and D2 above, the master device must write a one to the appropriate bit in the interrupt request register to clear the interrupt.

Interrupt Mask Register — Address = 07h

D7	D6	D5	D4	D3	D2	D1	D0
dTXT	dCAP	dXDS	dSCH	dLOK	EOF	DLE	DAV

This register identifies which activities in the interrupt request register will be used to cause an interrupt. Setting a bit to a one enables the interrupt when the corresponding event becomes active. Setting all bits of this register to zero disables interrupts.

Caption Activity Register — Address = 08h

D7	D6	D5	D4	D3	D2	D1	D0
T4	T3	T2	T1	CC4	CC3	CC2	CC1

Activity Bits, CC1–T4 — Each bit will be set HIGH when a mode setting command for its data channel has been received. The bit will be cleared to the LOW state if no activity is detected in that data channel during the next 12 – 16 s or if there is a loss of lock.

XDS DATA RECOVERY

The MC144144 is able to recover extended data services (XDS) information from the input video signal. This data, formatted according to the Electronics Industries Association (EIA) recommended practice, EIA–608, can contain a wide variety of information about current and future programs, the channel currently tuned, other channels and miscellaneous data including time of day.

XDS data is only present in the even field. The MC144144 can recover XDS data even while performing its normal caption decoder or OSD functions.

XDS data packets are tagged according to a class/type system defined by EIA–608. The data may be filtered to extract only the classes of interest to the application. An additional level of filtering is provided that permits selection of certain groups of packets that are of use in specific applications. XDS filtering reduces the traffic on the serial bus, reduces the load of the TV/VCR control processor, and simplifies external XDS decoding.

XDS data recovery is enabled by selecting one or more classes in the XDS filter register. Optionally, a secondary filter code can be specified which further limits the packets to be recovered. Once XDS recovery is enabled filtered data pairs will be loaded into the serial output registers of the MC144144 immediately upon receipt. The DAV and RD2 bits of the serial status (SS) register will then go high, indicating the availability of two output bytes. The external TV control processor does not need to send a READ SELECT command in order to read these data bytes.

When the XDS filter register is set to zero (the default state) XDS recovery is disabled.

When XDS data recovery is enabled, the external controller should avoid performing any other read operation, except SS reads, in the beginning of field 2. This is most easily accomplished by using the end of field (EOF) or data line end (DLE) interrupt to locate the end of field 2 or the vertical blanking interval (VBI) of field 1, and then perform the READ SELECT and READ functions during this portion of the video frame. Commands other than READ SELECTS will not interfere with XDS data recovery regardless of their position in the video frame.

Some examples of WRITE commands that could be used to set the XDS FILTER register are shown below. The XDS Filter register bit assignments are defined in the **Internal Registers** section.

{C5,1F} All XDS packets recovered.

{C5,01} All current class packets recovered.

{C5,41} All In band, current class packets recovered.

{C5,62} All out of band, future class packets recovered.

{C5,28} Time information only recovered. Will extract the time of day (TOD) and local time zone (LTZ) packets from the miscellaneous class data.

{C5,9F} VCR Information recovered. Will select TOD, LTZ, net ID, local call letters, impulse capture, tape delay, composite 2, and out of band channel number packets for recovery.

ON–SCREEN DISPLAY

OSD Operation

The user can supply information for display in an OSD fashion through the serial port. In addition to all the normal and extended features of the VBI data display modes, OSD mode also has available added graphics characters, double high and double wide characters, and the ability to position the display anywhere on the screen with an adjustable (vertical) box size. The OSD display mode can use either 13 or 15 lines per row, with box or drop shadow. The default is 15 scan lines per row and drop shadow. Enhanced attributes are always enabled.

The 15 scan line per row display can only show 13 rows on–screen when in the NTSC mode. Rows 14 and 15 will be off–screen and should not be addressed. In the PAL mode all rows will be visible.

The 15 scan lines per row mode display can show the full graphic characters and accented capital letters and descenders without the potential overlap that would result from the 13 scan line per row display. If the OSD display mode is changed to a 13 scan line per row mode, the top two scan lines of any graphics or accented capital letter will be “ored” together with the bottom two scan lines from the row above. In 13 line – drop shadow mode this will also result in a side shadow effect. Graphics characters should not be used in the 13 line – drop shadow mode.

The OSD character set is shown in Figures 8 and 9. There are 256 possible addresses and Figure 8 shows the address map in the range 00h – BFh. This portion of the addressable space contains the control bytes and regular character set. Figure 9 shows the address map in the range C0h – FFh. These addresses are shared by the extended character set and the graphics character set. Any particular OSD screen can use one or the other of these sets of characters but not both.

The character set in force is controlled by the type of display mode being invoked. When drop shadow is being used, by default, the graphics character set will be displayed in response to an address in the C0h – FFh range. However, if a BOX display is used, the extended character set is invoked.

In either case the user can switch to the other set by means of the appropriate command, GRAPHICS or EXTENDED.

The VIN/INTRO pin serves as the input for a vertical pulse from the TV receiver when V lock = VIN mode is enabled. This permits an OSD display even when no video input is present. If this mode is not required the default state V lock = VIDEO should be active and this pin will then carry the INTRO output signal.

OSD Commands

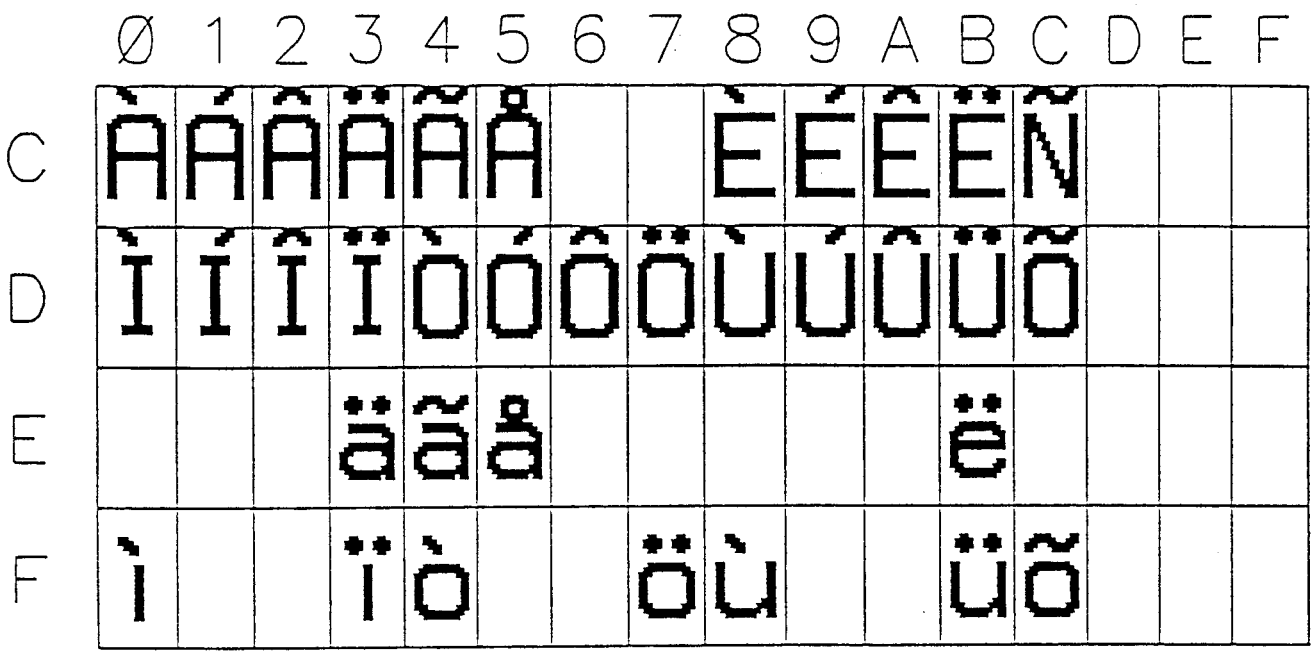
OSD commands are one and two byte commands. They are used to control the loading of data for OSD display and their presentation to the screen. Normally OSD display mode uses 15 TV lines per display row to enhance the OSD presentation.

The two byte commands enable direct access to any location on the display screen. The user may construct displays of his own choosing by using these commands. Each command byte pair consists of an instruction byte followed by a data byte.

In this document one and two byte commands are written as 1 or 2, two digit Hex values, separated by a comma, within curly braces. For example, the WRITE CHAR command for entering the letter A as a single width character would be shown as {A3,41}. This command would write the letter A to the current cursor position of the display row being addressed. Refer to the **Commands and Registers** and **XDS Data Recovery** sections for further details of the serial communications and the OSD commands.

The one byte commands provide a simple means of creating OSD displays using preset screen formats built into the part. These built–in modes provide the user with a simple way to generate OSD screens. Two preset display modes are available called POPSET and TEXTSET.

Figure 8.



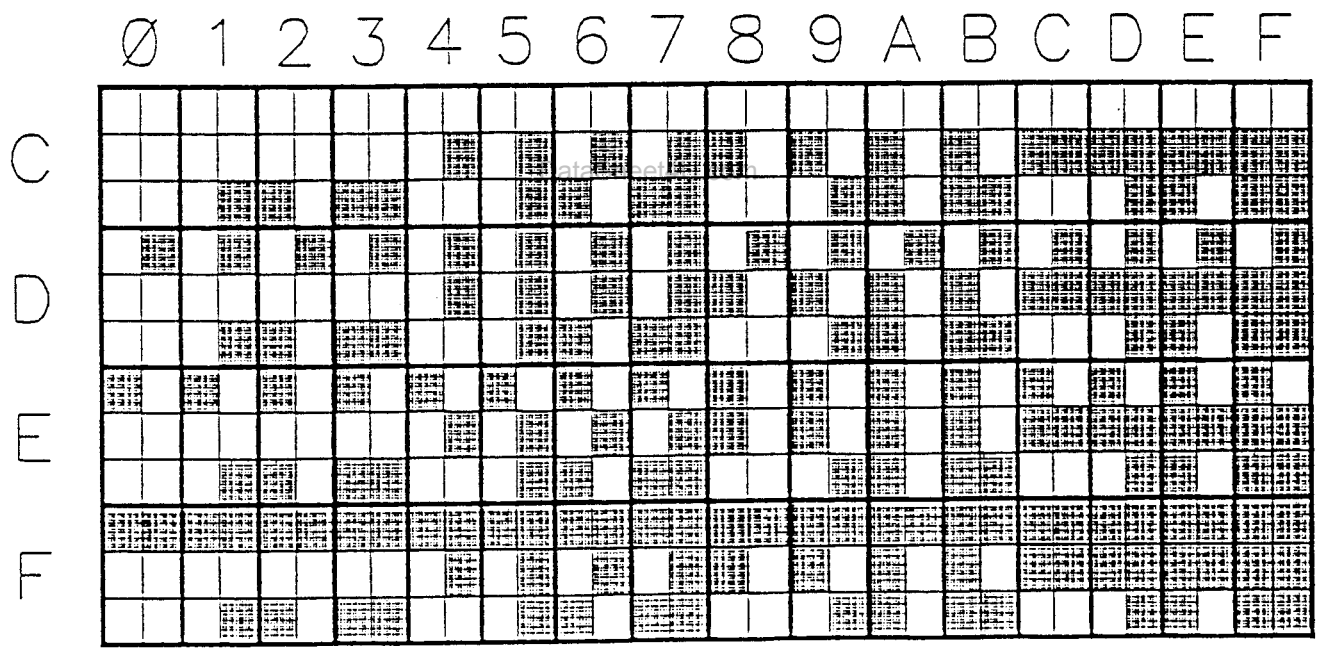


Figure 9.

Using POPSET

POPSET provides an OSD mode that operates in a fashion similar to the caption pop–on mode. The POPSET command organizes the memory into two eight–row blocks, one visible on–screen and the other off–screen. An OSD screen can then be created by loading the off–screen memory by the command sequence POP ROW SEL, WRITE CHAR .. WRITE CHAR .. POP ROW SEL .. WRITE CHAR .. WRITE CHAR. The data can then be presented with the FLIP command.

The following is an example of a command sequence that will create an OSD screen using the POPSET mode. It creates a typical menu screen used in television receivers. As noted earlier, in this document commands are written as 1 or 2, two digit Hex values, separated by a comma, within curly braces. A comment field is written following the command to describe the action of the command or sequence of commands, where appropriate. The comment field is identified by an * and anything following the * will be taken as a “comment”.

```
{33}        * select pop mode. Sets up the memory organization.
            *
            * The first block of cmds will display > VIDEO in double wide chars.
            * Each character is entered with the WRITE CHARD cmd.
            *
{A0,02}     * select poprow 2, cursor at char col 1
{A2,00}     * move cursor to 0
{A3,08}     * PAC for RED chars written in PAC location.
{A5,3e}     * Double wide char “>” will display in char col 1 & 2
{A3,02}     * Green mid code written to char col 3
{A5,56}     * “V” written to char col 4 & 5.
{A5,49}     * “I”
{A5,44}     * “D”
{A5,45}     * “E”
{A5,4f}     * “O”
            *
            * The next block of cmds will display  AUDIO in row 4 double width.
            *
{A0,04}     * select poprow 4, cursor in char col 1
{A2,03}     * cursor to char col 3
{A3,02}     * Green mid code written to char col 3
{A5,41}     * “A” written to char col 4 & 5.
{A5,55}     * “U”
{A5,44}     * “D”
{A5,49}     * “I”
{A5,4f}     * “O”
            *
            * The next cmds will display  TIME in row 6 with double wide chars.
            * Spacing is obtained without the A2 Cursor Set cmd to illustrate an alternate
            * means of column alignment.
            *
{A0,06}     * select poprow 6, cursor in char col 1
{A3,02}     * Green mid code written to char col 1
{A5,20}     * double wide space char written to char col 2 & 3
{A5,54}     * “T” written to char col 4 & 5.
{A5,49}     * “I”
{A5,4d}     * “M”
{A5,45}     * “E”
            *
            * SET UP will be displayed in row 8 using double wide chars
{A0,08}     * select poprow 8
{A2,03}     * cursor to 3
{A3,02}     * Green char
{A5,53}     * “S”
{A5,45}     * “E”
{A5,54}     * “T”
{A5,20}     * “ ”
{A5,55}     * “U”
{A5,50}     * “P”
            *
            * CLOSED CAPTION displayed in row 10 using double wide chars
            * The last letter, N, will appear in char col 30 & 31.
```

```
{A0,0a}     * select poprow a
{A2,03}     * cursor to 3
{A3,02}     * Green char
{A5,43}     * “C”
{A5,4c}     * “L”
{A5,4f}     * “O”
{A5,53}     * “S”
{A5,45}     * “E”
{A5,44}     * “D”
{A5,20}     * “ ”
{A5,43}     * “C”
{A5,41}     * “A”
{A5,50}     * “P”
{A5,54}     * “T”
{A5,49}     * “I”
{A5,4f}     * “O”
{A5,4e}     * “N”
            *
            * The line, Select: ENTER EXIT: MENU, will appear in row 12, starting in
            * char col 2. These will be single wide chars.
{A0,0c}     * select poprow c
{A3,06}     * CYAN char
{A3,53}     * “S”
{A3,65}     * “e”
{A3,6c}     * “l”
{A3,65}     * “e”
{A3,63}     * “c”
{A3,74}     * “t”
{A3,3a}     * “:”
{A3,20}     * “ ”
{A3,45}     * “E”
{A3,4e}     * “N”
{A3,54}     * “T”
{A3,45}     * “E”
{A3,52}     * “R”
{A3,20}     * “ ”
{A3,20}     * “ ”
{A3,45}     * “E”
{A3,78}     * “x”
{A3,69}     * “i”
{A3,74}     * “t”
{A3,3a}     * “:”
{A3,20}     * “ ”
{A3,4d}     * “M”
{A3,45}     * “E”
{A3,4e}     * “N”
{A3,55}     * “U”
            *
{36}        * FLIP cmd. Will flip memories, popping the full menu on–screen.
```


Using TEXTSET

TEXTSET provides an OSD mode that will paint on the screen in a manner similar to a TEXT mode display. The memory will be organized using the current information in the text position register and the display will follow the current setting in the display register. The default display parameters for OSD are 15 lines per row, drop shadow mode. The TEXTSET command can be followed by successive WRITE CHAR commands interspersed with the RETURN command at the appropriate points to paint on an OSD display starting at the top of the text window as set by the text position register and moving to the next line at each RETURN command. The display will scroll if a RETURN command is sent when at the bottom of the text window. A subsequent TEXTSET command will clear the screen and generate a new OSD screen.

The following example shows an OSD display generated using TEXTSET. This screen will paint on rather than pop on. Features like flash are included in the command sequence for demonstration purposes.

```
            * The TEXT display is first set to 4 rows at the bottom of the screen.
{C3,D4}     * set Textpos reg for base row 13, 4 rows
{C1,80}     * set OSD display for BOX mode, 15 lines/row
{C2,A6}     * set BOX to Blue, keep HPOS unchanged
            *
{32}        * select TEXTSET mode
            *
            * The next two cmds are used for positioning and color.
            *
{A2,05}     * cursor to char pos 5
{A3,08}     * mid code to make Red chars. Cursor moves to 6
            *
{A3,B9}     * mid code to start Flash, Cursor moves to 7
{A5,57}     * ‘W’ double wide, char col 7,8
{A5,41}     * ‘A’ double wide, char col 9,10
{A5,52}     * ‘R’ double wide, char col 11,12
{A5,4E}     * ‘N’ double wide, char col 13,14
{A5,49}     * ‘I’ double wide, char col 15,16
{A5,4E}     * ‘N’ double wide, char col 17,18
{A5,47}     * ‘G’ double wide, char col 19,20
{A5,20}     * ‘ ’ double wide, char col 21,22
            *
{30}        * Return moves cursor to next row, char pos 1
            *
{A2,00}     * Cursor to char pos 0
{A3,0A}     * PAC sets color to Yellow, cursor moves to char pos 1
{A3,54}     * ‘T’ single width, cursor moves to char pos 2
{A3,68}     * ‘h’
{A3,65}     * ‘e’
{A3,72}     * ‘r’
{A3,65}     * ‘e’
{A3,20}     * ‘ ’
{A3,69}     * ‘i’
{A3,73}     * ‘s’
{A3,20}     * ‘ ’
{A3,61}     * ‘a’
{A3,20}     * ‘ ’
{A3,74}     * ‘t’
{A3,6F}     * ‘o’
{A3,72}     * ‘r’
{A3,6E}     * ‘n’
{A3,61}     * ‘a’
{A3,64}     * ‘d’
{A3,6F}     * ‘o’
{A3,20}     * ‘ ’
{A3,69}     * ‘i’
{A3,6E}     * ‘n’
{A3,20}     * ‘ ’
{A3,74}     * ‘t’
{A3,68}     * ‘h’
{A3,65}     * ‘e’
{A3,20}     * ‘ ’
{A3,61}     * ‘a’
{A3,72}     * ‘r’
{A3,65}     * ‘e’
{A3,61}     * ‘a’
{A3,2E}     * ‘.’
            *
{30}        * Return moves cursor to next row, char pos 1
{A3,50}     *‘P’
{A3,6C}     *‘l’
{A3,65}     *‘e’
{A3,61}     *‘a’
```

```
{A3,73}     *‘s’
{A3,65}     *‘e’
{A3,20}     *‘ ’
{A3,74}     *‘t’
{A3,61}     *‘a’
{A3,6B}     *‘k’
{A3,65}     *‘e’
{A3,20}     *‘ ’
{A3,61}     *‘a’
{A3,6C}     *‘l’
{A3,6C}     *‘l’
{A3,20}     *‘ ’
{A3,6E}     *‘n’
{A3,65}     *‘e’
{A3,63}     *‘c’
{A3,65}     *‘e’
{A3,73}     *‘s’
{A3,73}     *‘s’
{A3,61}     *‘a’
{A3,72}     *‘r’
{A3,79}     *‘y’
            *
{30}
{A3,70}     *‘p’
{A3,72}     *‘r’
{A3,65}     *‘e’
{A3,63}     *‘c’
{A3,61}     *‘a’
{A3,75}     *‘u’
{A3,74}     *‘t’
{A3,69}     *‘i’
{A3,6F}     *‘o’
{A3,6E}     *‘n’
{A3,73}     *‘s’
{A3,20}     *‘ ’
{A3,69}     *‘i’
{A3,6D}     *‘m’
{A3,6D}     *‘m’
{A3,65}     *‘e’
{A3,64}     *‘d’
{A3,69}     *‘i’
{A3,61}     *‘a’
{A3,74}     *‘t’
{A3,65}     *‘e’
{A3,6C}     *‘l’
{A3,79}     *‘y’
{A3,2E}     *‘.’.
            *
            * At this point all 4 rows are on–screen. The following wait command will
            * hold the display for a period = (12x16)/30 seconds.
{a6,c0}     * wait for 6.4 seconds.
            *
            * Create a smooth scroll to clear the screen with the following 4 row sequence.
            *
{30}        * Return, first row.
{a6,0f}     * wait 15 frames
{30}        * Return second row.
{a6,0f}
{30}        * Return third row.
{a6,0f}
{30}        * Return fourth row.
{a6,0f}
            *
```

```
            * Create a new screen display
            *
{a3,74}     *‘t’
{a3,68}     *‘h’
{a3,69}     *‘i’
{a3,73}     *‘s’
{a3,20}     *‘ ’
{a3,77}     *‘w’
{a3,61}     *‘a’
{a3,73}     *‘s’
{a3,20}     *‘ ’
{a3,6f}     *‘o’
{a3,6e}     *‘n’
{a3,6c}     *‘l’
{a3,79}     *‘y’
{a3,20}     *‘ ’
{a3,61}     *‘a’
{a3,20}     *‘ ’
{a3,74}     *‘t’
{a3,65}     *‘e’
{a3,73}     *‘s’
{a3,74}     *‘t’
            *
{30}        * Return
            *
{a3,64}     *‘d’
{a3,6f}     *‘o’
{a3,6e}     *‘n’
{a3,27}     *‘’’
{a3,74}     *‘t’
{a3,20}     *‘ ’
{a3,70}     *‘p’
{a3,61}     *‘a’
{a3,6e}     *‘n’
{a3,69}     *‘i’
{a3,63}     *‘c’
{a3,2e}     *‘.’
```


Using the Wait Command

The WAIT command will suspend serial port communications for a period of time. The TEXTSET example above used the WAIT command in two ways. First to hold a display on–screen for a period of time before taking a second action. Then it was used to create a smooth scroll by timing the wait to the scroll rate.

The WAIT command can also be used to control the appearance of two OSD displays in sequence without tying up the master device for the total display time. In the following example, the POPSET mode is used to pop on two sequential menu screens with a built in pause between the two displays. In this case the WAIT is placed just before the last FLIP command. This allows the entire command sequence to be sent to the MC144144 at once, since the RDY bit will be set by the WAIT command, thus allowing the FLIP to be input as well.

The command sequence would be as follows:

```
{33}        * select pop mode
{ .. }      * screen generation commands for first display
{ .. }      *    ”      ”      ”      ”          ”
{ .. }      *    ”      ”      ”      ”          ”
            *
{36}        * FLIP cmd. Will flip memories, popping the first menu on–screen.
            *
{38}        * OENM, to insure non–displayed memory is erased.
            *
{ .. }      * screen generation commands for second display
{ .. }      *    ”      ”      ”      ”          ”
{ .. }      *    ”      ”      ”      ”          ”
            *
{A6,C0}     * wait 6 seconds
{36}        * FLIP cmd. Will flip memories, popping the second menu on–screen.
```

Using the Graphics Character Set

The following example creates an OSD screen which illustrates several features of the MC144144 including the use of the graphics character set to generate a large font word. The particular features shown are purely for demonstration purposes and not intended to suggest a particular application.

For the sake of brevity, the “text” to be displayed will be shown as a string within quotes rather than as the actual command sequences required. Single quotes, ’, will signify standard characters while double quotes, ”, will signify double wide characters.

```
{33}        * select pop mode
            *
{A0,02}     * select poprow 2
{A2,00}     * Move cursor to 0
{A3,03}     * PAC, GREEN chars
            *
‘THIS IS A DEMONSTRATION OF OSD’
            *
{A0,03}     * select poprow 3
{A2,00}     * cursor to 0
{A3,08}     * PAC, RED char
            *
‘The MC144144 has many features’
            *
{A0,04}     * select poprow 4
{A2,00}     * cursor to 0
{A3,04}     * Blue char
            *
‘besides displaying Captions.’
            *
{A0,06}     * select poprow 6
{A2,00}     * Move cursor to 0
{A3,07}     * PAC, Cyan Underlined
            *
‘Color and Underline may be used’
            *
{A0,08}     * select poprow 8
{A2,00}     * Move cursor to 0
{A3,0a}     * PAC, Yellow chars
            *
” DOUBLE WIDE”
            *
{A0,09}     * select poprow 9
{A2,00}     * Move cursor to 0
{A3,0c}     * PAC, Magenta chars
            *
‘Graphics can be created like’
            *
            * The next group of cmds will use Graphic Char patterns to make the two row
            * word HELLO. The data byte of the WRITE CHAR cmd is the address
            * location for the graphic cell desired as shown in Fig. 5.
            *
{A0,0b}     * select poprow 11
{A2,00}     * Move cursor to 0
{A3,06}     * PAC, Cyan chars
            *
{84,30}     * Set Graphics mode in case another user had changed it earlier.
            *
{A5,20}     * “ ”
{A5,20}     * “ ”
{A5,20}     * “ ”
{A5,20}     * “ ”
{A3,20}     * “ ”
{A3,eb}     * Graphic Cell
{A3,ea}     * Graphic Cell
{A3,20}     * “ ”
{A3,fb}     * Graphic Cell
```

```
{A3,20}     * “ ”
{A3,ea}     * Graphic Cell
{A3,20}     * “ ”
{A3,ea}     * Graphic Cell
{A3,20}     * “ ”
{A3,fa}     * Graphic Cell
{A3,f5}     * Graphic Cell
            *
{A0,0c}     * select poprow 12
{A2,00}     * Move cursor to 0
{A3,06}     * PAC, Cyan chars
            *
{A5,20}     * “ ”
{A5,20}     * “ ”
{A5,20}     * “ ”
{A5,20}     * “ ”
{A3,20}     * “ ”
{A3,ea}     * Graphic Cell
{A3,ea}     * Graphic Cell
{A3,20}     * “ ”
{A3,eb}     * Graphic Cell
{A3,20}     * “ ”
{A3,eb}     * Graphic Cell
{A3,20}     * “ ”
{A3,eb}     * Graphic Cell
{A3,20}     * “ ”
{A3,eb}     * Graphic Cell
{A3,d7}     * Graphic Cell
            *
{36}        * flip
            *
```


Manual Row Mapping and Control

For most OSD displays the POPSET, POP ROW SEL, FLIP, TEXTSET, and RETURN commands should be used to control row positioning.

TEXTSET mode provides automatic row allocation from top to bottom of the screen with all rows continuously visible. Additionally, TEXTSET screens have a definable vertical window size and position and support automatic text scrolling at the bottom of the window.

POPSET screens are created in off–screen memory while the previous screen is displaying. Up to eight rows of characters can be defined. These rows can be mapped to any of 15 display rows using the POP ROW SEL command. Double high rows may also be defined with POP ROW SEL. The FLIP command is then used to “pop–on” up to eight rows of characters replacing the previous screen. The off–screen rows may be mapped to the same row numbers as the on–screen rows.

In some applications it may be necessary to access the display hardware at a lower level to achieve special screen effects. Examples of these special situations include the following:

- More than eight on–screen rows required in a “pop–on” style screen
- Characters need to be added dynamically to an on–screen display
- On–screen rows need to be dynamically moved, disabled or enabled

The MC144144 supports manual screen mapping and display control commands to handle these special applications. These commands allow each of the 16 physical rows of character memory implemented in the device to be mapped to any of 15 display row positions. Additionally the 16 physical rows can be set for single or double height and independently enabled and disabled. Manual row mapping and control commands should only be used in the POPSET OSD mode.

The procedure for manual row control is as follows:

1. Use the POPSET command to select the OSD pop–up mode. This command prepares the MC144144 for OSD input, clears the row maps, and erases character memory.
2. Select a physical row (0 through 15) using the PHY ROW SEL command.
3. Use the WRITE MAP command to set the display row (1 through 15), double high bit, and enable bit of the selected physical row.

The CURSOR SET, WRITE CHAR, and WRITE CHARD commands are used to position the cursor and write the characters in the selected physical row.

A physical row may be reselected at any time to change its characters, row maps, double high mode, or enable status. For example, it may be desirable to load several rows of characters into physical memory without enabling them. All of the rows could then be made to “pop” onto the screen all at once by setting their enable bits.

The following example uses manual row mapping and control to write three rows of characters. The first row is a double high row that is enabled before the characters are sent. This allows the characters to “paint” onto the screen as they are received. The second and third row are not initially mapped or enabled when the characters are written. They are then mapped and enabled after a two second pause. A new row is then created off–screen to replace the third row. Finally, after a 2 s pause the second row is moved to a new display row, the original third row is disabled and the new third row is mapped and enabled.

```
{33}        * select POPSET mode
            *
{A1,00}     * select physical row 0
{A4,31}     * map it to display row 1, enable, double
{A2,02}     * cursor to 1
{A3,02}     * green
            * double wide text
”The First Row ”
            *
{A1,01}     * select physical row 1
{A2,00}     * cursor to 0
{A3,0a}     * yellow
            * single wide text
’These two rows are’
            *
{A1,07}     * select prow 7
{A2,00}     * cursor to 0
{A3,06}     * cyan
            * Single wide text
’enabled after a pause’
            *
{A6,40}     * wait 2 seconds
            *
            * do the map and enable
            *
{A1,01}     * select physical row 1
{A4,16}     * map it to display row 6, enable
            *
{A1,07}     * select prow 7
{A4,17}     * map it to drow 7, enable
            *
            *
            * prepare a new row to replace row 7
            *
{A1,08}     * select physical row 8
{A2,00}     * cursor to 0
{A3,06}     * cyan
            * Single wide text
’moved after a pause’
            *
{A6,40}     * wait 2 seconds
            *
            * make the modified display
{A1,01}     * select physical row 1
{A4,1A}  * map it to display row 10, enable, double
{A1,07}     * select prow 7
{A4,00}     * disable it
{A1,08}     * select prow 8
{A4,1B}     * map it to row 11,enable, double
```

BLOCK DIAGRAM DESCRIPTION

The MC144144 is designed to process both fields of Line 21 of the television VBI and provide the functional performance of a Line 21 closed–caption decoder and extended data service decoder. It requires two input signals, composite video and a horizontal timing signal (HIN), and several passive components for proper operation. A vertical input signal is also required if OSD display mode is desired when no video signal is present. The decoder performs several functions, namely extraction of the data from Line 21, separation of the normal Line 21 data from the XDS data, display of the selected data, and outputting of the XDS data.

The block diagram is shown at the beginning of this data sheet.

INPUT SIGNALS

The composite video input should be a signal which is nominally 1.0 Vp–p with sync tips negative and band limited to 600 kHz. The MC144144 will operate with an input level variation of at least ± 3 dB.

The HIN input signal is required to bring the VCO close to the desired operating frequency. It must be a CMOS level signal. The HIN signal can have positive or negative polarity and is only required to be within 3% of the standard H frequency. When configured for EXT HLK operation, this signal should correspond to the H flyback signal.

The timing difference between HIN rising edge and the leading edge of composite sync (of VIDEO input) is one of the factors which will effect the horizontal position of the display. Any shift resulting from the timing of this signal can be compensated for with the horizontal timing value in the H position register.

VIDEO INPUT SIGNAL PROCESSING

The comp video input is ac coupled to the IC where the sync tip is internally clamped to a fixed reference voltage by means of a dual clamp. Initially, the unlocked signal is clamped using a simple clamp. Improved impulse noise performance is then achieved after the internal sync circuits lock to the incoming signal. Noise rejection is obtained by making the clamp operative only during the sync tip. The clamped composite video signal is fed to both the data slicer and sync slicer blocks.

The data slicer generates a clean CMOS level data signal by slicing the signal at its midpoint. The slice level is established on an adaptive basis during Line 21. The resultant value is stored until the next occurrence of that Line 21. A high level of noise immunity is achieved by using this process.

The sync slicer processes the clamped comp video signal to extract comp sync. This signal is used to lock the internally generated sync to the incoming video when the video lock mode of operation has been enabled. Sync slicing is performed in two steps. In the non–locked mode, the sync is sliced at a fixed offset level from the sync tip. When proper lock operation has been achieved, the slice level voltage switches from a fixed reference level to an adaptive level. The slice level is stored on the sync slice capacitor, CSYNC.

The data clock recovery circuit operates in conjunction with the digital H lock circuit. They produce a 32 H clock signal (DCLK) that is locked in phase to the clock run–in burst portion of the sliced data obtained from the data slicer. When Line 21 code appears, DCLK phase lock is achieved during the clock run–in burst and used to reclock the sliced data. Once phase lock is established it is maintained until a change in video signal occurs.

The digital H lock circuit produces the video timing gates, PG, STG, etc., which are locked in phase with HSYNC, the video timing signal, no matter which H lock mode is used in the display generation circuits. This independent phase lock loop is able to respond quickly to changes in video timing, without concern for display stability requirements.

VCO AND ONE SHOT

All internal timing and synchronizing signals are derived from the on–board 12 MHz VCO. Its output is the dot Clk signal used to drive the horizontal and vertical counter chains and for display timing. The one shot circuit produces a horizontal timing signal derived from the incoming video and qualified by the copy guard logic circuits.

The VCO can be locked in phase to two different sources. For television operation, where a good horizontal display timing signal is available, the VCO is locked to the HIN input through the action of the phase detector (PH2). When a proper HIN signal is not available, such as in a VCR, the VCO can be locked to the incoming video through the phase detector (PH1). In this case the frequency detector (FR) circuit is activated as required to bring the VCO within the pull–in range of PH1.

TIMING AND COUNTING CIRCUITS

The dot Clk is first divided down to produce the character timing clock CHAR CLK. This signal is then further divided to generate the horizontal timing signals: H, 2H, and HSQR. These timing signals are used in the data output (display) circuits.

The H signal is further divided in the LINE and FLD CNTR to produce the various decodes used to establish vertical lock and to time the display and control functions required for proper operation. The H signal is also used to generate the smooth scroll timing signal for display.

The V lock circuits produce a noise–free vertical pulse derived from the horizontal timing signal. When user selects video as the vertical lock source, the internal synchronizing signals are phased up with the incoming video by comparing the internally generated vertical pulse to an input vertical pulse derived from the comp sync signal provided by the sync slicer. In the vertical lock set to VIN mode the VIN signal is used in place of the signal derived from comp sync. In either case, when proper phasing has been established, this circuit outputs the LOCK signal which is used to provide additional noise immunity to the slicing circuits.

The LOCKed state is established only after several successive fields have occurred in which these two vertical pulses remain in sync. Once LOCKed, the internal timing will flywheel until such time as the two vertical pulses lose coincidence for a number of consecutive fields. Until LOCK is established, the decoder operates on a pulse for pulse basis.

COMMAND PROCESSOR

The command processor circuit controls the manipulation of the data for storage and display. It processes the control port input commands to determine the display status desired and the data channel selected. During the display time (lines 43 – 237), this information is used to control the loading, addressing and clearing of the display RAM and the operations of the character ROM and output logic circuits.

During data recovery time (TV lines 21 – 42), the command processor, in conjunction with the data recovery circuits, recovers the XDS data and the data for the selected data channel. Data is sent to the RAM for storage and display and/or to the serial port, as appropriate. Where necessary, the command processor converts the input data to the appropriate form.

OUTPUT LOGIC

The output logic circuits operate together to generate the output color signals RED, GREEN, and BLUE and the Box signal. When MONOchrome mode is selected all three color outputs will carry the luminance information. These outputs are positive output logic signals.

The character ROM contains the dot pattern for all the characters. The output logic provides the hardware underline, graphics characters, and the italics slant generator circuits. The smooth scroll display is achieved by the smooth scroll counter logic controlling the addressing of the character ROM.

DECODER CONTROL CIRCUIT

The decoder control circuit block is the user's communications port. It converts the information provided to the control port into the internal control signals required to establish the operating mode of the decoder. This port can be operated in one of two serial modes. The SMS pin is used to establish the serial control mode to be used.

In the two–wire (I^2C) control mode, the MC144144 will respond to its slave address for both the read and write conditions. If the read bit is low (indicating a WRITE sequence) then the MC144144 will respond with an acknowledge. The master should then send an address byte followed by a data byte. If the read bit is high (indicating a READ sequence) then the MC144144 will respond with an acknowledge followed by a status byte then a data byte. Read data will only be available through indirect addressing. Write addressing will have both indirect and direct modes. The busy bit in the status byte will indicate if the write operation has been completed or if read data is available.

The SPI mode is a three–wire bus with the MC144144 performing as the slave device. Communications is synchronized by the SCK signal generated by the master. Typically, the serial data output is transmitted on the falling edge of SCK and the received data is captured on the rising edge of SCK. All data is exchanged as eight–bit bytes.

VOLTAGE/CURRENT REFERENCE

The voltage/current reference circuit uses an externally connected resistor to establish the reference levels that are used throughout the IC. The use of an external resistor provides improved internal precision at low additional cost.

PIN DESCRIPTIONS

INPUTS

Video (Pin 7)

Composite NTSC video input, 1.0 Vp–p (nom), band limited to 600 kHz. Circuit will operate with signal variation between 0.7 – 1.4 Vp–p. The polarity is sync tips negative. This signal pin should be ac coupled through a 0.1 μF capacitor and driven by a source impedance of 470 Ω or less.

HIN (Pin 5)

Horizontal sync input at CMOS levels. When the part is used in the VIDEO LOCK mode, this signal pulls the on–chip VCO within the proper range. The circuit uses the frequency of this signal which must be within ± 3% of F_h but can be of either polarity. When used in the H LOCK mode the VCO phase locks to the rising edge of this signal. The HPOL bit of the H position register can be set to operate with either polarity of input signal. This is usually the H flyback signal. The timing difference between HIN rising edge and the leading edge of composite sync (of VIDEO input) is one of the factors which will affect the horizontal position of the display. Any shift resulting from the timing of this signal can be compensated for with the horizontal timing value in H position register.

SMS (Pin 6)

Mode select pin for the serial control port. When this input is at a CMOS HIGH state (1) the serial control port will operate in the SPI mode. When the input is LOW (0), the serial control port will operate in the I^2C slave mode. In the I^2C mode, the SEN pin must be tied HIGH (see **Reset Operation** discussion below).

SEN (Pin 4)

Enable signal for the SPI mode operation of the serial control port. When this pin is LOW (0), the SPI port is disabled and the SDO pin is in the high–impedance state. Transitions on the SCK and SDA pins are ignored. SPI mode operation is enabled when this pin is HIGH (1).

SCK (Pin 15)

Input pin for serial clock signal from the master control device. In I^2C mode operation the clock rate is expected to be within I^2C limits. In SPI mode, the maximum clock frequency is 10 MHz.

RESET OPERATION

When the SMS and SEN pins are both in the LOW (0) state, the part will be in the RESET state. Therefore, in the I^2C mode the SEN pin can be used as an NRESET input. When SPI mode is used, if three–wire operation is desired, both SMS and SEN can be tied together and used as the NRESET input. In either mode, NRESET must be held LOW (0) for at least 100 ns. Refer to **XDS Data Recovery** for further details.

INPUT–OUTPUT

VIN/INTRO (Pin 13)

EXT VLK Mode: In this mode of operation the internal vertical sync circuits will lock to the VIN input signal applied at this pin. The part will lock to the rising or falling edge of the signal in accordance with the setting of the V polarity command. The default is rising edge. The VIN pulse must be at least 2 lines wide.

INTRO Mode: When configured for internal vertical synchronization, this pin will be an output pin providing an interrupt signal to the master control device in accordance with the settings in the interrupt mask register.

SDA (Pin 14)

When the serial control port has been set to I^2C mode operation, this pin serves as the bidirectional data line for sending and receiving serial data. In SPI mode operation it operates as serial data input. SPI mode output data is available on the SDO pin.

OUTPUTS

SDO (Pin 16)

Provides the serial data output when SPI mode communications have been selected. This pin is not used in I^2C mode operation.

BOX (Pin 17)

Black box keying output. This active HIGH, CMOS level signal is used to key in the black box in the captions/text displays. This output will be in the high–impedance state when the background attribute has been set to semi–transparent.

RED, GREEN, BLUE (Pins 18, 2, 3)

Positive acting, CMOS levels signals.

Color Mode: Red, green, and blue character video outputs for use in a color receiver.

Mono Mode: All three outputs carry the character luminance information.

EXTERNAL COMPONENTS

CSYNC (Pin 8)

Sync slice level. A 0.1µF capacitor must be tied between this pin and analog ground (V_{SS}(A)). This capacitor stores the sync slice level voltage.

LPF (Pin 9)

Loop filter. A series RC low–pass filter must be tied between this pin and analog ground (V_{SS}(A)). There must also be a second capacitor from the pin to V_{SS}(A). Values for the three parts to be specified.

RREF (Pin 10)

Reference setting resistor. Must be a 10 kΩ, 2% resistor.

POWER SUPPLY

V_{DD} (Pin 12)

The voltage on this pin is nominally 5.0 V and may range between 4.75 to 5.25 V with respect to the V_{SS} pins.

V_{SS} (Pins 1 and 11)

These pins are the lowest potential power pins for the analog and digital circuits. They are normally tied to system ground.

The recommended printed circuit pattern for implementing the power connection and critical components will be supplied at a later date.

APPLICATIONS INFORMATION

PCB DESIGN

To maximize the performance of the MC144144, noise should be kept to a minimum. Good printed circuit board design will enhance the operation of the MC144144. Separate analog and digital grounds will reduce noise and decoding errors. In addition, separate filters on V_{DD}(A) and V_{DD}(D) will also help to minimize noise and decoding errors. Sufficient decoupling and short leads will also improve performance.

When designing mixed analog/digital printed circuit boards, separate ground planes for digital ground and analog ground should be employed. Large switching currents generated by digital circuits will be amplified by analog circuitry and can quickly make a circuit unusable. Digital oscillators can become a source of EMI (electromagnetic interference) problems. Care should be taken to ensure analog ground does not inadvertently become part of the digital ground. The analog and digital grounds should be connected together at only one point. This should be the V_{DD}(A) and V_{DD}(D) pins on the MC144144 if possible. Additionally, when interconnecting several printed circuit boards together, care must be taken to ensure cabling does not interconnect digital and analog grounds together to produce a path for digital switching currents through analog ground.

When using any device that combines digital and analog circuitry, such as the MC144144, ground planes are desirable. Loosely interconnected traces and/or random areas of ground strewn around the printed circuit board are inadequate for high performance circuitry. While distribution of V_{DD}(A) and V_{DD}(D) can be done by bussing, to do so with the ground system is disastrous. Stray ground inductance can increase radiation and make EMI suppression very difficult.

A 1–inch long conductor is an 18 nH inductor. The cross sectional area of the conductor affects the exact value of the inductance, but for most PCB traces this is approximately correct. If the ground system is composed of traces or clumps of ground loosely interconnected, it will be inductive. The amount of inductance will be proportional to the length of the conductors making up the ground. This inductance cannot be decoupled away. It must be designed out.

A CMOS device exhibits a characteristic input capacitance of about 10 pF. If this gate is driven by a digital signal that switches 2.5 V in a period of 5 ns, the equation for the average current flowing during the switching time will be:

$$I_{AV} = Cdv/dt.$$

A voltage change of 2.5 V in 5 ns requires an average current of 5 mA. If we assume a linear ramp starting from zero, the total change in current will be 10 mA. The change in current per nanosecond per gate can be found by dividing the change in current by the time

$$10\ mA/5\ ns = 2\ mA/ns.$$

For a device with outputs driving one gate for each output,

$$di/dt = 16 \times 2\ mA/ns = 32\ mA/ns.$$

If the above 1–inch wire is in this current path, then the voltage dropped across it can be found from the formula

$$v = Ldi/dt = 18\ nH \times 32\ mA/ns = 0.576\ V.$$

If the inductor is in the ground system, it is in the signal path. The voltage generated by the switching currents through this inductor will be added to the signal. At best it will be superimposed on the analog signal as unwanted noise. At worst, it can render the entire circuit unusable. Even the digital signal path is not immune to this type of signal. It can false trigger clock circuits causing timing errors, confuse compara-

tor type circuits, and cause digital signals to be misinterpreted as wrong values.

When laying out the PCB, use electrolytic capacitors of sufficient size at the power input to the printed circuit board. Adding low ESR (effective series resistance) decoupling capacitors of about 0.1 mF capacitance between V_{DD}(A) and ground and V_{DD}(D) and ground at the device power pins will help reduce noise in general, and also reduce EMI and ESD (electrostatic discharge) susceptibility. Implementation of a good ground plane ground system can all but eliminate the type of noise described above.

To summarize, use sufficient electrolytic capacitor filtering, make separate ground planes for analog ground and digital ground, tie these grounds together at one and only one point, keep the ground planes as continuous and unbroken as possible, use low ESR capacitors of about 0.1 mF capacitance on V_{DD}(A) and V_{DD}(D) at each device, and keep all leads as short as possible.

EMI SUPRESSION

When using ICs in or near television receiver circuits, EMI (electromagnetic interference) and subsequent unwanted display artifacts and distortion are probable unless adequate EMI suppression is implemented. A common misconception is that some offending digital device is the culprit. This is erroneous in that an IC itself has insufficient surface area to produce sufficient radiation. The device, while it is the generator of interfering signals, must be coupled to an antenna before EMI is radiated. The source for the EMI is not the IC which generates the offending signals but rather the circuitry which is attached to the IC.

Potential EMI signals are generated by ***all*** digital devices. Whether they become a nuisance is dependent upon their frequency and whether they have a sufficient antenna. The frequency and number of these signals is affected by both circuit design within the IC and the manufacturing process. Device speed is also a major contributor of potential EMI. Because the design is determined by the anticipated application, the manufacturing process is fixed and the drive for speed ever increasing, the only effective point to implement EMI suppression is in the PC board design. The PC board usually is the antenna which radiates the EMI. The most efficient method of minimizing EMI radiation is to minimize the efficiency of this antenna.

The most common cause of inadequate EMI suppression lies with the ground system of the suspected digital devices. As pointed out previously, di/dt transitions can be significant in digital circuits. If the di/dt transitions appear in the ground system and the ground system is inductive, the harmonics present in these transitions are a source of potential EMI signals. The unfortunate result of putting digital devices on a reactive ground system is guaranteed EMI problems.

The area which should be addressed first as a potential EMI source is the ground. Without an adequate ground system, EMI cannot be effectively reduced by decoupling. If at all possible, the ground should be a complete unbroken plane. Figure 10 shows two examples of relieving ground around device pins. When relieving vias and plated through holes, large areas of ground loss should be avoided. When the relief pattern is equal to half the distance between pins, over–etching and process errors may remove ground between pins. If sufficient ground around enough pins is removed, the ground system can become isolated or nearly isolated “patches” which will appear inductive. If ground, such as the vicinity of an IC, must be removed, replace with a cross hatch of ground lines with the mesh as small as possible.

If a single unbroken plane can be devoted to the ground system, EMI can usually be sufficiently suppressed by using ferrite beads on suspect EMI paths and decoupling with adequate values of capacitors. The value of the decoupling capacitor depends on the frequency and amplitude of the offending signals. Ferrite beads are available in a wide variety of shape, size, and material to fit virtually any application.

Choose a ferrite bead for desired impedance at the desired frequency and construct a low pass filter using one or more appropriate capacitors in a “L”, “T”, or “PI” arrangement. Use only capacitors of low inductive and resistive properties such as ceramic or mica. Install filters in series with each IC pin suspected of contributing offending EMI signals and as close to the pin as possible. Analysis using a spectrum analyzer can help determine which pins are suspect.

Where PC board costs constrain the number of layers available, and if the EMI frequencies are far removed from the frequencies of operation, ferrite beads and decoupling capacitors may still be effective in reducing EMI emissions. Where only two (or in some cases, only one!) layer is used, the ground system is always reactive and poses an EMI problem. If the offending EMI and normal operating frequency differ sufficiently, filtering can still work.

An “island” is constructed in the ground system for the digital device using ferrite beads and decoupling capacitors as shown by the example in Figure 11. The ground must be cut so that the digital ground for the device is isolated from the rest of the ground system. Next choose a ferrite bead of the appropriate value. Install this bead between the isolated ground and the ground system. Install low pass filters in all suspect lines with the capacitor closest to the device pin connected to the isolated ground in all signal lines where EMI is suspect. Also cut the power to the device and insert a ferrite bead as shown in Figure 11. Finally, decouple the device between the power pin(s) and isolated ground pin(s) using a low inductive/resistive capacitor of adequate value.

The methods described above will work acceptably when the EMI frequency and the frequency of operation of the device generating the EMI differ greatly. Where the EMI is disturbing the high VHF or UHF channels and the device generating the EMI is operating within the NTSC/PAL bandwidth, the energy contained in the harmonics generating the EMI is situated well above the operating frequency and suppressing this type of EMI poses no great problem. However, if the EMI is present on low VHF channels and/or the operation of the device is outside the NTSC/PAL bandwidth, such as a 2X pixel clock or 4fsc oscillator, compromise between video quality and suppression complexity is usually required to obtain an acceptable solution. For those cases where the operating frequency of the device is very near the frequency of the EMI disturbance, careful attention to PCB layout, multiple layer PCB, and even shielding may be necessary to obtain an acceptable design.

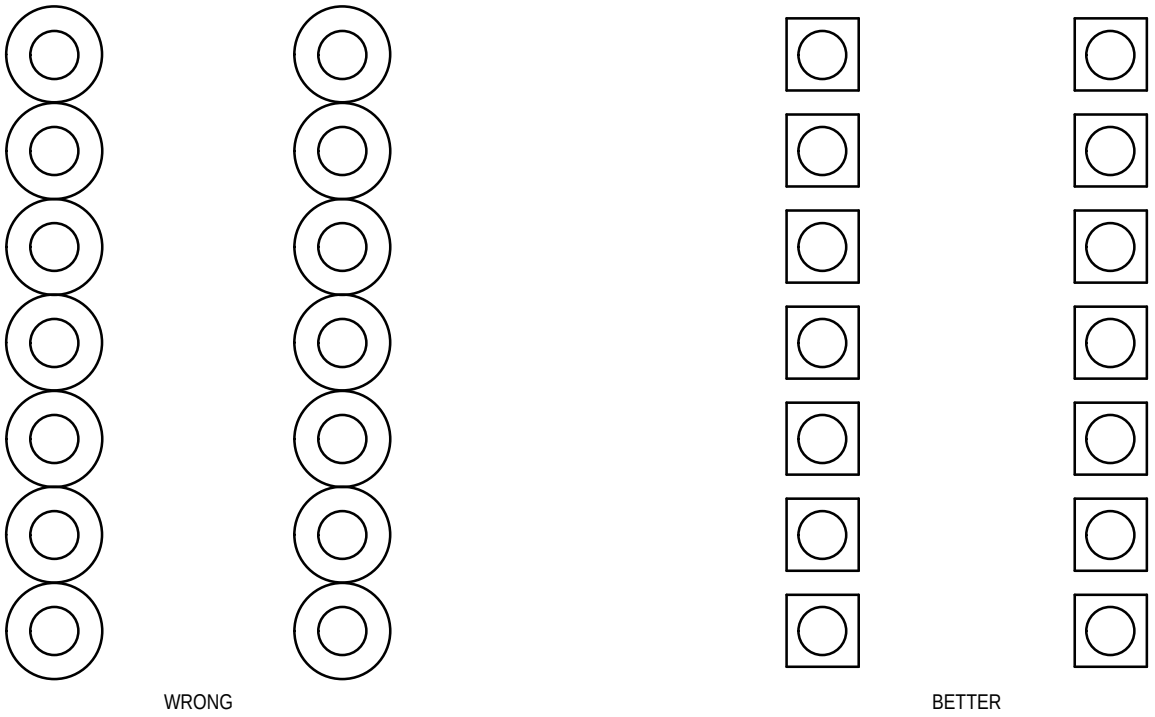


Figure 10.

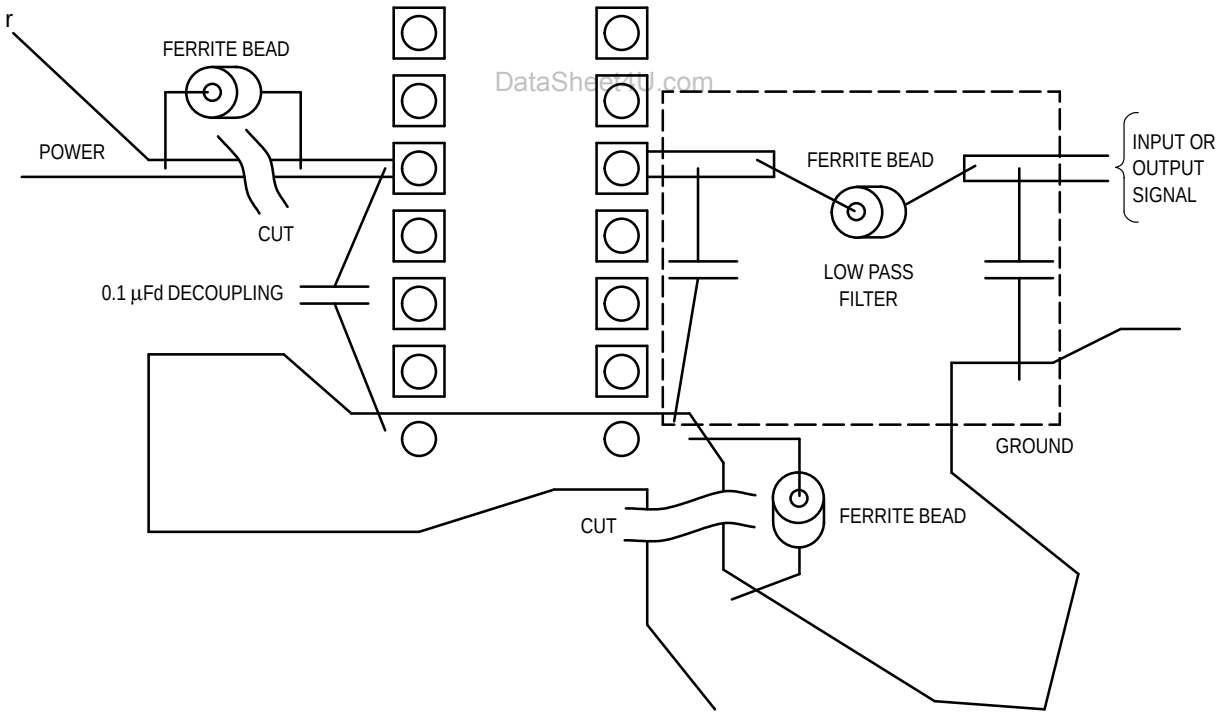


Figure 11.

LOOP FILTER CALCULATION

This section is not intended as complete loop theory; its aim is merely to point out the peculiarities of the loop, and provide the user with enough information for the filter components selection. For a more in–depth covering, the cited references should be consulted, especially [1].

The following remarks apply to the loop:

- The loop frequency is 15 kHz.
- In spite of the sampled nature of the loop, a continuous time approximation is possible if the loop bandwidth is sufficiently small.
- Ripple on Vc is a function of loop bandwidth.
- The loop is a type ||, 3rd order; however, since C2 is small, the pole it creates is far removed from the low frequency dominant poles, and the loop can be analyzed as a 2nd order loop.

These remarks apply to the PFD:

- Phase and frequency sensitive.
- Independent of duty cycle.
- PFD has 3 allowed states: up, down, high–Z.
- The VCO is always pulled in the right direction (during acquisition).
- PFD gain is higher near lock.

The last two remarks imply that only the higher value need be taken into account, as acquisition will be slower, but always in the proper direction, whereas the higher gain will enter into the action as soon as the error reaches $\pm 2\pi$.

The following values are selected and defined:

C2 = C/10 or less, to satisfy the requirement that the effect of C2 on the low frequency response of the loop be minimal, and similar to a second order loop.

$\zeta = 0.707$ for the damping factor.

$i = 15625 \bullet 2\pi$ the input pulsation.

$\tau = RC$ as the loop filter.

$K = Ko \bullet Ip \bullet R/(2 \bullet \pi \bullet N)$ the loop gain.

$K' = K \bullet \tau = 4\ \zeta^2$ is the 'normalized' loop gain.

$Ko = 49 \bullet 10^6$ [rad/Vs] (7.8 MHz/V).

Stability analysis, with $C2 \leq C/10$ and $K' = 2$ (= 0.707) gives a minimum value of 7.5 for the ration /K and to have some margin, a reasonable value can be 15 to 20 or higher [1].

Selecting $i/K = 20$, gives: $K = i/20 \approx 5000$.

With $K' = 2$, $\tau = 2/K = 400\ \mu s$.

Using $K = Ko \bullet Ip \bullet R/(2 \bullet \pi \bullet N)$ and setting $Ip = 120\ \mu A$, and N an average value of 1000, we get $R = 5.1\ k\Omega$.

Then for $\tau = 400\ \mu s$, C becomes 82 nF and C2, 3.3 nF for C2 = C/25.

With these values, the loop natural frequency (n) and the loop bandwidth (3 dB) can be calculated:

$n = [(Ko/N) \bullet Ip/(2\pi C)]^{1/2} = 3400$ and $fn = 3400/2\pi = 540$ Hz.

3 dB = 2 • n = 1080 Hz (valid if ζ is close to 0.707).

REFERENCES

[1] "Charge–Pump Phase–Lock Loops", Floyd M. Gardner, *IEEE Transactions on Communications*, Vol. Com–28, No. 11, November 1980.

[2] *Phaselock Techniques*, Floyd M. Gardner, J. Wiley & Sons, 1979.

[3] *Phase–Locked Loops*, Roland E. Best, McGraw–Hill, 1984.

[4] "Phase Locked Loop Systems", Motorola.

APPENDIX
DEMONSTRATION PROGRAMS

COMMUNICATING WITH THE MC144144

Communications with the MC144144 is accomplished using its serial communications interface. Through hardware setup, this interface can be configured into either of two serial protocols, I^2C or SPI. The details of hardware setup have been provided in the data sheet and will not be dealt with in this appendix. It is assumed that the user is familiar with the serial protocol requirements.

In the following descriptions **<ENTER>** means press the Enter key and ***** signifies that everything following the asterisk in that line is a comment.

I^2C OPERATION

The MC144144 is configurable as an I^2C slave device with the slave address 0010100. The accompanying C language programs enable a PC to perform as the I^2C master device of an application. The PC communicates with the MC144144 through the parallel port. These programs are not intended as examples of how to program the application but are only provided as a means of illustrating the serial control process.

The three programs provided are titled IICO, SCRIPTI, and XDSCAP. These programs have been compiled and run satisfactorily with the MC144144 in a test board. Compiled versions are available on disk.

IICO Program

This program will send one byte to the MC144144 without checking the status of the READY bit. The program returns the contents of the serial status (SS) register after the command has been entered. When the program is active the screen will display:

```
IIC Command Byte >
```

The user may enter any valid one byte command such as FB (Reset) or 00 (NOP) and then hit the ENTER key. The screen will then display the byte entered and the SS register contents as follows:

```
IIC Byte = 00
IIC Status = 83h
```

The illustration above shows the NOP command was entered. The SS register contents, 83h, indicates that the RDY, FLD, and LOCK bits are “ones” indicating that the serial port is ready for further input, that the input video signal was in field 1 at the time the status was read, and that the part is operating in video lock mode.

The IICO program is exited by entering a Control C (^C) character.

For example, entering the following single byte commands would:

```
FB,FC,00    *  Resets the part.
00          *  Clear the reset.
17          *  Set the part to CC1 display
               mode, decoder ON.
23          *  Change to the XDS Graze
               display mode, 16Sec Timer ON.
17          *  Return to the CC1 display
               mode, decoder ON.
```

The commands that control most of the display capability of the MC144144 are all one byte commands which can be entered using the IICO program. These commands are tabulated below for convenience.

General Commands

Command	Byte
NOP	00
Reset	FB,FC,00

Caption/Text Display Commands

CMD Byte	Data Channel and DEC ON	CMD Byte	Data Channel and DEC OFF
17	CC1	16	CC1
15	CC2	14	CC2
1F	CC3	1E	CC3
1D	CC4	1C	CC4
13	T1	12	T1
11	T2	10	T2
1B	T3	1A	T3
19	T4	18	T4

XDS and Miscellaneous Display Mode Commands

CMD Byte	XDS Disp	16 Sec Timer
23	XDSG	ON
27	XDSG	OFF
21	XDSF	ON
25	XDSF	OFF
20	*	ON
24	*	OFF

*Does not effect the display mode currently in operation.

SCRIPTI Program

This program is designed to send any number of one or two byte commands to the MC144144. The list of commands to be executed are contained in script files that have the extension .SER. Examples of such files will be presented in the following paragraphs. SCRIPTI can be used to control the display modes in the same manner as the IICO program except that the one byte command to be sent must be in a Script file. For example a file called CC1.SER would contain the one byte command:

```
{17}          * send CC1, decoder ON
```

The program is invoked by typing:

```
SI File_name <ENTER>      *  File_name without
                             the .SER extension
```

The screen will display:

```
EEG CCD2 Serial Interface Script Player
  Version x.xx
Slave Address is 28h

Script File Done
```

The responding slave address is reported to the screen. When all the commands in the file have been successfully

sent to the MC144144, the PC will return to the system prompt.

The program checks the RDY status before sending each byte. If, during the entry of a command, the RDY bit is not found to be a “one” after an extended wait, the program will report the contents of the SS register and then continue checking for RDY.

Script Files

Script files can be generated to perform all of the setup and control functions required to use the part in an application. The script files shown below are examples of such files used to setup the MC144144 for different operating conditions. Some of the files contain only a single command while others include several commands. The user should refer to the data sheet for command and register details. Although the following examples are organized according to a particular register, some of the files contain information for several registers.

Configuration Register Script Files

File Name	CMD	Comments
FIGM	{c0,02}	* set config to mono
FIGVH	{c7,00}	* set INT Mask Reg clear
	{c0,0c}	* set config to ext VLK & HLK
	{83,12}	* bit set ext V pulse for pos
	{c2,1d}	* center h display
FIGN	{c0,00}	* set config back to default state
	{c2,26}	* return h display to center
FIGPAL	{c1,d2}	* change display reg to C15 & T15
	{c3,ff}	* change text pos reg to base row 15, 15 rows
	{c0,01}	* set config reg to TVS=1. Changes VBI line to L22 PAL.

Display Register Script Files

DN	{c1,c0}	* set display reg to default conditions
DT1	{c1,c1}	* Set display reg to TEXT drop shadow
DT2	{c1,c2}	* set display reg to TEXT 15 lines per row
DT3	{c1,c3}	* set display reg to TEXT drop shadow, 15 lines
DT3A	{c1,c3}	* 15 tv lines and drop text
	{c3,dd}	* 13 rows of text, base row 13
DCE	{c1,e0}	* disable CAP Enhanced mode

H Position Register Script Files

HPOSC	{c2,26}	* center box
HPOSR	{c2,1d}	* move box right 2.97 uSec (from ctr)
HPOSL	{c2,29}	* move box left 0.99 uSec (from ctr)
HPOSCB	{c2,a6}	* center box & make Box Blue

Text Position Register Script Files

TPOS15	{c3,ff}	* text, base row 15, 15 rows
TPOS13	{c3,fd}	* text base row 15, 13 rows
TPOS10	{c3,fa}	* text base row 15, 10 rows
TPOS10A	{c3,ba}	* text base row 11, 10 rows

XDSCAP Program

This program performs the application’s task of XDS data recovery. XDS recovery must first have been enabled through the appropriate XDS filter command. Examples of script files for setting the XDS filter register are shown below.

When the program is invoked the screen will show:

EEG CCD2 XDS Data Recovery Test Program
Version x.xx

Slave Address is 28h

The responding slave address is reported to the screen.

Once communications is acknowledged the program will display all XDS data recovered from those packets that were enabled through the XDS filter command. For example:

{01,03}Current Program{00}{0F,7F}....etc

The ASCII characters are shown as ASCII characters while the non–printing characters are displayed by their hex value within curly braces. Byte pairs, such as class, type, are shown as pairs within the curly braces, separated by a comma, i.e. {01,03}.

If no data is received within approximately 45 seconds, the program will time out, report **“Data Not Available”**, and exit the program. The XDSCAP program can also be exited by entering a Control C (^C) character.

XDS Filter Register Script Files

FILA	{c5,1F}	* set xds filter to all
FIL0	{c5,00}	* set xds filter to none. Turns off xds recovery
FILCA	{c5,01}	* set xds filter to all current class
FILC	{c5,41}	* set xds filter to current, in band class
FILFA	{c5,02}	* set xds filter to all future class
FILCH	{c5,04}	* set xds filter to channel class
FILM	{c5,08}	* set xds filter for misc info
FILTIME	{c5,28}	* set xds filter time only
FILVCR	{c5,9e}	* set xds filter vcr info

Using Interrupts

Interrupts involve the use of the Line 21 activity register, the Interrupt request register, and the interrupt mask register. The MC144144 must be configured for VLK internal so that the VINTRO signal, pin 13 is an output providing the interrupt output signal. It should be noted that the interrupt status can be polled through bit D3 of the SS register if the interrupt signal cannot be used.

Interrupts are disabled when the interrupt mask register has been set to all zeros. Conversely, interrupts are enabled by setting one or more of the active bits to a one. When enabled, the INTRO signal will become a one when the enabled mask event(s) becomes active. If more than one event has been activated, the interrupt request register must be queried to determine which event has occurred. The DLE

and EOF interrupts will be cleared at the end of the field in which they occurred.

Interrupt Mask Register Script Files

INTRD	{c7,02}	* set DLE active
INTRLK	{c7,08}	* set dLOK active
INTRX	{c7,20}	* set dXDS active
INTRC	{c7,12}	* set DLE & dC/T active

SPI OPERATION

The serial port of the MC144144 may be configured to operate as an SPI interface. The MC144144 always acts as the slave device with the master generating the required clock and input data signals. The accompanying C language programs enable a PC to perform as the SPI master device of an application. The PC communicates with the MC144144 through its parallel port. These programs are not intended as examples of how to program the application but are only provided as a means of illustrating the serial control process.

The two programs provided, SEROUT and SCRIPT the SPI equivalent to the I^2C programs IICO and SCRIPTI, respectively. These programs have been compiled and run satisfactorily with the MC144144 in a test board. Compiled versions are available on disk.

SEROUT Program

This program will send one byte to the MC144144 without checking the status of the READY bit. The program returns the contents of the serial status (SS) register after the command has been entered. When the program is active the screen will display:

SPI Command Byte >

The user may enter any valid one byte command and then hit the ENTER key. The screen will then display the byte entered and the SS register contents as follows:

SPI Byte = 00
SPI Return Val = 83h

The illustration above shows the NOP command was entered. The SS register contents, 83h, indicates that the RDY, FLD, and LOCK bits are “ones” indicating that the serial port is ready for further input, that the input video signal was in Field 1 at the time the status was read and that the part is operating in video lock mode.

When this program is used a modified version of the RESET can only be used. It is entered as two 1–byte commands, FB and 00.

The SEROUT program is exited by entering a Control C (^C) character.

SCRIPT Program

This program is designed to send any number of one or two byte commands to the MC144144. The list of commands to be executed are contained in Script files that have the extension .SER. The Script files used with the I^2C version, SCRIPTI, can be used with this program.

The program is invoked by typing:

S File_name <ENTER> * File_name without the .SER extension

The screen will display:

EEG CCD2 Serial Interface Script Player
Version x.xx

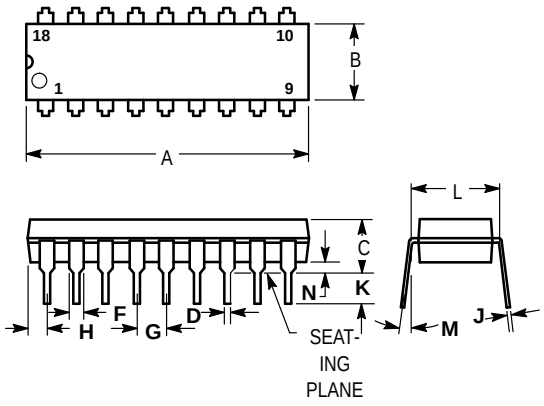
Script File Done

When all the commands in the file have been successfully sent to the MC144144, the PC will return to the system prompt.

The program checks the RDY status before sending each byte. If, during the entry of a command, the RDY bit is not found to be a “one”, the program will report the contents of the SS register and then continue checking for RDY.

PACKAGE DIMENSIONS

P SUFFIX
PLASTIC DIP (DUAL IN–LINE PACKAGE)
CASE 707–02



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTE: Introduction of this device in a surface–mount package is dependent on market demand.

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