

# MC14503B

## Hex Non-Inverting 3-State Buffer

The MC14503B is a hex non-inverting buffer with 3-state outputs, and a high current source and sink capability. The 3-state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

### Features

- 3-State Outputs
- TTL Compatible – Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1)

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	$V_{DD}$	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	$V_{in}, V_{out}$	-0.5 to $V_{DD}$ + 0.5	V
Input Current (DC or Transient) per Pin	$I_{in}$	$\pm 10$	mA
Output Current (DC or Transient) per Pin	$I_{out}$	$\pm 25$	mA
Power Dissipation, per Package (Note 2)	$P_D$	500	mW
Ambient Temperature Range	$T_A$	-55 to +125	$^{\circ}C$
Storage Temperature Range		-65 to +150	$^{\circ}C$
Lead Temperature (8-Second Soldering)		260	$^{\circ}C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
"D/DW" Package: -7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

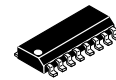
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



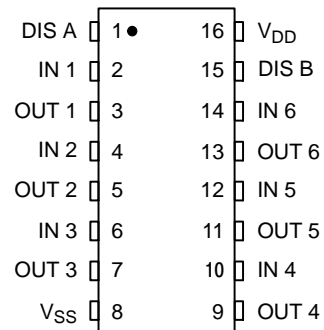
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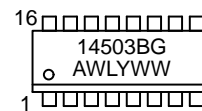


1  
SOIC-16  
D SUFFIX  
CASE 751B

### PIN ASSIGNMENT



### MARKING DIAGRAM



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G = Pb-Free Package

### TRUTH TABLE

$In_n$	Appropriate Disable Input	$Out_n$
0	0	0
1	0	1
X	1	High Impedance

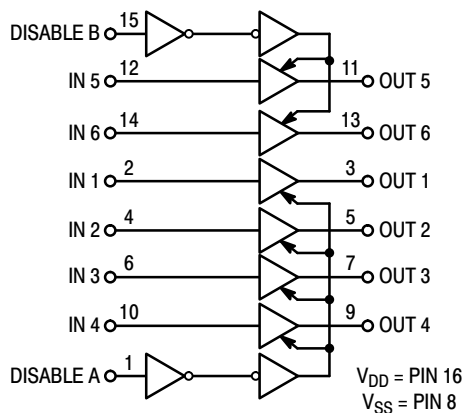
X = Don't Care

### ORDERING INFORMATION

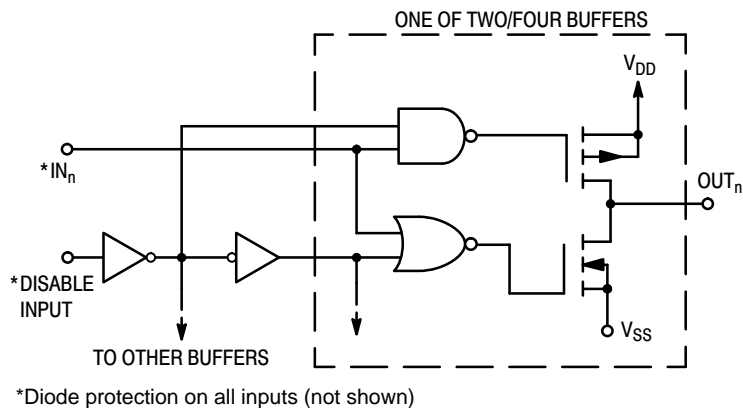
See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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**LOGIC DIAGRAM**



**CIRCUIT DIAGRAM**



**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55 °C		25 °C			125 °C		Unit
			Min	Max	Min	Typ (Note 3)	Max	Min	Max	
Output Voltage V <sub>in</sub> = 0	"0" Level V <sub>OL</sub>	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
		10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	-	0	0.05	-	0.05	
V <sub>in</sub> = V <sub>DD</sub>	"1" Level V <sub>OH</sub>	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
		10	9.95	-	9.95	10	-	9.95	-	
		15	14.95	-	14.95	15	-	14.95	-	
Input Voltage (V <sub>O</sub> = 3.6 or 1.4 Vdc) (V <sub>O</sub> = 7.2 or 2.8 Vdc) (V <sub>O</sub> = 11.5 or 3.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc
		10	-	3.0	-	4.50	3.0	-	3.0	
		15	-	4.0	-	6.75	4.0	-	4.0	
	"1" Level V <sub>IH</sub>	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
		10	7.0	-	7.0	5.50	-	7.0	-	
		15	11	-	11	8.25	-	11	-	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source I <sub>OH</sub>	4.5	-4.3	-	-3.6	-5.0	-	-2.5	-	mAdc
		5.0	-5.8	-	-4.8	-6.1	-	-3.0	-	
		5.0	-1.2	-	-1.02	-1.4	-	-0.7	-	
		10	-3.1	-	-2.6	-3.7	-	-1.8	-	
		15	-8.2	-	-6.8	-14.1	-	-4.8	-	
	Sink I <sub>OL</sub>	4.5	2.2	-	1.8	2.1	-	1.2	-	mAdc
		5.0	2.6	-	2.1	2.3	-	1.3	-	
		10	6.5	-	5.5	6.2	-	3.8	-	
		15	19.2	-	16.1	25	-	11.2	-	
		Input Current	I <sub>in</sub>	15	-	±0.1	-	±0.00001	±0.1	
Input Capacitance, (V <sub>in</sub> = 0)	C <sub>in</sub>	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current, (Per Package)	I <sub>Q</sub>	5.0	-	1.0	-	0.002	1.0	-	30	μAdc
		10	-	2.0	-	0.004	2.0	-	60	
		15	-	4.0	-	0.006	4.0	-	120	
Total Supply Current (Note 4, 5) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs) (All outputs switching, 50% Duty Cycle)	I <sub>T</sub>	5.0	I <sub>T</sub> = (2.5 μA/kHz) f + I <sub>DD</sub>							μAdc
		10	I <sub>T</sub> = (6.0 μA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (10 μA/kHz) f + I <sub>DD</sub>							
3-State Output Leakage Current	I <sub>TL</sub>	15	-	±0.1	-	±0.0001	±0.1	-	±3.0	μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

5. To calculate total supply current at loads other than 50 pF: I<sub>T</sub>(C<sub>L</sub>) = I<sub>T</sub>(50 pF) + (C<sub>L</sub> - 50) Vfk where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.006.

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## SWITCHING CHARACTERISTICS (Note 6) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ $V_{CC}$	All Types		Unit
			Typ (Note 7)	Max	
Output Rise Time $t_{TLH} = (0.5 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.3 \text{ ns/pF}) C_L + 8.0 \text{ ns}$ $t_{TLH} = (0.2 \text{ ns/pF}) C_L + 8.0 \text{ ns}$	$t_{TLH}$	5.0 10 15	45 23 18	90 45 35	ns
Output Fall Time $t_{THL} = (0.5 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.3 \text{ ns/pF}) C_L + 8.0 \text{ ns}$ $t_{THL} = (0.2 \text{ ns/pF}) C_L + 8.0 \text{ ns}$	$t_{THL}$	5.0 10 15	45 23 18	90 45 35	ns
Turn-Off Delay Time, all Outputs $t_{PLH} = (0.3 \text{ ns/pF}) C_L + 60 \text{ ns}$ $t_{PLH} = (0.15 \text{ ns/pF}) C_L + 27 \text{ ns}$ $t_{PLH} = (0.1 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{PLH}$	5.0 10 15	75 35 25	150 70 50	ns
Turn-On Delay Time, all Outputs $t_{PHL} = (0.3 \text{ ns/pF}) C_L + 60 \text{ ns}$ $t_{PHL} = (0.15 \text{ ns/pF}) C_L + 27 \text{ ns}$ $t_{PHL} = (0.1 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{PHL}$	5.0 10 15	75 35 25	150 70 50	ns
3-State Propagation Delay Time Output "1" to High Impedance	$t_{PHZ}$	5.0 10 15	75 40 35	150 80 70	ns
Output "0" to High Impedance	$t_{PLZ}$	5.0 10 15	80 40 35	160 80 70	ns
High Impedance to "1" Level	$t_{PZH}$	5.0 10 15	65 25 20	130 50 40	ns
High Impedance to "0" Level	$t_{PZL}$	5.0 10 15	100 35 25	200 70 50	ns

6. The formulas given are for the typical characteristics only at 25°C.

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

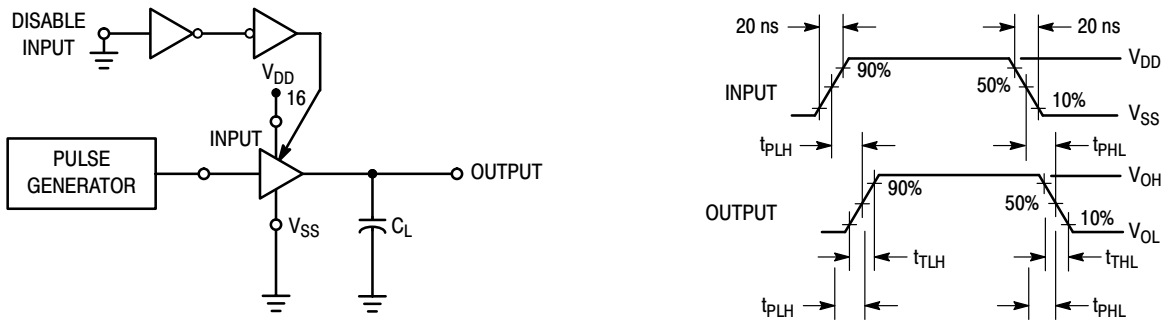
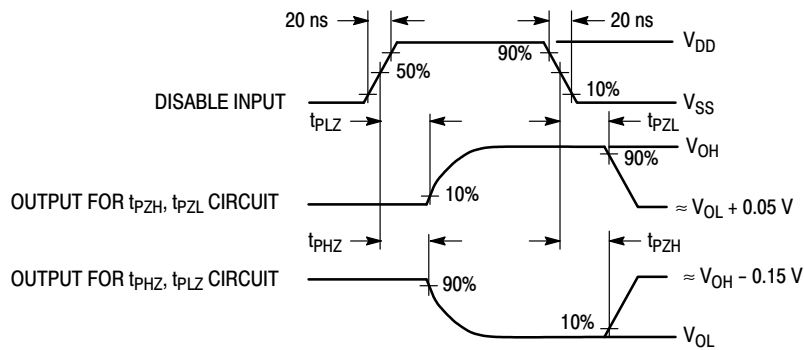
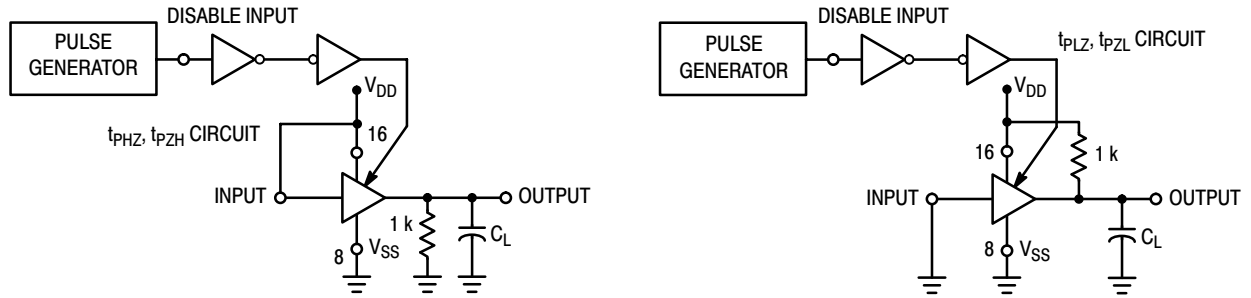


Figure 1. Switching Time Test Circuit and Waveforms ( $t_{TLH}$ ,  $t_{THL}$ ,  $t_{PHL}$ , and  $t_{PLH}$ )

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**Figure 2. 3-State AC Test Circuit and Waveforms**  
( $t_{PLZ}$ ,  $t_{PHZ}$ ,  $t_{PZH}$ ,  $t_{PZL}$ )

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC14503BDG	SOIC-16 (Pb-Free)	48 / Rail
MC14503BDR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
NLV14503BDR2G*	SOIC-16 (Pb-Free)	2500 / Tape & Reel

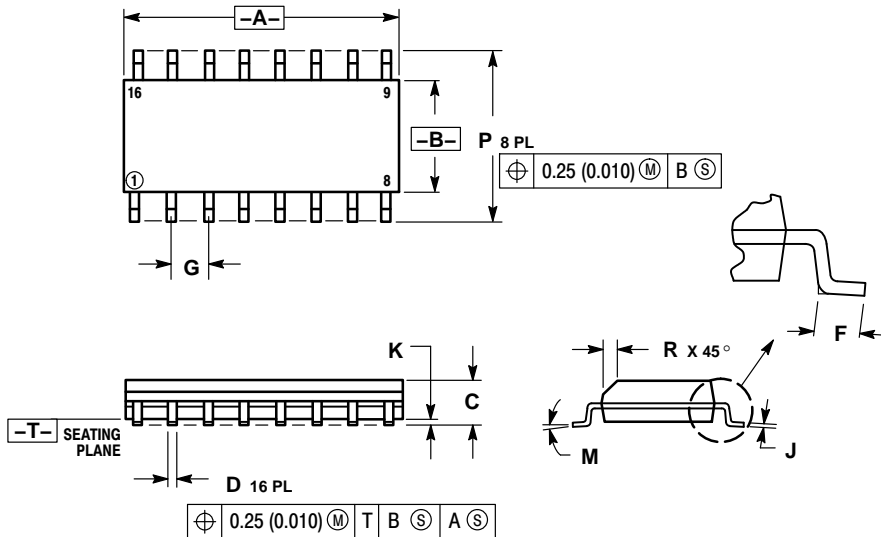
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

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## PACKAGE DIMENSIONS

SOIC-16  
CASE 751B-05  
ISSUE K

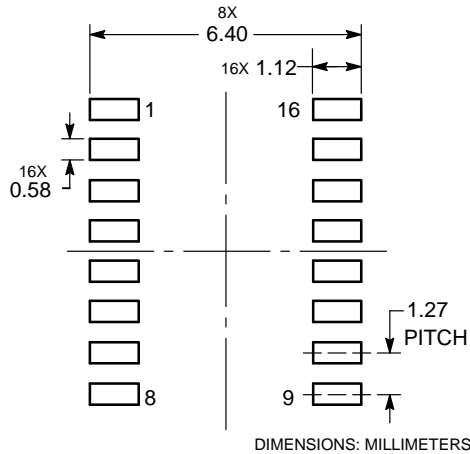



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0° 7°		0° 7°	
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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