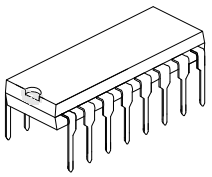
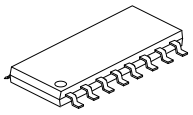
MC14511

CMOS IC

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER



DIP-16



SOP-16

■ DESCRIPTION

The UTC **MC14511** BCD–to–seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light-emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

■ FEATURES

* Low Logic Circuit Power Dissipation
* High–Current Sourcing Outputs (Up to 25 mA)
* Latch Storage of Code
* Blanking Input
* Lamp Test Provision
* Readout Blanking on all Illegal Input Combinations
* Lamp Intensity Modulation Capability
* Time Share (Multiplexing) Facility
* Supply Voltage Range = 3.0V ~ 18V

■ ORDERING INFORMATION

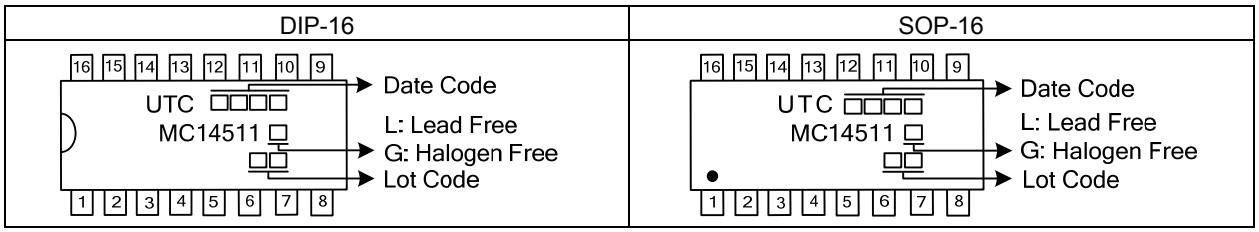
Ordering Number		Package	Packing
Lead Free	Halogen Free		
MC14511L-D16-T	MC14511G-D16-T	DIP-16	Tube
MC14511L-S16-R	MC14511G-S16-R	SOP-16	Tape Reel

MC14511G-D16-T

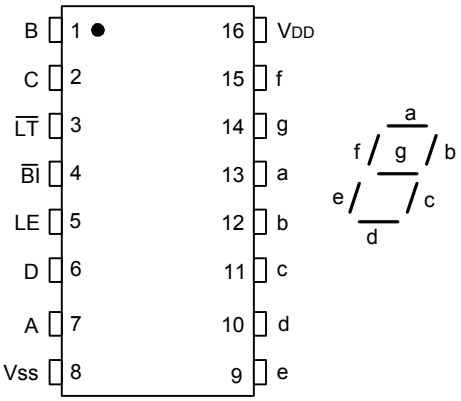
(1) Packing Type
(2) Package Type
(3) Green Package

(1) T: Tube, R: Tape Reel
(2) D16: DIP-16, S16: SOP-16
(3) G: Halogen Free and Lead Free, L: Lead Free

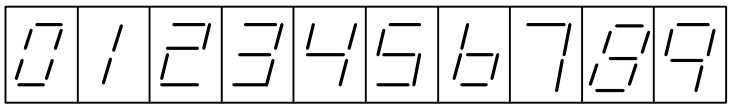
■ MARKING



■ PIN CONFIGURATION



DISPLAY



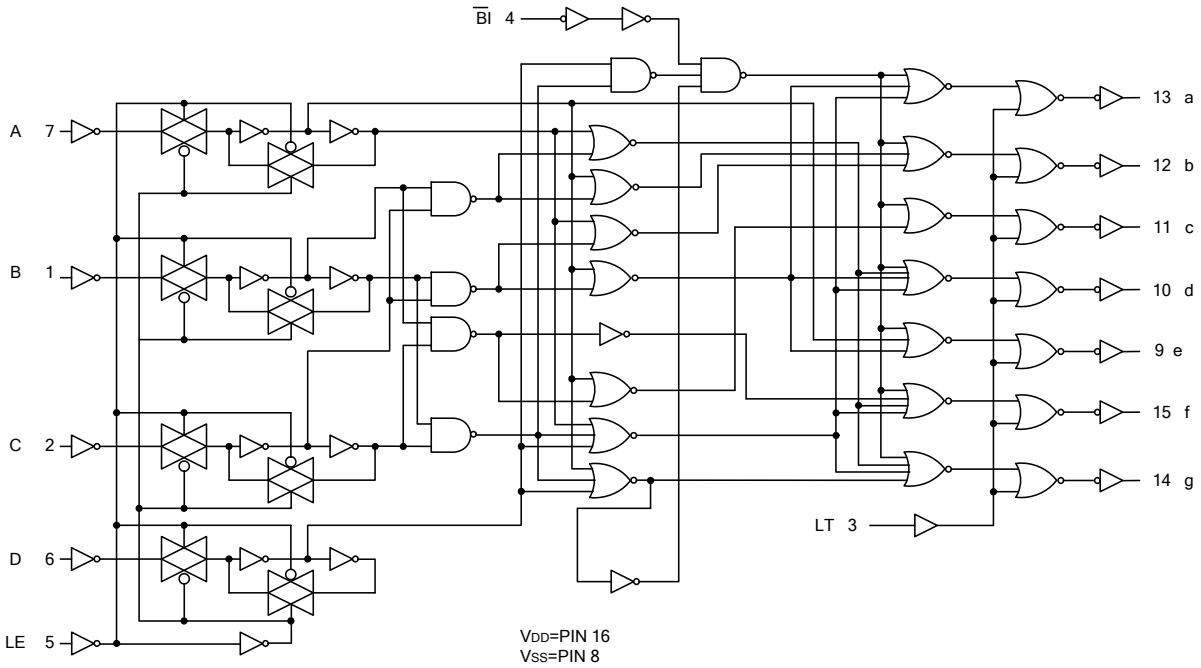
■ TRUTH TABLE

Inputs							Outputs							
LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X	*							*

X=Don't Care

*Depends upon the BCD code previously applied when LE=0

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Note 3)

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage Range	V_{DD}	-0.5 ~ +18.0	V
Input Voltage Range, All Inputs	V_{IN}	-0.5 ~ V_{DD}+0.5	V
DC Current Drain per Input Pin	I	10	mA
Power Dissipation, per Package	P_D	500	mW
Maximum Output Drive Current (Source) per Output	I_{OHMAX}	25	mA
Maximum Continuous Output Power (Source) per Output (Note 2)	P_{OHMAX}	50	mA
Operating Temperature Range	T_A	-55 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. $P_{OHMAX} = I_{OH} (V_{DD} – V_{OH})$

3.This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high current mode may occur if V_{IN} and V_{OUT} are not constrained to the range:

$V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER		SYMBOL	V_{DD} V_{DC}	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
Output Voltage	“0” Level	V_{OL}	5.0	$V_{IN}=V_{DD}$ or 0		0	0.05	V
			10			0	0.05	
			15			0	0.05	
	“1” Level	V_{OH}	5.0	V_{IN}=0 or V_{DD}	4.1	4.57		V
			10		9.1	9.58		
			15		14.1	14.59		
Input Voltage (Note 1)	“0” Level	V_{IL}	5.0	V_O=3.8 or 0.5 V		2.25	1.5	V
			10	V_O=8.8 or 1.0 V		4.50	3.0	
			15	V_O=13.8 or 1.5V		6.75	4.0	
	“1” Level	V_{IH}	5.0	V_O=0.5 or 3.8 V	3.5	2.75		V
			10	V_O=1.0 or 8.8 V	7.0	5.50		
			15	V_O=1.5 or 13.8 V	11	8.25		
Output Drive Voltage (Source)		V_{OH}	5.0	I_{OH}=0mA	4.1	4.57		V
				I_{OH}=5.0mA		4.24		
				I_{OH}=10mA	3.9	4.12		
				I_{OH}=15mA		3.94		
				I_{OH}=20mA	3.4	3.70		
				I_{OH}=25mA		3.54		
			10	I_{OH}=0mA	9.1	9.58		V
				I_{OH}=5.0mA		9.26		
				I_{OH}=10mA	9.0	9.17		
				I_{OH}=15mA		9.04		
				I_{OH}=20mA	8.6	8.90		
				I_{OH}=25mA		8.70		

■ ELECTRICAL CHARACTERISTICS (Cont.) (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	V_{DD} V_{DC}	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Drive Voltage (Source)	V_{OH}	15	I_{OH}=0mA I_{OH}=5.0mA I_{OH}=10mA I_{OH}=15mA I_{OH}=20mA I_{OH}=25mA	14.1 14 13.6 	14.59 14.27 14.18 14.07 13.95 13.70		V
Output Drive Current (Sink)	I_{OL}	5.0 10 15	V_{OL}=0.4V V_{OL}=0.5V V_{OL}=1.5V	0.51 1.3 3.4	0.88 2.25 8.8		mA
Input Current	I_{IN}	15			±0.00001	±0.1	μA
Input Capacitance	C_{IN}				5.0	7.5	pF
Quiescent Current	I_{DD}	5.0 10 15	(Per Package) V_{IN} =0 or V_{DD}, I_{OUT}=0μA		0.005 0.010 0.015	5.0 10 20	μA
Total Supply Current (Notes 2 & 3)	I_T	5.0 10 15	(Dynamic plus Quiescent, Per Package) (C_L=50pF on all outputs, all buffers switching)	I_T=(1.9μA/kHz) f+I_{DD} I_T=(3.8μA/kHz) f+I_{DD} I_T=(5.7μA/kHz) f+I_{DD}			μA

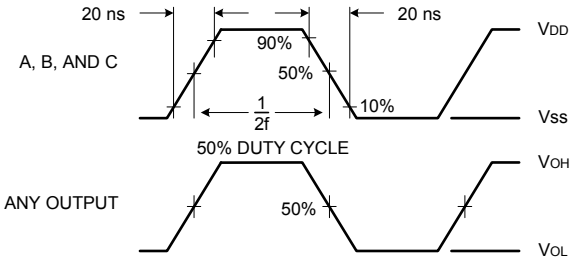
Notes: 1. Noise immunity specified for worst–case input combination..
Noise Margin for both “1” and “0” level =
1.0 V min @ V_{DD} = 5.0 V
2.0 V min @ V_{DD} = 10 V
2.5 V min @ V_{DD} = 15 V
2. The formulas given are for the typical characteristics only at 25°C.
3. To calculate total supply current at loads other than 50 pF:
I_T (C_L) = I_T(50 pF) + 3.5 x 10^{-3} (C_L – 50) V_{DD}f.
Where: IT is inμA (per package), CL in pF, V_{DD} in Vdc, and f in kHz is input frequency

■ SWITCHING CHARACTERISTICS (Note 1) (C_L=50pF, T_A=25°C)

PARAMETER	SYMBOL	V_{DD} V_{DC}	TEST CONDITIONS	Min	TYP	MAX	UNIT
Output Rise Time	t_{TLH}	5.0 10 15	t_{TLH}=(0.40 ns/pF) C_L+20 ns t_{TLH}=(0.25 ns/pF) C_L+17.5 ns t_{TLH}=(0.20 ns/pF) C_L+15 ns		40 30 25	80 60 50	ns
Output Fall Time	t_{THL}	5.0 10 15	t_{THL}=(1.5 ns/pF) C_L+50 ns t_{THL}=(0.75 ns/pF) C_L+37.5 ns t_{THL}=(0.55 ns/pF) C_L+37.5 ns		125 75 65	250 150 130	ns
Data Propagation Delay Time	t_{PLH}	5.0 10 15	t_{PLH}=(0.40 ns/pF) C_L+620 ns t_{PLH}=(0.25 ns/pF) C_L+237.5 ns t_{PLH}=(0.20 ns/pF) C_L+165 ns		640 250 175	1280 500 350	ns
	t_{PHL}	5.0 10 15	t_{PHL}=(1.3 ns/pF) C_L+655 ns t_{PHL}=(0.60 ns/pF) C_L+260 ns t_{PHL}=(0.35 ns/pF) C_L+182.5 ns		720 290 200	1440 580 400	
$\overline{\text{Blank}}$ Propagation Delay Time	t_{PLH}	5.0 10 15	t_{PLH}=(0.30 ns/pF) C_L+585 ns t_{PLH}=(0.25 ns/pF) C_L+187.5 ns t_{PLH}=(0.15 ns/pF) C_L+142.5 ns		600 200 150	750 300 220	ns
	t_{PHL}	5.0 10 15	t_{PHL}=(0.85 ns/pF) C_L+442.5 ns t_{PHL}=(0.45 ns/pF) C_L+177.5 ns t_{PHL}=(0.35 ns/pF) C_L+142.5 ns		485 200 160	970 400 320	
$\overline{\text{Lamp}}$ Test Propagation Delay Time	t_{PLH}	5.0 10 15	t_{PLH}=(0.45 ns/pF) C_L+290.5 ns t_{PLH}=(0.25 ns/pF) C_L+112.5 ns t_{PLH}=(0.20 ns/pF) C_L+80 ns		313 125 90	625 250 180	ns
	t_{PHL}	5.0 10 15	t_{PHL}=(1.3 ns/pF) C_L+248 ns t_{PHL}=(0.45 ns/pF) C_L+102.5 ns t_{PHL}=(0.35 ns/pF) C_L+72.5 ns		313 125 90	625 250 180	
Setup Time	t_{su}	5.0 10 15		100 40 30			ns
Hold Time	t_h	5.0 10 15		60 40 30			ns
Latch Enable Pulse Width	t_{WL}	5.0 10 15		520 220 130	260 110 65		ns

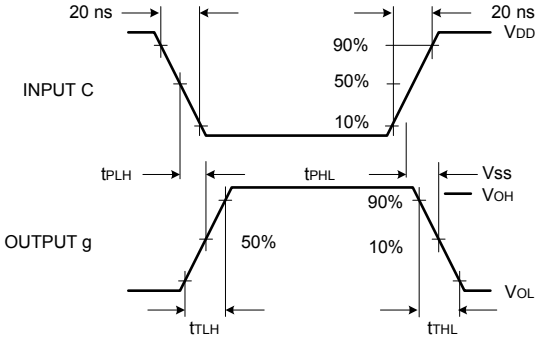
Note 1: The formulas given are for the typical characteristics only.

■ SWITCHING TIME WAVEFORMS

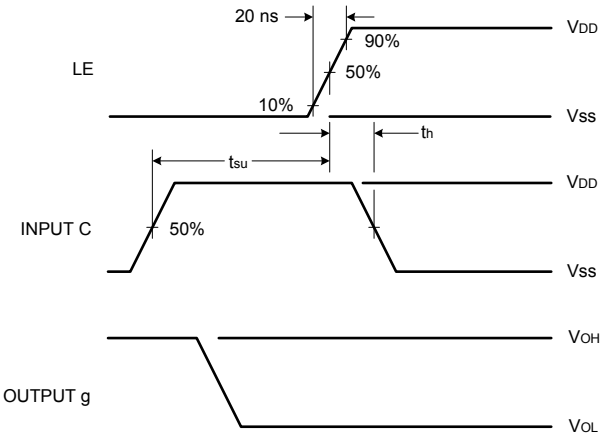


Input LE low, and Inputs D, $\overline{BI}$ and $\overline{LT}$ high.
f in respect to a system clock.
All outputs connected to respective C_L loads.

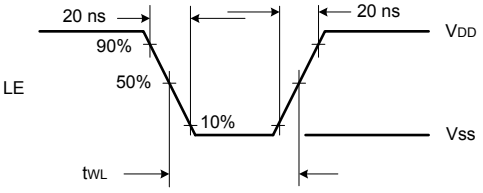
Figure 1. Dynamic Power Dissipation Signal Waveforms



(a) Inputs D and LE low, and Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high



(b) Input D low, Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high

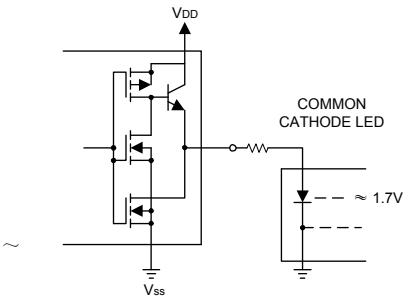


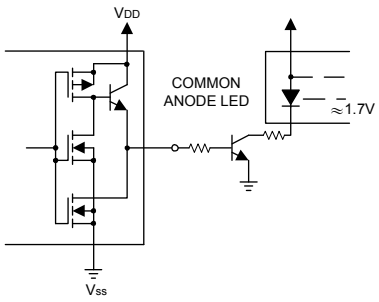
(c) Data DCBA strobed into latches.

Figure 2. Dynamic Signal Waveforms

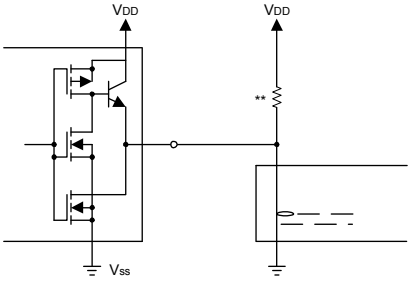
■ CONNECTIONS TO VARIOUS DISPLAY READOUTS

LIGHT EMITTING DIODE (LED) READOUT

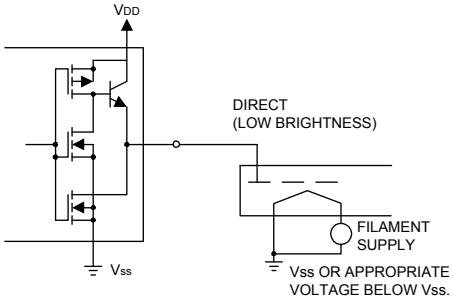




INCANDESCENT READOUT

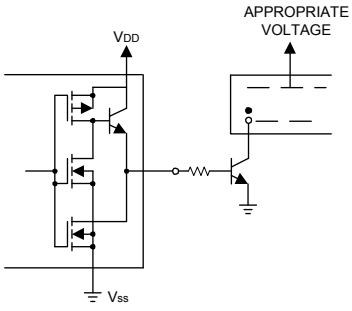


FLUORESCENT READOUT

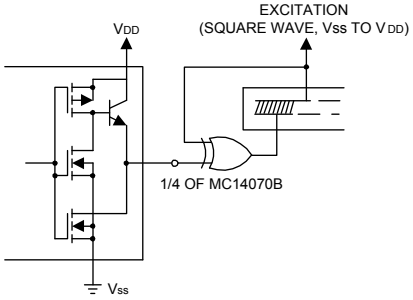


(CAUTION: Maximum working voltage=18.0V)

GAS DISCHARGE READOUT



LIQUID CRYSTAL(LCD) READOUT



** A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct dc drive of LCD's not recommended for life of LCD readouts.