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Trivelo

Motorola CMOS/NMOS
Special Functions
DataSale

MOTOROLA

MC145157-1
MC145158-1

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

SERIAL INPUT PLL
FREQUENCY SYNTHESIZER

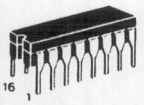
SERIAL INPUT PLL FREQUENCY SYNTHESIZERS

The MC145157-1 and MC145158-1 have fully programmable 14-bit reference counters, as well as fully programmable ÷ N (MC145157-1) and ÷ N/ ÷ A (MC145158-1) counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

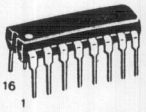
When combined with a loop filter and VCO, these devices can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a fixed-divide prescaler can be used between the VCO and the PLL for the MC145157-1 and a dual-modulus prescaler for the MC145158-1.

The MC145157-1 and MC145158-1 offer improved performance over the MC145157 and MC145158. Modulus Control output drive has been increased and the ac characteristics have been improved. Input current requirements have also been modified.

- General Purpose Applications:
  CATV
  AM/FM Radios
  Two-Way Radios
  TV Tuning
  Scanning Receivers
  Amateur Radio
- Low Power Consumption
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and ÷ N Counters
- ÷ R Range = 3 to 16383
- ÷ N Range = 3 to 16383 for the MC145157-1
  = 3 to 1023 for the MC145158-1
- Dual Modulus Capability for the MC145158-1
  ÷ A Range = 0 to 127
- f_V and f_r Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- "Linearized" Digital Phase Detector
- Single-Ended (Three-State) or Double-Ended Phase Detector Outputs



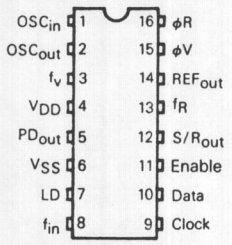
MC145157L1
MC145158L1
CERAMIC PACKAGE
CASE 620



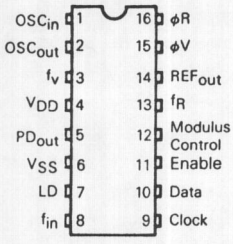
MC145157P1
MC145158P1
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT

MC145157-1



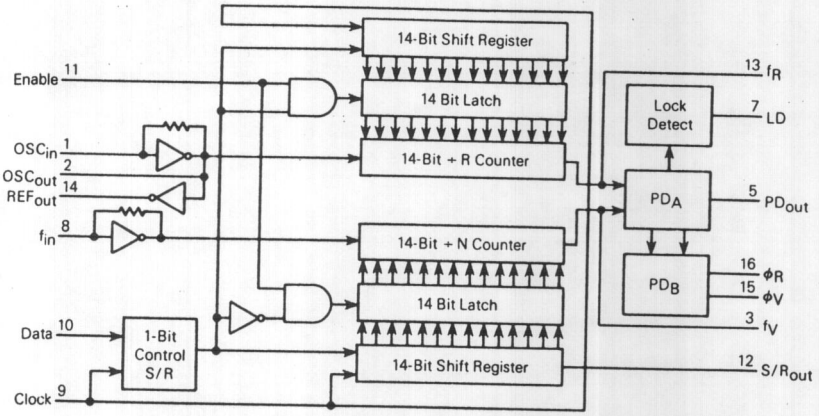
MC145158-1



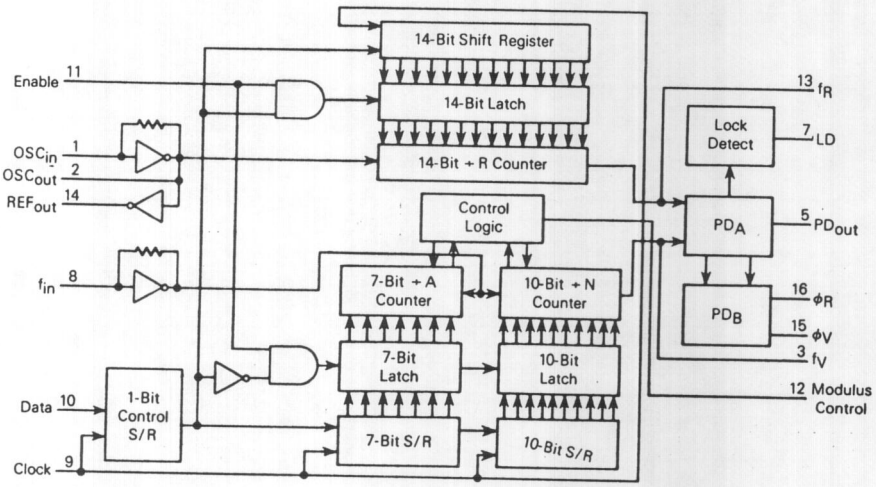
This is advance information and specifications are subject to change without notice.

6

MC145157-1



MC145158-1



V_{DD} = Pin 4
V_{SS} = Pin 6

6

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Power Dissipation Temperature Derating:
Plastic "P" Package: −12 mW/°C from 65°C to 85°C
Ceramic "L" Package: No derating

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

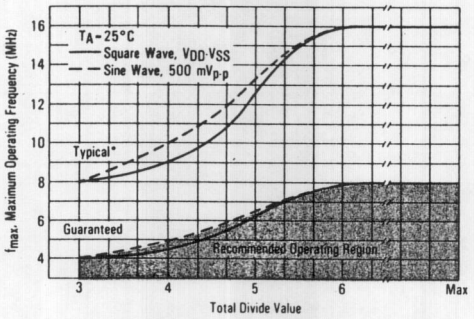
Characteristic	Symbol	V_{DD}	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Units
Power Supply Voltage Range	V_{DD}	–	3	9	3	–	9	3	9	V
Output Voltage 0 Level	V_{OL}	3	–	0.05	–	0.001	0.05	–	0.05	V
V_{in} = 0 V or V_{DD}		5	–	0.05	–	0.001	0.05	–	0.05	
$I_{out} \approx 0$ μA		9	–	0.05	–	0.001	0.05	–	0.05	
1 Level	V_{OH}	3	2.95	–	2.95	2.999	–	2.95	–	
		5	4.95	–	4.95	4.999	–	4.95	–	
		9	8.95	–	8.95	8.999	–	8.95	–	
Input Voltage 0 Level	V_{IL}	3	–	0.9	–	1.35	0.9	–	0.9	V
V_{out} = 0.5 V or V_{DD} − 0.5 V		5	–	1.5	–	2.25	1.5	–	1.5	
(All Outputs Except OSC_{out})		9	–	2.7	–	4.05	2.7	–	2.7	
1 Level	V_{IH}	3	2.1	–	2.1	1.65	–	2.1	–	
		5	3.5	–	3.5	2.75	–	3.5	–	
		9	6.3	–	6.3	4.95	–	6.3	–	
Output Current – Modulus Control	I_{OH}									mA
V_{out} = 2.7 V Source		3	−0.60	–	−0.50	−1.5	–	−0.30	–	
V_{out} = 4.6 V		5	−0.90	–	−0.75	−2.0	–	−0.50	–	
V_{out} = 8.5 V		9	−1.50	–	−1.25	−3.2	–	−0.80	–	
V_{out} = 0.3 V Sink	I_{OL}	3	1.30	–	1.10	5.0	–	0.66	–	
V_{out} = 0.4 V		5	1.90	–	1.70	6.0	–	1.08	–	
V_{out} = 0.5 V		9	3.80	–	3.30	10.0	–	2.10	–	
Output Current – Other Outputs	I_{OH}									mA
V_{out} = 2.7 V Source		3	−0.44	–	−0.35	−1.0	–	−0.22	–	
V_{out} = 4.6 V		5	−0.64	–	−0.51	−1.2	–	−0.36	–	
V_{out} = 8.5 V		9	−1.30	–	−1.00	−2.0	–	−0.70	–	
V_{out} = 0.3 V Sink	I_{OL}	3	0.44	–	0.35	1.0	–	0.22	–	
V_{out} = 0.4 V		5	0.64	–	0.51	1.2	–	0.36	–	
V_{out} = 0.5 V		9	1.30	–	1.00	2.0	–	0.70	–	
Input Current – Data, Clock, Enable	I_{in}	9	–	±0.3	–	±0.00001	±0.1	–	±1.0	μA
Input Current – f_{in}, OSC_{in}	I_{in}	9	–	±50	–	±10	±25	–	±22	μA
Input Capacitance	C_{in}	–	–	10	–	6	10	–	10	pF
3-State Output Capacitance – PD_{out}	C_{out}	–	–	10	–	6	10	–	10	pF
Quiescent Current	I_{DD}	3	–	800	–	200	800	–	1600	μA
V_{in} = 0 V or V_{DD}		5	–	1200	–	300	1200	–	2400	
I_{out} = 0 μA		9	–	1600	–	400	1600	–	3200	
3-State Leakage Current – PD_{out}	I_{OZ}	9	–	±0.3	–	±0.0001	±0.1	–	±3.0	μA
V_{out} = 0 V or 9 V										

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $C_L = 50$ pF)

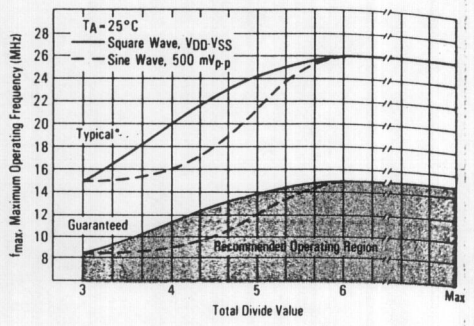
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Units
Output Rise Time, Modulus Control (Figures 2 and 8)	t_{TLH}	3	–	50	115	ns
		5	–	30	60	
		9	–	20	40	
Output Fall Time, Modulus Control (Figures 2 and 8)	t_{THL}	3	–	25	60	ns
		5	–	17	34	
		9	–	15	30	
Output Rise and Fall Time, LD, f_V, f_R, S/R_{out}, ϕV, ϕR (Figures 2 and 8)	t_{TLH}, t_{THL}	3	–	60	140	ns
		5	–	40	80	
		9	–	30	60	
Propagation Delay Time f_{in} to Modulus Control (Figures 3 and 8)	t_{PLH}, t_{PHL}	3	–	55	125	ns
		5	–	40	80	
		9	–	25	50	
Setup Times	t_{su}					ns
Data to Clock (Figure 4)		3	30	12	–	
		5	20	10	–	
		9	18	9	–	
Clock to Enable (Figure 4)		3	70	30	–	
		5	32	16	–	
		9	25	12	–	
Hold Time Clock to Data (Figure 4)	t_h	3	12	−8	–	ns
		5	12	−6	–	
		9	15	−5	–	
Recovery Time Enable to Clock (Figure 4)	t_{rec}	3	5	−15	–	ns
		5	10	−8	–	
		9	20	0	–	
Output Pulse Width ϕR, ϕV with f_R in Phase with f_V (Figures 5 and 8)	$t_{w\phi}$	3	25	100	175	ns
		5	20	60	100	
		9	10	40	70	
Input Rise and Fall Times Any Input (Figure 6)	t_r, t_f	3	–	20	5	μs
		5	–	5	2	
		9	–	2	0.5	
Input Pulse Width, Enable, Clock (Figure 7)	t_w	3	40	30	–	ns
		5	35	20	–	
		9	25	15	–	

GRAPH 1 – OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TOTAL DIVIDE VALUE

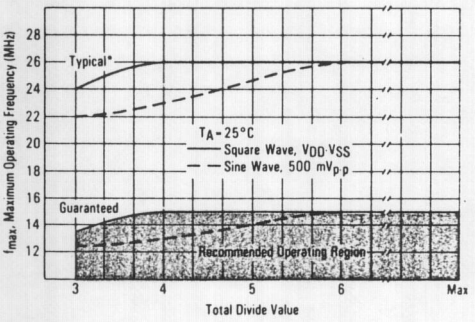
GRAPH 1A – V_{DD} = 3 V



GRAPH 1B – V_{DD} = 5 V

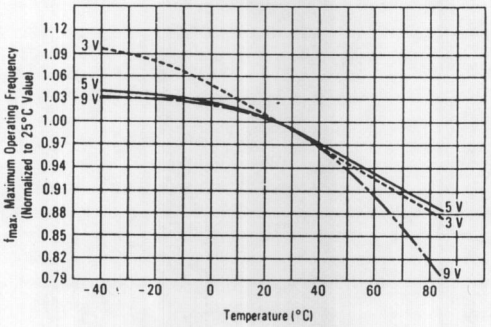


GRAPH 1C – V_{DD} = 9 V

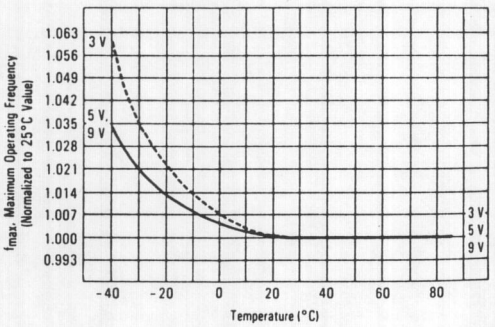


GRAPH 2 – OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TEMPERATURE FOR SINE AND SQUARE WAVE INPUTS

GRAPH 2A – TOTAL DIVIDE VALUE = 3, 4, OR 5



GRAPH 2B – TOTAL DIVIDE VALUE ≥ 6



* Data labelled "Typical" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

PIN DESCRIPTIONS

For the following text, the dash number has been omitted from the part number for simplicity.

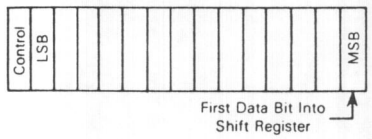
INPUTS

OSC_{in}, OSC_{out} (Pins 1, 2) — These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

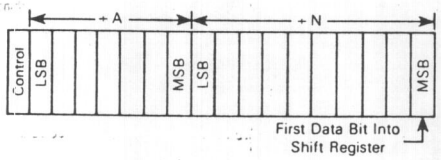
f_{in} (Pin 8) — Input frequency from VCO output. A rising edge signal on this input decrements the ÷ N counter (÷ A or ÷ N counter for the MC145158). This input has an inverter biased in the linear region to allow use with AC signals as low as 500 mV p-p or with a square wave of V_{DD} to V_{SS}.

Clock, Data (Pins 9, 10) — Shift register clock and data input. Each low-to-high transition of the clock shifts one bit of data into the on-chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic one selects the reference counter latch and a logic zero selects the ÷ N counter latch (÷ A, ÷ N counter latch for the MC145158). The data entry format is as follows:

MC145157 ÷ R and ÷ N Data Input
MC145158 ÷ R Data Input



MC145158 ÷ A, ÷ N Data Input



OUTPUTS

f_R, f_V (Pins 13, 3) — Divided reference and f_{in} frequency outputs. The f_R and f_V outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

PD_{out} (Pin 5) — Single ended (three-state) phase detector output. This output produces a loop error signal that is used with a loop filter to control a VCO. This phase detector output is described below and illustrated in Figure 9.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State

ϕ_R, ϕ_V (Pins 16, 15) — Double-ended phase detector outputs. These outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high (see Figure 9 for illustration).

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low; ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

S/R_{out} (Pin 12 of the MC145157) — Shift register output. This output can be connected to an external shift register to provide band switching, control information, and counter programming code checking.

Modulus Control (Pin 12 of the MC145158) — Modulus control output. This output generates a signal by the on-chip control logic circuitry for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N — A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual modulus prescaler divide values respectively for high and low modulus control levels, N the number programmed into the ÷ N counter and A the number programmed into the ÷ A counter. Note that when a prescaler is needed, the dual modulus version offers a distinct advantage. The dual modulus prescaler allows a higher reference frequency at the phase detector input, increasing system performance capability, and simplifying the loop filter design.

LD (Pin 7) — Lock detect signal. This output is at a high logic level when the loop is locked (f_R, f_V of same phase and frequency), and pulses low when the loop is out of lock.

REF_{out} (Pin 14) — Buffered reference oscillator output. This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

CONTROLS

Enable (Pin 11) — Latch Enable Input. A logic high on this pin latches the data from the shift register into the reference divider or ÷ N, ÷ A latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N, ÷ A latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters.

DUAL MODULUS PRESCALING

The technique of dual modulus prescaling is well established as a method of achieving high performance frequency

synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that would otherwise result if a fixed (single modulus) divider was used for the prescaler.

In dual modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P+1 in the prescaler for the required amount of time (see modulus control definition). The MC145158 contains this feature and can be used with a variety of dual modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P+1 divide values in the range of ÷3/÷4 to ÷128/÷129 can be controlled by the MC145158.

Several dual modulus prescaler approaches suitable for use with the MC145158 are given in Figure 1. The approaches range from the low cost ÷15/÷16, MC3393P device capable of system speeds in excess of 100 MHz to the MC12000 series having capabilities extending to greater than 500 MHz.

DESIGN GUIDELINES APPLICABLE TO THE MC145158

The system total divide value (N_{total}) will be dictated by the application, i.e.

$$N_{total} = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \bullet P + A$$

N is the number programmed into the ÷N counter; A is the number programmed into the ÷A counter. P and P+1 are the two selectable divide ratios available in the two modulus prescalers. To have a range of N_{total} values in sequence, the ÷A counter is programmed from zero through P−1 for a particular value N in the ÷N counter. N is then incremented to N+1 and the ÷A is sequenced from zero through P−1 again.

There are minimum and maximum values that can be achieved for N_{total}. These values are a function of P and the size of the ÷N and ÷A counters. the constraint $N \geq A$ always applies. If $A_{max} = P-1$ the $N_{min} \geq P-1$. Then $N_{(total-min)} = (P-1)P + A$ or $(P-1)P$ since A is free to assume the value of zero.

$$N_{(total-max)} = N_{max} \bullet P + A_{max}$$

To maximize system frequency capability, the dual modulus prescaler's output must go from low to high after each group of P or P+1 input cycles. The prescaler should divide by P when its modulus control line is high and by P+1 when its modulus control is low.

For the maximum frequency into the prescaler ($F_{vco}max$), the value used for P must be large enough such that:

A. f_{vco} max divided by P may not exceed the frequency capability of Pin 8 of the MC145158.

B. The period of $f_{vco(max)}$, divided by P, must be greater than the sum of the times:

   a. Propagation delay through the dual modulus prescaler.

   b. Prescaler setup or release time relative to its modulus control signal.

   c. Propagation time from f_{in} to the modulus control output for the MC145158.

A sometimes useful simplification in the MC145158 programming code can be achieved by choosing the values for P of 8, 16, 32, 64 or 128. For these cases, the desired value for N_{total} will result when N_{total} in binary is used as the program code to the ÷N and ÷A counters treated in the following manner:

A. Assume the ÷A counter contains "b" bits where $2^b = P$.

B. Always program all higher order ÷A counter bits above "b" to zero.

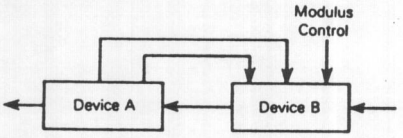
C. Assume the ÷N counter and the ÷A counter (with all the higher order bits above "b" ignored) combined into a single binary counter of 10+b bits in length. The MSB of this "hypothetical" counter is to correspond to the MSB of ÷N and the LSB is to correspond to the LSB of ÷A. The system divide value, N_{total}, now results when the value of N_{total} in binary is used to program the "New" 10+b bit counter.

FIGURE 1 — HIGH FREQUENCY DUAL MODULUS PRESCALERS FOR USE WITH THE MC145158

MC12009	÷5/÷6	440 MHz Min
MC12011	÷8/÷9	500 MHz Min
MC12013	÷10/÷11	500 MHz Min
MC12015	÷32/÷33	225 MHz Min
MC12016	÷40/÷41	225 MHz Min
MC12017	÷64/÷65	225 MHz Min
*MC12018	÷128/÷129	520 MHz Min
MC3393	÷15/÷16	140 MHz Typ

* Proposed Introduction 1983

By using two devices several dual modulus values are achievable:



Device A \ Device B	MC12009	MC12011	MC12013
MC10131	÷20/÷21	÷32/÷33	÷40/÷41
MC10138	÷50/÷51	÷80/÷81	÷100/÷101
MC10154	÷40/÷41 or ÷80/÷81	÷64/÷65 or ÷128/÷129	÷80/÷81

NOTE: MC12009, MC12011 and MC12013 are pin equivalent.
MC12015, MC12016, and MC12017 are pin equivalent.

145158 Xtal ÷10/11 Prescaler
P = 10
A = 0-127
N = 3-1023
f_{vco} = 45-75 MHz
N_{total} = NP+A
f_{ref} = 10MHz
R = 3-16383

$f_{vco} \div N_{total} = f_{ref} \div R$
$f_{vco} = (f_{ref} \div R) \cdot (NP+A)$

SWITCHING WAVEFORMS

FIGURE 2

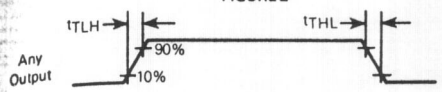


FIGURE 3

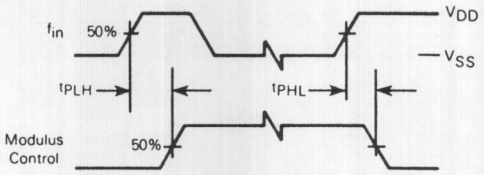


FIGURE 4

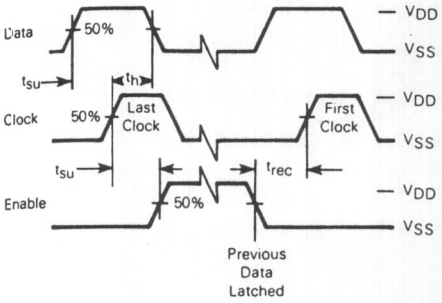
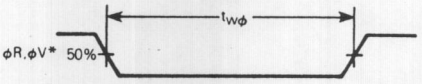


FIGURE 5



* f_R in phase with f_V

6

FIGURE 6

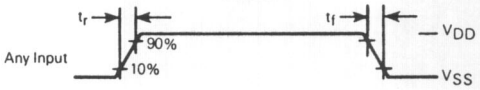


FIGURE 7

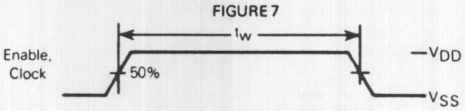


FIGURE 8 — TEST CIRCUIT

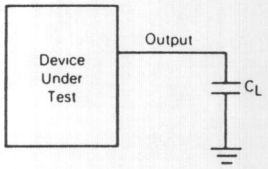
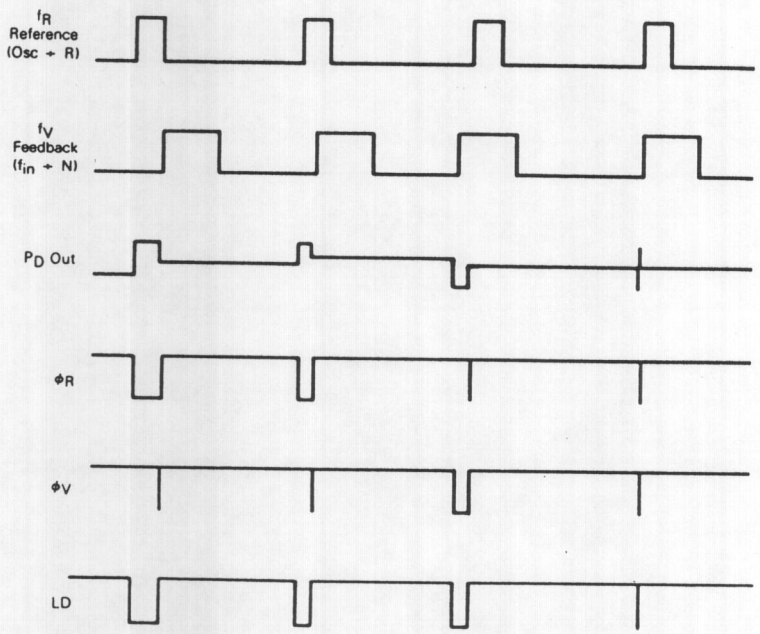


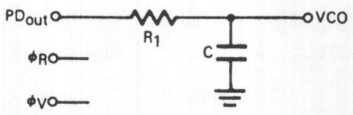
FIGURE 9
PHASE DETECTOR OUTPUT WAVEFORMS



NOTE: The P_D output state is approximately equal to either V_{DD} or V_{SS} when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

PHASE LOCKED LOOP — LOW PASS FILTER DESIGN

A)

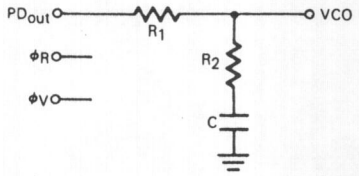


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1CS + 1}$$

B)

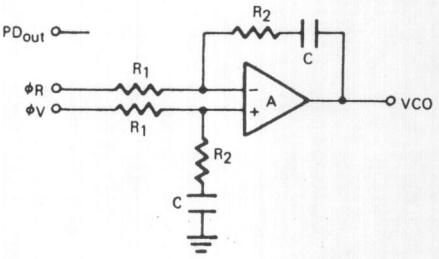


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\omega_n\left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2CS + 1}{S(R_1C + R_2C) + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

Assuming gain A is very large, then:

$$F(s) = \frac{R_2CS + 1}{R_1CS}$$

6

NOTE: Sometimes R_1 is split into two series resistors each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS: N = Total Division Ratio in feedback loop

$K_\phi = V_{DD}/4\pi$ for PD_{out}

$K_\phi = V_{DD}/2\pi$ for ϕ_V and ϕ_R

$$K_{VCO} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

for a typical design $\omega_n \cong \frac{2\pi f_r}{10}$ (at phase detector input),

$$\zeta \cong 1$$

RECOMMENDED FOR READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley-Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley-Interscience, 1980.
Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design*. New York, Wiley-Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley-Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice-Hall, 1983.
Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TXCOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TXCOs and data clock oscillators, please contact: Motorola Inc., Component Products, 2553 N. Edgington St., Franklin Park, IL 60131, phone (312) 451-1000.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12060, MC12061, MC12560, or MC12561 MECL devices. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure A.

For $V_{DD}=5$ V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_O + \frac{C1 \cdot C2}{C1+C2}$$

where C_{in} = 5 pF (see Figure C)
C_{out} = 6 pF (see Figure C)
C_a = 5 pF (see Figure C)
C_O = The crystal's holder capacitance (see Figure B)
C1 and C2 = External capacitors (see Figure A)

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the values for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure B. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure A limits the drive level. The use of R1 may not be necessary in some cases; i.e. R1 = 0 ohms.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table A.

TABLE A — PARTIAL LIST OF CRYSTAL MANUFACTURERS

NAME	ADDRESS	PHONE
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	1000 Crystal Dr., Ft. Myers, FL 33906	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

RECOMMENDED FOR READING

Technical Note TN-24, Statek Corp.

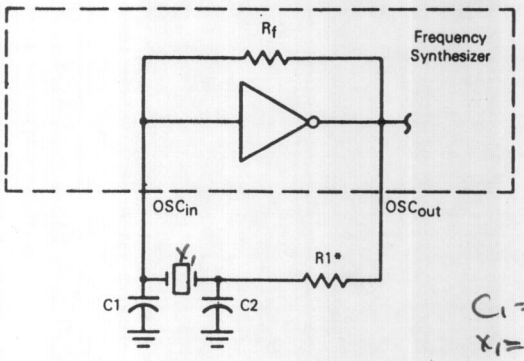
Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", *Proc. IEEE*, Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology*, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

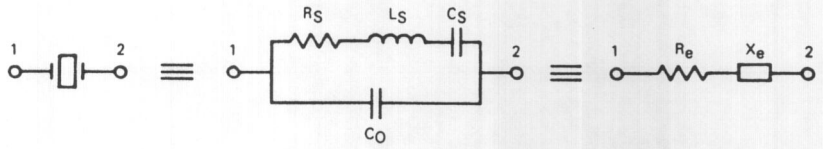
FIGURE A — PIERCE CRYSTAL OSCILLATOR CIRCUIT



*May be deleted in certain cases. See text.

$C_1 = C_2 = 1n$
$X_1 = 10\,MHz$
R_1 unnecessary
} deleted July/August 88 Sept. 88

FIGURE B — EQUIVALENT CRYSTAL NETWORKS



Values are supplied by crystal manufacturer (parallel resonant crystal).

6

FIGURE C — PARASITIC CAPACITANCES OF THE AMPLIFIER