# MOTOROLA
## SEMICONDUCTOR TECHNICAL DATA

## PLL Frequency Synthesizer with Serial Interface
### CMOS

The MC145170 is a single–chip synthesizer capable of direct usage in the MF, HF, and VHF bands. A special architecture makes this PLL the easiest to program in the industry. Either a bit– or byte–oriented format may be used. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 2–byte serial transfer to the 16–bit N register.

The device features fully programmable R and N counters, an amplifier at the $f_{in}$ pin, on–chip support of an external crystal, a programmable reference output, and both single– and double–ended phase detectors with linear transfer functions. A new feature on the MC145170 is the C register (configuration register). The C register allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing noise and interference.

In order to reduce lock times and prevent erroneous data from being loaded into the counters, a patented jam–load feature is included. Whenever a new divide ratio is loaded into the N register, both the N and R counters are jam loaded with their respective values and begin counting down together. The phase detectors are also initialized during the jam load.

- Operating Voltage Range: 2.5 to 6.0 V
- Maximum Operating Frequency:
  160 MHz @ $V_{in}$ = 500 mV p–p, 4.5 V Minimum Supply
  100 MHz @ $V_{in}$ = 500 mV p–p, 3.0 V Minimum Supply
- Operating Temperature Range: – 40 to 85°C.
- R Counter Division Range: 5 to 32,767 Plus Direct Access to Phase Detector Input
- N Counter Division Range: 40 to 65,535
- Direct Interface to Motorola SPI and National MICROWIRE™ Serial Data Ports
- Higher Frequency Versions Available (Part Numbers MC145170P1 and MC145170D1)
- Chip Complexity: 4800 FETs or 1200 Equivalent Gates
- See Application Note AN1207

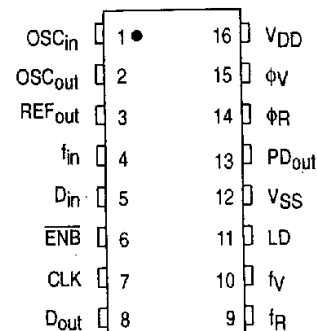## MC145170
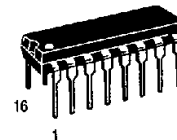
P SUFFIX
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CASE 648
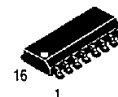
D SUFFIX
SOG PACKAGE
CASE 751B

### ORDERING INFORMATION

MC145170P    Plastic DIP
MC145170D    SOG Package

### PIN ASSIGNMENT

| | | | |
|---|---|---|---|
| OSC$_{in}$ | 1● | 16 | V$_{DD}$ |
| OSC$_{out}$ | 2 | 15 | φV |
| REF$_{out}$ | 3 | 14 | φR |
| f$_{in}$ | 4 | 13 | PD$_{out}$ |
| D$_{in}$ | 5 | 12 | V$_{SS}$ |
| ENB | 6 | 11 | LD |
| CLK | 7 | 10 | f$_V$ |
| D$_{out}$ | 8 | 9 | f$_R$ |

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**For new designs, the MC145170P1 and MC145170D1 are preferred devices over the MC145170P and MC145170D, respectively. Please see the MC145170–1 data sheet.**
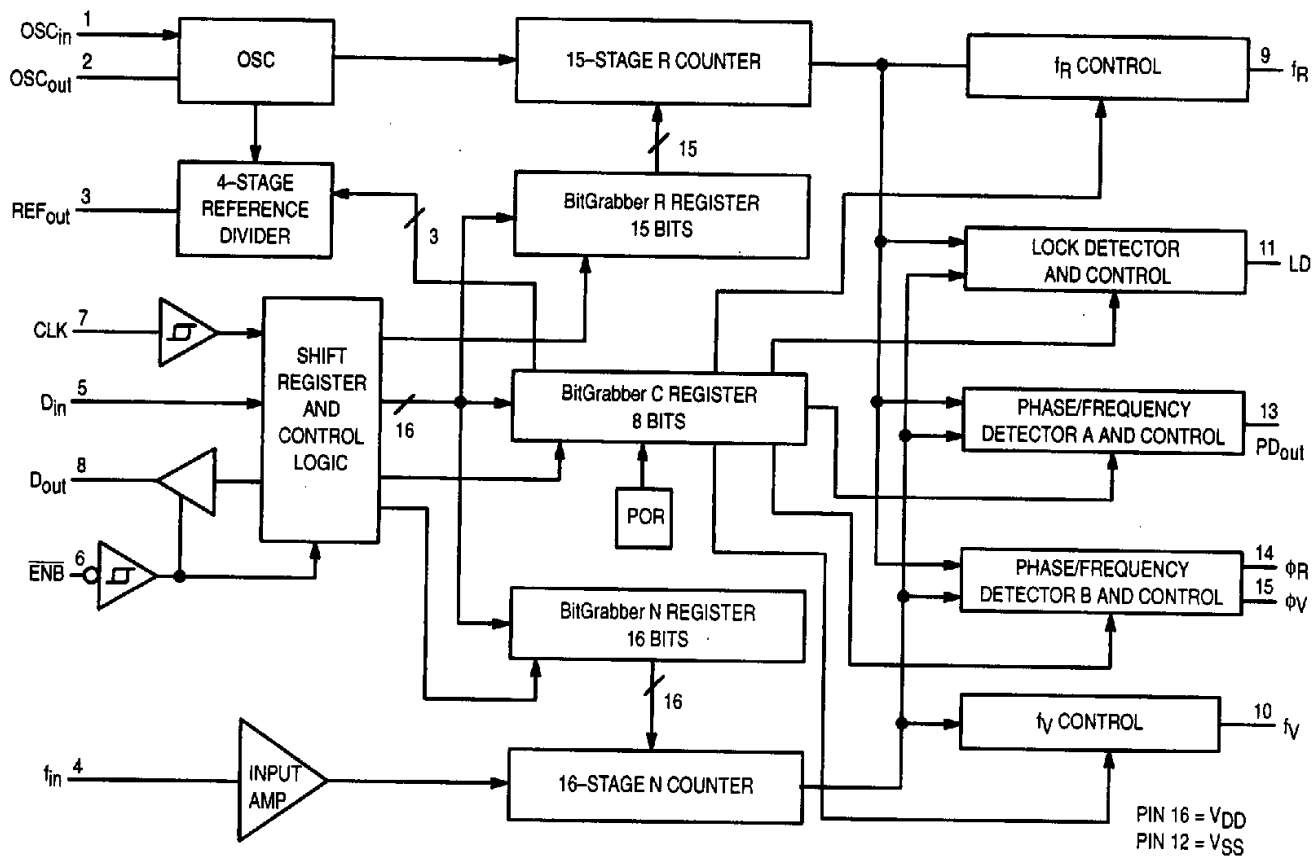
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BitGrabber is a trademark of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

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## BLOCK DIAGRAM

## MAXIMUM RATINGS* (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $V_{DD}$ | DC Supply Voltage | − 0.5 to + 6.0 | V |
| $V_{in}$ | DC Input Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $V_{out}$ | DC Output Voltage | − 0.5 to $V_{DD}$ + 0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ± 10 | mA |
| $I_{out}$ | DC Output Current, per Pin | ± 20 | mA |
| $I_{DD}$ | DC Supply Current, $V_{DD}$ and $V_{SS}$ Pins | ± 30 | mA |
| $P_D$ | Power Dissipation, per Package | 300 | mW |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 seconds | 260 | °C |

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.

**MOTOROLA**

MC145170

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$, $T_A$ = – 40 to +85°C)

| Symbol | Parameter | Test Condition | $V_{DD}$ V | Guaranteed Limit | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage Range | | — | 2.5 to 6.0 | V |
| $V_{IL}$ | Maximum Low–Level Input Voltage ($D_{in}$, CLK, $\overline{ENB}$) | | 2.5 / 4.5 / 6.0 | 0.50 / 1.35 / 1.80 | V |
| $V_{IH}$ | Minimum High–Level Input Voltage ($D_{in}$, CLK, $\overline{ENB}$) | | 2.5 / 4.5 / 6.0 | 2.00 / 3.15 / 4.20 | V |
| $V_{Hys}$ | Minimum Hysteresis Voltage (CLK, $\overline{ENB}$) | | 2.5 / 6.0 | 0.15 / 0.20 | V |
| $V_{OL}$ | Maximum Low–Level Output Voltage (Any Output) | $I_{out}$ = 20 µA | 2.5 / 6.0 | 0.1 / 0.1 | V |
| $V_{OH}$ | Minimum High–Level Output Voltage (Any Output) | $I_{out}$ = – 20 µA | 2.5 / 6.0 | 2.4 / 5.9 | V |
| $I_{OL}$ | Minimum Low–Level Output Current ($PD_{out}$, $REF_{out}$, $f_R$, $f_V$, LD, $\phi_R$, $\phi_V$) | $V_{out}$ = 0.3 V / $V_{out}$ = 0.4 V / $V_{out}$ = 0.5 V | 2.5 / 4.5 / 6.0 | 0.12 / 0.36 / 0.50 | mA |
| $I_{OH}$ | Minimum High–Level Output Current ($PD_{out}$, $REF_{out}$, $f_R$, $f_V$, LD, $\phi_R$, $\phi_V$) | $V_{out}$ = 2.2 V / $V_{out}$ = 4.1 V / $V_{out}$ = 5.5 V | 2.5 / 4.5 / 6.0 | – 0.12 / – 0.36 / – 0.50 | mA |
| $I_{OL}$ | Minimum Low–Level Output Current ($D_{out}$) | $V_{out}$ = 0.4 V | 4.5 | 1.6 | mA |
| $I_{OH}$ | Minimum High–Level Output Current ($D_{out}$) | $V_{out}$ = 4.1 V | 4.5 | – 1.6 | mA |
| $I_{in}$ | Maximum Input Leakage Current ($D_{in}$, CLK, $\overline{ENB}$, $OSC_{in}$) | $V_{in}$ = $V_{DD}$ or $V_{SS}$ | 6.0 | ± 1.0 | µA |
| $I_{in}$ | Maximum Input Current ($f_{in}$) | $V_{in}$ = $V_{DD}$ or $V_{SS}$ | 6.0 | ± 120 | µA |
| $I_{OZ}$ | Maximum Output Leakage Current ($PD_{out}$) | $V_{in}$ = $V_{DD}$ or $V_{SS}$, Output in High–Impedance State | 6.0 | ± 100 | nA |
| | ($D_{out}$) | | 6.0 | ± 5 | µA |
| $I_{DD}$ | Maximum Quiescent Supply Current | $V_{in}$ = $V_{DD}$ or $V_{SS}$; Outputs Open; Excluding $f_{in}$ Amp Input Current Component | 6.0 | 100 | µA |
| $I_{dd}$ | Maximum Operating Supply Current | $f_{in}$ = 160 MHz @ 500 mV p–p; $OSC_{in}$ = 10 MHz @ 1 V p–p; $f_R$, $f_V$, $REF_{out}$ = Inactive and No Connect; $OSC_{out}$, $\phi_V$, $\phi_R$, $PD_{out}$, LD = No Connect; $D_{in}$, ENB, CLK = $V_{DD}$ or $V_{SS}$ | 5.0 | * | mA |

\* The nominal value is 7 mA. This is not a guaranteed limit.
Current consumption is reduced at lower frequencies and/or lower supply voltages (i.e., at 100 MHz with a 3 V supply, the device draws about 2.5 mA).

MC145170     **MOTOROLA**

## AC INTERFACE CHARACTERISTICS ($T_A$ = – 40 to + 85°C, $C_L$ = 50 pF, Input $t_r$ = $t_f$ = 10 ns unless otherwise indicated)

| Symbol | Parameter | | Figure No. | $V_{DD}$ V | Guaranteed Limit | Unit |
|---|---|---|---|---|---|---|
| $f_{clk}$ | Serial Data Clock Frequency (Note: Refer to Clock $t_w$ Below) | | 1 | 2.5<br>4.5<br>6.0 | —<br>dc to 4.0<br>dc to 4.0 | MHz |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, CLK to $D_{out}$ | | 1, 5 | 2.5<br>4.5<br>6.0 | —<br>85<br>85 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Maximum Disable Time, $D_{out}$ Active to High Impedance | | 2, 6 | 2.5<br>4.5<br>6.0 | —<br>200<br>200 | ns |
| $t_{PZL}$, $t_{PZH}$ | Access Time, $D_{out}$ High Impedance to Active | | 2, 6 | 2.5<br>4.5<br>6.0 | —<br>0 to 100<br>0 to 100 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, $D_{out}$ | CL = 50 pF | 1, 5 | 2.5<br>4.5<br>6.0 | —<br>50<br>50 | ns |
| | | CL = 200 pF | 1, 5 | 2.5<br>4.5<br>6.0 | —<br>150<br>150 | ns |
| $C_{in}$ | Maximum Input Capacitance — $D_{in}$, $\overline{ENB}$, CLK | | | — | 10 | pF |
| $C_{out}$ | Maximum Output Capacitance — $D_{out}$ | | | — | 15 | pF |

NOTE: For low–voltage applications, the MC145170–1 is recommended. The new MC145170–1 data sheet contains guaranteed 2.5 V parameters.

## TIMING REQUIREMENTS ($T_A$ = – 40 to + 85°C, Input $t_r$ = $t_f$ = 10 ns unless otherwise indicated)

| Symbol | Parameter | Figure No. | $V_{DD}$ V | Guaranteed Limit | Unit |
|---|---|---|---|---|---|
| $t_{su}$, $t_h$ | Minimum Setup and Hold Times, $D_{in}$ vs CLK | 3 | 2.5<br>4.5<br>6.0 | —<br>40<br>40 | ns |
| $t_{su}$, $t_h$, $t_{rec}$ | Minimum Setup, Hold, and Recovery Times, $\overline{ENB}$ vs CLK | 4 | 2.5<br>4.5<br>6.0 | —<br>100<br>100 | ns |
| $t_{w(H)}$ | Minimum Inactive–High Pulse Width, $\overline{ENB}$ | 4 | 2.5<br>4.5<br>6.0 | —<br>300<br>300 | ns |
| $t_w$ | Minimum Pulse Width, CLK | 1 | 2.5<br>4.5<br>6.0 | —<br>125<br>125 | ns |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Times, CLK | 1 | 2.5<br>4.5<br>6.0 | 100<br>100<br>100 | µs |

NOTE: For low–voltage applications, the MC145170–1 is recommended. The new MC145170–1 data sheet contains guaranteed 2.5 V parameters.
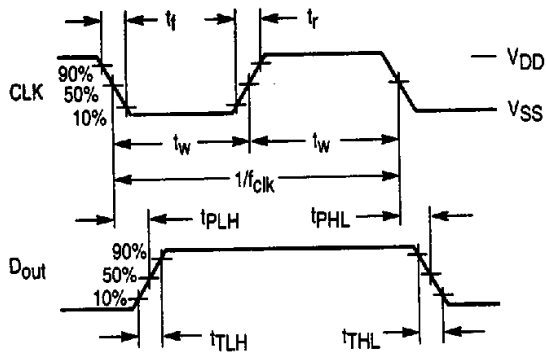
MOTOROLA

MC145170

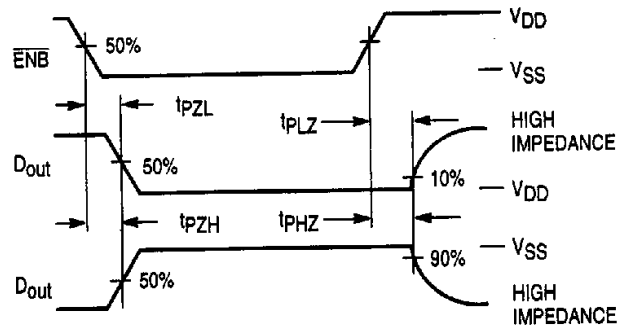## SWITCHING WAVEFORMS

**Figure 1.**

**Figure 2.**

**Figure 3.**

**Figure 4.**

DEVICE UNDER TEST

TEST POINT

$C_L$*

* Includes all probe and fixture capacitance.

**Figure 5. Test Circuit**

DEVICE UNDER TEST

TEST POINT

7.5 kΩ

$C_L$*

CONNECT TO $V_{DD}$ WHEN TESTING $t_{PLZ}$ AND $t_{PZL}$. CONNECT TO $V_{SS}$ WHEN TESTING $t_{PHZ}$ AND $t_{PZH}$.

* Includes all probe and fixture capacitance.
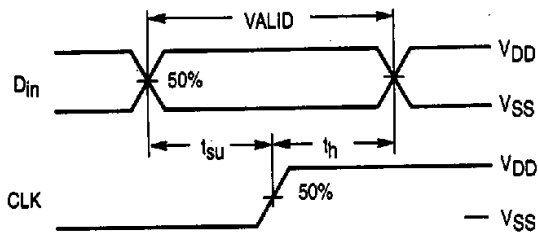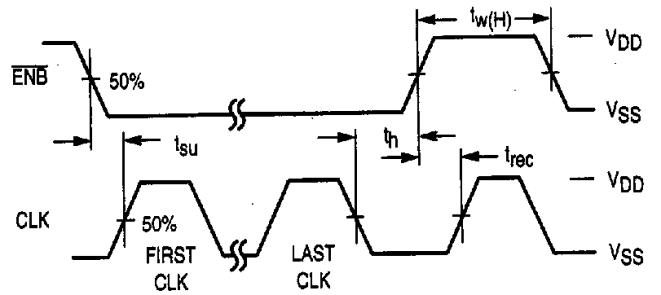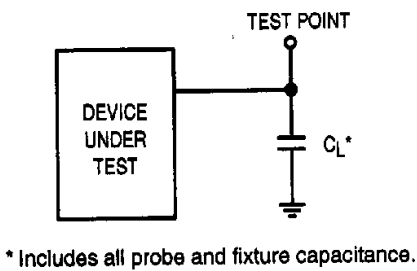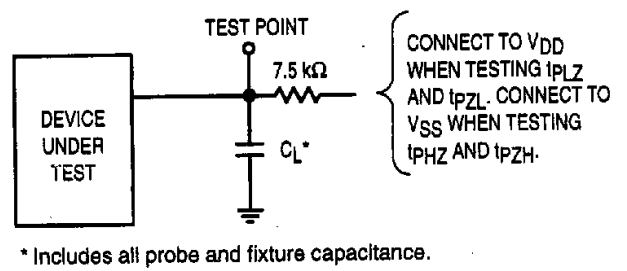
**Figure 6. Test Circuit**

**LOOP SPECIFICATIONS** ($T_A = -40$ to $+85°C$)

| Symbol | Parameter | Test Condition | Figure No. | $V_{DD}$ V | Guaranteed Range | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| f | Input Frequency, $f_{in}$ | $V_{in} \geq 500$ mV p–p Sine Wave, N Counter set to divide ratio such that $f_V \leq 2$ MHz | 7 | 2.5 | — | — | MHz |
| | | | | 3.0 | — | 100 | |
| | | | | 4.5 | — | 160 | |
| | | | | 6.0 | — | 160 | |
| f | Input Frequency, $OSC_{in}$ Externally Driven with ac Coupled Signal | $V_{in} \geq 1$ V p–p Sine Wave, $OSC_{out}$ = No Connect, R Counter set to divide ratio such that $f_R \leq 2$ MHz | 8 | 2.5 | 1 | 12 | MHz |
| | | | | 3.0 | 1 | 14 | |
| | | | | 4.5 | 1 | 20 | |
| | | | | 6.0 | 1 | 20 | |
| $f_{XTAL}$ | Crystal Frequency, $OSC_{in}$ and $OSC_{out}$ | C1 $\leq$ 30 pF, C2 $\leq$ 30 pF, Includes Stray Capacitance | 9 | 2.5 | 2 | 12 | MHz |
| | | | | 3.0 | 2 | 12 | |
| | | | | 4.5 | 2 | 15 | |
| | | | | 6.0 | 2 | 15 | |
| $f_{out}$ | Output Frequency, $REF_{out}$ | $C_L = 30$ pF | 10, 12 | 2.5 | dc | — | MHz |
| | | | | 3.0 | dc | — | |
| | | | | 4.5 | dc | 10 | |
| | | | | 6.0 | dc | 10 | |
| f | Operating Frequency of the Phase Detectors | | | 2.5 | dc | — | MHz |
| | | | | 3.0 | dc | — | |
| | | | | 4.5 | dc | 2 | |
| | | | | 6.0 | dc | 2 | |
| $t_w$ | Output Pulse Width, $\phi_R$, $\phi_V$, and LD | $f_R$ in Phase with $f_V$, $C_L = 50$ pF | 11, 12 | 2.5 | — | — | ns |
| | | | | 3.0 | — | — | |
| | | | | 4.5 | 20 | 100 | |
| | | | | 6.0 | 16 | 90 | |
| $t_{TLH}$, $t_{THL}$ | Output Transition Times, $\phi_R$, $\phi_V$, LD, $f_R$, and $f_V$ | $C_L = 50$ pF | 11, 12 | 2.5 | — | — | ns |
| | | | | 3.0 | — | — | |
| | | | | 4.5 | — | 65 | |
| | | | | 6.0 | — | 60 | |
| $C_{in}$ | Input Capacitance   $f_{in}$ / $OSC_{in}$ | | — / — | — / — | — / — | 5 / 5 | pF |

NOTE: For low–voltage applications, the MC145170–1 is recommended. The new MC145170–1 data sheet contains guaranteed 2.5 V parameters.

SINE WAVE GENERATOR —○— 100 pF — $f_{in}$ MC145170 $f_V$ ○ TEST POINT

50 Ω* $V_{in}$ $V_{SS}$ $V_{DD}$ V+
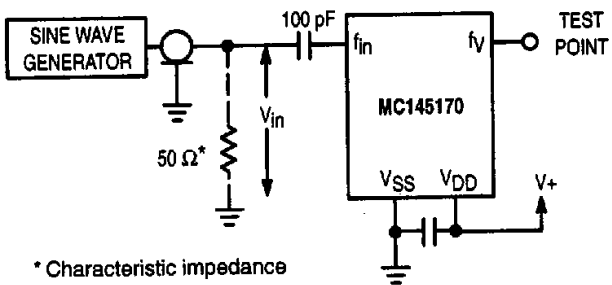
* Characteristic impedance

**Figure 7. Test Circuit**

SINE WAVE GENERATOR —○— 0.01 μF — $OSC_{in}$ MC145170 $f_R$ ○ TEST POINT

50 Ω $V_{in}$ 10 MΩ $OSC_{out}$ $V_{SS}$ $V_{DD}$ V+

**Figure 8. Test Circuit**

C1 $OSC_{in}$ MC145170 $REF_{out}$ ○ TEST POINT

C2 $OSC_{out}$ $V_{SS}$ $V_{DD}$ V+
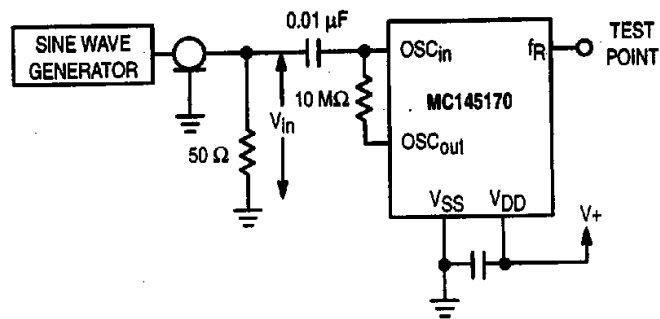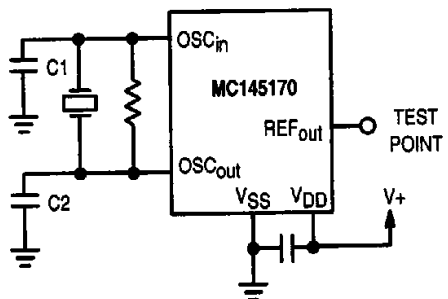
**Figure 9. Test Circuit**

$REF_{out}$ ← 1/f $REF_{out}$ → 50%
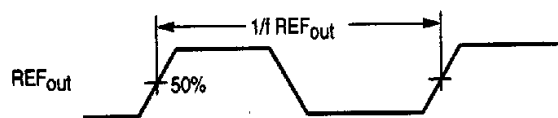
**Figure 10. Switching Waveform**

OUTPUT 50% 90% $t_W$ 10% $t_{THL}$ $t_{TLH}$
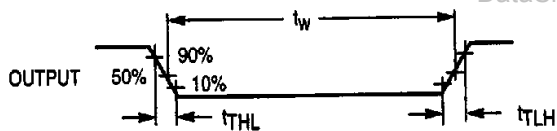
**Figure 11. Switching Waveform**

DEVICE UNDER TEST OUTPUT —○ TEST POINT $C_L$*
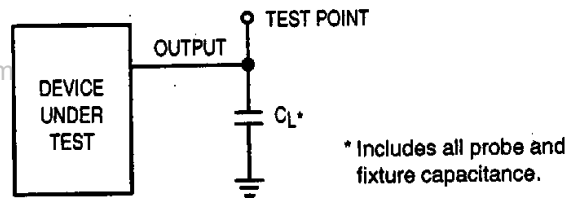
* Includes all probe and fixture capacitance.

**Figure 12. Test Circuit**

# PIN DESCRIPTIONS

## DIGITAL INTERFACE PINS

### $D_{in}$
**Serial Data Input (Pin 5)**

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R register. Optionally, the R register can be accessed with a 15–bit transfer (see Table 1). The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.5 to 6.0 V. The formats are shown in Figures 13, 14, and 15.

$D_{in}$ typically switches near 50% of $V_{DD}$ to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull-up resistor of 1 to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case $I_{OL}$ of the driving device, maximum tolerable power consumption, and maximum data rate.

**Table 1. Register Access**
(MSBs are shifted in first, C0, N0, and R0 are the LSBs)

| Number of Clocks | Accessed Register | Bit Nomenclature |
|---|---|---|
| 8 | C Register | C7, C6, C5, . . ., C0 |
| 16 | N Register | N15, N14, N13, . . ., N0 |
| 15 or 24 | R Register | R14, R13, R12, . . ., R0 |
| Other Values ≤ 32 | None | |
| Values > 32 | TBD | |

### CLK
**Serial Data Clock Input (Pin 7)**

Low–to–high transitions on Clock shift bits available at $D_{in}$, while high–to–low transitions shift bits from $D_{out}$. The chip's 16–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. Either 15 or 24 cycles can be used to access the R register (see Table 1 and Figures 13, 14, and 15).

CLK typically switches near 50% of $V_{DD}$ and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of $D_{in}$ for more information.

**CAUTION**

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at the potential of either the $V_{SS}$ or $V_{DD}$ pin during power up. Do *not* float or toggle the CLK input during power up.

### $\overline{ENB}$
**Active Low Enable Input (Pin 6)**

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited, $D_{out}$ is forced to the high–impedance state, and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via $D_{in}$ and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C, N, or R register depending on the data stream length per Table 1.

**CAUTION**

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 50% of $V_{DD}$, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of $D_{in}$ for more information.

### $D_{out}$
**Three–State Serial Data Output (Pin 8)**

Data is transferred out of the 16–1/2 stage shift register through $D_{out}$ on the high–to–low transition of CLK. This output is a No Connect, unless used in one of the manners discussed below.

$D_{out}$ could be fed back to an MCU/MPU to perform a wrap-around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, PC board traces, solder joints, etc. The pin could be monitored at an in–line QA test during board manufacturing.

Finally, $D_{out}$ facilitates troubleshooting a system.

## REFERENCE PINS

### $OSC_{in}/OSC_{out}$
**Reference Oscillator Input/Output (Pins 1, 2)**

These pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1 to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The MC145170 is designed to operate with crystals up to 15 MHz with a 4.5 to 6.0 V supply. With supplies less than 4.5 V, up to 12 MHz crystals may be used. (See Figure 9.)

If desired, an external clock source can be ac coupled to $OSC_{in}$. A 0.01 µF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications. An external feedback resistor of approximately 10 MΩ is required across the $OSC_{in}$ and $OSC_{out}$ pins in the ac–coupled case (see Figure 8). *$OSC_{out}$ is an internal node on the device and should not be used to drive any loads* (i.e., $OSC_{out}$ is unbuffered). However, the buffered $REF_{out}$ is available to drive external loads.

The external signal level must be at least 1 V p–p; the maximum frequencies are given in the **Loop Specifications** table. These maximum frequencies apply for R Counter divide ratios as indicated in the table. For very small ratios, the

**2**

maximum frequency is limited to the divide ratio times 2 MHz when the internal phase/frequency detectors are used. (Reason: the phase/frequency detectors are limited to a maximum input frequency of 2 MHz.)

If an external source is available which swings from at least the $V_{IL}$ to $V_{IH}$ levels listed in the **Electrical Characteristics** table, then dc coupling can be used. In the dc coupled case, no external feedback resistor is needed. $OSC_{out}$ must be a No Connect to avoid loading an internal node on the MC145170, as noted above. For frequencies below 1 MHz, dc coupling must be used. The R counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the $OSC_{in}$ pin.

Each rising edge on the $OSC_{in}$ pin causes the R counter to decrement by one.

## $REF_{out}$
### Reference Frequency Output (Pin 3)

This output is the buffered output of the crystal-generated reference frequency or externally provided reference source. This output may be enabled, disabled, or scaled via bits in the C register (see Figure 13).

$REF_{out}$ can be used to drive a microprocessor clock input, thereby saving a crystal. Upon power up, the on-chip power-on-initialize circuit forces $REF_{out}$ to the $OSC_{in}$ divided-by-8 mode.

$REF_{out}$ is capable of operation to 10 MHz; see the **Loop Specifications** table. Therefore, divide values for the reference divider are restricted to two or higher for $OSC_{in}$ frequencies above 10 MHz.

If unused, the pin should be floated and should be disabled via the C register to minimize dynamic power consumption and electromagnetic interference (EMI).

## COUNTER OUTPUT PINS

### $f_R$
### R Counter Output (Pin 9)

This signal is the buffered output of the 15-stage R counter. $f_R$ can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The $f_R$ signal can be used to verify the R counter's divide ratio. This ratio extends from 5 to 32,767 and is determined by the binary value loaded into the R register. Also, direct access to the phase detector via the $OSC_{in}$ pin is allowed by choosing a divide value of 1 (see Figure 14). The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of $f_R$ must not exceed 2 MHz unless an external phase detector is used. The maximum frequency for driving external phase detectors is TBD.

When activated, the $f_R$ signal appears as normally low and pulses high.

### $f_V$
### N Counter Output (Pin 10)

This signal is the buffered output of the 16-stage N counter. $f_V$ can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The $f_V$ signal can be used to verify the N counter's divide ratio. This ratio extends from 40 to 65,535 and is determined by the binary value loaded into the N register. The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of $f_V$ must not exceed 2 MHz unless an external phase detector is used. The maximum frequency for driving external phase detectors is TBD.

When activated, the $f_V$ signal appears as normally low and pulses high.

## LOOP PINS

### $f_{in}$
### Frequency Input (Pin 4)

This pin is a frequency input from the VCO. This pin feeds the on-chip amplifier which drives the N counter. This signal is normally sourced from an external voltage-controlled oscillator (VCO), and is ac coupled into $f_{in}$. A 100 pF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications (see Figure 7). The frequency capability of this input is dependent on the supply voltage as listed in the **Loop Specifications** table. For small divide ratios, the maximum frequency is limited to the divide ratio times 2 MHz when the internal phase/frequency detectors are used. (Reason: the phase/frequency detectors are limited to a maximum frequency of 2 MHz.)

For signals which swing from at least the $V_{IL}$ to $V_{IH}$ levels listed in the **Electrical Characteristics** table, dc coupling may be used. Also, for low frequency signals, dc coupling is a requirement. The N counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the $f_{in}$ pin.

Each rising edge on the $f_{in}$ pin causes the N counter to decrement by 1.

### $PD_{out}$
### Single-Ended Phase/Frequency Detector Output (Pin 13)

This is a three-state output for use as a loop-error signal when combined with an external low-pass filter. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 16.

POL bit (C7) in the C register = low (see Figure 13)

Frequency of $f_V$ > $f_R$ or Phase of $f_V$ Leading $f_R$: negative pulses from high impedance

Frequency of $f_V$ < $f_R$ or Phase of $f_V$ Lagging $f_R$: positive pulses from high impedance

Frequency and Phase of $f_V$ = $f_R$: essentially high-impedance state; voltage at pin determined by loop filter

POL bit (C7) = high

Frequency of $f_V$ > $f_R$ or Phase of $f_V$ Leading $f_R$: positive pulses from high impedance

Frequency of $f_V$ < $f_R$ or Phase of $f_V$ Lagging $f_R$: negative pulses from high impedance

Frequency and Phase of $f_V$ = $f_R$: essentially high-impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD$_{out}$ can be forced to the high–impedance state by utilization of the disable feature in the C register (patented).

## $\phi$R and $\phi$V
### Double–Ended Phase/Frequency Detector Outputs (Pins 14, 15)

These outputs can be combined externally to generate a loop–error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 16.

POL bit (C7) in the C register = low (see Figure 13)

Frequency of f$_V$ > f$_R$ or Phase of f$_V$ Leading f$_R$: $\phi$V = negative pulses, $\phi$R = essentially high

Frequency of f$_V$ < f$_R$ or Phase of f$_V$ Lagging f$_R$: $\phi$V = essentially high, $\phi$R = negative pulses

Frequency and Phase of f$_V$ = f$_R$: $\phi$V and $\phi$R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of f$_V$ > f$_R$ or Phase of f$_V$ Leading f$_R$: $\phi$R = negative pulses, $\phi$V = essentially high

Frequency of f$_V$ < f$_R$ or Phase of f$_V$ Lagging f$_R$: $\phi$R = essentially high, $\phi$V = negative pulses

Frequency and Phase of f$_V$ = f$_R$: $\phi$V and $\phi$R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via the C register (patented).

## LD
### Lock Detector Output (Pin 11)

This output is essentially at a high level with narrow low-going pulses when the loop is locked (f$_R$ and f$_V$ of the same phase and frequency). The output pulses low when f$_V$ and f$_R$ are out of phase or different frequencies (see Figure 16).

This output can be enabled and disabled via the C register (patented). Upon power–up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

## POWER SUPPLY

### V$_{DD}$
#### Most Positive Supply Potential (Pin 16)

This pin may range from + 2.5 to 6.0 V with respect to V$_{SS}$.

For optimum performance, V$_{DD}$ should be bypassed to V$_{SS}$ using low–inductance capacitor(s) mounted very close to the MC145170. Lead lengths on the capacitor(s) should be minimized. (The very fast switching speed of the device causes current spikes on the power leads.)

### V$_{SS}$
#### Most Negative Supply Potential (Pin 12)

This pin is usually ground. For measurement purposes, the V$_{SS}$ pin is tied to a ground plane.
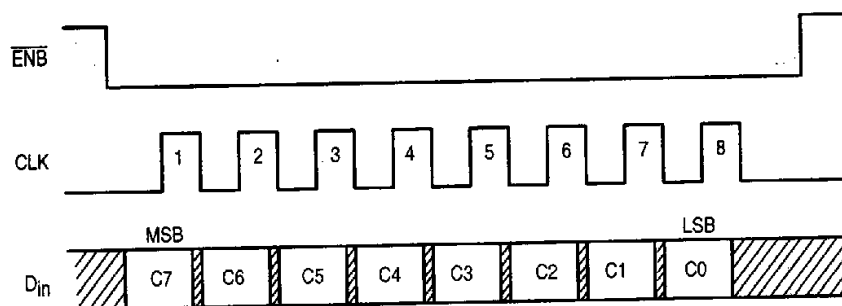
C7 – POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts $PD_{out}$ and interchanges the $\phi_R$ function with $\phi_V$ as depicted in Figure 16. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power–up.

C6 – PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A ($PD_{out}$) and disables phase/frequency detector B by forcing $\phi_R$ and $\phi_V$ to the static high state. When cleared low, phase/frequency detector B is enabled ($\phi_R$ and $\phi_V$) and phase/frequency detector A is disabled with $PD_{out}$ forced to the high–impedance state. This bit is cleared low at power–up.

C5 – LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power–up.

C4 – C2, OSC2 – OSC0: Reference output controls which determine the $REF_{out}$ characteristics as shown below. Upon power–up, the bits are initialized such that $OSC_{in}/8$ is selected.

| C4 | C3 | C2 | $REF_{out}$ Frequency |
|----|----|----|---------------------|
| 0 | 0 | 0 | dc (Static Low) |
| 0 | 0 | 1 | $OSC_{in}$ |
| 0 | 1 | 0 | $OSC_{in}/2$ |
| 0 | 1 | 1 | $OSC_{in}/4$ |
| 1 | 0 | 0 | $OSC_{in}/8$ |
| 1 | 0 | 1 | $OSC_{in}/16$ |
| 1 | 1 | 0 | $OSC_{in}/8$ |
| 1 | 1 | 1 | $OSC_{in}/16$ |

C1 – $f_V$E: Enables the $f_V$ output when set high. When cleared low, the $f_V$ output is forced to a static low level. The bit is cleared low upon power–up.

C0 – $f_R$E: Enables the $f_R$ output when set high. When cleared low, the $f_R$ output is forced to a static low level. The bit is cleared low upon power–up.

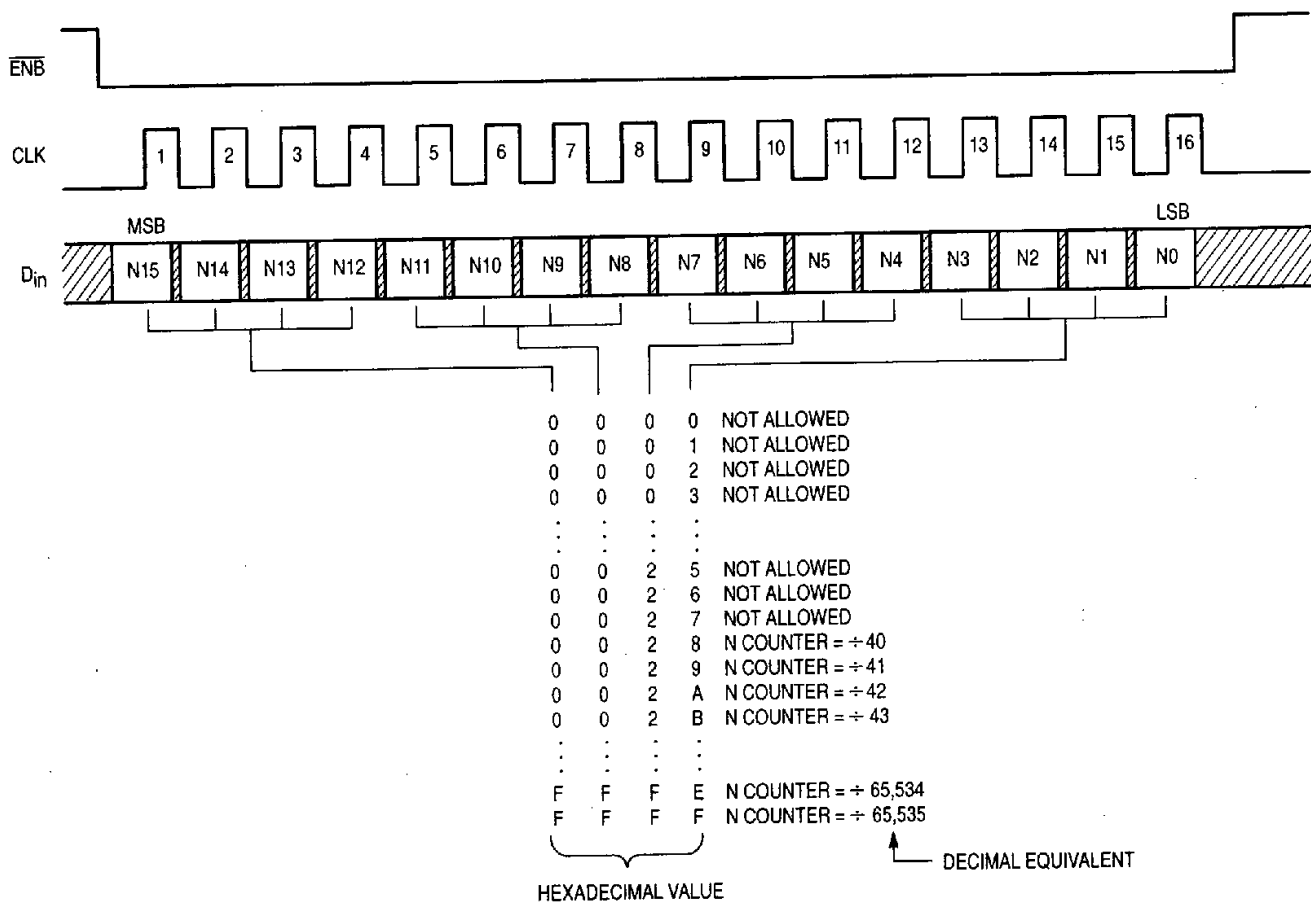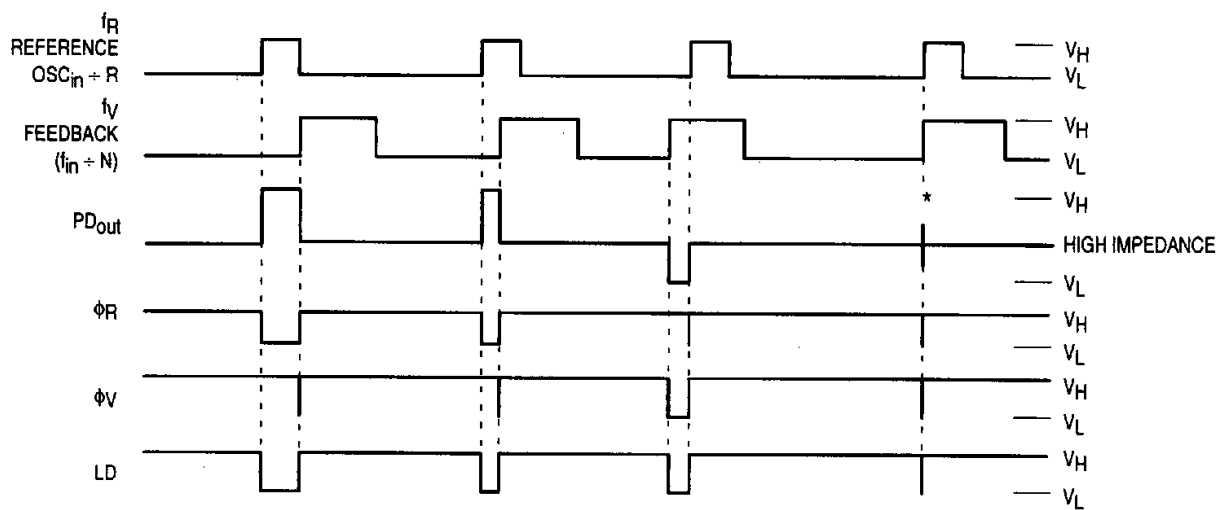**Figure 13. C Register Access and Format (8 Clock Cycles are Used)**

2

LSB

R0 R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14

SEE BELOW

SEE BELOW

SEE BELOW

SEE BELOW

DON'T CARE BITS

MSB

X X X X X X X X

ENB

CLK

D<sub>in</sub>

LSB

R0 R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14

MSB

ENB

CLK

D<sub>in</sub>

DIRECT ACCESS TO REFERENCE SIDE OF PHASE/FREQUENCY DETECTOR)

| | | HEXADECIMAL VALUE | DECIMAL EQUIVALENT |
|---|---|---|---|
| 0 0 0 | 0 | NOT ALLOWED | |
| 0 0 0 | 1 | R COUNTER = ÷1 (DIRECT ACCESS TO REFERENCE SIDE OF PHASE/FREQUENCY DETECTOR) | |
| 0 0 0 | 2 | NOT ALLOWED | |
| 0 0 0 | 3 | NOT ALLOWED | |
| 0 0 0 | 4 | NOT ALLOWED | |
| 0 0 0 | 5 | R COUNTER = ÷5 | |
| 0 0 0 | 6 | R COUNTER = ÷6 | |
| 0 0 0 | 7 | R COUNTER = ÷7 | |
| . . . | . | . . . . | |
| 7 F F | E | R COUNTER = ÷32,766 | |
| 7 F F | F | R COUNTER = ÷32,767 | |

OCTAL VALUE

HEXADECIMAL VALUE

DECIMAL EQUIVALENT

**Figure 14. R Register Access and Formats (Either 24 or 15 Clock Cycles can be Used)**

MOTOROLA

MC145170

Figure 15. N Register Access and Format (16 Clock Cycles are Used)

The figure shows timing waveforms for $\overline{ENB}$, CLK (clock cycles 1–16), and $D_{in}$ with bits from MSB (N15) to LSB (N0): N15, N14, N13, N12, N11, N10, N9, N8, N7, N6, N5, N4, N3, N2, N1, N0.

| | | | | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | NOT ALLOWED |
| 0 | 0 | 0 | 1 | NOT ALLOWED |
| 0 | 0 | 0 | 2 | NOT ALLOWED |
| 0 | 0 | 0 | 3 | NOT ALLOWED |
| . | . | . | . | |
| 0 | 0 | 2 | 5 | NOT ALLOWED |
| 0 | 0 | 2 | 6 | NOT ALLOWED |
| 0 | 0 | 2 | 7 | NOT ALLOWED |
| 0 | 0 | 2 | 8 | N COUNTER = ÷ 40 |
| 0 | 0 | 2 | 9 | N COUNTER = ÷ 41 |
| 0 | 0 | 2 | A | N COUNTER = ÷ 42 |
| 0 | 0 | 2 | B | N COUNTER = ÷ 43 |
| . | . | . | . | |
| F | F | F | E | N COUNTER = ÷ 65,534 |
| F | F | F | F | N COUNTER = ÷ 65,535 |

DECIMAL EQUIVALENT

HEXADECIMAL VALUE

MC145170

$V_H$ = High voltage level.

$V_L$ = Low voltage level.

* At this point, when both $f_R$ and $f_V$ are in phase, both the source and sink turn on for a very short time.

NOTE: The $PD_{out}$ generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor. $PD_{out}$, $\phi R$, and $\phi V$ are shown with the polarity bit (POL) = low; see Figure 13 for POL.

**Figure 16. Phase/Frequency Detectors and Lock Detector Output Waveforms**

2

## DESIGN CONSIDERATIONS

### CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

### Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC$_{in}$. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC$_{in}$ may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog*, the *Gold Book*, or similar publications.

### Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC$_{in}$ (see Figure 8). For large amplitude signals (standard CMOS logic levels), dc coupling is used.

### Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 17.

The crystal should be specified for a loading capacitance (C$_L$) which does not exceed 20 pF when used at the highest operating frequency. Larger C$_L$ values are possible for lower frequencies. Assuming R1 = 0 Ω, the shunt load capacitance (C$_L$) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

where
  C$_{in}$ = 5 pF (see Figure 18)
  C$_{out}$ = 6 pF (see Figure 18)
  C$_a$ = 1 pF (see Figure 18)
  C1 and C2 = external capacitors (see Figure 17)
  C$_{stray}$ = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC$_{in}$ and OSC$_{out}$ pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C$_{in}$ and C$_{out}$. For this approach, the term C$_{stray}$ becomes 0 in the above expression for C$_L$.

Power is dissipated in the effective series resistance of the crystal, R$_e$, in Figure 19. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 17 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency at the REF$_{out}$ pin (OSC$_{out}$ is not used because loading impacts the oscillator). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 2).
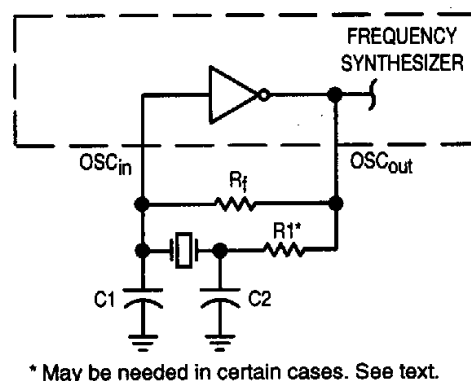


* May be needed in certain cases. See text.
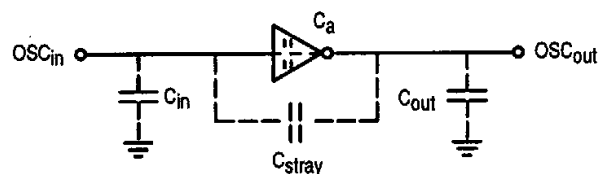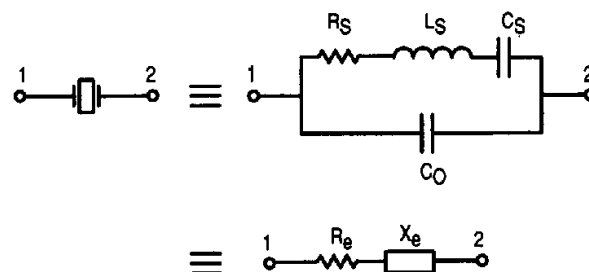
**Figure 17. Pierce Crystal Oscillator Circuit**



**Figure 18. Parasitic Capacitances of the Amplifier and C$_{stray}$**



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

**Figure 19. Equivalent Crystal Networks**

## RECOMMENDED READING

Technical Note TN–24, Statek Corp.
Technical Note TN–7, Statek Corp.
E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.
D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology,* June 1969.
P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design,* May 1966.
D. Babin, "Designing Crystal Oscillators", *Machine Design,* March 7, 1985.
D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design,* April 25, 1985.

**2**

### Table 2. Partial List of Crystal Manufacturers

| Name | Address | Phone |
|---|---|---|
| United States Crystal Corp. | 3605 McCart Ave., Ft. Worth, TX 76110 | (817) 921–3013 |
| Crystek Crystal | 2351 Crystal Dr., Ft. Myers, FL 33907 | (813) 936–2109 |
| Statek Corp. | 512 N. Main St., Orange, CA 92668 | (714) 639–7810 |
| Fox Electronics | 5570 Enterprise Parkway, Ft. Myers, FL 33905 | (813) 693–0099 |

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.
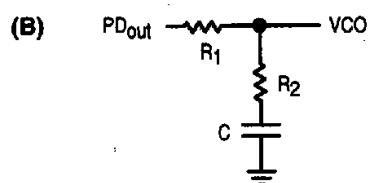
## PHASE–LOCKED LOOP — LOW PASS FILTER DESIGN

(A)
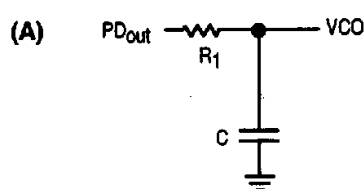
$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$
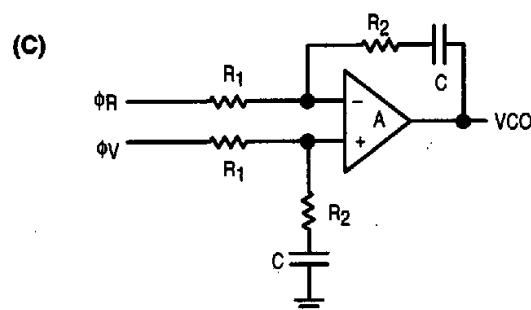
$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

(B)

$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left( R_2C + \frac{N}{K_\phi K_{VCO}} \right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

(C)

$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTE:

For (C), $R_1$ is frequently split into two series resistors; each resistor is equal to $R_1$ divided by 2. A capacitor $C_C$ is then placed from the midpoint to ground to further filter the error pulses. The value of $C_C$ should be such that the corner frequency of this network does not significantly affect $\omega_n$.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

$K_\phi$ (Phase Detector Gain) = $V_{DD}/4\pi$ V/radian for $PD_{out}$

$K_\phi$ (Phase Detector Gain) = $V_{DD}/2\pi$ V/radian for $\phi_V$ and $\phi_R$

$$K_{VCO} \text{ (VCO Gain)} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where $f_R$ is the frequency at the phase detector input. Larger $\omega_n$ values result in faster loop lock times and, for similar sideband filtering, higher $f_R$–related VCO sidebands.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley–Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley–Interscience, 1980.
Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design*. New York, Wiley–Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley–Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice–Hall, 1983.
Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN*. March 5, 1980.
AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design*, 1987.
AN1207, The MC145170 in Basic HF and VHF Oscillators, Motorola Semiconductor Products, Inc., 1992.
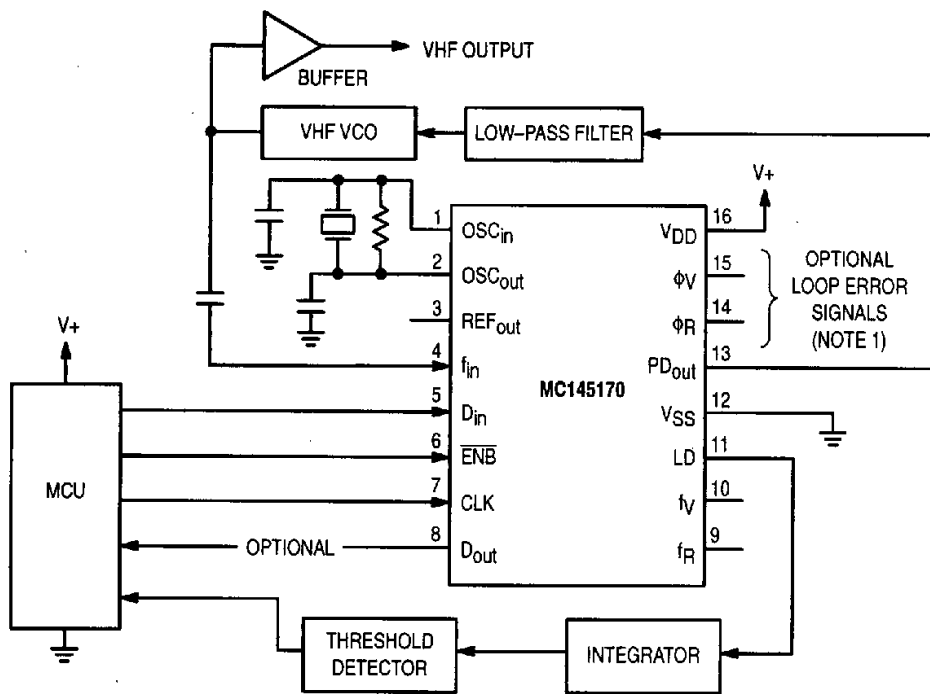
NOTES:
1. The $\phi_R$ and $\phi_V$ outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. For optimum performance, bypass the $V_{DD}$ pin to $V_{SS}$ (GND) with one or more low–inductance capacitors.
3. The R counter is programmed for a divide value = $OSC_{in}/f_R$. Typically, $f_R$ is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R$ = N, where N is the divide value of the N counter.

**Figure 20. Example Application**