

MC14569B

Programmable Divide-By-N Dual 4-Bit Binary/BCD Down Counter

The MC14569B is a programmable divide-by-N dual 4-bit binary or BCD down counter constructed with MOS P-Channel and N-Channel enhancement mode devices (complementary MOS) in a monolithic structure.

This device has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

Features

- Speed-up Circuitry for Zero Detection
- Each 4-Bit Counter Can Divide Independently in BCD or Binary Mode
- Can be Cascaded With MC14526B for Frequency Synthesizer Applications
- All Outputs are Buffered
- Schmitt Triggered Clock Conditioning
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	± 10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	-55 to +125	$^{\circ}C$
T_{stg}	Storage Temperature Range	-65 to +150	$^{\circ}C$
T_L	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Package: -7.0 mW/ $^{\circ}C$ From 65 $^{\circ}C$ To 125 $^{\circ}C$

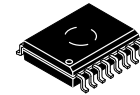
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



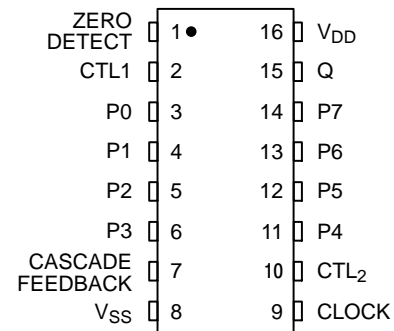
ON Semiconductor®

<http://onsemi.com>

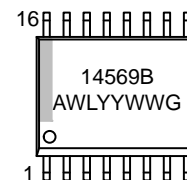


SOIC-16 WB
DW SUFFIX
CASE 751G

PIN ASSIGNMENT



MARKING DIAGRAM



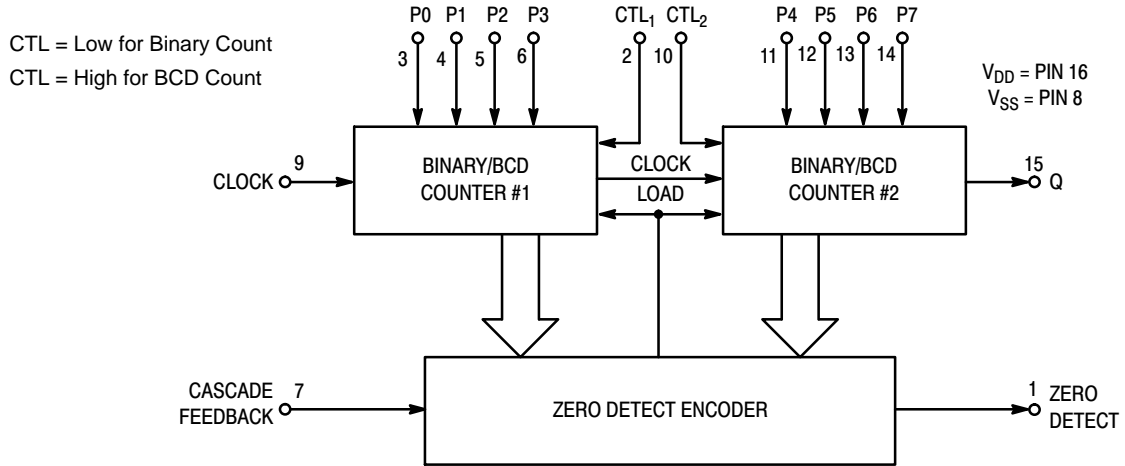
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC14569B

BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
MC14569BDWG	SOIC-16 WB (Pb-Free)	47 Units / Rail
MC14569BDWR2G	SOIC-16 WB (Pb-Free)	1000 Units / Tape & Reel
NLV14569BDWR2G*	SOIC-16 WB (Pb-Free)	1000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MC14569B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	- 55° C		25° C			125° C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	“0” Level V _{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc	
		10	–	0.05	–	0	0.05	–	0.05		
15		–	0.05	–	0	0.05	–	0.05			
V _{in} = 0 or V _{DD}	“1” Level V _{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc	
		10	9.95	–	9.95	10	–	9.95	–		
		15	14.95	–	14.95	15	–	14.95	–		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	“0” Level V _{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc	
		10	–	3.0	–	4.50	3.0	–	3.0		
		15	–	4.0	–	6.75	4.0	–	4.0		
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	“1” Level V _{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc	
		10	7.0	–	7.0	5.50	–	7.0	–		
		15	11	–	11	8.25	–	11	–		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
			5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	
			10	–1.6	–	–1.3	–2.25	–	–0.9	–	
			15	–4.2	–	–3.4	–8.8	–	–2.4	–	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink	I _{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
			10	1.6	–	1.3	2.25	–	0.9	–	
			15	4.2	–	3.4	8.8	–	2.4	–	
Input Current	I _{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	–	–	–	–	5.0	7.5	–	–	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc	
		10	–	10	–	0.010	10	–	300		
		15	–	20	–	0.015	20	–	600		
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.58 μA/kHz) f + I _{DD} I _T = (1.20 μA/kHz) f + I _{DD} I _T = (1.95 μA/kHz) f + I _{DD}							μAdc	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

MC14569B

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} Vdc	All Types			Unit
			Min	Typ (Note 5)	Max	
Output Rise Time	t _{TLH}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Output Fall Time	t _{THL}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Turn-On Delay Time Zero Detect Output Q Output	t _{PLH}	5.0	–	420	700	ns
		10	–	175	300	
		15	–	125	250	
		5.0	–	675	1200	ns
		10	–	285	500	
		15	–	200	400	
Turn-Off Delay Time Zero Detect Output Q Output	t _{PHL}	5.0	–	380	600	ns
		10	–	150	300	
		15	–	100	200	
		5.0	–	530	1000	ns
		10	–	225	400	
		15	–	155	300	
Clock Pulse Width	t _{WH}	5.0	300	100	–	ns
		10	150	45	–	
		15	115	30	–	
Clock Pulse Frequency	f _{cl}	5.0	–	3.5	2.1	MHz
		10	–	9.5	5.1	
		15	–	13.0	7.8	
Clock Pulse Rise and Fall Time	t _{TLH} , t _{THL}	5.0	NO LIMIT			μs
		10				
		15				

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING WAVEFORMS

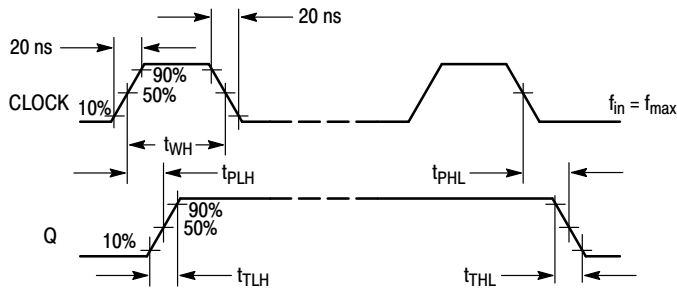


Figure 1.

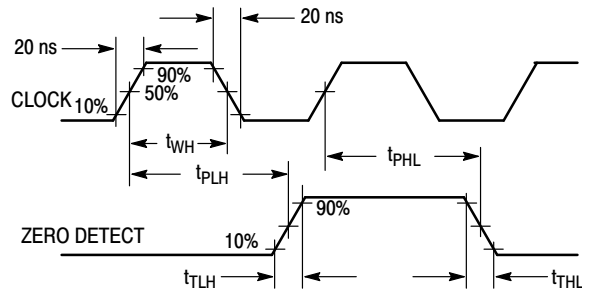


Figure 2.

MC14569B

PIN DESCRIPTIONS

INPUTS

P0, P1, P2, P3 (Pins 3, 4, 5, 6) – Preset Inputs. Programmable inputs for the least significant counter. May be binary or BCD depending on the control input.

P4, P5, P6, P7 (Pins 11, 12, 13, 14) – Preset Inputs. Programmable inputs for the most significant counter. May be binary or BCD depending on the control input.

Clock (Pin 9) – Preset data is decremented by one on each positive transition of this signal.

OUTPUTS

Zero Detect (Pin 1) – This output is normally low and goes high for one clock cycle when the counter has decremented to zero.

Q (Pin 15) – Output of the last stage of the most significant counter. This output will be inactive unless the preset input P7 has been set high.

CONTROLS

Cascade Feedback (Pin 7) – This pin is normally set high. When low, loading of the preset inputs (P0 through P7) is inhibited, i.e., P0 through P7 are “don’t cares.” Refer to Table 1 for output characteristics.

CTL₁ (Pin 2) – This pin controls the counting mode of the least significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

CTL₂ (Pin 10) – This pin controls the counting mode of the most significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

SUPPLY PINS

V_{SS} (Pin 18) – Negative Supply Voltage. This pin is usually connected to ground.

V_{DD} (Pin 16) – Positive Supply Voltage. This pin is connected to a positive supply voltage ranging from 3.0 V to 18 V.

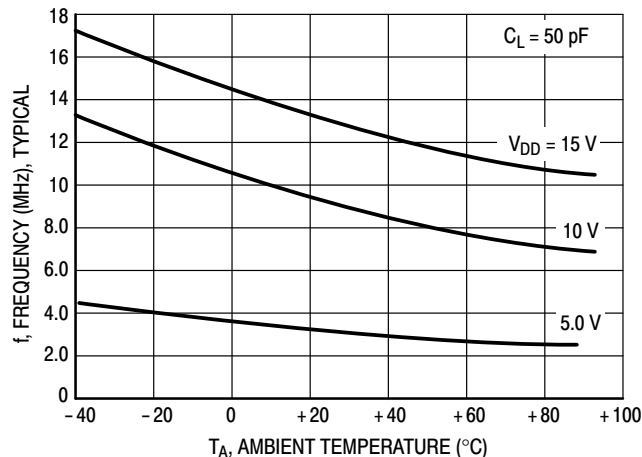
OPERATING CHARACTERISTICS

The MC14569B is a programmable divide-by-N dual 4-bit down counter. This counter may be programmed (i.e., preset) in BCD or binary code through inputs P0 to P7. For each counter, the counting sequence may be chosen independently by applying a high (for BCD count) or a low (for binary count) to the control inputs CTL₁ and CTL₂.

The divide ratio N (N being the value programmed on the preset inputs P0 to P7) is automatically loaded into the counter as soon as the count 1 is detected. Therefore, a division ratio of one is not possible. After N clock cycles,

one pulse appears on the Zero Detect output. (See Timing Diagram.) The Q output is the output of the last stage of the most significant counter (See Tables 1 through 5, Mode Controls.)

When cascading the MC14569B to the MC14526B, the Cascade Feedback input, Q, and Zero Detect outputs must be respectively connected to “0”, Clock, and Load of the following counter. If the MC14569B is used alone, Cascade Feedback must be connected to V_{DD}.



MC14569B

Table 1 Mode Controls (Cascade Feedback = Low)

Counter Control Values		Divide Ratio	
CTL ₁	CTL ₂	Zero Detect	Q
0	0	256	256
0	1	160	160
1	0	160	160
1	1	100	100

NOTE: Data Preset Inputs (P0–P7) are “Don't Cares” while Cascade Feedback is Low.

Table 2 Mode Controls (CTL₁ = Low, CTL₂ = Low, Cascade Feedback = High)

Preset Inputs								Divide Ratio		Comments
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	
0	0	0	0	0	0	0	0	256	256	Max Count Illegal State Min Count
0	0	0	0	0	0	0	1	X	X	
0	0	0	0	0	0	1	0	2	X	
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	0	0	0	0	0	32	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	0	0	0	0	0	64	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	1	1	1	1	1	127	X	
1	0	0	0	0	0	0	0	128	128	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	0	1	0	0	0	136	136	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	1	1	1	1	1	1	1	255	255	
2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰			Bit Value
128	64	32	16	8	4	2	1			Counting Sequence
Counter #2 Binary				Counter #1 Binary						

Q Output Active
↓

X = No Output (Always Low)

MC14569B

Table 3 Mode Controls (CTL₁ = High, CTL₂ = Low, Cascade Feedback = High)

Preset Inputs								Divide Ratio		Comments	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q		
0	0	0	0	0	0	0	0	160	160	Max Count Illegal State Min Count	
0	0	0	0	0	0	0	1	X	X		
0	0	0	0	0	0	1	0	2	X		
0	0	0	0	0	0	1	1	3	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
0	0	0	0	1	0	0	1	9	X		
0	0	0	1	0	0	0	0	10	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
0	0	0	1	1	0	0	1	19	X		
0	0	1	0	0	0	0	0	20	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
0	0	1	1	0	0	0	0	30	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
0	1	0	0	0	0	0	0	40	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
0	1	0	1	0	0	0	0	50	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
0	1	1	0	0	0	0	0	60	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
0	1	1	1	0	0	0	0	70	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
1	0	0	0	0	0	0	0	80	80	Q Output Active ↓	
•	•	•	•	•	•	•	•	•	•		
•	•	•	•	•	•	•	•	•	•		
•	•	•	•	•	•	•	•	•	•		
1	0	0	1	0	0	0	0	90	90		
•	•	•	•	•	•	•	•	•	•		
•	•	•	•	•	•	•	•	•	•		
•	•	•	•	•	•	•	•	•	•		
1	1	1	1	0	0	0	0	150	150		
•	•	•	•	•	•	•	•	•	•		
•	•	•	•	•	•	•	•	•	•		
•	•	•	•	•	•	•	•	•	•		
1	1	1	1	1	0	0	1	159	159		
80	40	20	10	8	4	2	1				Bit Value
Counter #2 Binary				Counter #1 BCD							Counting Sequence

X = No Output (Always Low)

MC14569B

Table 4 Mode Controls (CTL₁ = Low, CTL₂ = High, Cascade Feedback = High)

Preset Values								Divide Ratio		Comments
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	
0	0	0	0	0	0	0	0	160	160	Max Count Illegal State Min Count
0	0	0	0	0	0	0	1	X	X	
0	0	0	0	0	0	1	0	2	X	
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	1	1	1	1	1	31	X	
0	0	1	0	0	0	0	0	32	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	1	0	0	0	0	48	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	0	0	0	0	0	0	64	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	0	1	0	0	0	0	80	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	1	1	0	0	0	0	112	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	0	0	0	0	0	128	128	Q Output Active ↓
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	144	144	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	1	1	1	1	159	159	
2 ⁷ 128	2 ⁶ 64	2 ⁵ 32	2 ⁴ 16	2 ³ 8	2 ² 4	2 ¹ 2	2 ⁰ 1			Bit Value
Counter #2 BCD				Counter #1 Binary						Counting Sequence

X = No Output (Always Low)

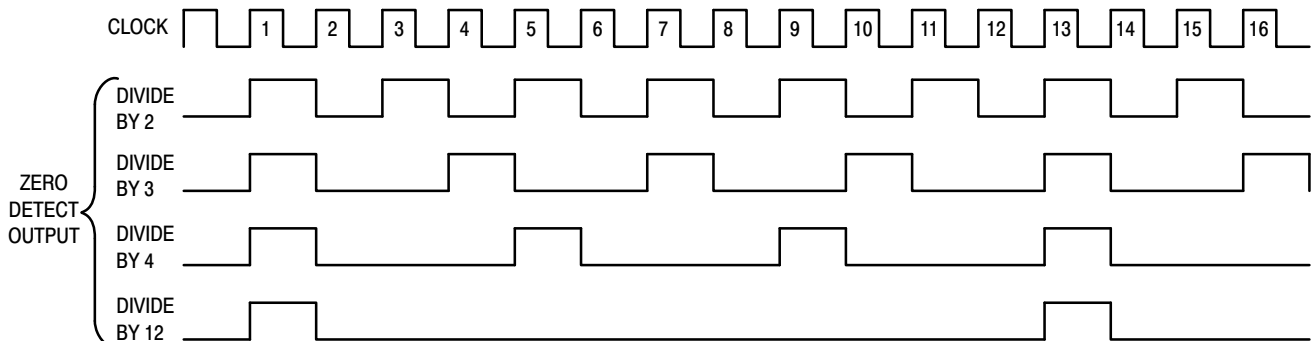
MC14569B

Table 5 Mode Controls (CTL₁ = High, CTL₂ = High, Cascade Feedback = High)

Preset Values								Divide Ratio		Comments	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q		
0	0	0	0	0	0	0	0	100	100	Max Count illegal state Min Count	
0	0	0	0	0	0	0	1	X	X		
0	0	0	0	0	0	1	0	2	X		
0	0	0	0	0	0	1	1	3	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
0	0	0	0	1	0	0	1	9	X		
0	0	0	1	0	0	0	0	10	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
0	0	1	1	0	0	0	0	30	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
0	1	0	0	0	0	0	0	40	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
0	1	0	1	0	0	0	0	50	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
0	1	1	1	0	0	0	0	70	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
1	0	0	0	0	0	0	0	80	80	Q Output Active ↓	
•	•	•	•	•	•	•	•	•	•		
•	•	•	•	•	•	•	•	•	•		
•	•	•	•	•	•	•	•	•	•		
1	0	0	1	0	0	0	0	90	90		
•	•	•	•	•	•	•	•	•	•		
•	•	•	•	•	•	•	•	•	•		
1	0	0	1	1	0	0	1	99	99		
80	40	20	10	8	4	2	1				Bit Value
Counter #2 BCD				Counter #1 BCD							

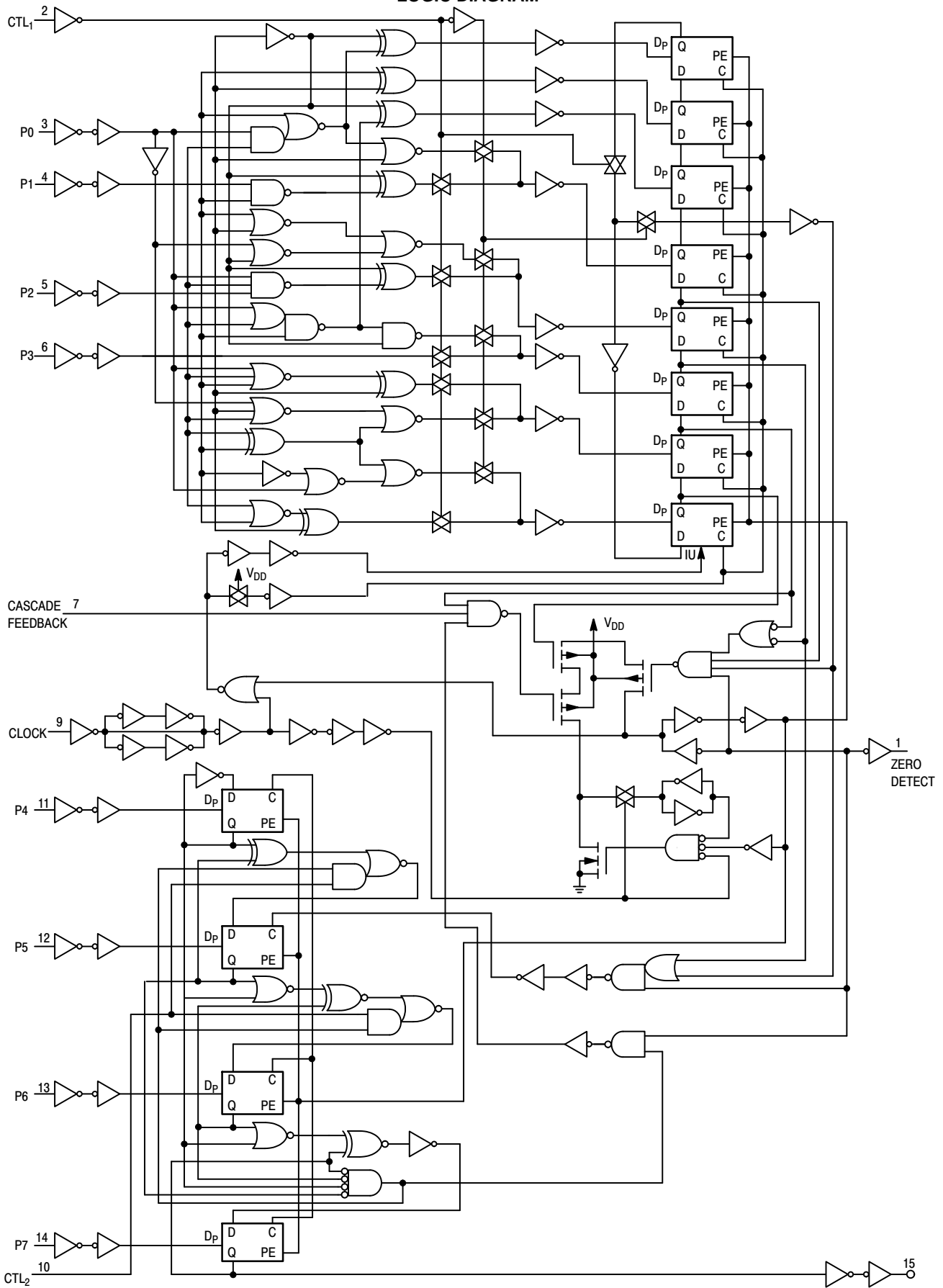
X = No Output (Always Low)

TIMING DIAGRAM MC14569B



MC14569B

LOGIC DIAGRAM



MC14569B

TYPICAL APPLICATIONS

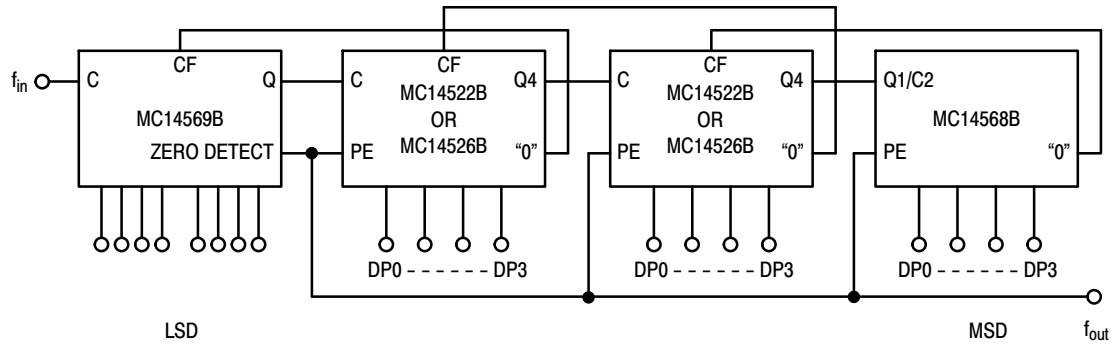
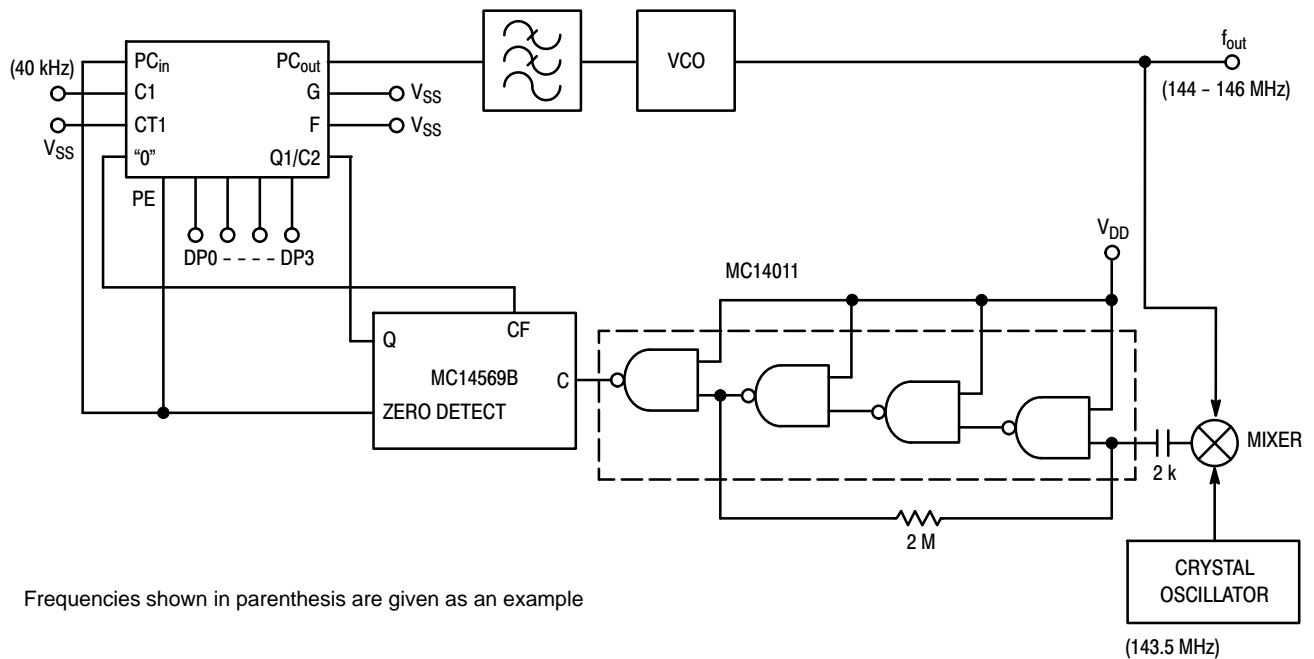


Figure 3. Cascading MC14568B and MC14522B or MC14526B with MC14569B



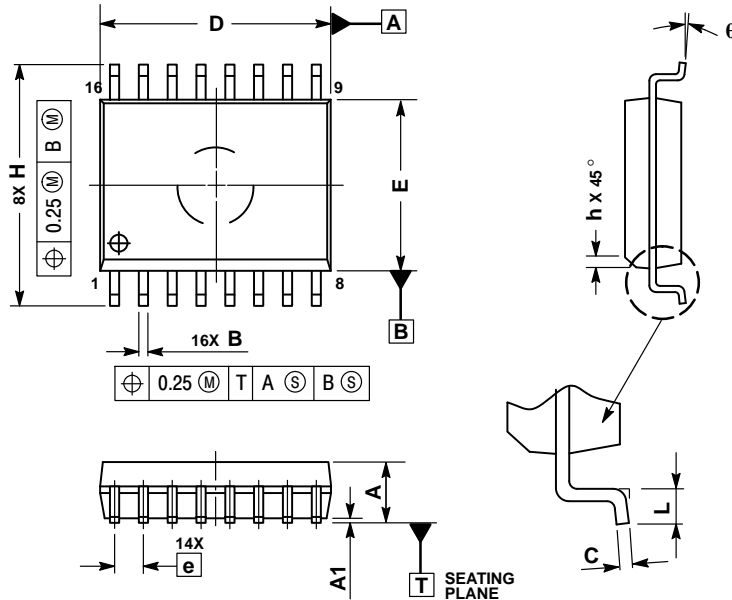
Frequencies shown in parenthesis are given as an example

Figure 4. Frequency Synthesizer with MC14568B and MC14569B Using a Mixer (Channel Spacing 10 kHz)

MC14569B

PACKAGE DIMENSIONS

SOIC-16 WB
CASE 751G-03
ISSUE D

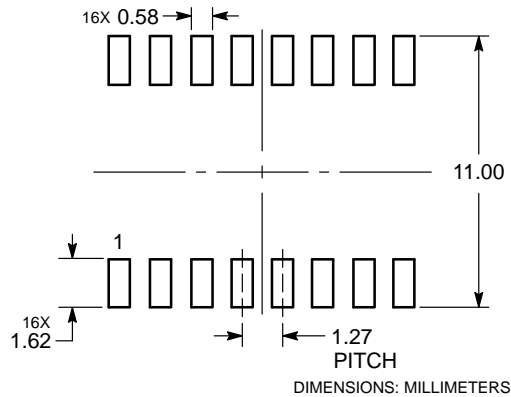



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

MILLIMETERS		
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0°	7°

SOLDERING FOOTPRINT



ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative