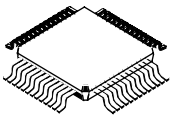
MC14LC5002
MC14LC5003
MC14LC5004

72-Segment / 128-Segment LCD Drivers
CMOS



QFP
FU SUFFIX
CASE 848B
TQFP
FB SUFFIX
CASE 873A

ORDERING INFORMATION

MC14LC5002FB	TQFP
MC14LC5003FU	QFP
MC14LC5004FU	QFP
MCC14LC5003	BARE DIE
MCC14LC5004	BARE DIE
MCC14LC5003Z	AU BUMP DIE
MCC14LC5004Z	AU BUMP DIE

The MC14LC5003/5004 are 128-segment, multiplexed-by-four LCD Drivers. The MC14LC5002 is the same as MC14LC5003 except for 72 segments. The three devices are functionally the same except for their data input protocols. The MC14LC5002/5003 use a serial interface data input protocol. The devices may be interfaced to the MC68HCXX product families using a minimal amount of software (see example). The MC14LC5004 has a IIC interface and has essentially the same protocol, except that the device sends an acknowledge bit back to the transmitter after each eight-bit byte is received. MC14LC5004 also has a “read mode”, whereby data sent to the device may be retrieved via the IIC bus.

The MC14LC5002/5003/5004 drive the liquid crystal displays in a multiplexed-by-four configuration. The devices accept data from a microprocessor or other serial data source to drive one segment per bit. The chip does not have a decoder, allowing for the flexibility of formatting the segment data externally.

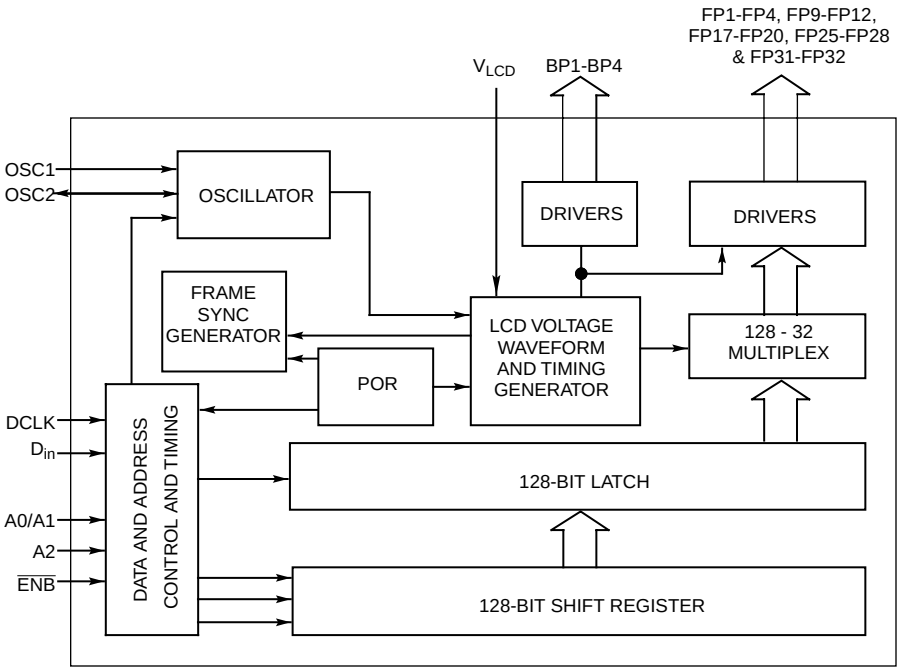
Devices are independently addressable via a two-wire (or three-wire) communication link which can be common with other peripheral devices.

The MC14LC5003/5004 are low cost version of MC145003 and MC145004 without cascading function.

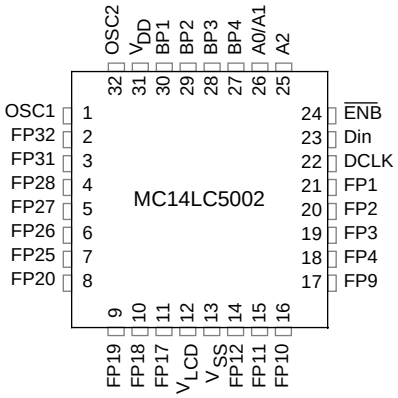
- Drives 72 Segments Per MC14LC5002’s Package
- Drives 128 Segments Per MC14LC5003/5004’s Package
- May Be Used with the Following LCDs: Segmented Alphanumeric, Bar Graph, Dot Matrix, Custom
- Quiescent Supply Current: 30 μA @ 2.7 V V_{DD}
- Operating Voltage Range: 2.7 to 5.5 V
- Operating Temperature Range: -40 to 85°C
- Separate Access to LCD Drive Section’s Supply Voltage to Allow for Temperature Compensation
- See Application Notes AN1066 and AN442

REV 7
02/98

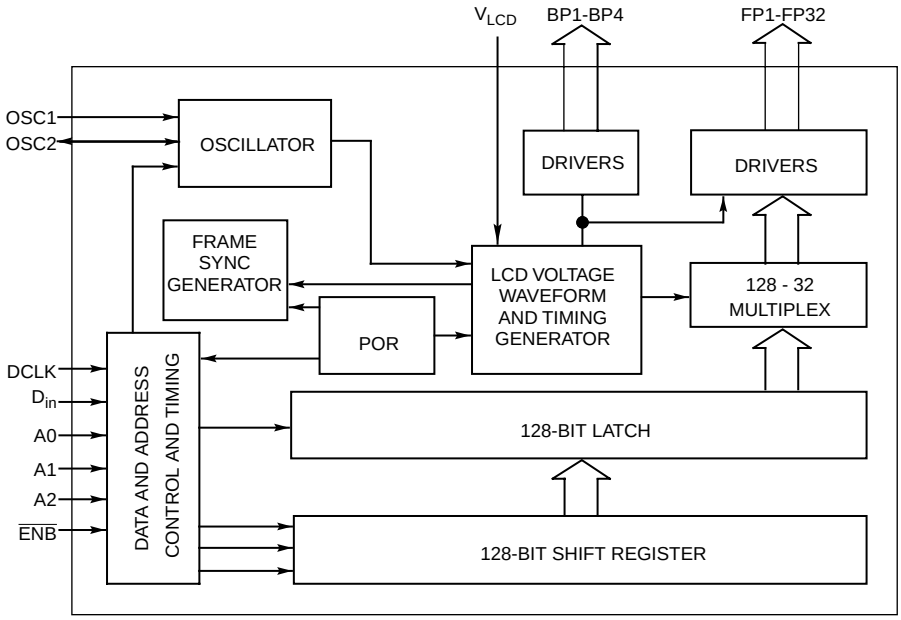
MC14LC5002 BLOCK DIAGRAM



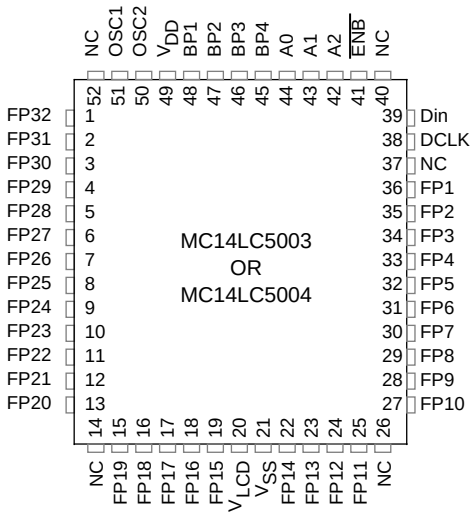
MC14LC5002 PIN ASSIGNMENT



MC14LC5003/MC14LC5004 BLOCK DIAGRAM



MC14LC5003/MC14LC5004 PIN ASSIGNMENT



NC=NO CONNECTION

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	- 0.5 to + 6.5	V
V_{in}	Input Voltage, D_{in}, and Data Clock	- 0.5 to + 15	V
$V_{in\ osc}$	Input Voltage, OSC_{in} of Master	- 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
T_A	Operating Temperature Range	- 40 to + 85	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A= 25°C)

Characteristic	Symbol	V_{DD} V	V_{LCD} V	Min	Typical	Max	Unit
Output Drive Current — Frontplanes							µA
V_O = 0.15 V	I_{FH}	5	2.7	260	—	—	
	I_{FL}	5	2.7	260	—	—	
V_O = 2.65 V	I_{FH}	5	2.7	-240	—	—	
	I_{FL}	5	2.7	-240	—	—	
V_O = 1.72 V	I_{FH}	5	2.7	-40	—	—	
	I_{FL}	5	2.7	—	—	-1.5	
V_O = 1.08 V	I_{FH}	5	2.7	40	—	—	
	I_{FL}	5	2.7	—	—	2	
V_O = 0.15 V	I_{FH}	5	5.5	600	—	—	
	I_{FL}	5	5.5	600	—	—	
V_O = 5.35 V	I_{FH}	5	5.5	-520	—	—	
	I_{FL}	5	5.5	-520	—	—	
V_O = 3.52 V	I_{FH}	5	5.5	-35	—	—	
	I_{FL}	5	5.5	—	—	-1.5	
V_O = 1.98 V	I_{FH}	5	5.5	55	—	—	
	I_{FL}	5	5.5	—	—	1	
Supply Standby Currents (No Clock)							µA
I_{DD} = Standby @ I_{out} = 0 µA	I_{DDS}	2.7	—	—	—	30	
I_{LCD} = Standby @ I_{out} = 0 µA	I_{LCDS}	—	2.7	—	—	800	
I_{DD} = Standby @ I_{out} = 0 µA	I_{DDS}	5.5	—	—	—	50	
I_{LCD} = Standby @ I_{out} = 0 µA	I_{LCDS}	—	5.5	—	—	1500	
Supply Currents (f_{OSC}) = 110 kHz							µA
I_{DD} = Quiescent @ I_{out} = 0 µA, no loading	I_{DDQ}	2.7	—	—	30	—	
I_{DD} = Quiescent @ loading = 270pF	I_{DDQ}	2.7	—	—	—	70	
I_{DD} = Quiescent @ I_{out} = 0 µA, no loading	I_{DDQ}	5.5	—	—	170	—	
I_{DD} = Quiescent @ loading = 270pF	I_{DDQ}	5.5	—	—	—	400	
I_{LCD} = Quiescent @ I_{out} = 0 µA, no loading	I_{LCDQ}	—	2.7	—	—	40	
I_{LCD} = Quiescent @ I_{out} = 0 µA, no loading	I_{LCDQ}	—	5.5	—	—	70	
Input Current	I_{in}	—	—	-0.1	—	0.1	µA
Input Capacitance	C_{in}	—	—	—	—	7.5	pF

(continued)

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	V_{DD} V	V_{LCD} V	Min	Typical	Max	Unit
Frequencies							
OSC2 Frequency @ R1; R1 = 200 kΩ	f_{OSC2}	5	5	100	—	150	kHz
BP Frequency @ R1	f_{BP}	5	5	100	—	150	Hz
OSC2 Frequency @ R2; R2 = 996 kΩ	f_{OSC2}	5	5	23	—	33	kHz
Average DC Offset Voltage (BP Relative to FP)	V_{OO}	5	2.8	-50	—	+50	mV
Input Voltage "0" Level	V_{IL}	2.8	5	—	—	0.85	V
	V_{IL}	5.5	5	—	—	1.65	
"1" Level	V_{IH}	2.8	5	2	—	—	
	V_{IH}	5.5	5	3.85	—	—	
Output Drive Current — Backplanes V_O = 2.65 V	I_{BH} *	5	2.8	-240	—	—	µA
	I_{BL}	5	2.8	-240	—	—	
V_O = 0.15 V	I_{BH}	5	2.8	260	—	—	
	I_{BL}	5	2.8	260	—	—	
V_O = 1.08V	I_{BH}	5	2.8	40	—	—	
	I_{BL}	5	2.8	—	—	2	
V_O = 1.72 V	I_{BH}	5	2.8	-40	—	—	
	I_{BL}	5	2.8	—	—	-1	
V_O = 5.35 V	I_{BH}	5	5.5	-520	—	—	
	I_{BL}	5	5.5	-520	—	—	
V_O = 0.15 V	I_{BH}	5	5.5	600	—	—	
	I_{BL}	5	5.5	600	—	—	
V_O = 1.98 V	I_{BH}	5	5.5	55	—	—	
	I_{BL}	5	5.5	—	—	1	
V_O = 3.52 V	I_{BH}	5	5.5	-35	—	—	
	I_{BL}	5	5.5	—	—	-1	
Pulse Width, Data Clock (Figure 1)	t_w	5		100	—	—	ns
		3		100	—	—	
DCLK Rise/Fall Time (Figure 1)	t_r, t_f	5		—	—	120	µs
		3		—	—	120	
Setup Time, D_{in} to DCLK (Figure 2)	t_{su}	5		20	—	—	ns
		3		20	—	—	
Hold Time, D_{in} to DCLK (Figure 2)	t_h	5		40	—	—	ns
		3		60	—	—	
Hold Time for START condition (Figure 2)	t_{start}	5		100	—	—	ns
		3		100	—	—	
Hold Time for STOP condition (Figure 2)	t_{stop}	5		100	—	—	ns
		3		100	—	—	
DCLK Low to $\overline{ENB}$ High (Figure 3)	t_h	5		20	—	—	ns
		3		20	—	—	
$\overline{ENB}$ High to DCLK High (Figure 3)	t_{rec}	5		20	—	—	ns
		3		20	—	—	
$\overline{ENB}$ High Pulse Width (Figure 3)	t_w	5		100	—	—	ns
		3		100	—	—	
$\overline{ENB}$ Low to DCLK High (Figure 3)	t_{su}	5		20	—	—	ns
		3		20	—	—	

NOTE: Timing for Figures 1, 2, and 3 are design estimates only.

* For a time (t = 4/OSC FREQ.) after the backplane waveform changes to a new voltage level, the circuit is maintained in the high-current state to allow the load capacitances to charge quickly. The circuit is then returned to the low-current state until the next voltage change.

SWITCHING WAVEFORMS

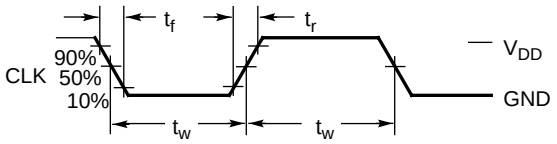


Figure 1.

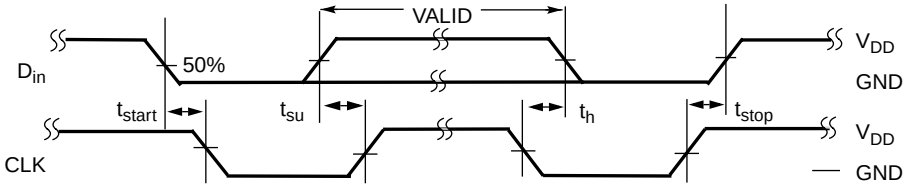


Figure 2.

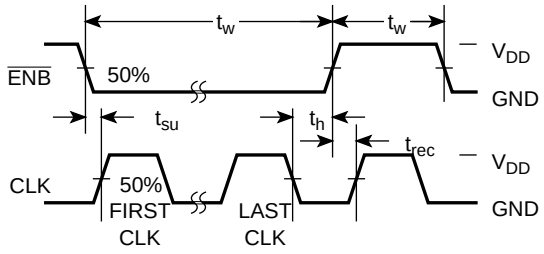


Figure 3.

FUNCTIONAL DESCRIPTION

The MC14LC5002/5003/5004 have essentially two sections which operate asynchronously from each other; the data input and storage section and the LCD drive section. The LCD drive and timing is derived from the oscillator, while the data input and storage is controlled by the Data In (D_{in}), Data Clock (DCLK), Address (A0, A1, A2), and Enable ($\overline{ENB}$) pins.

Data is shifted serially into the 128-bit shift register and arranged into four consecutive blocks of 32 parallel data bits. A time-multiplex of the four backplane drivers is made (each backplane driver becoming active then inactive one after another) and, at the start of each backplane active period, the corresponding block of 32 bits is made available at the frontplane drivers. A high input to a plane driver turns the driver on, and a low input turns the driver off.

Figure 4 shows the sequence of backplanes. Figure 5 shows the possible configurations of the frontplanes relative to the backplanes. When a backplane driver is on, its output switches from V_{LCD} to 0 V, and when it is off, it switches from 1/3 V_{LCD} to 2/3 V_{LCD}. When a frontplane driver is on, its output switches from 0 V to V_{LCD}, and when it is off, it switches from 2/3 V_{LCD} to 1/3 V_{LCD}.

The LCD drive and timing section provides the multiplex signals and backplane driver input signals and formats the frontplane and backplane waveforms.

The address pins are used to uniquely distinguish LCD driver from any other chips on the same bus and to define LCD driver as the "master" in the system. There must be one master in any system.

The enable pin may be used as a third control line in the communication bus. It may be used to define the moment when the data is latched. If not used, then the data is latched after 128 bits of data have been received.

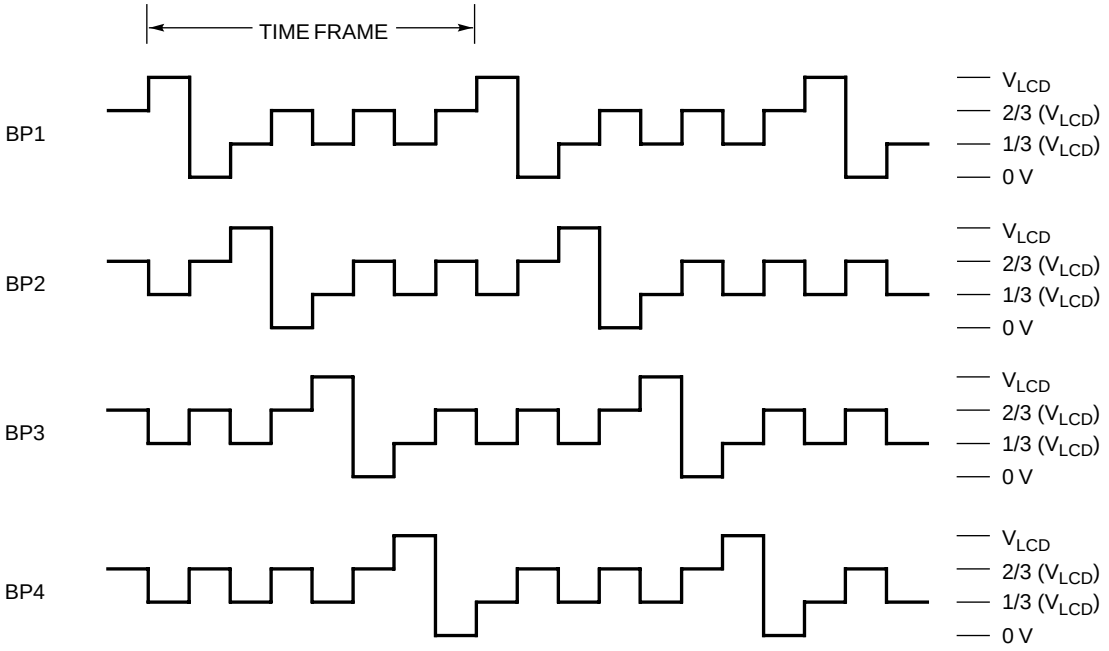


Figure 4. Backplane Sequence

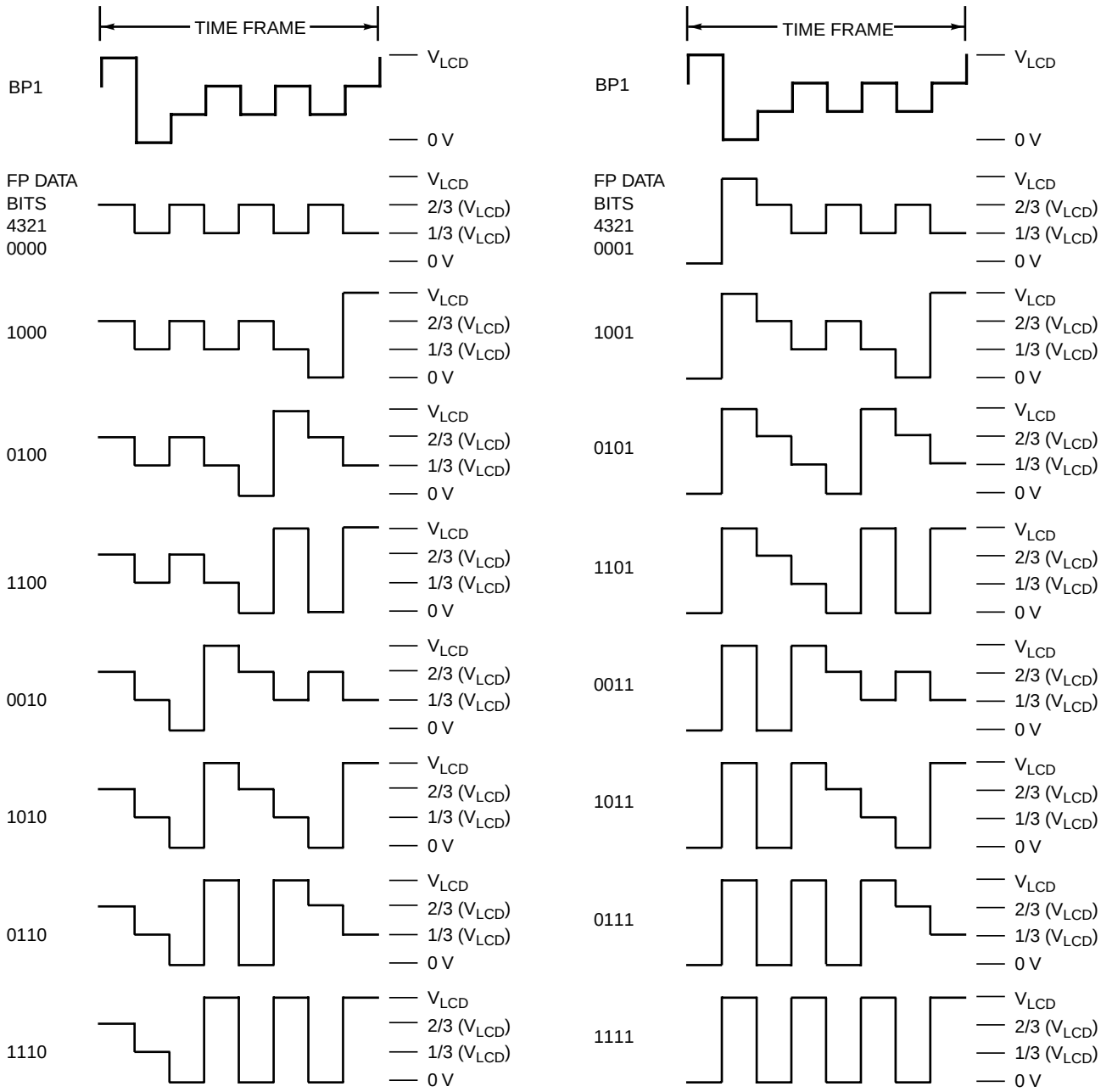


Figure 5. Frontplane Combinations

A0, A1,A2 for MC14LC5003/5004

A0/A1,A2 for MC14LC5002

Address Inputs

The address pins must be tied to V_{DD}. This defines the normal operation mode.

CAUTION

The configuration A0, A1, A2 = 111 must be used. The configuration A0, A1, A2 = 000 is reserved for Motorola's use only. All three address pins should never be tied to 0 V simultaneously.

$\overline{ENB}$
Enable Input

If the $\overline{ENB}$ pin is tied to V_{DD}, the MC14LC5002/5003/5004 will always latch the data after 128 bits have been received. The latched data is multiplexed and fed to the frontplane drivers for display. If external control of this latching function is required, then the $\overline{ENB}$ pin should be held low, followed by one high pulse on $\overline{ENB}$ when data display is required. (This may be useful in a system where MC14LC5002/5003/5004 is permanently addressed and only the last 128 bits of data sent are required to be latched for display). The pulse on the $\overline{ENB}$ pin must occur while DCLK is high.

DCLK, D_{in}
Data Clock and Data Input

Address input and data input controls. See **Data Input Protocol** sections for relevant option.

OSC1, OSC2
Oscillator Pins

To use the on-board oscillator, an external resistor should be connected between OSC1 and OSC2. Optionally, the OSC1 pin may be driven by an externally generated clock signal.

A resistor of 680 kΩ connected between OSC1 and OSC2 pins gives an oscillator frequency of about 30 kHz, giving approximately 30 Hz as seen at the LCD driver outputs. A resistor of 200 kΩ gives about 100 kHz, which results in 100 Hz at the driver outputs. LCD manufacturers recommend an LCD drive frequency of between 30 Hz and 100 Hz. See Figure 6.

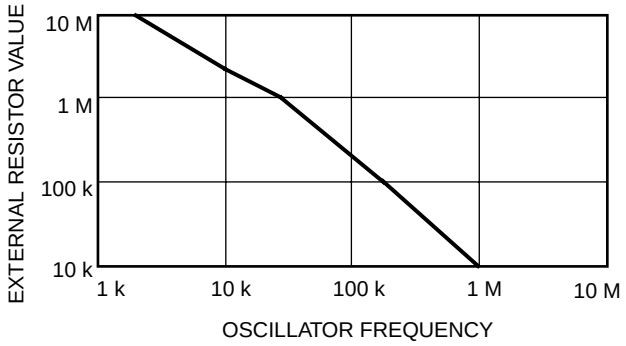


Figure 6. Oscillator Frequency vs. Load Resistance (Approximate)

FP1-FP32
Frontplane Drivers

Frontplane driver outputs.

BP1-BP4
Backplane Drivers

Backplane driver outputs.

V_{LCD}
LCD Driver Supply

Power supply input for LCD drive outputs. May be used to supply a temperature-compensated voltage to the LCD drive section, which can be separate from the logic voltage supply, V_{DD}.

V_{DD}
Positive Power Supply

This pin supplies power to the main processor interface and logic portions of the device. The voltage range is 2.7 to 5.5 V with respect to the V_{SS} pin.

For optimum performance, V_{DD} should be bypassed to V_{SS} using a low inductance capacitor mounted very closely to these pins. Lead length on this capacitor should be minimized.

V_{SS}
Ground

Common ground.

DATA INPUT PROTOCOL

Two-wire communication bus DCLK, D_{in}; three-wire communication bus DCLK, D_{in}, $\overline{ENB}$.

MC14LC5002/5003 — SERIAL INTERFACE DEVICE (FIGURE 7)

Before communication with an MC14LC5002/5003 can begin, a start condition must be set up on the bus by the transmitter. To establish a start condition, the transmitter must pull the data line low for at least one clock-pulse time while the clock line is high. The "idle" state for the clock line and data line is the high state.

After the start condition has been established, an eight-bit address (01111110) should be sent by the transmitter. If the address sent corresponds to the address of the MC14LC5002/5003 then on each successive clock pulse, the addressed device will accept a data bit.

If the $\overline{ENB}$ pin is permanently high, then the addressed MC14LC5002/5003's internal counter latches the data to be displayed after 128 data bits have been received. Otherwise, the control of this latch function may be overridden by holding the $\overline{ENB}$ line low until the new data is required to be displayed, then a high pulse should be sent on the $\overline{ENB}$ line. The high pulse must be sent during DCLK high (clock idle).

To end communication with an MC14LC5002/5003, a stop condition should be set up on the bus (or another start condition may be set up if another communication is desired). To establish a stop condition, the transmitter must pull the data line high for at least one clock-pulse time while the clock line is high. Note that the communication channel to an addressed device may be left open after the 128 data bits have been sent by not setting up a stop or a start condition. In such a case, the 129th rising DCLK edge, which normally would be used to set up the stop or start condition, is ignored by the MC14LC5002/5003 and data continues to be received on the 130th rising DCLK. The latch function continues to work as normal (i.e., data is be latched either after each block of 128 data bits has been received or under external control as required).

At any time during data transmission, the transfer may be interrupted with a stop condition. Data transmission may be resumed with a start condition and resending the address.

MC14LC5004 — IIC DEVICE (FIGURE 8)

Before communication with an MC14LC5004 can begin, a start condition must be set up on the bus by the controller. To establish a start condition, the controller must pull the data line low for at least one clock-pulse time while the clock line is high.

After the start condition has been established, an eight-bit address ($0111111X_0$) should be sent by the controller followed by an extra clock pulse while the data line is left high. In this option, only the seven most significant bits of the address are used to uniquely define devices on the bus, the least significant bit X_0 is used as a read/write control: if the least significant bit is 0, then the controller writes to the LCD driver; if it is 1, then the controller reads from the LCD driver's 128-bit shift register on a first-in first-out basis. If the seven most significant address bits sent correspond to the address of the LCD driver then the addressed LCD driver responds by sending an "acknowledge" bit back to the controller (i.e., the LCD driver pulls the data line low during the extra clock pulse supplied by the controller). If the least significant address bit was 0, then the controller should continue to send data to the LCD driver in blocks of eight bits followed by an extra ninth clock pulse to allow the LCD driver to pull the data line D_{in} low as an acknowledgment. If the least significant address bit was 1, then the LCD driver sends data back to the controller (the clock is supplied by the controller). After each successive group of eight bits sent, the LCD driver leaves the data line high for one pulse.

If the $\overline{ENB}$ pin is permanently high, then the addressed MC14LC5004's internal counter latches the data to be displayed after 128 data bits have been received. Otherwise the control of this latch function may be overridden by holding the $\overline{ENB}$ line low until the new data is required to be displayed, then a high pulse should be sent on the $\overline{ENB}$ line. The high pulse must be sent during DCLK high (clock idle).

To end communication with an MC14LC5004, a stop condition should be set up on the bus (or another start condition may be set up if another communication is desired). To establish a stop condition, the transmitter must pull the data line high for at least one clock-pulse time while the clock line is high. Note that the communication channel to an addressed device may be left open after the 128 data bits have been sent by not setting up a stop or a start condition. In such a case the rising DCLK edge which comes after all 128 data bits have been sent and after the last acknowledge-related clock pulse has been made is ignored; data continues to be received on the following DCLK high. The latch function continues to work as normal (i.e., data is latched either after each block of 128 data bits has been received or under external control as required).

At any time during data transmission, the transfer may be interrupted with a stop condition. Data transmission may be resumed with a start condition and resending the address.

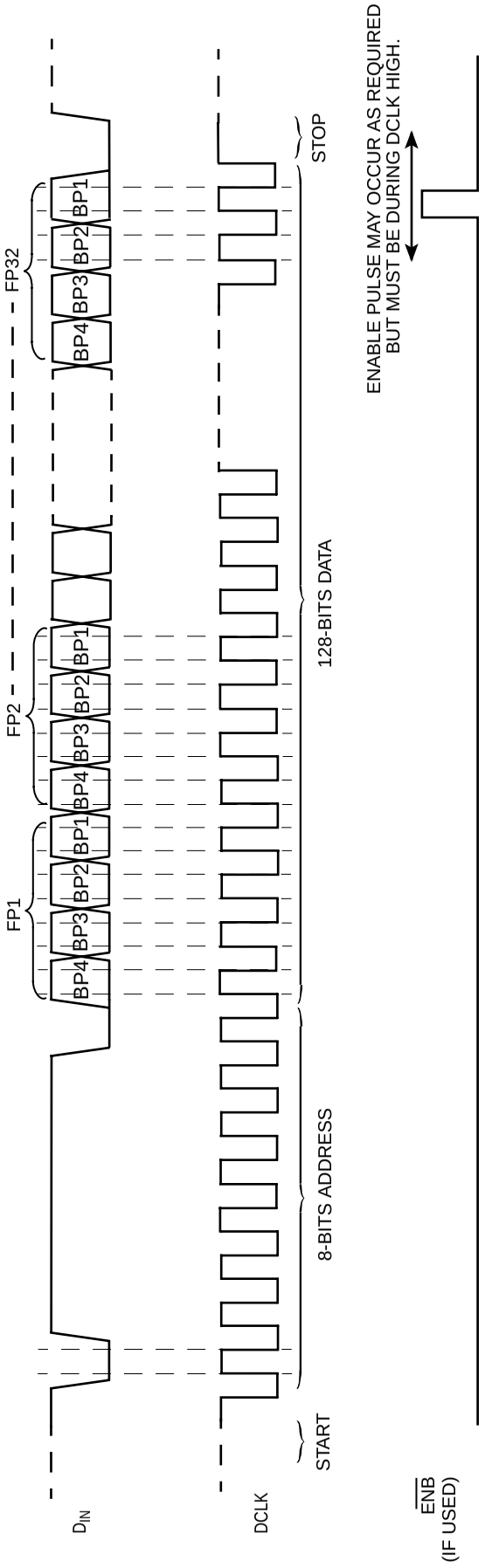


Figure 7a. Data Input—MC14LC5002/5003

Figure 7. MC14LC5002/5003 (SERIAL INTERFACE DEVICE)

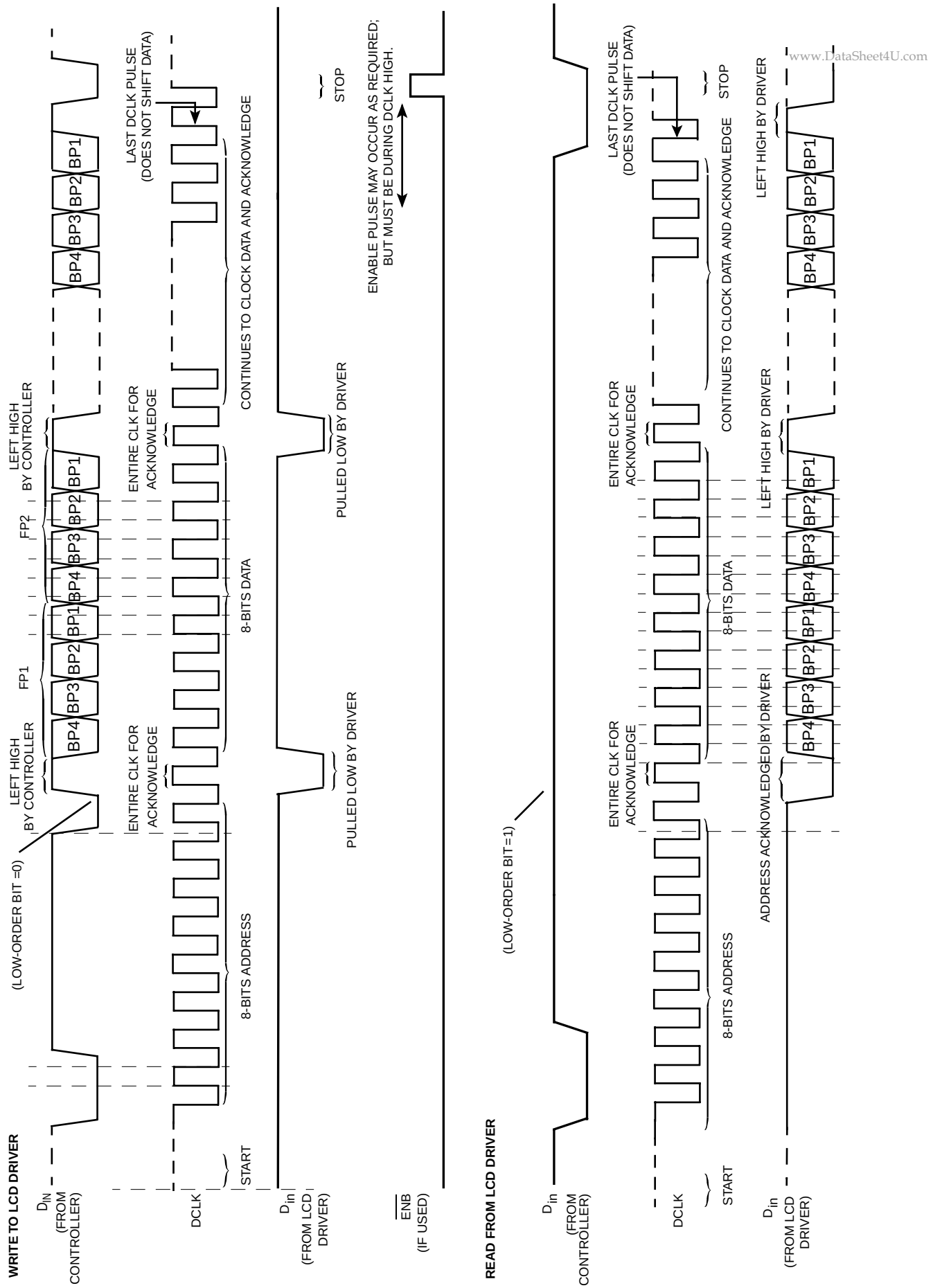


Figure 8 . Data Input MC14LC5004 (IIC Device)

Figure 9 shows an interface example for serial data interface.
Example 1 contains the software to use HC05 with MC14LC5003 in serial data interface.

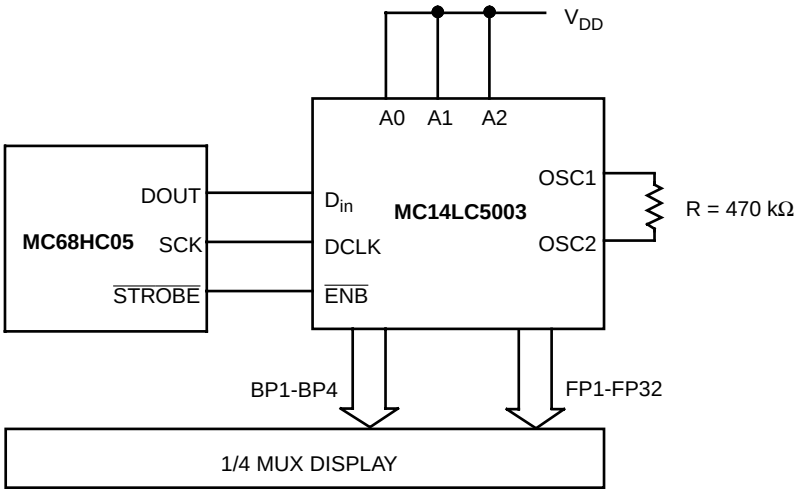


Figure 9. Serial Interface Example Between MC68HC05 and MC14LC5003

```
PORTC   EQU     $02         PORTC
DDRC    EQU     $06         PORTDC
SEN     EQU     $07         ENABLE PIN, PC7
SCL     EQU     $06         CLOCK PIN, PC6
SDA     EQU     $05         DATA PIN, PC5
DOUT    EQU     $FF         OUTPUT DATA

        ORG     $0050

W1      RMB     1
COUNT   RMB     1

        ORG     $1FFE       ADDRESS OF RESET VECTOR OF MC68HC805C4
        FCB     #$01        RESET VECTOR
        FCB     #$00

*** Main Program start at 0100 ***

        ORG     $0100
START   LDA     #DOUT       SET DATA LINE OUTPUT
        STA     DDRC

AGAIN
        LDX     #$00
        BSET    SDA,PORTC   IDLE STATE
        BSET    SCL,PORTC   CLOCK AND DATA ARE HIGH

READY   BSET    SEN,PORTC   EN=1
        LDA     #$11        SET ADDRESS AND 8 CHARACTERS
        STA     W1
        BCLR    SDA,PORTC   START CONDITION, DATA LOW WHILE CLOCK HIGH

LBYTE   CLC
        LDA     #$08
        STA     COUNT           8 BITS TO SHIFT
        LDA     SEND,X          GET A BYTE
        INCX
```

```
LBIT    BCLR    SCL,PORTC   CLOCK LOW
        ROLA
        BCC     DZERO       DATA BIT=0 ?
        BSET    SDA,PORTC   NO, BIT=1 AND DATA HIGH
        JMP     CLKHI
DZERO   BCLR    SDA,PORTC   DATA LOW
CLKHI   BSET    SCL,PORTC       CLOCK HIGH
        DEC     COUNT
        BNE     LBIT
        DEC     W1
        BNE     LBYTE       LAST BYTE ?

STOP    BCLR    SCL,PORTC
        BCLR    SDA,PORTC   STOP CONDITION
        BSET    SCL,PORTC   DATA GOES HIGH WHILE CLOCK HIGH
        BSET    SDA,PORTC
        BCLR    SEN,PORTC   EN=0
        RTS

*** End of Program ***

*** LCD Address and Data ***

SEND
        FCB     $7E                                         LCD DRIVER ADDRESS
        FCB     $FF, $FF, $FF, $FF, $FF, $FF, $FF, $FF      DATA TO SENT
        FCB     $FF, $FF, $FF, $FF, $FF, $FF, $FF, $FF
        RTS
```


Example 1. Serial Data Interface Method

Figure 10 shows an interface example for IIC interface.

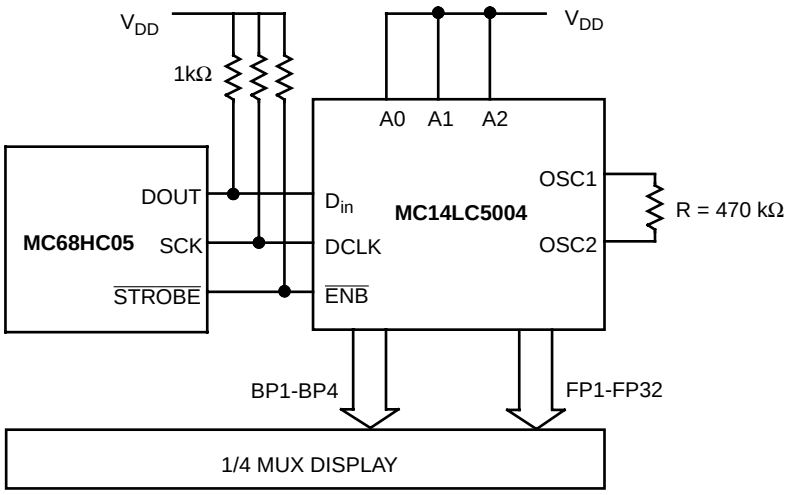
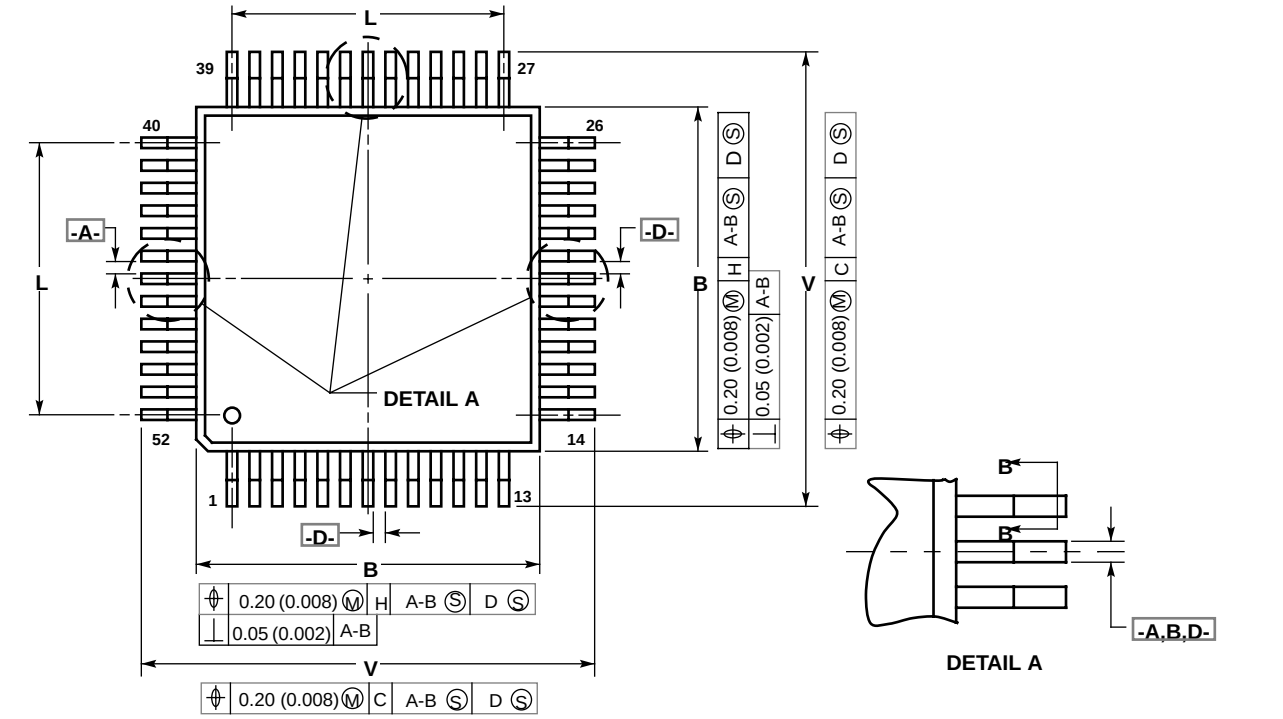


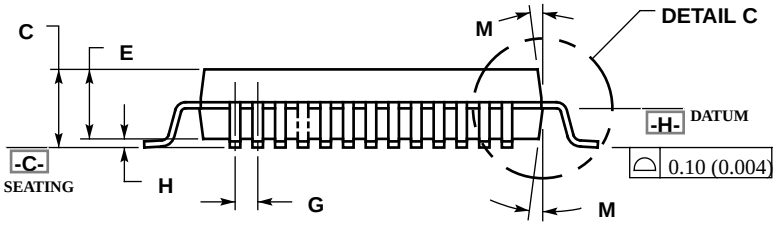
Figure 10. IIC Interface Example Between MC68HC05 and MC14LC5004

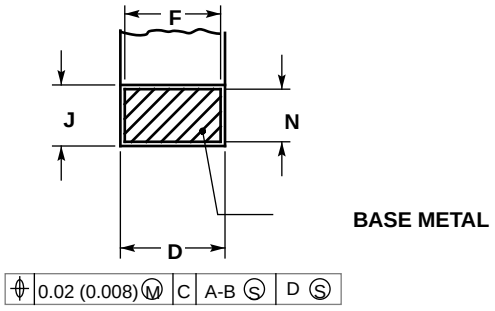
PACKAGE DIMENSIONS

QFP
FU SUFFIX
CASE 848B-02

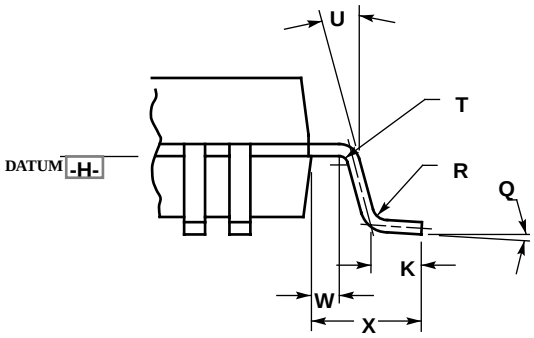


DETAIL A





SECTION B-B



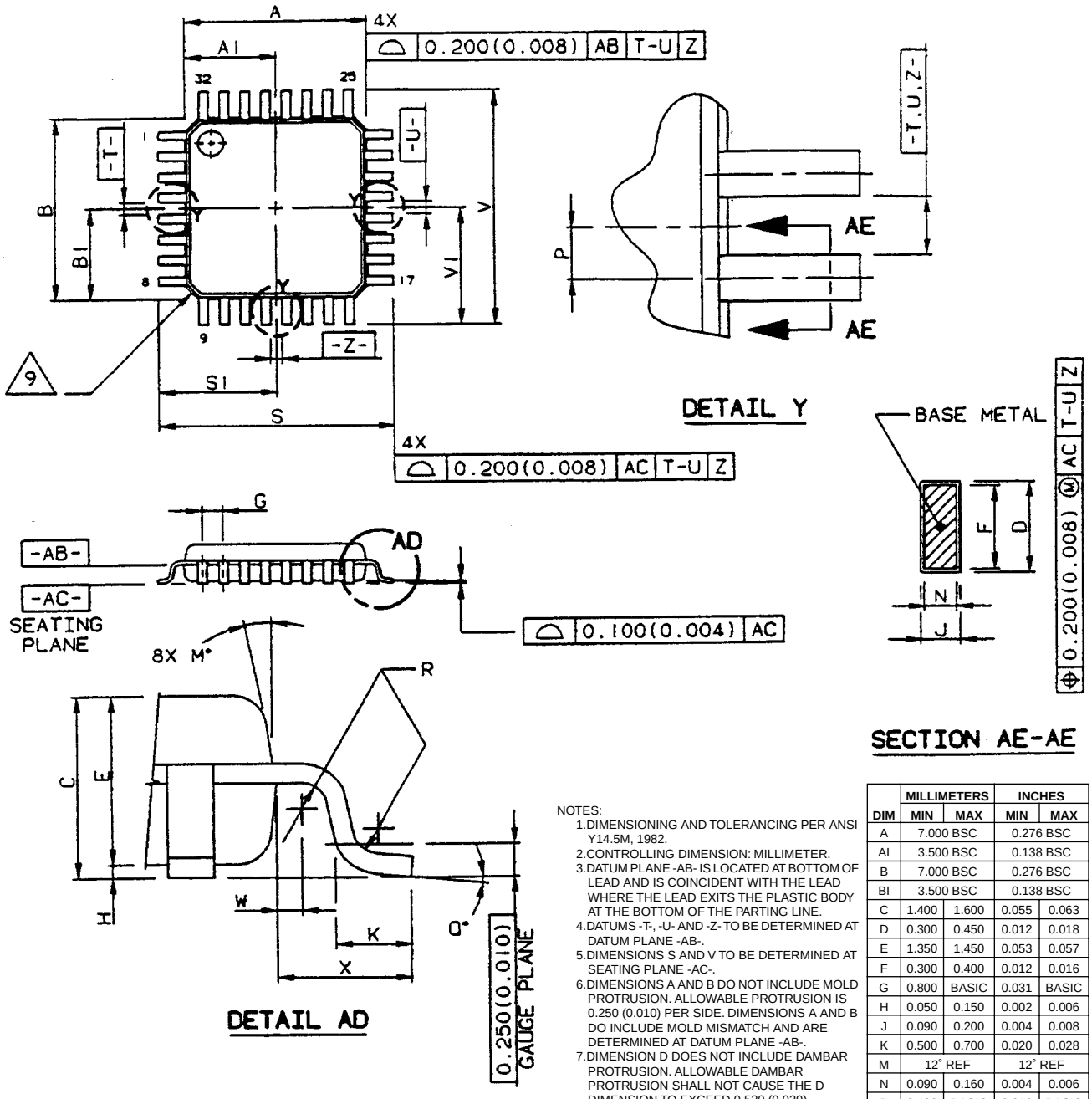
DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.22	0.38	0.009	0.015
E	2.00	2.10	0.079	0.083
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	--	0.25	--	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	7.80 REF		0.307 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	--	0.005	--
U	0°	--	0°	--
V	12.95	13.45	0.510	0.530
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.063 REF	

PACKAGE DIMENSIONS

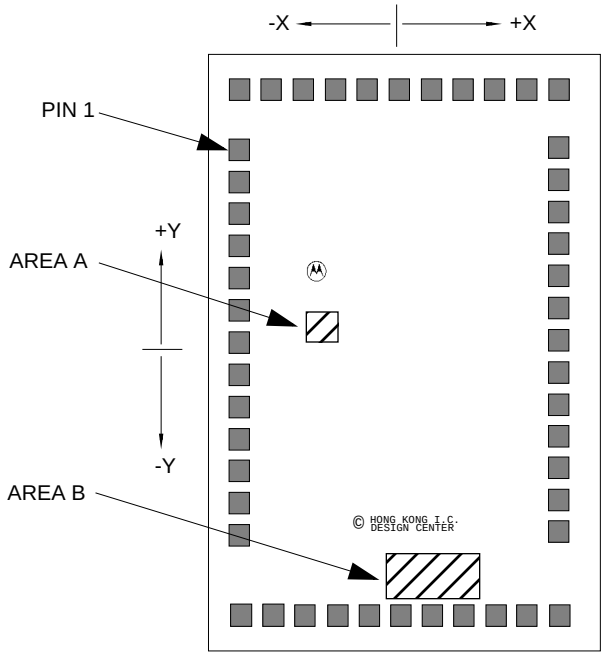
TQFP
FB SUFFIX
CASE 873A-02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -T-, -U- AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
AI	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
BI	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800	BASIC	0.031	BASIC
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400	BASIC	0.016	BASIC
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
SI	4.500 BSC		0.014 BSC	
V	9.000 BSC		0.354 BSC	
VI	4.500 BSC		0.014 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

BOND PAD LAYOUT



For MCC14LC5003 / MCC14LC5004 BARE DIE & MCC14LC5003Z / MCC14LC5004Z AU BUMP DIE :

DIE SIZE : 1981.2 x 3022.6 μm^2

(78 x 119 mil^2, 1 mil ~ 25.4µm)

AU BUMP SIZE : 70 x 70 μm^2

RESERVED AREA :

AREA	COORDINATES	
	X	Y
A	-445	193
	-445	45
	-300	45
	-300	193
B	-74	-910
	-74	-1100
	368	-1100
	368	-910

Dimensions in µm

Note :

1. Reserved area contains dummy bumps for IC bumping process alignment and IC identifications.
2. No conductive tracks should be laid underneath reserved area to avoid short circuit.
3. Reserved area applies to Au bump die only. It does not apply to bare die.

Die Pad Coordinates

Die Pad No.	Pin Name	Coordinates	
		X	Y
1	FP32	-736.002	929.199
2	FP31	-736.002	781.999
3	FP30	-736.002	634.799
4	FP29	-736.002	487.599
5	FP28	-736.002	340.399
6	FP27	-736.002	193.199
7	FP26	-736.002	45.999
8	FP25	-736.002	-101.201
9	FP24	-736.002	-248.401
10	FP23	-736.002	-395.601
11	FP22	-736.002	-542.801
12	FP21	-736.002	-690.001
13	FP20	-736.002	-837.201
14	FP19	-736.002	-1205.601
15	FP18	-588.802	-1205.601
16	FP17	-441.602	-1205.601
17	FP16	-294.402	-1205.601
18	FP15	-147.202	-1205.601
19	V_{LCD}	0.000	-1205.600
20	V_{SS}	147.200	-1205.600
21	FP14	294.398	-1205.601
22	FP13	441.598	-1205.601
23	FP12	588.798	-1205.601
24	FP11	735.998	-1205.601

Die Pad No.	Pin Name	Coordinates	
		X	Y
25	FP10	735.998	-837.201
26	FP9	735.998	-690.001
27	FP8	735.998	-542.801
28	FP7	735.998	-395.601
29	FP6	735.998	-248.401
30	FP5	735.998	-101.201
31	FP4	735.998	45.999
32	FP3	735.998	193.199
33	FP2	735.998	340.399
34	FP1	735.998	487.599
35	NC	736.000	634.800
36	DCLK	736.000	782.000
37	D_{IN}	736.000	929.200
38	$\overline{ENB}$	736.000	1205.600
39	A2	588.800	1205.600
40	A1	441.600	1205.600
41	A0	294.400	1205.600
42	BP4	147.198	1205.599
43	BP3	-0.002	1205.599
44	BP2	-147.202	1205.599
45	BP1	-294.402	1205.599
46	V_{DD}	-441.600	1205.600
47	OSC2	-588.800	1205.600
48	OSC1	-736.000	1205.600

Dimensions in µm