ORDERING INFORMATION

Device	Temperature Range	Package
MC1552G	−55°C to +125°C	Metal Can
MC1553G	−55°C to +125°C	Metal Can

MC1552G
MC1553G

HIGH FREQUENCY VIDEO AMPLIFIER

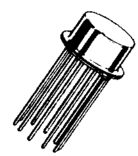
SILICON MONOLITHIC INTEGRATED CIRCUIT

VIDEO AMPLIFIERS

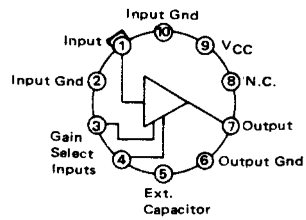
These devices consist of a three-stage, direct-coupled, common-emitter cascade incorporating series feedback to achieve stable voltage gain, low distortion, and wide bandwidth. They employ a temperature-compensated dc feedback loop to stabilize the operating point and a current-biased emitter follower output and are intended for use as either wide-band linear amplifiers or as fast rise pulse amplifiers.

- High Gain – 34 dB ± 1 dB (MC1552)
  52 dB ± 1 dB (MC1553)
- Wide Bandwidth – 40 MHz (MC1552)
  35 MHz (MC1553)
- Low Distortion – 0.2% at 200 kHz
- Low Temperature Drift – ±0.002 dB/°C

CASE 603B
METAL PACKAGE



PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 9	V_{CC}	9.0	Vdc
Input Differential Voltage, Pin 1 to Pin 2 (R_S = 500 ohms)	V_{ID}	1.0	V(rms)
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6	mW mW/°C
Operating Ambient Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

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REPRESENTATIVE CIRCUIT SCHEMATICS

FIGURE 1 – MC1552 (LOW GAIN)

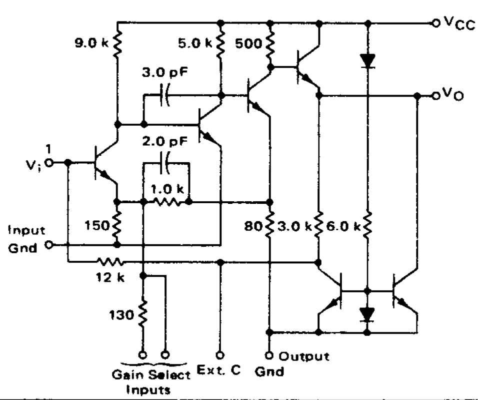
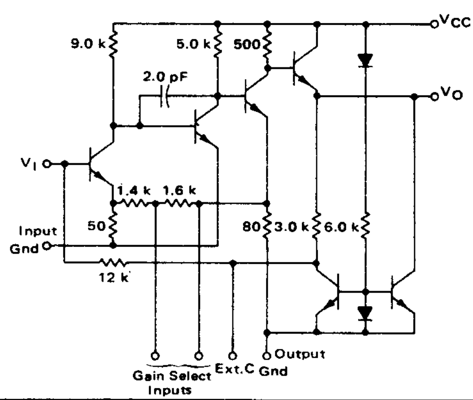


FIGURE 2 – MC1553 (HIGH GAIN)



ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $T_A = 25^oC$, $V_{CC} = 6.0$ V and specification applies for all Gain Selection options.

Characteristic	Test Figure	Symbol	MC1552G			MC1553G			Unit
			Min	Typ	Max	Min	Typ	Max	
Voltage Gain	3	A_V							V/V
(Gain Option = 50)			44	50	56	–	–	–	
(Gain Option = 100)			87	100	113	–	–	–	
(Gain Option = 200)			–	–	–	175	200	225	
(Gain Option = 400)			–	–	–	350	400	450	
$-55^oC \leq T_A \leq 125^oC$									
(Gain Option = 50)			42	–	58	–	–	–	
(Gain Option = 100)			83	–	117	–	–	–	
(Gain Option = 200)			–	–	–	171	–	230	
(Gain Option = 400)			–	–	–	342	–	461	
Voltage Gain Variation ($-55^oC \leq T_A \leq 125^oC$)	3	ΔA_V	–	±0.2	–	–	±0.2	–	dB
Small-Signal Bandwidth	3,6	BW							MHz
(Gain Option = 50)			21	40	–	–	–	–	
(Gain Option = 100)			17	35	–	–	–	–	
(Gain Option = 200)			–	–	–	17	35	–	
(Gain Option = 400)			–	–	–	7.5	15	–	
Input Impedance (f = 100 kHz, R_L = 1.0 kΩ)		z_i	7.0	10	–	7.0	10	–	kΩ
Output Impedance (f = 100 kHz, R_S = 50 Ω)		z_o	–	16	50	–	16	50	Ω
DC Output Voltage	3	V_O	2.5	2.9	3.2	2.5	2.9	3.2	Vdc
($-55^oC \leq T_A \leq 125^oC$)			2.3	–	3.4	2.4	–	3.3	
DC Output Voltage Variation ($-55^oC \leq T_A \leq 125^oC$)	3	ΔV_O	–	±0.05	–	–	±0.05	–	Vdc
Output Voltage Range ($z_L \leq 1.0$ kΩ, C_i = 100 mV rms)	3	V_{OR}	3.6	4.2	–	3.6	4.2	–	V p-p
($-55^oC \leq T_A \leq 125^oC$)						3.4			
Power Supply Current	–	I_{CC}	–	12.5	20	–	12.5	20	mA
($-55^oC \leq T_A \leq 125^oC$)			–	–	24	–	–	23	
Propagation Delay Time	3,4	t_{PHL}							ns
(Gain Option = 50)			–	8.0	–	–	–	–	
(Gain Option = 100)			–	9.0	–	–	–	–	
(Gain Option = 200)			–	–	–	–	10	–	
(Gain Option = 400)			–	–	–	–	25	–	
Transition (Rise) Time	3,4	t_{THL}							ns
(Gain Option = 50)			–	9.0	16	–	–	–	
(Gain Option = 100)			–	12	20	–	–	–	
(Gain Option = 200)			–	–	–	–	11	20	
(Gain Option = 400)			–	–	–	–	30	45	
Overshoot	3,4	$100\ V_{OS}/V_P$	–	5.0	–	–	5.0	–	%
Noise Figure (R_S = 400 Ω, f_o = 30 MHz,BW = 3.0 MHz) (See Figure 14)	–	NF	–	3.0	–	–	3.0	–	dB
Total Harmonic Distortion (V_o = 2.0 V p-p, f = 200 kHz, R_L = 1.0 kΩ)	–	THD	–	0.2	–	–	0.2	–	%

NOTES

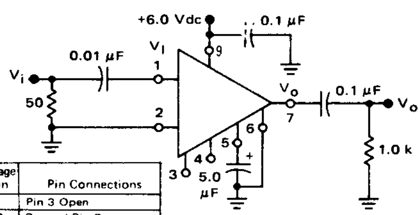
1. Ground Pin 6 as close to package as possible to minimize overshoot. Best results are usually obtained by directly grounding the package.
2. If large input and output coupling capacitors are used, place a shield between them to avoid input-output coupling.
3. A high-frequency capacitor must always be used to by-pass the power supply. This capacitor should be as close to the circuit as possible.
4. Voltage gain can be adjusted to any value between 50 and 3000 by connecting an external resistor from Pin 4 to ground on MC1552, or from Pin 3 to ground on MC1553, as shown in Figure 8. Under these conditions, the following equations must be used to determine C1 and C2 rather than the circuits shown in Figure 5.

Fig. 5b $C1 = \frac{1}{2\pi f_c (1.7 \times 10^4)}$ Farads; $C2 = 8\,C1(V_o/V_i)$ Farads

Fig. 5c $C1 = \frac{V_o/V_i}{2\pi f_c (1.5 \times 10^4)}$ Farads

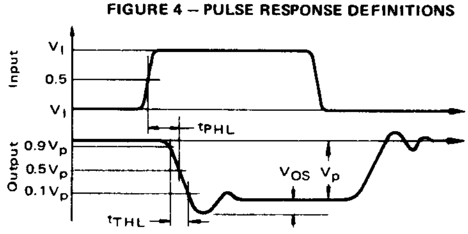
Fig. 5d $C2 = \frac{V_o/V_i}{2\pi f_c (3 \times 10^3)}$ Farads

FIGURE 3 – TEST CIRCUIT



Type	Voltage Gain	Pin Connections
MC1552	50	Pin 3 Open
	100	Ground Pin 3
MC1553	200	Connect Pin 3 to Pin 4
	400	Pins 3 and 4 Open

FIGURE 4 – PULSE RESPONSE DEFINITIONS



TYPICAL CHARACTERISTICS

$T_A = +25^oC$

FIGURE 5a – FREQUENCY RESPONSE

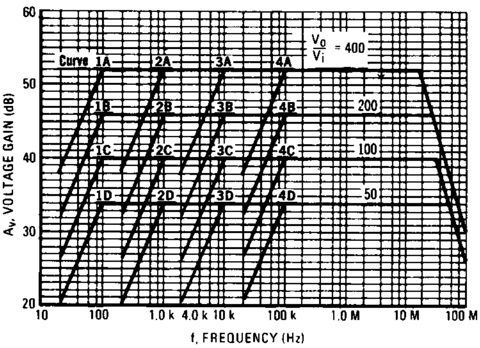
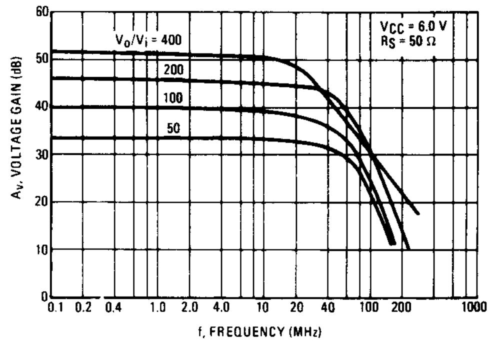
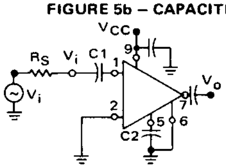


FIGURE 6 – VOLTAGE GAIN versus FREQUENCY



TEST CIRCUITS FOR FREQUENCY RESPONSE

FIGURE 5b – CAPACITIVE COUPLED INPUT ($R_s < 5\ k\Omega$)



Curve No.	C1 (μF)	C2 (μF)
1A	0.1	250
1B	0.1	150
1C	0.1	70
1D	0.1	40

Curve No.	C1 (μF)	C2 (μF)
2A	0.01	30
2B	0.01	18
2C	0.01	8.0
2D	0.01	4.0
	(pF)	
3A	1000	3.0
3B	1000	1.8
3C	1000	0.8
3D	1000	0.4
4A	100	0.3
4B	100	0.18
4C	100	0.08
4D	100	0.04

FIGURE 7 – MAXIMUM NEGATIVE SWING SLEW RATE versus LOAD CAPACITANCE

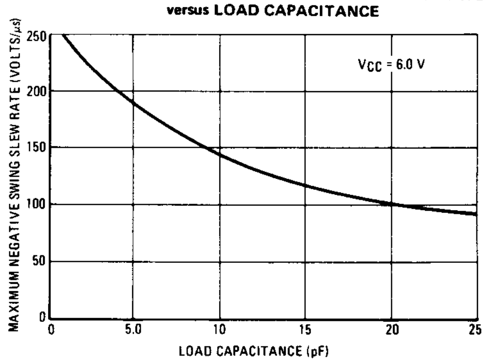
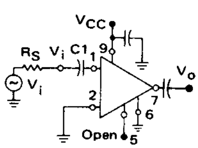


FIGURE 5c – CAPACITIVE COUPLED INPUT ($R_s < 500\ \Omega$)



Curve No.	C1 (μF)
1A	20
1B	10
1C	7.0
1D	3.0
2A	3.0
2B	1.0
2C	0.8
2D	0.5

Curve No.	C1 (μF)
3A	0.4
3B	0.2
3C	0.1
3D	0.06
4A	0.04
4B	0.02
4C	0.01
4D	0.007

FIGURE 8 – VOLTAGE GAIN ADJUSTMENT BY USE OF EXTERNAL RESISTOR

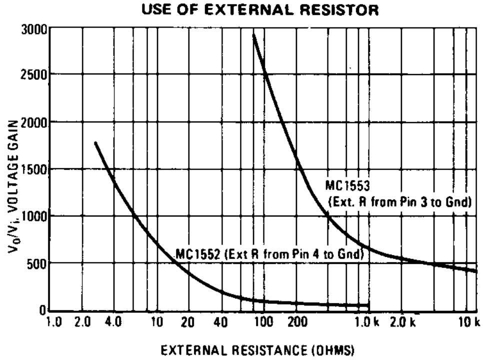
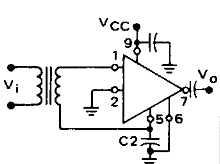


FIGURE 5d – TRANSFORMER COUPLED INPUT



Curve No.	C2 (μF)
1A	200
1B	100
1C	70
1D	30
2A	20
2B	10
2C	7.0
2D	3.0

Curve No.	C1 (μF)
3A	2.0
3B	1.0
3C	0.7
3D	0.3
4A	0.2
4B	0.1
4C	0.07
4D	0.03

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INPUT ADMITTANCE

(V_{CC} = 6.0 Vdc, R_L = 1.0 kΩ, T_A = +25°C)

FIGURE 9 – GAIN = 50

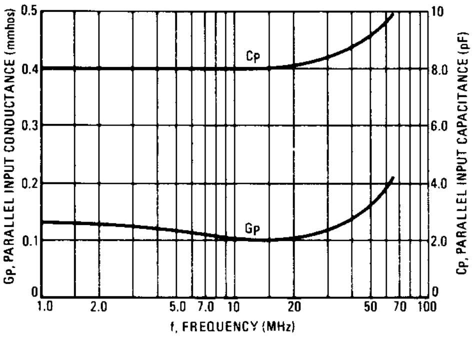

FIGURE 10 – GAIN = 100

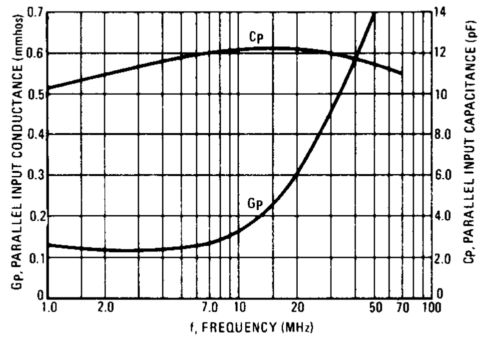

FIGURE 11 – GAIN = 200

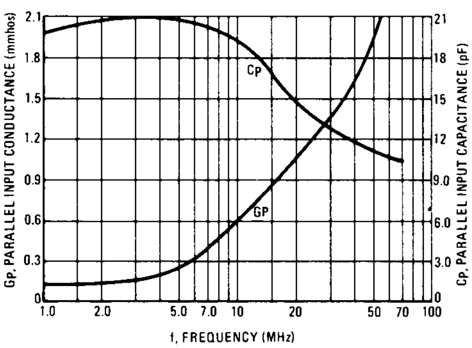

FIGURE 12 – GAIN = 400

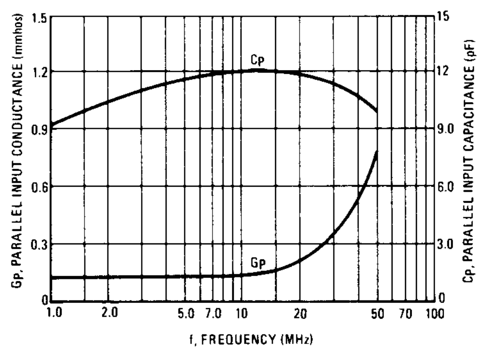

FIGURE 13 – OUTPUT IMPEDANCE versus FREQUENCY

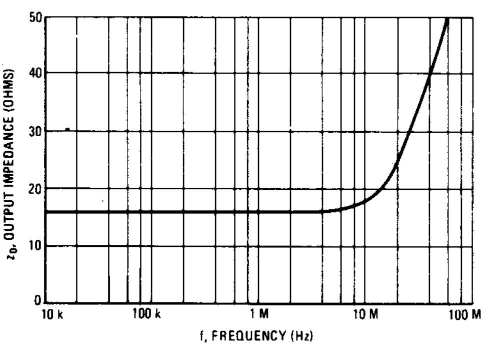

FIGURE 14 – BANDWIDTH versus SOURCE RESISTANCE