Specifications Ver. 1.03

Driver LSI for a color TFT LCD Panel

MC2TA7402

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1. Introduction

The MC2TA7402 is a one-chip controller driver LSI for a TFT liquid crystal display of 262,144 colors, with the integrated DDRAM for graphics data of 176 RGB x 220 dots at maximum, gate drivers, source drivers and power supply circuits.

The MC2TA7402 supports high-speed parallel interfaces with 8-, 9-, 16-, 18-bit buses and a high-speed serial peripheral interface (SPI) to write RAM graphics data at high speed. In addition, the MC2TA7402 has RGB interfaces (VSYNC, HSYNC, DOTCLK, ENABLE, and D17-0) and VSYNC interface for displaying a moving picture.

The MC2TA7402 incorporates step-up circuits for generating voltages for driving a TFT LCD and a voltage follower circuit. The MC2TA7402 also supports a function to display images in 8 color mode and standby mode, allowing low power consumption by software. These features make the MC2TA7402 an ideal LCD driver for medium or small sized portable products having color display such as digital cellular phones or small PDAs, where long battery life is a measure concern.

2. Features

• A controller driver for a liquid crystal TFT display of 176RGB x 220-dot graphics data in 262,144 colors.
• Single chip solution for a TFT LCD module
• System interfaces
  – High-speed interfaces with 8-, 9-, 16-, and 18-bit parallel ports
  – Serial Peripheral Interface (SPI)
• Interfaces for moving picture display
  – 6-, 16-, 18-bit RGB interfaces (VSYNC, HSYNC, DOTCLK, ENABLE, D17-0)
  – VSYNC interface (System interface + VSYNC)
• Window address function for making a rectangular area on the internal DDRAM to write data
  – Facilitates moving picture display at any area on the screen via a moving picture display interface
  – Limits the data rewriting area and reduce data transfers
  – Enables simultaneous display of moving picture and data in the internal DDRAM
• Abundant functions to control color display
  – Display in 262,144 colors
• Line-unit vertical scrolling function
• Low-power architecture
  – Features of low voltage operation:
    IOVCC = 1.6 to 3.3 V (interface I/O power supply)
    VCI= 2.5 to 3.3 V (analog power supply)
    DDVDH = 4.5 to 5.5 V (liquid-crystal drive voltage)
  – Power-saving function (sleep mode / standby mode, etc.)
  – Partial display function for selectively driving an LCD, enabling two displays at arbitrarily set positions
  – A voltage follower circuit for generating LCD driving voltages with a small direct current through bleeder resistors
• Incorporates step-up circuits for stepping up a liquid crystal drive voltage up to 6 times (x 6)
• 87,120-byte internal DDRAM
• Incorporates a 528-channel source driver, and a 220-channel gate driver
• The 1-line liquid crystal AC drive function
• Internal oscillator and hardware reset
• Reversible source driver shift direction
• For Cst structure only (Common VCOM formula)

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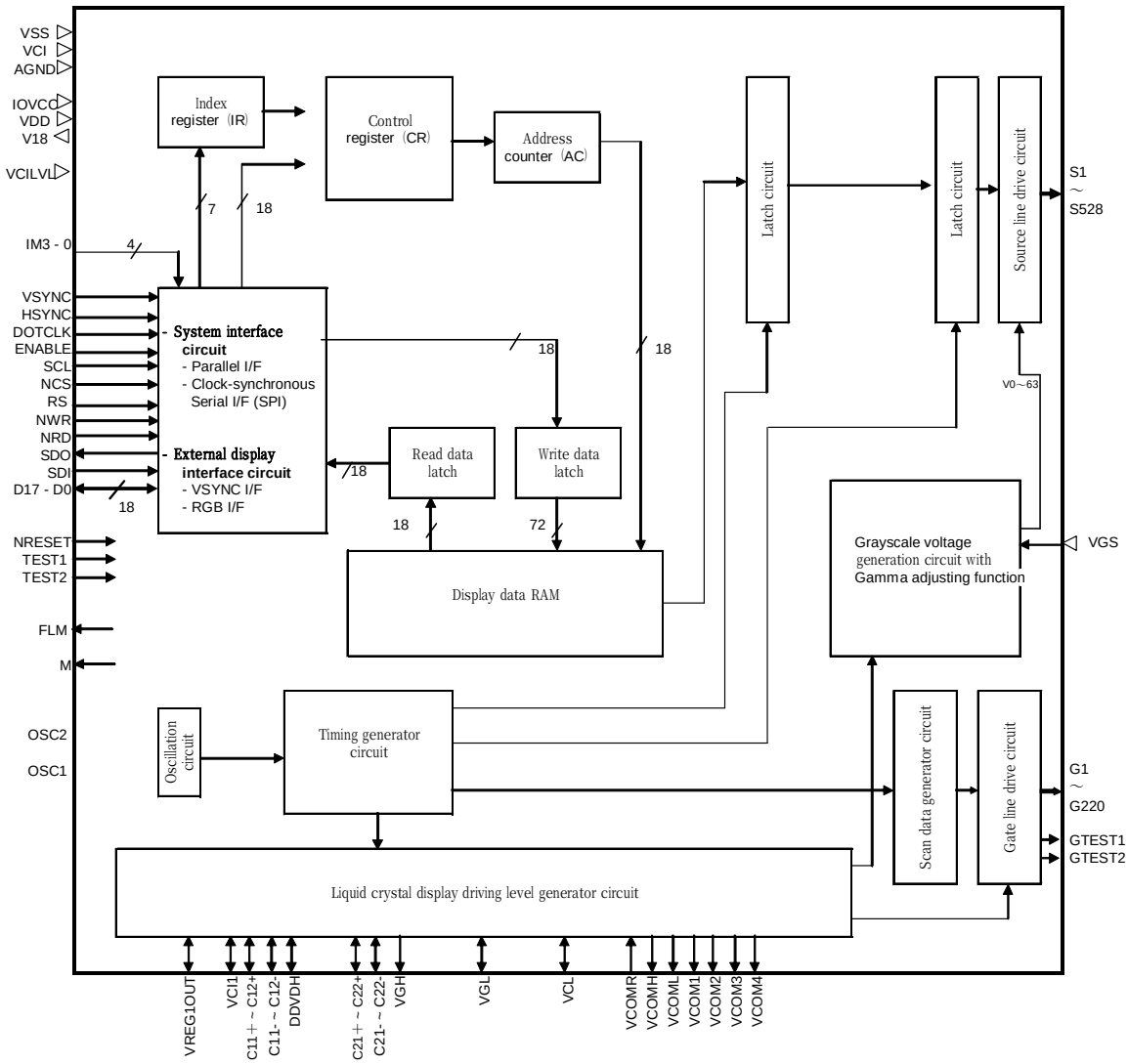
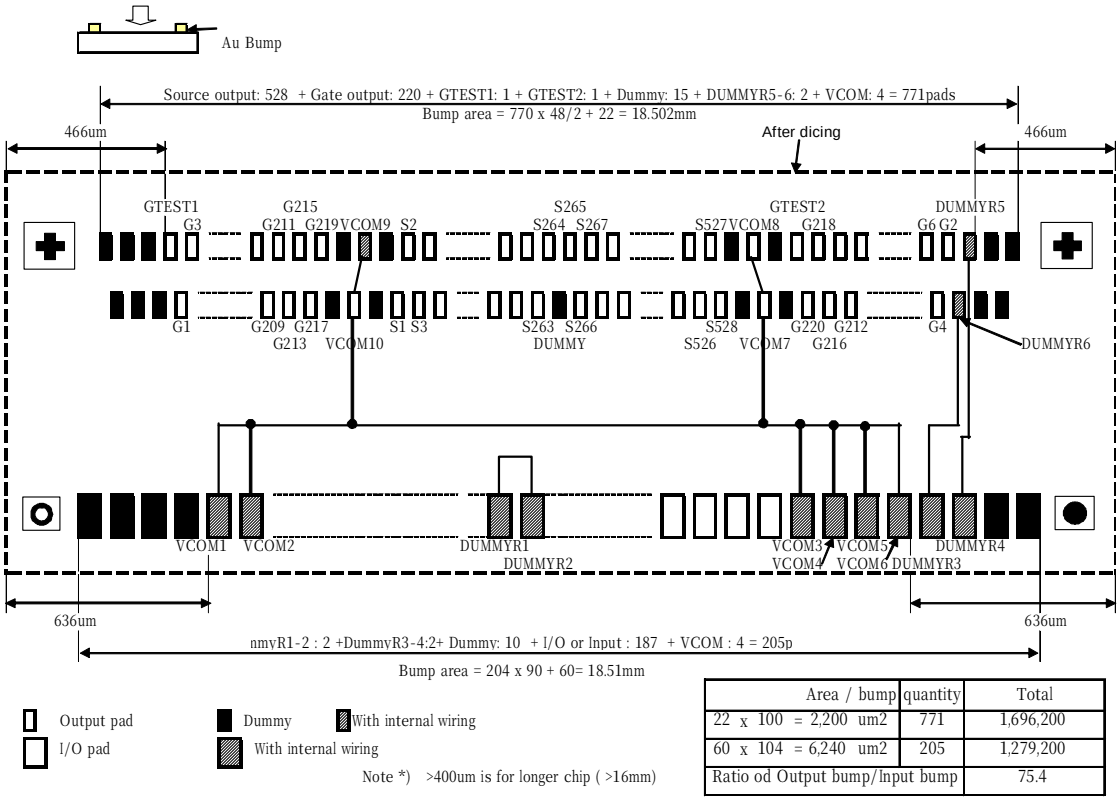
4. Block Diagram



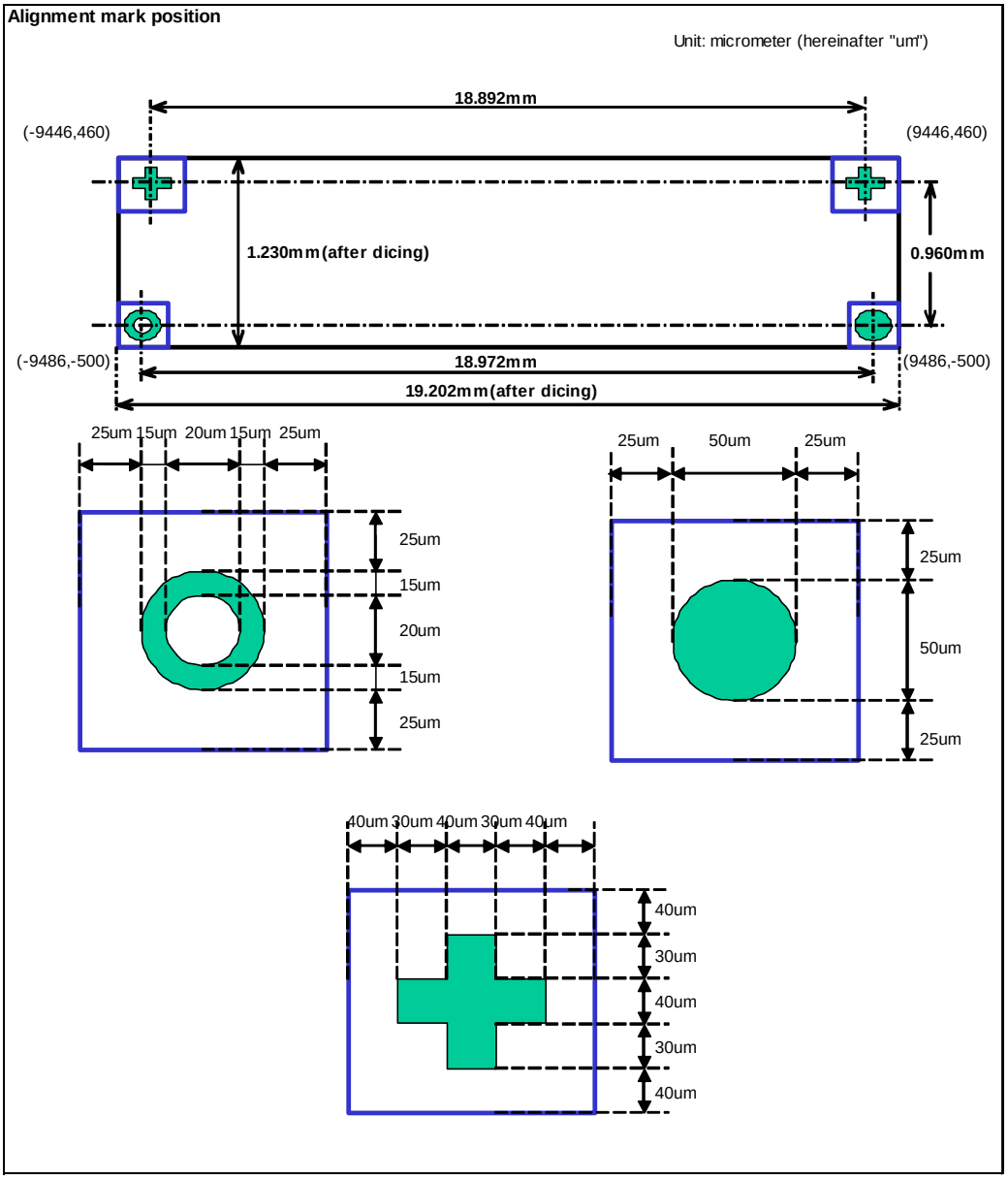
5. Bump Layout

5.1. Bump Placement



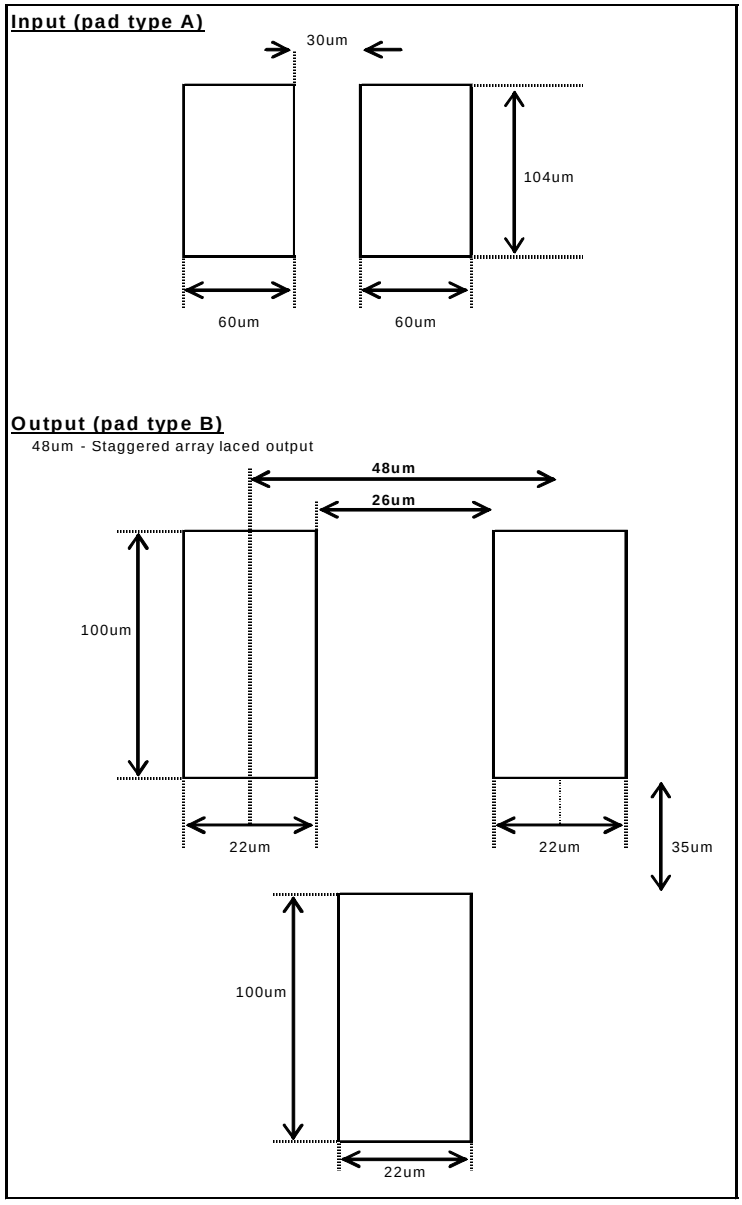
	Area / bump	quantity	Total
22 x 100 = 2,200 um2		771	1,696,200
60 x 104 = 6,240 um2		205	1,279,200
Ratio od Output bump/Input bump			75.4

5.2. Alignment Mark



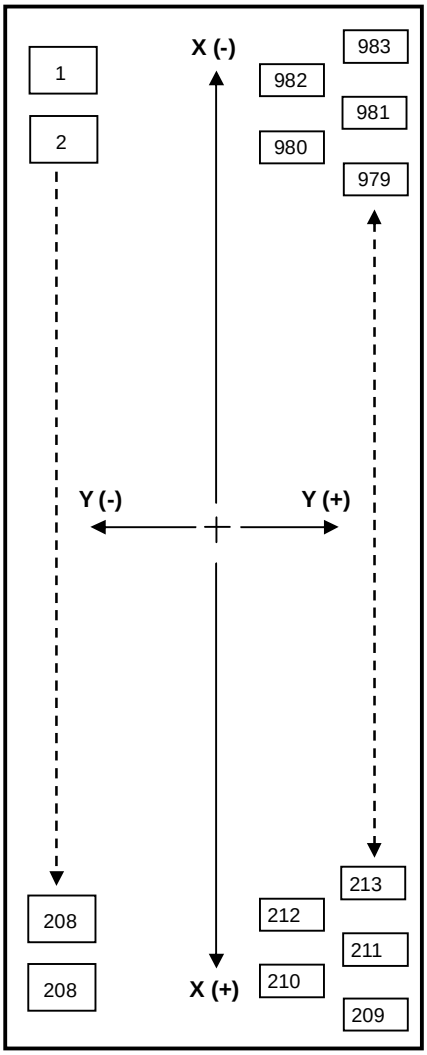
5.3. Bump Size

Wafer thickness	A type : 400um
	B type : 300um Wafer thickness is ordinary A type. If you need B type, please inform to MC sales of charge..
Bump Height	typical 15um



5.4. Chip Size

Chip Size(after dicing):19.202mm×1.230mm



Note) The chip origin is not the center of the vertical direction.

5.5. Bump Coordinates

Bump No.	Bump Name	X(um)	Y(um)	Pad type
1	DUMMY1	-9315	-493	A
2	DUMMY2	-9225	-493	A
3	DUMMY3	-9135	-493	A
4	DUMMY4	-9045	-493	A
5	VCOM1	-8955	-493	A
6	VCOM2	-8865	-493	A
7	DUMMY5	-8775	-493	A
8	VGH	-8685	-493	A
9	VGH	-8595	-493	A
10	DUMMY6	-8505	-493	A
11	C22P	-8415	-493	A
12	C22P	-8325	-493	A
13	C22M	-8235	-493	A
14	C22M	-8145	-493	A
15	C21P	-8055	-493	A
16	C21P	-7965	-493	A
17	C21M	-7875	-493	A
18	C21M	-7785	-493	A
19	C12P	-7695	-493	A
20	C12P	-7605	-493	A
21	C12P	-7515	-493	A
22	C12P	-7425	-493	A
23	C12M	-7335	-493	A
24	C12M	-7245	-493	A
25	C12M	-7155	-493	A
26	C12M	-7065	-493	A
27	DUMMY7	-6975	-493	A
28	VCL	-6885	-493	A
29	VCL	-6795	-493	A
30	VCL	-6705	-493	A
31	VCL	-6615	-493	A
32	VGL	-6525	-493	A
33	VGL	-6435	-493	A
34	VGL	-6345	-493	A
35	VGL	-6255	-493	A
36	VGL	-6165	-493	A
37	VGL	-6075	-493	A
38	VSS	-5985	-493	A
39	IM0	-5895	-493	A
40	IOVCC	-5805	-493	A
41	IM1	-5715	-493	A
42	VSS	-5625	-493	A
43	IM2	-5535	-493	A
44	IOVCC	-5445	-493	A
45	IM3	-5355	-493	A
46	NRESET	-5265	-493	A
47	NRESET	-5175	-493	A
48	VSYNC	-5085	-493	A
49	VSYNC	-4995	-493	A
50	HSYNC	-4905	-493	A
51	HSYNC	-4815	-493	A
52	DOTCLK	-4725	-493	A
53	DOTCLK	-4635	-493	A
54	ENABLE	-4545	-493	A
55	ENABLE	-4455	-493	A
56	D17	-4365	-493	A
57	D17	-4275	-493	A
58	D16	-4185	-493	A
59	D16	-4095	-493	A
60	D15	-4005	-493	A

Bump No.	Bump Name	X(um)	Y(um)	Pad type
61	D15	-3915	-493	A
62	D14	-3825	-493	A
63	D14	-3735	-493	A
64	D13	-3645	-493	A
65	D13	-3555	-493	A
66	D12	-3465	-493	A
67	D12	-3375	-493	A
68	D11	-3285	-493	A
69	D11	-3195	-493	A
70	D10	-3105	-493	A
71	D10	-3015	-493	A
72	D9	-2925	-493	A
73	VSS	-2835	-493	A
74	D8	-2745	-493	A
75	D8	-2655	-493	A
76	D7	-2565	-493	A
77	D7	-2475	-493	A
78	D6	-2385	-493	A
79	D6	-2295	-493	A
80	D5	-2205	-493	A
81	D5	-2115	-493	A
82	D4	-2025	-493	A
83	D4	-1935	-493	A
84	D3	-1845	-493	A
85	D3	-1755	-493	A
86	D2	-1665	-493	A
87	D2	-1575	-493	A
88	D1	-1485	-493	A
89	D1	-1395	-493	A
90	D0	-1305	-493	A
91	D0	-1215	-493	A
92	SDO	-1125	-493	A
93	SDO	-1035	-493	A
94	SDI	-945	-493	A
95	SDI	-855	-493	A
96	NWR	-765	-493	A
97	NWR	-675	-493	A
98	SCL	-585	-493	A
99	SCL	-495	-493	A
100	NRD	-405	-493	A
101	NRD	-315	-493	A
102	RS	-225	-493	A
103	RS	-135	-493	A
104	NCS	-45	-493	A
105	NCS	45	-493	A
106	FLM	135	-493	A
107	FLM	225	-493	A
108	IOVCC	315	-493	A
109	IOVCC	405	-493	A
110	VCI	495	-493	A
111	VCI	585	-493	A
112	VCI	675	-493	A
113	VCI	765	-493	A
114	VCI	855	-493	A
115	VCI	945	-493	A
116	VCILVL	1035	-493	A
117	VCILVL	1125	-493	A
118	VSS	1215	-493	A
119	VSS	1305	-493	A
120	VSS	1395	-493	A

Bump No.	Bump Name	X(um)	Y(um)	Pad type
121	VSS	1485	-493	A
122	VSS	1575	-493	A
123	VSS	1665	-493	A
124	VSS	1755	-493	A
125	VSS	1845	-493	A
126	AGND	1935	-493	A
127	AGND	2025	-493	A
128	AGND	2115	-493	A
129	AGND	2205	-493	A
130	AGND	2295	-493	A
131	AGND	2385	-493	A
132	AGND	2475	-493	A
133	AGND	2565	-493	A
134	VDD	2655	-493	A
135	VDD	2745	-493	A
136	VDD	2835	-493	A
137	VDD	2925	-493	A
138	VDD	3015	-493	A
139	VDD	3105	-493	A
140	VI18	3195	-493	A
141	VI18	3285	-493	A
142	VI18	3375	-493	A
143	VI18	3465	-493	A
144	VSS	3555	-493	A
145	VSS	3645	-493	A
146	TEST1	3735	-493	A
147	DUMMYR1	3825	-493	A
148	DUMMYR2	3915	-493	A
149	TEST2	4005	-493	A
150	VGS	4095	-493	A
151	VGS	4185	-493	A
152	VREG1OUT	4275	-493	A
153	VREG1OUT	4365	-493	A
154	VCI1	4455	-493	A
155	VCI1	4545	-493	A
156	VCI1	4635	-493	A
157	VCI1	4725	-493	A
158	DDVDH	4815	-493	A
159	DDVDH	4905	-493	A
160	DDVDH	4995	-493	A
161	DDVDH	5085	-493	A
162	DDVDH	5175	-493	A
163	DDVDH	5265	-493	A
164	DDVDH	5355	-493	A
165	DDVDH	5445	-493	A
166	DUMMY8	5535	-493	A
167	DUMMY9	5625	-493	A
168	OSC1	5715	-493	A
169	OSC1	5805	-493	A
170	OSC2	5895	-493	A
171	OSC2	5985	-493	A
172	DUMMY10	6075	-493	A
173	DUMMY11	6165	-493	A
174	C11M	6255	-493	A
175	C11M	6345	-493	A
176	C11M	6435	-493	A
177	C11M	6525	-493	A
178	C11M	6615	-493	A
179	C11M	6705	-493	A
180	C11P	6795	-493	A

Bump No.	Bump Name	X(um)	Y(um)	Pad type
181	C11P	6885	-493	A
182	C11P	6975	-493	A
183	C11P	7065	-493	A
184	C11P	7155	-493	A
185	C11P	7245	-493	A
186	DUMMY12	7335	-493	A
187	VREF	7425	-493	A
188	VREF	7515	-493	A
189	VCOMR	7605	-493	A
190	VCOMR	7695	-493	A
191	VCOML	7785	-493	A
192	VCOML	7875	-493	A
193	VCOML	7965	-493	A
194	VCOML	8055	-493	A
195	VCOMH	8145	-493	A
196	VCOMH	8235	-493	A
197	VCOMH	8325	-493	A
198	VCOMH	8415	-493	A
199	M	8505	-493	A
200	M	8595	-493	A
201	VCOM3	8685	-493	A
202	VCOM4	8775	-493	A
203	VCOM5	8865	-493	A
204	VCOM6	8955	-493	A
205	DUMMYR3	9045	-493	A
206	DUMMYR4	9135	-493	A
207	DUMMY13	9225	-493	A
208	DUMMY14	9315	-493	A
209	DUMMY15	9288	495	B
210	DUMMY16	9264	360	B
211	DUMMY17	9240	495	B
212	DUMMY18	9216	360	B
213	DUMMYR5	9192	495	B
214	DUMMYR6	9168	360	B
215	G<2>	9144	495	B
216	G<4>	9120	360	B
217	G<6>	9096	495	B
218	G<8>	9072	360	B
219	G<10>	9048	495	B
220	G<12>	9024	360	B
221	G<14>	9000	495	B
222	G<16>	8976	360	B
223	G<18>	8952	495	B
224	G<20>	8928	360	B
225	G<22>	8904	495	B
226	G<24>	8880	360	B
227	G<26>	8856	495	B
228	G<28>	8832	360	B
229	G<30>	8808	495	B
230	G<32>	8784	360	B
231	G<34>	8760	495	B
232	G<36>	8736	360	B
233	G<38>	8712	495	B
234	G<40>	8688	360	B
235	G<42>	8664	495	B
236	G<44>	8640	360	B
237	G<46>	8616	495	B
238	G<48>	8592	360	B
239	G<50>	8568	495	B
240	G<52>	8544	360	B

Bump No.	Bump Name	X(um)	Y(um)	Pad type
241	G<54>	8520	495	B
242	G<56>	8496	360	B
243	G<58>	8472	495	B
244	G<60>	8448	360	B
245	G<62>	8424	495	B
246	G<64>	8400	360	B
247	G<66>	8376	495	B
248	G<68>	8352	360	B
249	G<70>	8328	495	B
250	G<72>	8304	360	B
251	G<74>	8280	495	B
252	G<76>	8256	360	B
253	G<78>	8232	495	B
254	G<80>	8208	360	B
255	G<82>	8184	495	B
256	G<84>	8160	360	B
257	G<86>	8136	495	B
258	G<88>	8112	360	B
259	G<90>	8088	495	B
260	G<92>	8064	360	B
261	G<94>	8040	495	B
262	G<96>	8016	360	B
263	G<98>	7992	495	B
264	G<100>	7968	360	B
265	G<102>	7944	495	B
266	G<104>	7920	360	B
267	G<106>	7896	495	B
268	G<108>	7872	360	B
269	G<110>	7848	495	B
270	G<112>	7824	360	B
271	G<114>	7800	495	B
272	G<116>	7776	360	B
273	G<118>	7752	495	B
274	G<120>	7728	360	B
275	G<122>	7704	495	B
276	G<124>	7680	360	B
277	G<126>	7656	495	B
278	G<128>	7632	360	B
279	G<130>	7608	495	B
280	G<132>	7584	360	B
281	G<134>	7560	495	B
282	G<136>	7536	360	B
283	G<138>	7512	495	B
284	G<140>	7488	360	B
285	G<142>	7464	495	B
286	G<144>	7440	360	B
287	G<146>	7416	495	B
288	G<148>	7392	360	B
289	G<150>	7368	495	B
290	G<152>	7344	360	B
291	G<154>	7320	495	B
292	G<156>	7296	360	B
293	G<158>	7272	495	B
294	G<160>	7248	360	B
295	G<162>	7224	495	B
296	G<164>	7200	360	B
297	G<166>	7176	495	B
298	G<168>	7152	360	B
299	G<170>	7128	495	B
300	G<172>	7104	360	B

Bump No.	Bump Name	X(um)	Y(um)	Pad type
301	G<174>	7080	495	B
302	G<176>	7056	360	B
303	G<178>	7032	495	B
304	G<180>	7008	360	B
305	G<182>	6984	495	B
306	G<184>	6960	360	B
307	G<186>	6936	495	B
308	G<188>	6912	360	B
309	G<190>	6888	495	B
310	G<192>	6864	360	B
311	G<194>	6840	495	B
312	G<196>	6816	360	B
313	G<198>	6792	495	B
314	G<200>	6768	360	B
315	G<202>	6744	495	B
316	G<204>	6720	360	B
317	G<206>	6696	495	B
318	G<208>	6672	360	B
319	G<210>	6648	495	B
320	G<212>	6624	360	B
321	G<214>	6600	495	B
322	G<216>	6576	360	B
323	G<218>	6552	495	B
324	G<220>	6528	360	B
325	GTEST2	6504	495	B
326	DUMMY19	6480	360	B
327	DUMMY20	6456	495	B
328	VCOM7	6432	360	B
329	VCOM8	6408	495	B
330	DUMMY21	6384	360	B
331	DUMMY22	6360	495	B
332	S<528>	6336	360	B
333	S<527>	6312	495	B
334	S<526>	6288	360	B
335	S<525>	6264	495	B
336	S<524>	6240	360	B
337	S<523>	6216	495	B
338	S<522>	6192	360	B
339	S<521>	6168	495	B
340	S<520>	6144	360	B
341	S<519>	6120	495	B
342	S<518>	6096	360	B
343	S<517>	6072	495	B
344	S<516>	6048	360	B
345	S<515>	6024	495	B
346	S<514>	6000	360	B
347	S<513>	5976	495	B
348	S<512>	5952	360	B
349	S<511>	5928	495	B
350	S<510>	5904	360	B
351	S<509>	5880	495	B
352	S<508>	5856	360	B
353	S<507>	5832	495	B
354	S<506>	5808	360	B
355	S<505>	5784	495	B
356	S<504>	5760	360	B
357	S<503>	5736	495	B
358	S<502>	5712	360	B
359	S<501>	5688	495	B
360	S<500>	5664	360	B

Bump No.	Bump Name	X(um)	Y(um)	Pad type
361	S<499>	5640	495	B
362	S<498>	5616	360	B
363	S<497>	5592	495	B
364	S<496>	5568	360	B
365	S<495>	5544	495	B
366	S<494>	5520	360	B
367	S<493>	5496	495	B
368	S<492>	5472	360	B
369	S<491>	5448	495	B
370	S<490>	5424	360	B
371	S<489>	5400	495	B
372	S<488>	5376	360	B
373	S<487>	5352	495	B
374	S<486>	5328	360	B
375	S<485>	5304	495	B
376	S<484>	5280	360	B
377	S<483>	5256	495	B
378	S<482>	5232	360	B
379	S<481>	5208	495	B
380	S<480>	5184	360	B
381	S<479>	5160	495	B
382	S<478>	5136	360	B
383	S<477>	5112	495	B
384	S<476>	5088	360	B
385	S<475>	5064	495	B
386	S<474>	5040	360	B
387	S<473>	5016	495	B
388	S<472>	4992	360	B
389	S<471>	4968	495	B
390	S<470>	4944	360	B
391	S<469>	4920	495	B
392	S<468>	4896	360	B
393	S<467>	4872	495	B
394	S<466>	4848	360	B
395	S<465>	4824	495	B
396	S<464>	4800	360	B
397	S<463>	4776	495	B
398	S<462>	4752	360	B
399	S<461>	4728	495	B
400	S<460>	4704	360	B
401	S<459>	4680	495	B
402	S<458>	4656	360	B
403	S<457>	4632	495	B
404	S<456>	4608	360	B
405	S<455>	4584	495	B
406	S<454>	4560	360	B
407	S<453>	4536	495	B
408	S<452>	4512	360	B
409	S<451>	4488	495	B
410	S<450>	4464	360	B
411	S<449>	4440	495	B
412	S<448>	4416	360	B
413	S<447>	4392	495	B
414	S<446>	4368	360	B
415	S<445>	4344	495	B
416	S<444>	4320	360	B
417	S<443>	4296	495	B
418	S<442>	4272	360	B
419	S<441>	4248	495	B
420	S<440>	4224	360	B

Bump No.	Bump Name	X(um)	Y(um)	Pad type
421	S<439>	4200	495	B
422	S<438>	4176	360	B
423	S<437>	4152	495	B
424	S<436>	4128	360	B
425	S<435>	4104	495	B
426	S<434>	4080	360	B
427	S<433>	4056	495	B
428	S<432>	4032	360	B
429	S<431>	4008	495	B
430	S<430>	3984	360	B
431	S<429>	3960	495	B
432	S<428>	3936	360	B
433	S<427>	3912	495	B
434	S<426>	3888	360	B
435	S<425>	3864	495	B
436	S<424>	3840	360	B
437	S<423>	3816	495	B
438	S<422>	3792	360	B
439	S<421>	3768	495	B
440	S<420>	3744	360	B
441	S<419>	3720	495	B
442	S<418>	3696	360	B
443	S<417>	3672	495	B
444	S<416>	3648	360	B
445	S<415>	3624	495	B
446	S<414>	3600	360	B
447	S<413>	3576	495	B
448	S<412>	3552	360	B
449	S<411>	3528	495	B
450	S<410>	3504	360	B
451	S<409>	3480	495	B
452	S<408>	3456	360	B
453	S<407>	3432	495	B
454	S<406>	3408	360	B
455	S<405>	3384	495	B
456	S<404>	3360	360	B
457	S<403>	3336	495	B
458	S<402>	3312	360	B
459	S<401>	3288	495	B
460	S<400>	3264	360	B
461	S<399>	3240	495	B
462	S<398>	3216	360	B
463	S<397>	3192	495	B
464	S<396>	3168	360	B
465	S<395>	3144	495	B
466	S<394>	3120	360	B
467	S<393>	3096	495	B
468	S<392>	3072	360	B
469	S<391>	3048	495	B
470	S<390>	3024	360	B
471	S<389>	3000	495	B
472	S<388>	2976	360	B
473	S<387>	2952	495	B
474	S<386>	2928	360	B
475	S<385>	2904	495	B
476	S<384>	2880	360	B
477	S<383>	2856	495	B
478	S<382>	2832	360	B
479	S<381>	2808	495	B
480	S<380>	2784	360	B

Bump No.	Bump Name	X(um)	Y(um)	Pad type
481	S<379>	2760	495	B
482	S<378>	2736	360	B
483	S<377>	2712	495	B
484	S<376>	2688	360	B
485	S<375>	2664	495	B
486	S<374>	2640	360	B
487	S<373>	2616	495	B
488	S<372>	2592	360	B
489	S<371>	2568	495	B
490	S<370>	2544	360	B
491	S<369>	2520	495	B
492	S<368>	2496	360	B
493	S<367>	2472	495	B
494	S<366>	2448	360	B
495	S<365>	2424	495	B
496	S<364>	2400	360	B
497	S<363>	2376	495	B
498	S<362>	2352	360	B
499	S<361>	2328	495	B
500	S<360>	2304	360	B
501	S<359>	2280	495	B
502	S<358>	2256	360	B
503	S<357>	2232	495	B
504	S<356>	2208	360	B
505	S<355>	2184	495	B
506	S<354>	2160	360	B
507	S<353>	2136	495	B
508	S<352>	2112	360	B
509	S<351>	2088	495	B
510	S<350>	2064	360	B
511	S<349>	2040	495	B
512	S<348>	2016	360	B
513	S<347>	1992	495	B
514	S<346>	1968	360	B
515	S<345>	1944	495	B
516	S<344>	1920	360	B
517	S<343>	1896	495	B
518	S<342>	1872	360	B
519	S<341>	1848	495	B
520	S<340>	1824	360	B
521	S<339>	1800	495	B
522	S<338>	1776	360	B
523	S<337>	1752	495	B
524	S<336>	1728	360	B
525	S<335>	1704	495	B
526	S<334>	1680	360	B
527	S<333>	1656	495	B
528	S<332>	1632	360	B
529	S<331>	1608	495	B
530	S<330>	1584	360	B
531	S<329>	1560	495	B
532	S<328>	1536	360	B
533	S<327>	1512	495	B
534	S<326>	1488	360	B
535	S<325>	1464	495	B
536	S<324>	1440	360	B
537	S<323>	1416	495	B
538	S<322>	1392	360	B
539	S<321>	1368	495	B
540	S<320>	1344	360	B

Bump No.	Bump Name	X(um)	Y(um)	Pad type
541	S<319>	1320	495	B
542	S<318>	1296	360	B
543	S<317>	1272	495	B
544	S<316>	1248	360	B
545	S<315>	1224	495	B
546	S<314>	1200	360	B
547	S<313>	1176	495	B
548	S<312>	1152	360	B
549	S<311>	1128	495	B
550	S<310>	1104	360	B
551	S<309>	1080	495	B
552	S<308>	1056	360	B
553	S<307>	1032	495	B
554	S<306>	1008	360	B
555	S<305>	984	495	B
556	S<304>	960	360	B
557	S<303>	936	495	B
558	S<302>	912	360	B
559	S<301>	888	495	B
560	S<300>	864	360	B
561	S<299>	840	495	B
562	S<298>	816	360	B
563	S<297>	792	495	B
564	S<296>	768	360	B
565	S<295>	744	495	B
566	S<294>	720	360	B
567	S<293>	696	495	B
568	S<292>	672	360	B
569	S<291>	648	495	B
570	S<290>	624	360	B
571	S<289>	600	495	B
572	S<288>	576	360	B
573	S<287>	552	495	B
574	S<286>	528	360	B
575	S<285>	504	495	B
576	S<284>	480	360	B
577	S<283>	456	495	B
578	S<282>	432	360	B
579	S<281>	408	495	B
580	S<280>	384	360	B
581	S<279>	360	495	B
582	S<278>	336	360	B
583	S<277>	312	495	B
584	S<276>	288	360	B
585	S<275>	264	495	B
586	S<274>	240	360	B
587	S<273>	216	495	B
588	S<272>	192	360	B
589	S<271>	168	495	B
590	S<270>	144	360	B
591	S<269>	120	495	B
592	S<268>	96	360	B
593	S<267>	72	495	B
594	S<266>	48	360	B
595	S<265>	24	495	B
596	DUMMY23	0	360	B
597	S<264>	-24	495	B
598	S<263>	-48	360	B
599	S<262>	-72	495	B
600	S<261>	-96	360	B

Bump No.	Bump Name	X(um)	Y(um)	Pad type
601	S<260>	-120	495	B
602	S<259>	-144	360	B
603	S<258>	-168	495	B
604	S<257>	-192	360	B
605	S<256>	-216	495	B
606	S<255>	-240	360	B
607	S<254>	-264	495	B
608	S<253>	-288	360	B
609	S<252>	-312	495	B
610	S<251>	-336	360	B
611	S<250>	-360	495	B
612	S<249>	-384	360	B
613	S<248>	-408	495	B
614	S<247>	-432	360	B
615	S<246>	-456	495	B
616	S<245>	-480	360	B
617	S<244>	-504	495	B
618	S<243>	-528	360	B
619	S<242>	-552	495	B
620	S<241>	-576	360	B
621	S<240>	-600	495	B
622	S<239>	-624	360	B
623	S<238>	-648	495	B
624	S<237>	-672	360	B
625	S<236>	-696	495	B
626	S<235>	-720	360	B
627	S<234>	-744	495	B
628	S<233>	-768	360	B
629	S<232>	-792	495	B
630	S<231>	-816	360	B
631	S<230>	-840	495	B
632	S<229>	-864	360	B
633	S<228>	-888	495	B
634	S<227>	-912	360	B
635	S<226>	-936	495	B
636	S<225>	-960	360	B
637	S<224>	-984	495	B
638	S<223>	-1008	360	B
639	S<222>	-1032	495	B
640	S<221>	-1056	360	B
641	S<220>	-1080	495	B
642	S<219>	-1104	360	B
643	S<218>	-1128	495	B
644	S<217>	-1152	360	B
645	S<216>	-1176	495	B
646	S<215>	-1200	360	B
647	S<214>	-1224	495	B
648	S<213>	-1248	360	B
649	S<212>	-1272	495	B
650	S<211>	-1296	360	B
651	S<210>	-1320	495	B
652	S<209>	-1344	360	B
653	S<208>	-1368	495	B
654	S<207>	-1392	360	B
655	S<206>	-1416	495	B
656	S<205>	-1440	360	B
657	S<204>	-1464	495	B
658	S<203>	-1488	360	B
659	S<202>	-1512	495	B
660	S<201>	-1536	360	B

Bump No.	Bump Name	X(um)	Y(um)	Pad type
661	S<200>	-1560	495	B
662	S<199>	-1584	360	B
663	S<198>	-1608	495	B
664	S<197>	-1632	360	B
665	S<196>	-1656	495	B
666	S<195>	-1680	360	B
667	S<194>	-1704	495	B
668	S<193>	-1728	360	B
669	S<192>	-1752	495	B
670	S<191>	-1776	360	B
671	S<190>	-1800	495	B
672	S<189>	-1824	360	B
673	S<188>	-1848	495	B
674	S<187>	-1872	360	B
675	S<186>	-1896	495	B
676	S<185>	-1920	360	B
677	S<184>	-1944	495	B
678	S<183>	-1968	360	B
679	S<182>	-1992	495	B
680	S<181>	-2016	360	B
681	S<180>	-2040	495	B
682	S<179>	-2064	360	B
683	S<178>	-2088	495	B
684	S<177>	-2112	360	B
685	S<176>	-2136	495	B
686	S<175>	-2160	360	B
687	S<174>	-2184	495	B
688	S<173>	-2208	360	B
689	S<172>	-2232	495	B
690	S<171>	-2256	360	B
691	S<170>	-2280	495	B
692	S<169>	-2304	360	B
693	S<168>	-2328	495	B
694	S<167>	-2352	360	B
695	S<166>	-2376	495	B
696	S<165>	-2400	360	B
697	S<164>	-2424	495	B
698	S<163>	-2448	360	B
699	S<162>	-2472	495	B
700	S<161>	-2496	360	B
701	S<160>	-2520	495	B
702	S<159>	-2544	360	B
703	S<158>	-2568	495	B
704	S<157>	-2592	360	B
705	S<156>	-2616	495	B
706	S<155>	-2640	360	B
707	S<154>	-2664	495	B
708	S<153>	-2688	360	B
709	S<152>	-2712	495	B
710	S<151>	-2736	360	B
711	S<150>	-2760	495	B
712	S<149>	-2784	360	B
713	S<148>	-2808	495	B
714	S<147>	-2832	360	B
715	S<146>	-2856	495	B
716	S<145>	-2880	360	B
717	S<144>	-2904	495	B
718	S<143>	-2928	360	B
719	S<142>	-2952	495	B
720	S<141>	-2976	360	B

Bump No.	Bump Name	X(um)	Y(um)	Pad type
721	S<140>	-3000	495	B
722	S<139>	-3024	360	B
723	S<138>	-3048	495	B
724	S<137>	-3072	360	B
725	S<136>	-3096	495	B
726	S<135>	-3120	360	B
727	S<134>	-3144	495	B
728	S<133>	-3168	360	B
729	S<132>	-3192	495	B
730	S<131>	-3216	360	B
731	S<130>	-3240	495	B
732	S<129>	-3264	360	B
733	S<128>	-3288	495	B
734	S<127>	-3312	360	B
735	S<126>	-3336	495	B
736	S<125>	-3360	360	B
737	S<124>	-3384	495	B
738	S<123>	-3408	360	B
739	S<122>	-3432	495	B
740	S<121>	-3456	360	B
741	S<120>	-3480	495	B
742	S<119>	-3504	360	B
743	S<118>	-3528	495	B
744	S<117>	-3552	360	B
745	S<116>	-3576	495	B
746	S<115>	-3600	360	B
747	S<114>	-3624	495	B
748	S<113>	-3648	360	B
749	S<112>	-3672	495	B
750	S<111>	-3696	360	B
751	S<110>	-3720	495	B
752	S<109>	-3744	360	B
753	S<108>	-3768	495	B
754	S<107>	-3792	360	B
755	S<106>	-3816	495	B
756	S<105>	-3840	360	B
757	S<104>	-3864	495	B
758	S<103>	-3888	360	B
759	S<102>	-3912	495	B
760	S<101>	-3936	360	B
761	S<100>	-3960	495	B
762	S<99>	-3984	360	B
763	S<98>	-4008	495	B
764	S<97>	-4032	360	B
765	S<96>	-4056	495	B
766	S<95>	-4080	360	B
767	S<94>	-4104	495	B
768	S<93>	-4128	360	B
769	S<92>	-4152	495	B
770	S<91>	-4176	360	B
771	S<90>	-4200	495	B
772	S<89>	-4224	360	B
773	S<88>	-4248	495	B
774	S<87>	-4272	360	B
775	S<86>	-4296	495	B
776	S<85>	-4320	360	B
777	S<84>	-4344	495	B
778	S<83>	-4368	360	B
779	S<82>	-4392	495	B
780	S<81>	-4416	360	B

Bump No.	Bump Name	X(um)	Y(um)	Pad type
781	S<80>	-4440	495	B
782	S<79>	-4464	360	B
783	S<78>	-4488	495	B
784	S<77>	-4512	360	B
785	S<76>	-4536	495	B
786	S<75>	-4560	360	B
787	S<74>	-4584	495	B
788	S<73>	-4608	360	B
789	S<72>	-4632	495	B
790	S<71>	-4656	360	B
791	S<70>	-4680	495	B
792	S<69>	-4704	360	B
793	S<68>	-4728	495	B
794	S<67>	-4752	360	B
795	S<66>	-4776	495	B
796	S<65>	-4800	360	B
797	S<64>	-4824	495	B
798	S<63>	-4848	360	B
799	S<62>	-4872	495	B
800	S<61>	-4896	360	B
801	S<60>	-4920	495	B
802	S<59>	-4944	360	B
803	S<58>	-4968	495	B
804	S<57>	-4992	360	B
805	S<56>	-5016	495	B
806	S<55>	-5040	360	B
807	S<54>	-5064	495	B
808	S<53>	-5088	360	B
809	S<52>	-5112	495	B
810	S<51>	-5136	360	B
811	S<50>	-5160	495	B
812	S<49>	-5184	360	B
813	S<48>	-5208	495	B
814	S<47>	-5232	360	B
815	S<46>	-5256	495	B
816	S<45>	-5280	360	B
817	S<44>	-5304	495	B
818	S<43>	-5328	360	B
819	S<42>	-5352	495	B
820	S<41>	-5376	360	B
821	S<40>	-5400	495	B
822	S<39>	-5424	360	B
823	S<38>	-5448	495	B
824	S<37>	-5472	360	B
825	S<36>	-5496	495	B
826	S<35>	-5520	360	B
827	S<34>	-5544	495	B
828	S<33>	-5568	360	B
829	S<32>	-5592	495	B
830	S<31>	-5616	360	B
831	S<30>	-5640	495	B
832	S<29>	-5664	360	B
833	S<28>	-5688	495	B
834	S<27>	-5712	360	B
835	S<26>	-5736	495	B
836	S<25>	-5760	360	B
837	S<24>	-5784	495	B
838	S<23>	-5808	360	B
839	S<22>	-5832	495	B
840	S<21>	-5856	360	B

Bump No.	Bump Name	X(um)	Y(um)	Pad type
841	S<20>	-5880	495	B
842	S<19>	-5904	360	B
843	S<18>	-5928	495	B
844	S<17>	-5952	360	B
845	S<16>	-5976	495	B
846	S<15>	-6000	360	B
847	S<14>	-6024	495	B
848	S<13>	-6048	360	B
849	S<12>	-6072	495	B
850	S<11>	-6096	360	B
851	S<10>	-6120	495	B
852	S<9>	-6144	360	B
853	S<8>	-6168	495	B
854	S<7>	-6192	360	B
855	S<6>	-6216	495	B
856	S<5>	-6240	360	B
857	S<4>	-6264	495	B
858	S<3>	-6288	360	B
859	S<2>	-6312	495	B
860	S<1>	-6336	360	B
861	DUMMY24	-6360	495	B
862	DUMMY25	-6384	360	B
863	VCOM9	-6408	495	B
864	VCOM10	-6432	360	B
865	DUMMY26	-6456	495	B
866	DUMMY27	-6480	360	B
867	G<219>	-6504	495	B
868	G<217>	-6528	360	B
869	G<215>	-6552	495	B
870	G<213>	-6576	360	B
871	G<211>	-6600	495	B
872	G<209>	-6624	360	B
873	G<207>	-6648	495	B
874	G<205>	-6672	360	B
875	G<203>	-6696	495	B
876	G<201>	-6720	360	B
877	G<199>	-6744	495	B
878	G<197>	-6768	360	B
879	G<195>	-6792	495	B
880	G<193>	-6816	360	B
881	G<191>	-6840	495	B
882	G<189>	-6864	360	B
883	G<187>	-6888	495	B
884	G<185>	-6912	360	B
885	G<183>	-6936	495	B
886	G<181>	-6960	360	B
887	G<179>	-6984	495	B
888	G<177>	-7008	360	B
889	G<175>	-7032	495	B
890	G<173>	-7056	360	B
891	G<171>	-7080	495	B
892	G<169>	-7104	360	B
893	G<167>	-7128	495	B
894	G<165>	-7152	360	B
895	G<163>	-7176	495	B
896	G<161>	-7200	360	B
897	G<159>	-7224	495	B
898	G<157>	-7248	360	B
899	G<155>	-7272	495	B
900	G<153>	-7296	360	B

Bump No.	Bump Name	X(um)	Y(um)	Pad type
901	G<151>	-7320	495	B
902	G<149>	-7344	360	B
903	G<147>	-7368	495	B
904	G<145>	-7392	360	B
905	G<143>	-7416	495	B
906	G<141>	-7440	360	B
907	G<139>	-7464	495	B
908	G<137>	-7488	360	B
909	G<135>	-7512	495	B
910	G<133>	-7536	360	B
911	G<131>	-7560	495	B
912	G<129>	-7584	360	B
913	G<127>	-7608	495	B
914	G<125>	-7632	360	B
915	G<123>	-7656	495	B
916	G<121>	-7680	360	B
917	G<119>	-7704	495	B
918	G<117>	-7728	360	B
919	G<115>	-7752	495	B
920	G<113>	-7776	360	B
921	G<111>	-7800	495	B
922	G<109>	-7824	360	B
923	G<107>	-7848	495	B
924	G<105>	-7872	360	B
925	G<103>	-7896	495	B
926	G<101>	-7920	360	B
927	G<99>	-7944	495	B
928	G<97>	-7968	360	B
929	G<95>	-7992	495	B
930	G<93>	-8016	360	B
931	G<91>	-8040	495	B
932	G<89>	-8064	360	B
933	G<87>	-8088	495	B
934	G<85>	-8112	360	B
935	G<83>	-8136	495	B
936	G<81>	-8160	360	B
937	G<79>	-8184	495	B
938	G<77>	-8208	360	B
939	G<75>	-8232	495	B
940	G<73>	-8256	360	B
941	G<71>	-8280	495	B
942	G<69>	-8304	360	B
943	G<67>	-8328	495	B
944	G<65>	-8352	360	B
945	G<63>	-8376	495	B
946	G<61>	-8400	360	B
947	G<59>	-8424	495	B
948	G<57>	-8448	360	B
949	G<55>	-8472	495	B
950	G<53>	-8496	360	B
951	G<51>	-8520	495	B
952	G<49>	-8544	360	B
953	G<47>	-8568	495	B
954	G<45>	-8592	360	B
955	G<43>	-8616	495	B
956	G<41>	-8640	360	B
957	G<39>	-8664	495	B
958	G<37>	-8688	360	B
959	G<35>	-8712	495	B
960	G<33>	-8736	360	B

Bump No.	Bump Name	X(um)	Y(um)	Pad type
961	G<31>	-8760	495	B
962	G<29>	-8784	360	B
963	G<27>	-8808	495	B
964	G<25>	-8832	360	B
965	G<23>	-8856	495	B
966	G<21>	-8880	360	B
967	G<19>	-8904	495	B
968	G<17>	-8928	360	B
969	G<15>	-8952	495	B
970	G<13>	-8976	360	B
971	G<11>	-9000	495	B
972	G<9>	-9024	360	B
973	G<7>	-9048	495	B
974	G<5>	-9072	360	B
975	G<3>	-9096	495	B
976	G<1>	-9120	360	B
977	GTEST1	-9144	495	B
978	DUMMY28	-9168	360	B
979	DUMMY29	-9192	495	B
980	DUMMY30	-9216	360	B
981	DUMMY31	-9240	495	B
982	DUMMY32	-9264	360	B
983	DUMMY33	-9288	495	B

6. Pin Function

6.1. Power supply pins - 1

Bump No.	Signal	No. of Pins	I/O	Connected to	Function	Unused pins
110-115	VCI	6	I	Power supply	Power supply for the analog circuit and the VCI1 amplifier. Connect to an external power supply of 2.5 to 3.3V.	-
116-117	VCILVL	2	I	Power supply	A reference voltage (VCI1/REGP) is generated from the VCILVL (VCI) voltage level by stepping up by the rate set with the VC2-0 bits. VCILVL and VCI must be connected to the same power supply on the FPC. Make sure to separate the wiring of VCILVL from VCI on the FPC.	-
40,44 108-109	IOVCC	4	-	Power supply	Power supply for the interface pins (NRESET, NCS, NWR, NRD, RS, D17-0, VSYNC, HSYNC, DOTCLK, ENABLE). In case of COG, connect to VCI on the FPC if IOVCC=VCI, to prevent noise.	-
36,42,73 118-125	VSS	11		Power supply	Power supply GND level for logic and the DDRAM. VSS=0V.	-
126-133	AGND	8	-	Power supply	Power supply GND level for the analog circuit. AGND=0V. In case of COG, connect to VSS on the FPC to prevent noise.	-

6.2. Power supply pins - 2

Bump No.	Signal	No. of Pins	I/O	Connected to	Function	Unused pins
154, 155 156, 157	VCI1	4	I/O	Stabilizing capacitor	A reference voltage input to the step-up circuit 1. The VCI1 output level is set with the VC2-0 bits. Set so that the VGH, VGL and VCL levels will not exceed the limits set in the MC2TA7402 specifications.	-
158-165	DDVDH	8	I/O	Stabilizing capacitor	A step-up voltage by the step-up circuit 1 generated from VCI1. DDVDH=4.5 to 5.5V. A power supply to the source driver and for VCOM drive.	-
8-9	VGH	2	O	Stabilizing capacitor	A supply voltage to a gate driver incorporated in a TFT LCD panel. This voltage is generated from VCI1 and DDVDH from the step-up circuit 2. The step-up rate is set with the BT bits. VGH = max. 16.5V	-
32-35	VGL	6	I/O	Stabilizing capacitor	A supply voltage to a gate driver incorporated in a TFT LCD panel. An output voltage generated from VCI1 and DDVDH from the step-up circuit 2. The step-up rate is set with the BT bits. VGL=min. -16.5V	-
28-31	VCL	4	I/O	Stabilizing capacitor	A supply voltage for generating the VCOML level. Output voltage from the step-up circuit 3, -1 time the VCI1 level. . VCL=-0V to -3.3V	-
140-143	V18	4	O	Power supply Stabilizing capacitor	Outputs 1.8V. VDD and V18 must have the same electrical potential. Connect VDD and V18 on the FPC.	-
134-139	VDD	6	-	Power supply	Power supply for logic and the DDRAM: VDD VDD and V18 must have the same electrical potential. Connect VDD and V18 on the FPC.	-
152-153	VREG1OUT	2	I/O	Stabilizing	A voltage level generated from the REGP level (a reference voltage	Open

				capacitor or power supply	level generated internally from the VCI1-GND level) by applying a rate set with the GVD5-0 bits. VREG1OUT is used for VREG1OUT is used for a source driver grayscale reference voltage. Connect to a stabilizing capacitor. VREG1OUT=3.0 to (DDVDH-0.3) V.	
195-198	VCOMH	4	O	Stabilizing capacitor	The high level of VCOM AC voltage. Adjust VCOMH with either internal electric volumes or an external resistor from VCOMR.	Open
191-194	VCOML	4	O	Stabilizing capacitor	The low level of VCOM AC voltage. Adjust VCOML with the VDV bits. . VCOML = (VCL+0.3) V to 1V.	Open
189-190	VCOMR	2	I	Variable resistor	VCOMR is used when adjusting the VCOMH level with an external resistor. Place a variable resistor between VREG1OUT and VSS(GND level).	Open
150-151	VGS	2	I	VSS(GND level)or resistor	A reference level for the grayscale voltage generating circuit.	-

6.3. Logic I/O Pins

Bump No.	Signal	No. of Pins	I/O	Connected to	Function	Unused pins
39 41 43 45	IM3 IM2 IM1 IM0	1 1 1 1	I	VSS (GND level)/ IOVCC	Select an interfacing mode with the MPU. (Amplitude: IOVCC-VSS(GND level))	-

IM3	IM2	IM1	IM0	Interface Mode	data pin	Colors
0	0	0	0	68-system 16-bit interface	D17-10, D8-1	65,536
0	0	0	1	68-system 8bit interface	D17-10	262,144 65,536
0	0	1	0	80-sytem 16-bit interface	D17-10, D8-1	262,144 65.536
0	0	1	1	80-system 8-bit interface	D17-10	262,144 65,536
0	1	0	*	Serial Peripheral Interface (SPI)	----	262,144 65,536
0	1	1	*	Setting disabled	----	
1	0	0	0	68-system 18-bit interface	D17-0	262,144
1	0	0	1	68-system 9-bit interface	D17-9	262,144
1	0	1	0	80-system 18-bit interface	D17-0	262,144
1	0	1	1	80-system 9-bit interface	D17-9	262,144
1	1	*	*	Setting disabled		

46-47	NRESET	2	I	MPU or external RC circuit	A reset pin. Initializes the MC2TA7402 when the signal is low. Make sure to execute a power-on reset after supplying power. (Amplitude: IOVCC-VSS(GND level))	-
104-105	NCS	2	I	MPU	Selects the MC2TA7402 (Amplitude: IOVCC-VSS(GND level)) Low: the MC2TA7402 is selected and accessible High: the MC2TA7402 is not selected and not accessible	-
102-103	RS	2	I	MPU	A register selecting signal. (Amplitude: IOVCC-VSS(GND level)) Low: select the Index or status register High: select a control register	VSS(GND level)/ IOVCC

Bump No.	Signal	No. of Pins	I/O	Connected to	Function	Unused pins
96-97	NWR	2	I	MPU	Inputs a write strobe signal in 80-system bus interface mode and enables an operation to write data when the signal is low. (Amplitude: IOVCC-VSS(GND level)) Inputs an ENABLE signal for selecting a data read/write operation in 68-system interface mode.	VSS(GND level)/ IOVCC
100-101	NRD	2	I	MPU	Inputs a read strobe signal in 80-system bus interface mode and enables an operation to read out data when the signal is low. (Amplitude: IOVCC-VSS(GND level)) Inputs the ENABLE signal for triggering either a read or write operation in 68-system interface mode (Low: write, High: read out).	VSS(GND level)/ IOVCC
54-55	ENABLE	2	I	MPU	A data ENABLE signal in RGB interface mode. Low: select (access enabled) High: not selected (access inhibited) The EPL bit inverts the polarity of the ENABLE signal. (Amplitude: IOVCC-VSS(GND level))	VSS(GND level)/ IOVCC
48-49	VSYNC	2	I	MPU	A VSYNC synchronizing signal. The VSPL bit inverts the polarity of the VSYNC signal. (Amplitude: IOVCC-VSS(GND level))	VSS(GND level)/ IOVCC
50-51	HSYNC	2	I	MPU	A HSYNC synchronizing signal. The HSPL bit inverts the polarity of the HSYNC signal. (Amplitude: IOVCC-GNDlevel)	GND level/ IOVCC
52-53	DOTCLK	2	I	MPU	A dot clock signal. Data is input on the rising edge. (Amplitude: IOVCC-GND level)	GND level/ IOVCC
56-71 72 74-91	D17-10 D9 D8-0	2 x 8 1 2 x 9	I/O	MPU	An 18-bit parallel bi-directional data bus for 80-/68-system interfaces (Amplitude: IOVCC-GND level). ● 8-bit bus: D17-D10 ● 9-bit bus: D17-D9 ● 16-bit bus: D17-D10 and D8-D1 ● 18-bit bus: D17-D0 An 18-bit RGB data bus for RGB interfaces (Amplitude: IOVCC-GND level) ● 6-bit bus: D17-D12 ● 16-bit bus: D17-D13 and D11-D1 ● 18-bit bus: D17-D0	GND level/ IOVCC
94-95	SDI	2	I	MPU	A serial data input (SDI) pin. (Amplitude: IOVCC-GND level) Data are input on the rising edge of the SCL signal.	GND level/ IOVCC
92-93	SDO	2	O	MPU	A serial data output (SDO) pin. Data are output on the falling edge of the SCL signal.	Open
98-99	SCL	2	I	MPU	A synchronizing clock signal in SPI mode. (Amplitude: IOVCC-GND level)	GND level/ IOVCC
168-169 170-171	OSC1, OSC2	2 2	I/O	R	External resistor connection pins for CS oscillation.	-

6.4. Step-up Capacitor Pins

Bump No.	Signal	No. of Pins	I/O	Connected to	Function	Unused pins
180-185 174-179	C11P C11M	6 6	I/O	Step-up capacitor	Pins to connect capacitors for the step-up circuit 1.	-
19-22, 23-26	C12P C12M	4 4	I/O	Step-up capacitor	Pins to connect to capacitors for the step-up circuit 3. Connect a capacitor as required for the step-up rate in use.	-
15-16 17-18 11-12 13-14	C21P C21M C22P C22M	2 2 2 2	I/O	Step-up capacitor	Pins to connect to capacitors for the step-up circuit 2. Connect a capacitor as required for the step-up rate in use.	-

6.5. Driver Output Pins

Bump No.	Signal	No. of Pins	I/O	Connected to	Function	Unused pins
332-595 597-860	S528-S1	528	O	LCD	Pins for source line output.	Open
215-324 867-976	G2-G220 G219-G1	220	O	LCD	Pins for gate line output. ● VGH: the level for selecting gate lines ● VGL: the level for not selecting gate lines	Open
5-6 201-204 328-329 863-864	VCOM1 VCOM2 VCOM3 VCOM4 VCOM5 VCOM6 VCOM7 VCOM8 VCOM9 VCOM10	2 2 2 2 2	O	TFT LCD common electrode	A supply voltage to the common electrode of TFT LCD. Outputs AC voltages between VCOMH and VCOML levels. The AC voltages are set by registers.	Open
106-107	FLM	2	O	MPU	Output a frame head pulse signal. (Amplitude: IOVCC-GND level). The FLM signal is used when writing DDRAM data in synchronization with a frame.	Open
199-200	M	2	O	(VCOM)	This pin can be set the alternating cycle.	VSS(GND level)
187-188	VREF	2			Open pins.	Open

6.6. Test Pins and Others

Bump No.	Signal	No. of Pins	I/O	Connected to	Function	Unused pins
146-149	TEST1, TEST2	2 2	I	VSS(GND level)	Test pins.	VSS(GND level)
977 325	GTEST1 GTEST2	1 1	-	Open (TFT LCD panel)	Dummy output pins. Either connect them to panel's dummy gate or leave them open.	Open
147 148	DUMMYR1 DUMMYR2	1 1	-	-	Dummy pads. Use them to measure the COG contact resistance. DUMMYR1 and DUMMYR2 are short-circuited within the chip.	Open
205 206 213 214	DUMMYR3 DUMMYR4 DUMMYR5 DUMMYR6	1 1 1 1	-	VSS(GND level)	Each pad must be connected to GND level.	-
187-188 1-4 7,10,27 166-167 172-173 186 207-212 326-327 330-331 596 861-862 865-866 978-983	PSSP DUMMY1-4 DUMMY5-7 DUMMY8-9 DUMMY10-11 DUMMY12 DUMMY13-18 DUMMY19-20 DUMMY21-22 DUMMY23 DUMMY24-25 DUMMY26-27 DUMMY28-33	2 1 1 1 1 1 1 1 1 1 1 1 1	-	Open	Dummy pads. Leave these pins open. These pins have no ESD protection circuits.	Open

7. Block Function

7.1. System Interface

The MC2TA7402 supports nine high-speed system interfaces. The interface mode is selected by setting the IM3-0 pins.

- 80-system high-speed interfaces with 8-, 9-, 16-, 18-bit parallel ports
- 68-system high-speed interfaces with 8-, 9-, 16-, 18-bit parallel ports
- Serial Peripheral Interface (SPI)

Table 7-1: Interface Selection by IM3-0 pins

IM3	IM2	IM1	IM0	Interface Mode		data pin	Colors
0	0	0	0	68-system	16-bit interface	D17-10, D8-1	65,536
0	0	0	1	68-system	8bit interface	D17-10	262,144 / 65,536
0	0	1	0	80-sytem	16-bit interface	D17-10, D8-1	262,144 / 65,536
0	0	1	1	80-system	8-bit interface	D17-10	262,144 / 65,536
0	1	0	*	Serial Peripheral Interface (SPI)		-	262,144 / 65,536
0	1	1	*	Setting disabled		-	-
1	0	0	0	68-system	18-bit interface	D17-0	262,144
1	0	0	1	68-system	9-bit interface	D17-9	262,144
1	0	1	0	80-system	18-bit interface	D17-0	262,144
1	0	1	1	80-system	9-bit interface	D17-9	262,144
1	1	*	*	Setting disabled		-	-

The MC2TA7402 has a 16-bit index register (IR); an 18-bit write-data register (WDR); and an 18-bit read-data register (RDR). The IR is a register to store index information from control registers and the internal DDRAM. The WDR is a register to temporarily store data to be written to control registers and the internal DDRAM. The RDR is a register to temporarily store data read from the DDRAM. Data from the MPU to be written to the internal DDRAM are first written to the WDR and then automatically written to the internal DDRAM in internal operation. Data are read through the RDR from the internal DDRAM. Therefore, invalid data are read out to the data bus when the MC2TA7402 reads the first data

Instructions can be written consecutively because the execution time of an instruction other than starting the oscillator is a 0-clock cycle.

Table 7-2: Register Selection (8/9/16/18-bit Parallel Interface)

80-system

NWR	NRD	RS	Operation
1	0	0	Read an internal status
1	0	1	Read from the DDRAM through RDR.
0	1	0	Write an index to IR.
0	1	1	Write to control registers or the DDRAM through WDR.
1	1	-	Write/read operation is not performed.

68-system

NWR	NRD	RS	Operation
1	1	0	Read an internal status
1	1	1	Read from the DDRAM through RDR.
0	1	0	Write an index to IR.
0	1	1	Write to control registers or the DDRAM through WDR.
0	-	-	Write/read operation is not performed.

Table 7-3: NCS truth value table

NCS	Function
0	Data is written to/read from the DDRAM/registers. DDRAM address is updated.
1	Inhibit data write/read operation to the DDRAM/registers. DDRAM address is NOT updated.

Table 7-4: Register Selection (Serial Peripheral Interface)

Start bytes		Function
R/W	RS	
0	0	Write an index to IR
1	0	Read an internal status
0	1	Write to control registers and the DDRAM through WDR
1	1	Read from the DDRAM through RDR

7.2. RGB/VSYNC Interface

- The MC2TA7402 supports the RGB interface and the VSYNC interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, display data (D17-0) are written in synchronization with these signals according to the polarity of the enable signal (ENABLE) to prevent flicker on display while updating display data.
- In VSYNC interface mode, display operations are synchronized with the internal clock except executing frame synchronization, which is synchronized with the VSYNC signal. Display data are written to the internal DDRAM through the system interface.
- In this case, there are constraints in the speed and the method of writing data to the internal DDRAM. For details, see the "15. VSYNC Interface" and "16. RGB Interface" sections.
- The MC2TA7402 allows for switching between the RGB/VSYNC interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). All display data written through the RGB interface are written to the internal DDRAM to limit data transfers only to the occasions of updating data in order to reduce the power consumption required for moving picture display.

7.3. Address Counter (AC)

The address counter (AC) gives an address to the internal DDRAM. When the index of the register to set a DDRAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal DDRAM, the value in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set on the DDRAM.

7.4. Display Data RAM (DDRAM)

The DDRAM is graphics RAM that stores bit-pattern data of 87,120 bytes, using 18 bits per dot.

7.5. Grayscale Power Supply Voltage Generating Circuit

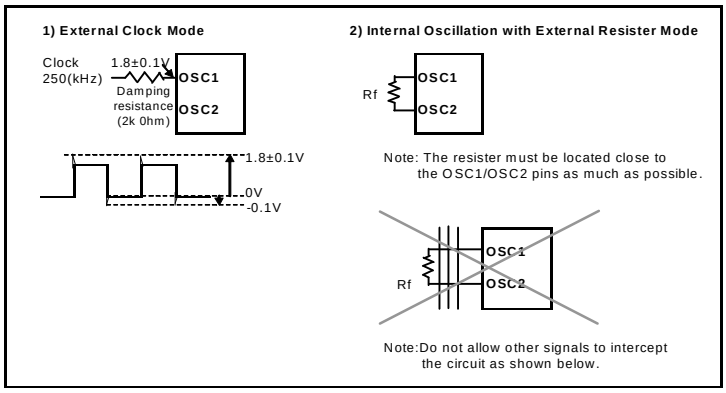
The grayscale voltage generating circuit generates a liquid crystal drive voltage according to the grayscale data set in the gamma-correction register to make 262,144 colors simultaneously available for the display. For details, see the "18. Gamma-Correction Function" section.

7.6. Timing Generator

The timing generator generates a timing signal for the operation of internal circuits such as the internal DDRAM. The timing for the display operation (DDRAM read operation, etc.) and the timing for the internal operation (access from the MPU, etc.) is generated in a way not to interfere each other.

7.7. OSCILLATION CIRCUIT (OSC)

The MC2TA7402 can provide RC oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pin. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulse can also be supplied externally. During standby mode, RC oscillation is halted to reduce power consumption. For details, see the"27. Oscillation Circuit" section.



7.8. LCD Driver Circuit

The LCD driver circuit is consisted of a source driver of S1 to S528 and a gate driver of G1 to G220.
Display pattern data are latched when data is input. The latched data control the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either a VGH or VGL level. The shift direction of source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for the LCD module.

7.9. LCD Drive Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels VGH, VGL, VCOMH/L and VREG1OUT for driving a LCD panel.

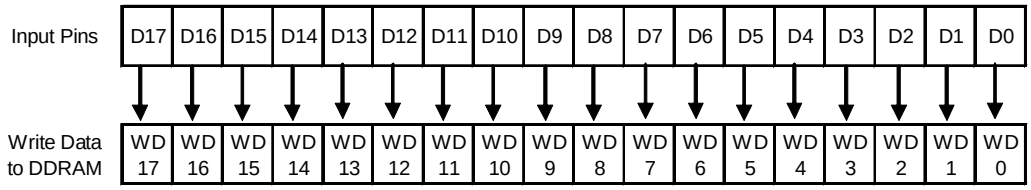
8. DDRAM Access

8.1. Write data to DDRAM

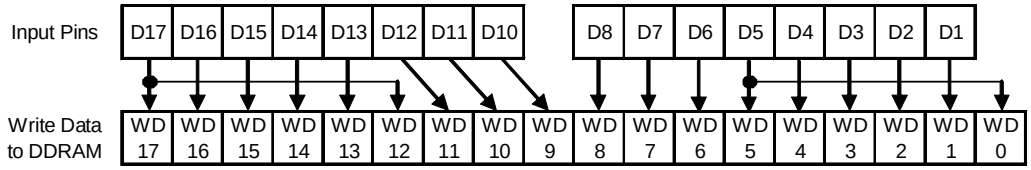
8.1.1. System Interface

The following figures show relation between input pins and DDRAM write for system interface.

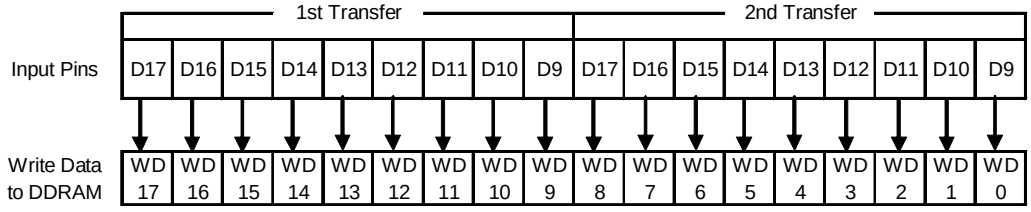
80-/68-System 18-bit Interface (262,144 colors)



80-/68-System 16-bit Interface (65,536 colors) **(R03h;TRI = "0", DFM1-0 = don't care)**



80-/68-System 9-bit Interface (2 transfers/pixel, 262,144 colors)



80-/68-System 8-bit Interface (2 transfers/pixel, 65,536 colors) **(R03h;TRI="0", DFM1-0=don't c**

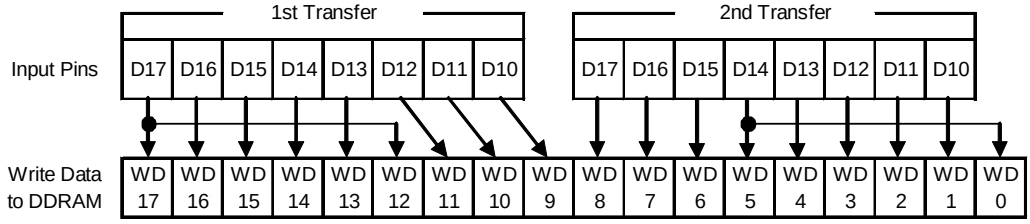
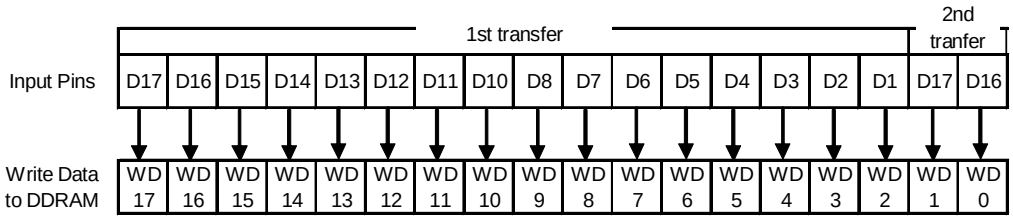
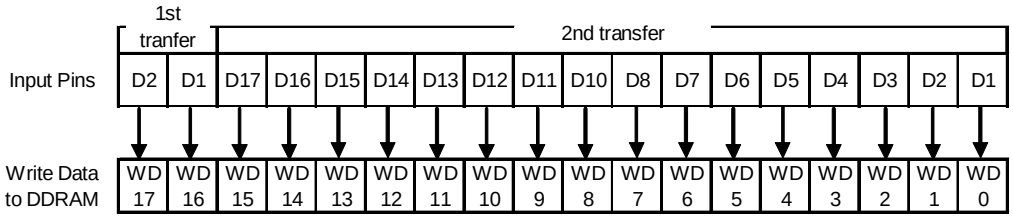


Figure 8-1: Input pins and DDRAM write (System Interface) -1

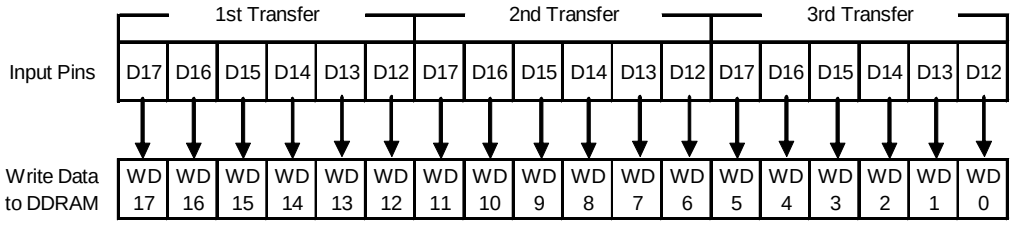
80-System 16-bit Interface (2 transfers/pixel, 262,144 colors) **(R03h;TRI = "1", DFM1-0 = "10")**



80-System 16-bit Interface (2 transfers/pixel, 262,144 colors) **(R03h;TRI = "1", DFM1-0 = "11")**



80-System 8-bit Interface (3 transfers/pixel, 262,144 colors) **(R03h;TRI="1", DFM1-0="10")**



80-System 8-bit Interface (3 transfers/pixel, 65,536 colors) **(R03h;TRI="1", DFM1-0="11")**

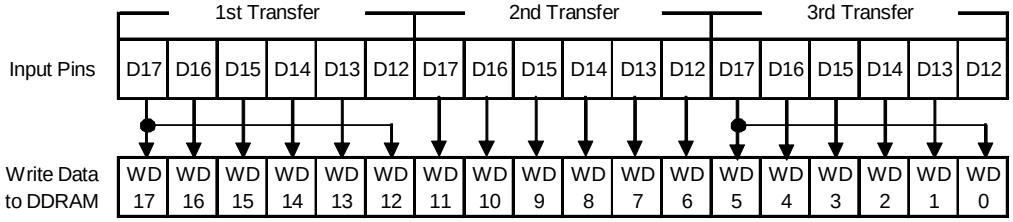


Figure 8-2: Input pins and DDRAM write (System Interface) -2

8.1.2. Serial Peripheral Interface (SPI)

The following figures show relation between input pins and DDRAM write for serial peripheral interface (SPI).

SPI (2 transfers/pixel, 65,536 colors) **(R03h;TRI = "0", DFM1-0 = don't care)**

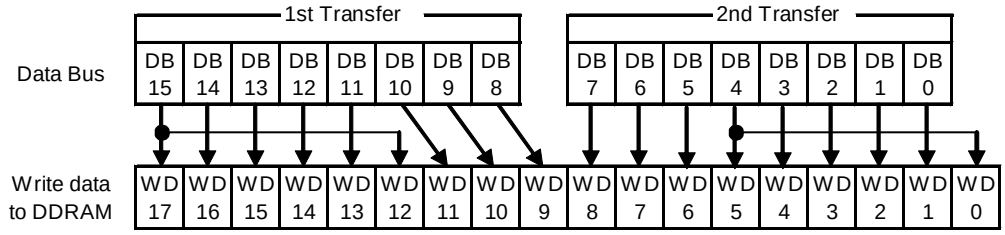
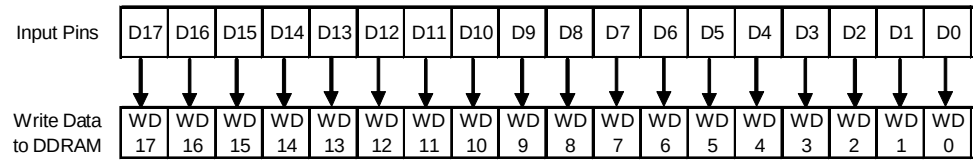


Figure 8-3: Input pins and DDRAM write (Serial Peripheral Interface (SPI))

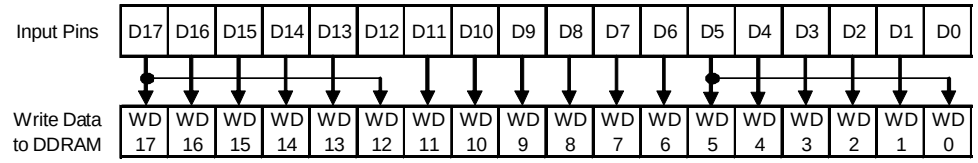
8.1.3. RGB Interface

The following figures show relation between input pins and DDRAM write for RGB interface.

18-bit RGB Interface (262,144 colors)



16-bit RGB Interface (65,536 colors)



6-bit RGB Interface (3 transfers/pixel, 262,144 colors)

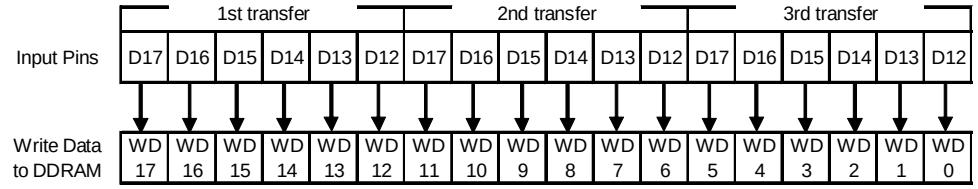
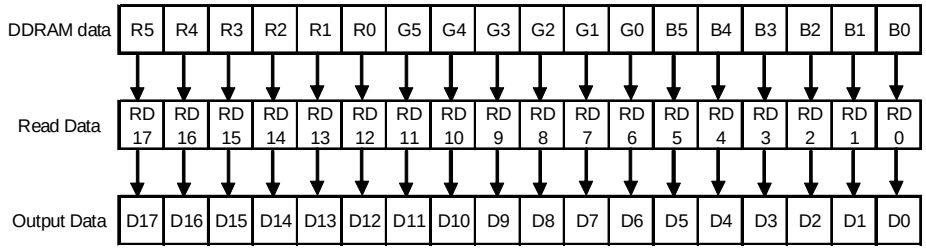


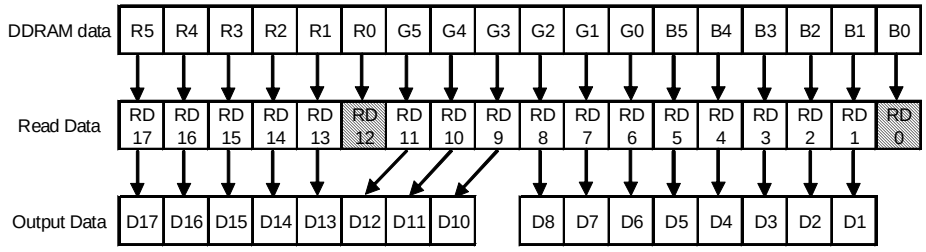
Figure 8-4: Input pins and DDRAM write (RGB Interface)

8.2. Read data from DDRAM

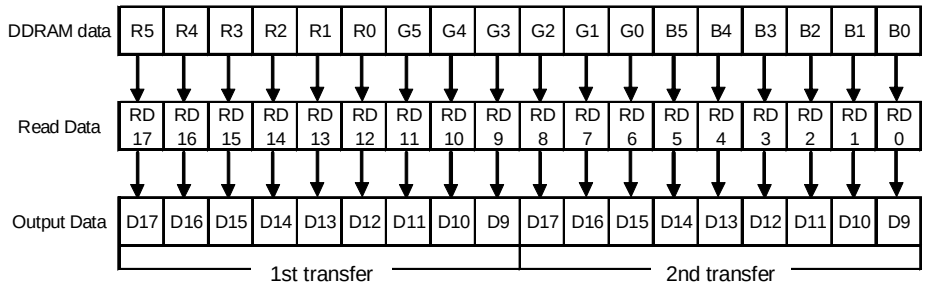
18-bit System Interface



16-bit System Interface



9-bit System Interface



8-bit System Interface / Serial Peripheral Interface (SPI)

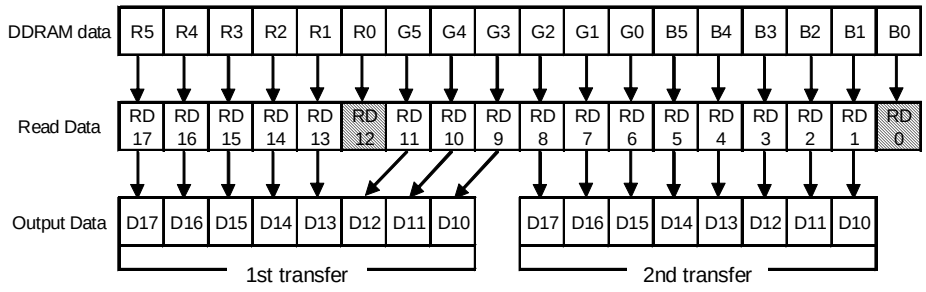


Figure 8-5: DDRAM data read (System Interface)

Note) Read data from DDRAM is not available in RGB interface mode.

9. DDRAM Address Map

9.1. DDRAM Address Map (SS="0")

Table 9-1: DDRAM address and display panel position (R01h;SS="0", R03h;BGR="0")

S/G pin		S1	S2	S3	S4	S5	S6	……	S523	S524	S525	S526	S527	S528
GS=0	GS=1	DB [17:12]	DB [11:6]	DB [5:0]	DB [17:12]	DB [11:6]	DB [5:0]	……	DB [17:12]	DB [11:6]	DB [5:0]	DB [17:12]	DB [11:6]	DB [5:0]
G1	G220	"0000"h			"0001"h			……	"00AE"h			"00AF"h		
G2	G219	"0100"h			"0101"h			……	"01AE"h			"01AF"h		
G3	G218	"0200"h			"0201"h			……	"02AE"h			"02AF"h		
G4	G217	"0300"h			"0301"h			……	"03AE"h			"03AF"h		
⋮		⋮			⋮			⋮	⋮			⋮		
G218	G3	"D900"h			"D901"h			……	"D9AE"h			"D9AF"h		
G219	G2	"DA00"h			"DA01"h			……	"DAAE"h			"DAAF"h		
G220	G1	"DB00"h			"DB01"h			……	"DBAE"h			"DBAF"h		

The upper 8 bits are for Y address and the lower 8 bits are for X address.

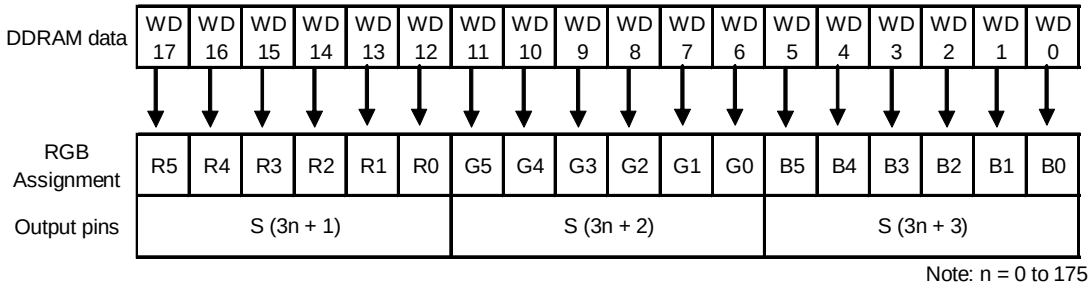


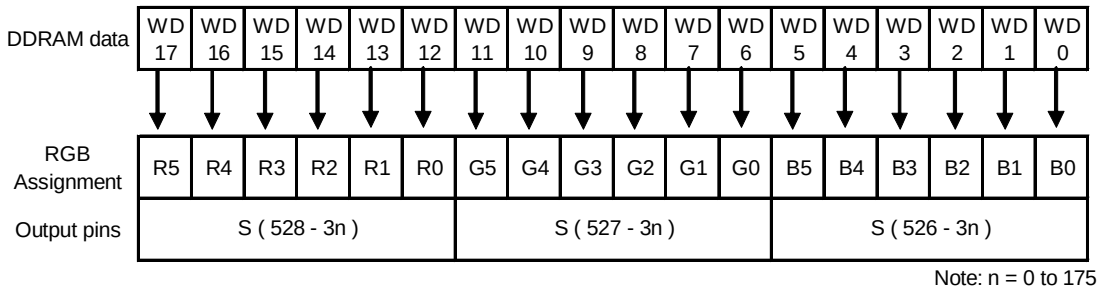
Figure 9-1: DDRAM address and display panel position (R01h;SS="0", R03h;BGR="0")

9.2. DDRAM Address Map (SS="1")

Table 9-2: DDRAM address and display panel position (R01h;SS="1", R03h;BGR="1")

S/G pin		S1	S2	S3	S4	S5	S6	……	S523	S524	S525	S526	S527	S528
GS=0	GS=1	DB [5:0]	DB [11:6]	DB [17:12]	DB [5:0]	DB [11:6]	DB [17:12]	……	DB [5:0]	DB [11:6]	DB [17:12]	DB [5:0]	DB [11:6]	DB [17:12]
G1	G220	"00AF"h			"00AE"h			……	"0001"h			"0000"h		
G2	G219	"01AF"h			"01AE"h			……	"0101"h			"0100"h		
G3	G218	"02AF"h			"02AE"h			……	"0201"h			"0200"h		
G4	G217	"03AF"h			"03AE"h			……	"0301"h			"0300"h		
⋮		⋮			⋮			⋮	⋮			⋮		
G218	G3	"D9AF"h			"D9AE"h			……	"D901"h			"D900"h		
G219	G2	"DAAF"h			"DAAE"h			……	"DA01"h			"DA00"h		
G220	G1	"DBAF"h			"DBAE"h			……	"DB01"h			"DB00"h		

The upper 8 bits are for Y address and the lower 8 bits are for X address.



Note: n = 0 to 175

Figure 9-2: DDRAM address and display panel position (R01h;SS="1", R03h;BGR="1")

10. Instructions

10.1. Outline

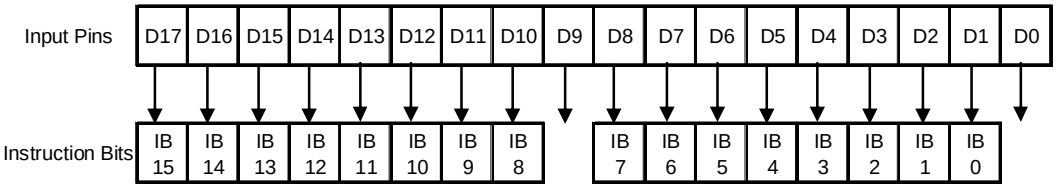
The MC2TA7402 adopts the 18-bit bus architecture to interface with a high-performance MPU. The MC2TA7402 starts internal processing after storing control information of externally sent 18-, 16-, 9-, 8-bit data in the index register (IR) and the data register (DR). Since internal operation of the MC2TA7402 is controlled by the signals sent from the MPU, the register selection signal (RS), the read/write signal (R/W), and the internal 16-bit data bus signals (IB15 to IB0) are called instructions. The MC2TA7402 access the internal DDRAM in units of 18 bits. The instructions of the MC2TA7402 are categorized into the following groups.

- Specify the index of register
- Read a status
- Display control
- Power management control
- Graphics data processing
- Set internal DDRAM address
- Transfer data to and from the internal DDRAM
- Internal grayscale gamma-correction

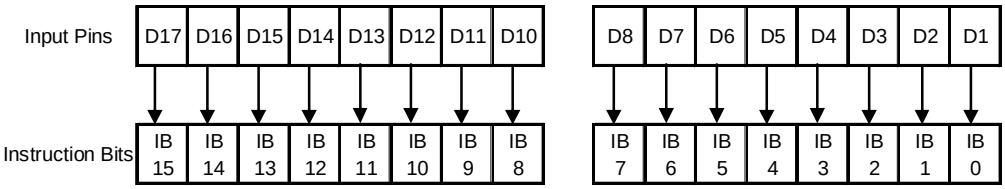
Normally, the instruction for writing data to the internal DDRAM is used most frequently. The DDRAM address in the address counter is updated automatically as data are written to the internal DDRAM, which, in combination with the window address function, contributes to minimizing data transfers., and thereby the load on the program run by the MPU. Since instructions are executed in a 0-cycle, it is possible to write instructions consecutively.

As the following figure shows, the way of assigning data to the 16 instruction bits (IB15-0) varies according to the interface. Set instructions in accordance with the following data transfer format.

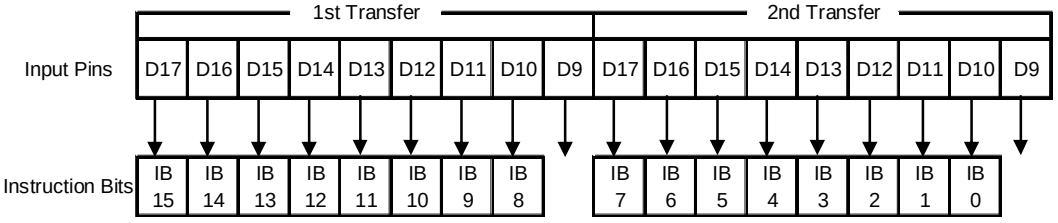
80-/68-System 18-bit Interface



80-/68-System 16-bit Interface



80-/68-System 9-bit Interface



80-/68-System 8-bit Interface/SPI (2 transfers)

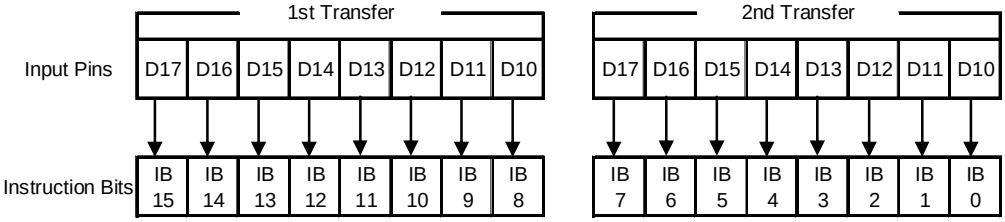


Figure 10-1: Instruction Bits (IB)

10.2. Explanation of each Instruction

The following are detailed explanations of instructions with illustrations of instruction bits (IB15-0) assigned to each interface.

10.2.1. Index (IR)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R00h to R50h) of a control register or DDRAM control to be accessed using binary numbers "000_0000" to "111_1111". The access to the register as well as instruction bits contained in it is prohibited unless its index is represented in this register.

10.2.2. Status Read (SR)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

The SR bits represent an internal status of the MC2TA7402.

L7-0: Indicate the position of the line that is currently driving liquid crystal.

10.2.3. Start Oscillation (R00h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
R	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	1	0

By setting IB0="1", the start oscillation instruction restarts the oscillator in a halt state in standby mode. After executing this instruction, wait at least 10 ms for stabilizing the oscillator before issuing the next instruction. For details, see the "25.2. Standby Mode" section.

The device code "7402"h is read out when reading out this register forcibly.

10.2.4. Driver Output Control (R01h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	0	VSPL	HSPL	DPL	EPL	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0

VSPL: Inverts the polarity of signals from the VSYNC pin.

VSPL = "0" : Low active.

VSPL = "1" : High active.

HSPL: Inverts the polarity of signals from the HSYNC pin.

HSPL = "0" : Low active.

HSPL = "1" : High active.

DPL: Inverts the polarity of signals from the DOTCLK pin.

DPL = "0" : Data are read on the rising edge of the DOTCLK.

DPL = "1" : Data are read on the falling edge of the DOTCLK.

EPL: Sets the polarity of the signal from the ENABLE pin in RGB interface mode.

EPL = "0" : ENABLE = "Low" / Write data to D17-0

: ENABLE = "High" / Inhibit data write operation

EPL ="1" : ENABLE = "Low" / Inhibit data write operation

: ENABLE = "High" / Write data to D17-0

Table 10-1:

EPL	ENABLE	DDRAM write	DDRAM address
0	L	Enabled	Updated
0	H	Inhibited	Retained
1	L	Inhibited	Retained
1	H	Enabled	Updated

SS: Selects the shift direction of the writing to DDRAM.

When SS="0", the writing direction to DDRAM is from "0000"h to "00AF"h.

When SS="1", the writing direction to DDRAM is from "00AF"h to "0000"h.

The combination of SS and R03h;BGR bits controls the order of assigning the RGB pixels .

When changing the SS or BGR (R03h) bit, DDRAM data must be rewritten.

Please refer to "9. DDRAM Address Map" section for more details.

SM: Sets the scan order by the gate driver.
Enables setting the scan order in accordance to the scan mode adopted in the module.

GS: Sets the shift direction of outputs from the gate driver.
Enables setting the scan order in accordance to the scan mode adopted in the module.

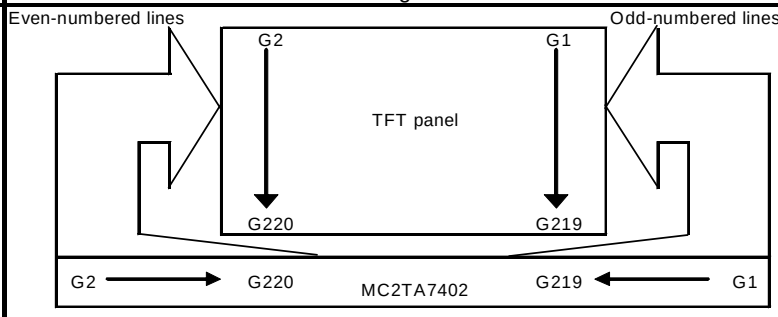
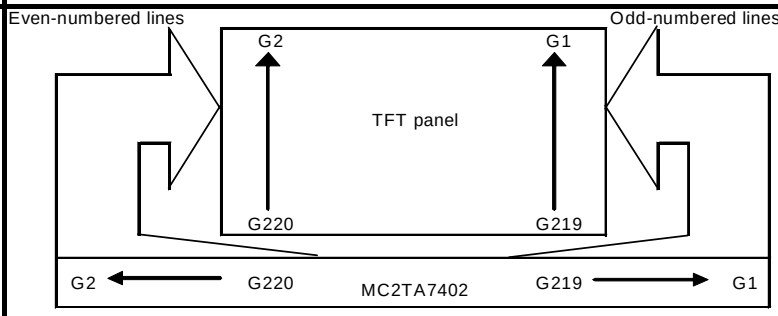
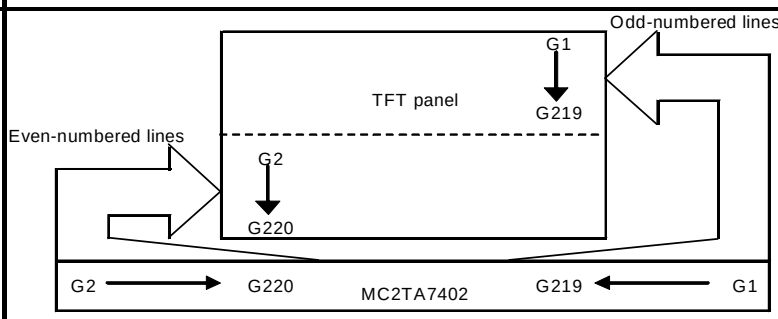
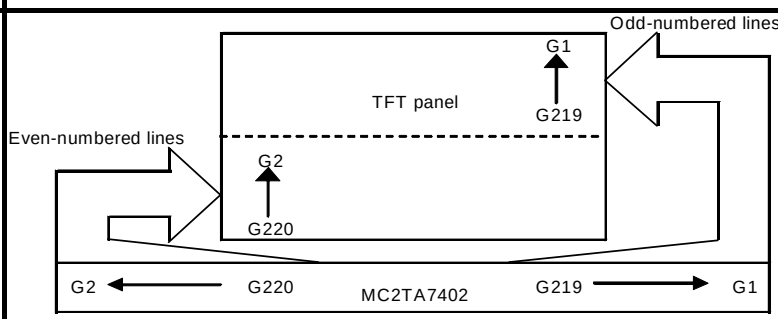
SM	GS	Scanning Direction	
0	0		G1, G2, G3, G4, ..., G218, G219, G220
0	1		G220, G219, G218, ..., G4, G3, G2, G1
1	0		G1, G3, G5, ..., G217, G219 G2, G4, G6, ..., G218, G220
1	1		G220, G218, G216, ...,G6, G4, G2 G219, G217, G215, ..., G5, G3, G1

Figure 10-2: Scan direction (SM, GS bit)

NL4-0: Sets the number of gate lines for driving liquid crystal at an interval of 8 lines as the following table shows. The number of gate lines set with the NL4-0 bits does not affect the DDRAM address mapping. Select the number of gate lines that is equal to or more than that of the panel in use.

Table 10-2: The number of drive gate line setting (NL4-0 bits)

NL4	NL3	NL2	NL1	NL0	Display Size	Lines	Driven gate lines
0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	1	528 x 16	16	G1 to G16
0	0	0	1	0	528 x 24	24	G1 to G24
0	0	0	1	1	528 x 32	32	G1 to G32
0	0	1	0	0	528 x 40	40	G1 to G40
0	0	1	0	1	528 x 48	48	G1 to G48
0	0	1	1	0	528 x 56	56	G1 to G56
0	0	1	1	1	528 x 64	64	G1 to G64
0	1	0	0	0	528 x 72	72	G1 to G72
:					:	:	:
:					:	:	:
1	1	0	0	0	528 x 200	200	G1 to G200
1	1	0	0	1	528 x 208	208	G1 to G208
1	1	0	1	0	528 x 216	216	G1 to G216
1	1	0	1	1	528 x 220	220	G1 to G220

Note 1) A front porch period (set with the FP bits) and a back porch period (set with the BP bits) are inserted as a blank period before and after driving all gate lines.

10.2.5. LCD Driver AC Control (R02h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	0	0	0	0	0	0

FLD1-0: Set the number of fields for 3-field interlaced scan. See the "21.3. 3-interlaced Scan" section for details. The FLD bits are disabled in RGB/VSYNC interface mode. When using the RGB/VSYNC interface, set FLD10= "01".

B/C: When the MC2TA7402 is set to generate a field-inversion waveform (B/C = "0"), the polarity is inverted at an interval of frame. The MC2TA7402 inverts the polarity at an interval of n lines, when a C-pattern waveform is generated (B/C = "1") according to the NW5-0 and EOR bits. For details, see "21.2. 1 line Reversed AC Drive Function".

EOR: When EOR = "1", the polarity is inverted according to the result of the EOR (exclusive OR) operation, which is performed on a signal for selecting either odd or even frames and a signal for inverting polarity in units of n lines when the MC2TA7402 is set to generate a C-pattern waveform (B/C = "1"). This instruction is used when the number of gate lines for driving liquid crystal is at odds with the interval of n lines set for inverting the polarity. For details, see "21.2. 1 line Reversed AC Drive Function".

Table 10-3:

FLD1-0	B/C	EOR	NW5-0	Operation
00	x	x	x	Prohibited
01	0	x	000000	Frame Reversed AC driving
	1	0	000000	Prohibited
	1	1	000000	1-line Reversed AC driving
10	x	x	x	Prohibited
11	0	x	000000	3-field Interlaced driving
	1	0	000000	Prohibited
	1	1	000000	Prohibited

Note) x: set either “0” or “1”.

10.2.6. Entry Mode (R03h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	TRI	DFM1	DFM0	BGR	0	0	0	0	0	0	I/D1	I/D0	AM	0	0	0

TRI: Sets the data transfer mode when transferring data to the internal DDRAM in 16-bit system interface and 8-bit system interface. When not using these interface modes, make sure to set TRI = "0".

DFM1-0: Sets the data transfer mode when transferring data to the internal DDRAM when TRI = "1". Please refer to Table 10-4 and "8. DDRAM Access" section for more details.

Table 10-4:

Interface	TRI	DFM1	DFM0	Data Transfer	Colors
16-bit interface	0	x	x	16 bits x 1 time	65,536
	1	1	0	16bits x 2 times (16bits + 2bits)	262,144
	1	1	1	16bits x 2 times (2bits + 16bits)	262,144
	1	0	x	Prohibited	-
8-bit interface	0	x	x	8 bits x 2 time	65,536
	1	1	0	8bits x 3 times (6 / 6 / 6 bits)	262,144
	1	1	1	8bits x 3 times (5 / 6 / 5 bits)	65,536
	1	0	x	Prohibited	-
other interfaces	1	x	x	Prohibited	-

Note) x: don't care

BGR: Reverses the order of RGB dots to BGR when writing 18-/16-bit pixel data to the internal DDRAM. The combination of R01h;SS and R03h;BGR bits controls the order of assigning the RGB pixels . When changing the SS or BGR bit, DDRAM data must be rewritten.

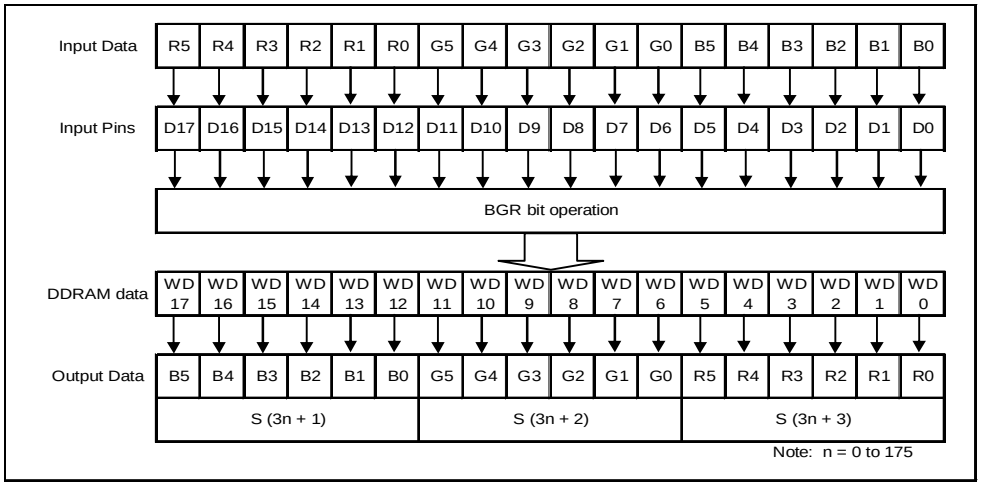
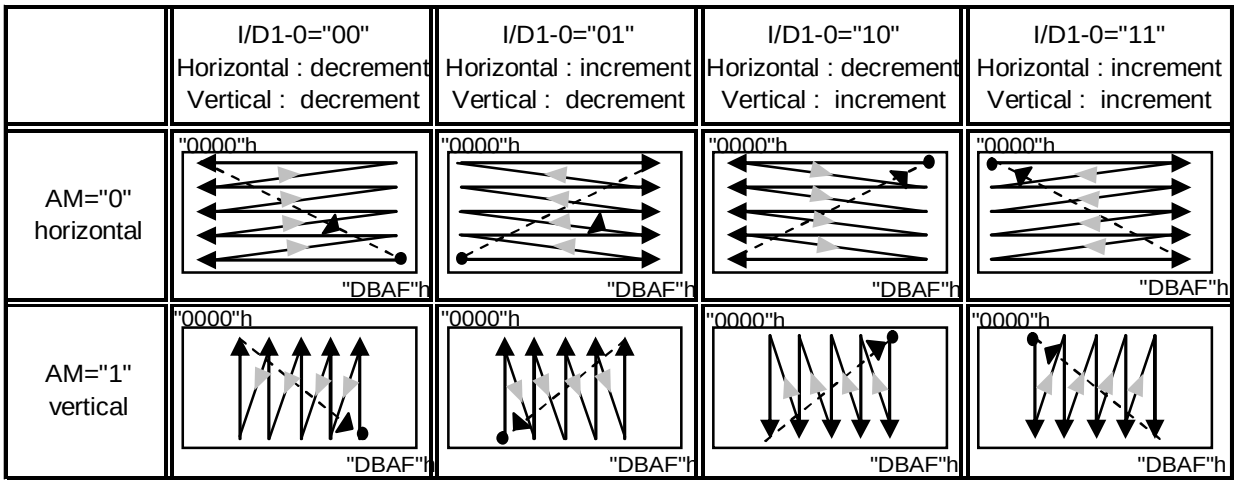


Figure 10-3: Example of BGR bit function (BGR = "1", SS = "0", 18-bit system interface)

I/D1-0: The address counter is automatically incremented by 1 as writing data to the internal DDRAM when I/D1,0 = "1". The address counter is automatically decremented by 1 as writing data to the internal DDRAM when I/D1,0 = "0". The increment/decrement can be set separately to each upper (AD15-8) / lower (AD7-0) byte of address. The transition direction of address (vertical/horizontal) when writing data to the internal DDRAM is set with the AM bit.

AM: Sets the direction of automatically updating address for writing data to the internal DDRAM in the address counter (AC). When AM = "0", the address is updated in the horizontal writing direction. When AM = "1", the address is updated in the vertical writing direction. When a window address area is set, data are written only to the DDRAM area specified with the window address in the writing direction set with I/D1-0 and AM bits.



Note: By making a window address area on the DDRAM, it is possible to limit the area for writing data.

Figure 10-4: Address transition directions

10.2.7. Display Control (1) (R07h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	0	GON	CL	REV	D1	D0

PT1-0: Sets the kind of source output in the non-display area in partial display mode.

For details, see the "20. Partial Display Function" section.

Table 10-5: Source, VCOM and Gate output in Non-display Area and Blank Period

PT1	PT0	Source Output		VCOM Output				Gate Output
				R09h; PTG2=0		R09h; PTG2=1		
		Positive	Negative	Positive	Negative	Positive	Negative	
0	0	VSS(GND level)	VSS(GND level)	VSS(GND level)	VSS(GND level)	Keep the final level of display area		R09h; PTG1-0 setting
0	1	V63	V0	VCOMH	VCOML			
1	0	V0	V63	VCOMH	VCOML			
1	1	Hi-Z	Hi-Z	VSS(GND level)	VSS(GND level)			

VLE2-1: When VLE1 = "1", the first display is scrolled in the vertical direction. When VLE2 = "1", the second display is scrolled in the vertical direction. The first and second displays cannot be scrolled simultaneously. This function is not available with the RGB interface and the VSYNC interface modes. In this case, set VLE2-1 = "00".

Table 10-6:

VLE2	VLE1	Image on 2nd screen	Image on 1st screen
0	0	Fixed	Fixed
0	1	Fixed	Scrolled
1	0	Scrolled	Fixed
1	1	Setting disabled	Setting disabled

SPT: When SPT="1", the LCD is driven in 2 split screens. For details, see the "20. Partial Display Function" section. This function is not available with the RGB/VSYNC interface. In this case, set SPT="0".

CL: When CL = "1", the 8-color display mode is selected. For details, see the "19. 8-Color Display Mode" section. The 8-color display mode is not available with the RGB interface and the VSYNC interface modes.

Table 10-7:

CL	Colors
0	260K/65K/4K
1	8

REV: Sets REV="1" for a normally-white panel and REV="0" for a normally-black panel.
By setting REV="1", the grayscale of an image can be inverted. This means, the REV bit allows both normally-black and normally-white panels to display an image from the same data. The source output level during front and back porch periods and a blank period in partial display mode is set with the R07h;PT1-0 bits.
Note) Normally-white panel: a panel with a white screen when no voltage is applied to the panel.
Normally-black panel: a panel with a black screen when no voltage is applied to the panel.

Table 10-8:

REV	DDRAM Data	Source Output in the Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000 to 18'h3FFFF	V63 to V0	V0 to V63
1	18'h00000 to 18'h3FFFF	V0 to V63	V63 to V0

GON: Sets the output level from gate lines as follows. When GON = "0", the VCOM level becomes VSS(GND level). Refer to Table 10-9.

D1-0: A graphics display appears on the screen when D1-0 = "11", and the screen displays a white or black color upon setting D1-0 = "10". In this case, the graphics display data are retained in the internal DDRAM and the display appears instantly on the screen upon setting D1 -0 to "11". When the D1 bit is "0", all source outputs are at the VSS(GND level).
In combination with the GON bit, the D1-0 bits controls ON/OFF of the graphics display. For details, see the flowcharts in the "25. Instruction Setting" section.

Table 10-9

GON	D1	D0	Gate Output	Source Output	VCOM Output	Internal display operation	Status
0	0	0	VGL	VSS(GND level)	VSS(GND level)	halt	Display Off
0	1	0	VGH	V63 / V0	VCOMH / VCOML	halt	Discharging panel charge
1	1	0	VGH / VGL	V63 / V0	VCOMH / VCOML	operate	Non-lit display (Note 2)
1	1	1	VGH / VGL	Normal Display	VCOMH / VCOML	operate	Displays images from DDRAM

Note 1) The data write operation to the DDRAM from the MPU is performed irrespective of the D1-0 bits.

Note 2) White is displayed on a normally-white panel. Black is displayed on a normally-black panel.

10.2.8. Display Control (2) (R08h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

FP3-0: Front porch, the blank period made at the beginning of a display.

BP3-0: Back porch, the blank period made at the end of a display.

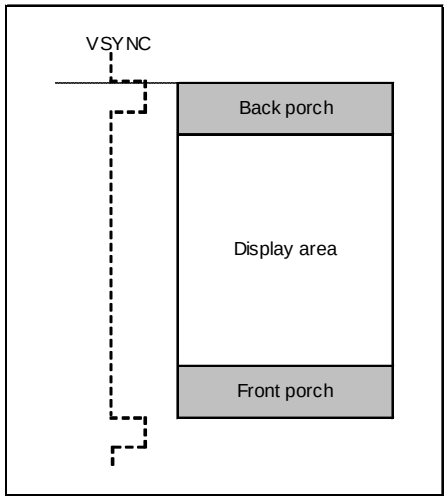
The FP3-0 and BP3-0 bits specify the number of lines for the front and back porch periods, respectively. In setting, make sure that the setting value follows the rules on Table 10-10 and 10-11.

Table 10-10:

FP3	FP2	FP1	FP0	Number of lines for the Front Porch
BP3	BP2	BP1	BP0	Number of lines for the Back Porch
0	0	0	0	Setting disabled
0	0	0	1	Setting disabled
0	0	1	0	2 lines
0	0	1	1	3 lines
0	1	0	0	4 lines
:	:	:	:	:
1	1	0	0	12 lines
1	1	0	1	13 lines
1	1	1	0	14 lines
1	1	1	1	Setting disabled

Table 10-11:

System interface	**R02h;FLD1-0 = "01"**	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines
	R02h;FLD1-0 = "11"	BP = 3 lines	FP = 5 lines	FP + BP + Blank Period = 16 lines
RGB interface		BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines
VSYNC interface		BP ≥ 2 lines	FP ≥ 2 lines	FP + BP=16 lines



In RGB/VSYNC interface mode, a back porch (BP) period starts on the falling edge of the VSYNC signal, followed by a display operation period. After the MC2TA7402 completes driving the number of lines set with the NL bits, a front porch period starts. After the front porch period, a blank period continues until the next input of the VSYNC signal.

Note) The output timing to the LCD is delayed by a 2-line period from the input of a synchronizing signal.

Figure 10-5: Back/Front porch BP3-0, FP3-0 Settings

10.2.9. Display Control (3) (R09h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	0	0	0	0	0	0	0	0	0	PTG2	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0

PTG2: Selects the VCOM operation in non-display area.

"0": VCOM operation at non-display area follows PT1-0.

"1": VCOM operation at non-display area keeps the final level.

Please refer to Figure 10-6.

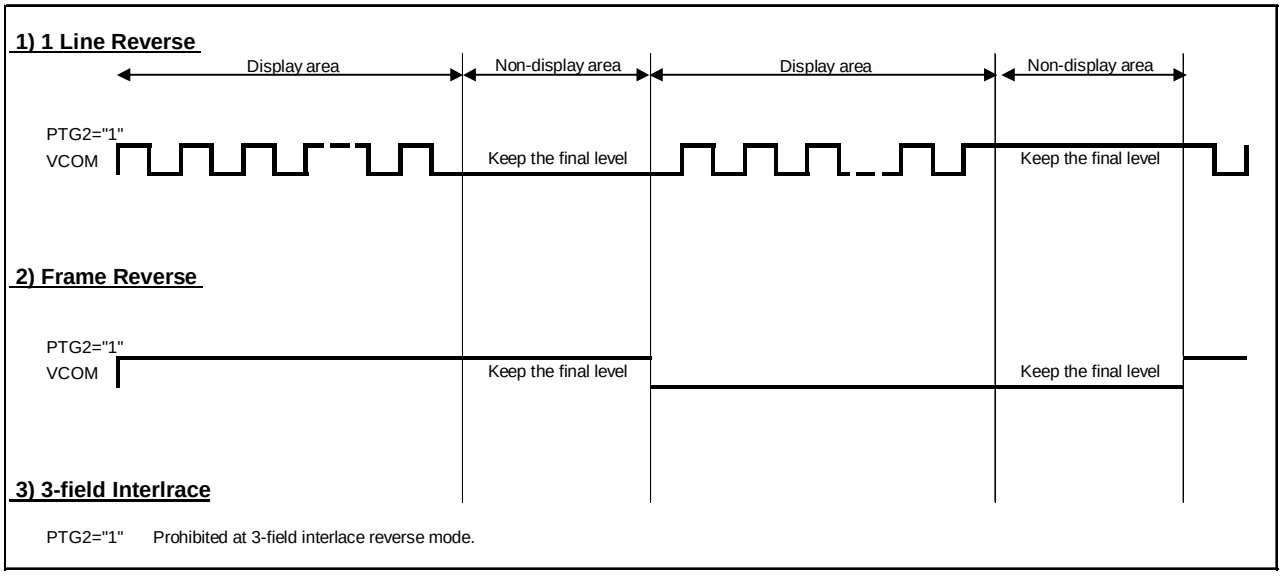


Figure 10-6: PTG2 bit operation

PTG1-0: Sets the scan mode by the gate driver in a non-display area.

Table 10-12: Source, VCOM and Gate output in Non-display Area and Blank Period

PTG1	PTG0	Gate output	Source output	VCOM output
0	0	Normal scan	R07h; PT1-0 setting	
0	1	VGL (Fixed)		
1	0	Interval scan		
1	1	Setting disabled	-	

ISC3-0: Sets the scan cycle by the gate driver when the PTG1-0 bits are set to the interval scan mode in a non-display area. The scan cycle can be set in units of n frames, where n is an odd number from 0 to 31. In this case, the polarity is inverted as gate lines are scanned.

Table 10-13

ISC3	ISC2	ISC1	ISC0	Interval period	Frame Frequency (in 60Hz)
0	0	0	0	0 frame	-
0	0	0	1	3 frames	50 ms
0	0	1	0	5 frames	84 ms
0	0	1	1	7 frames	117 ms
0	1	0	0	9 frames	150 ms
0	1	0	1	11 frames	184 ms
0	1	1	0	13 frames	217 ms
0	1	1	1	15 frames	251 ms
1	0	0	0	17 frames	284 ms
1	0	0	1	19 frames	317 ms
1	0	1	0	21 frames	351 ms
1	0	1	1	23 frames	384 ms
1	1	0	0	25 frames	418 ms
1	1	0	1	27 frames	451 ms
1	1	1	0	29 frames	484 ms
1	1	1	1	31 frames	518 ms

10.2.10. Frame Cycle Adjustment (R0Bh)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	NO1	NO0	SDT1	SDT0	ECS2	ECS1	ECS0	DIV1	DIV0	0	DCR_EX	DCR2	DCR1	DCR0	RTN1	RTN0

NO1-0: Sets non-overlap period for gate output.

Table 10-14:

NO1	NO0	Non-overlap period	
		System I/F Operation VSYNC I/F Operation (Reference clock: internal oscillator)	RGB I/F Operation (reference clock: DOTCLK)
0	0	2 clocks	16 clocks
0	1	4 clocks	32 clocks
1	0	6 clocks	48 clocks
1	1	8 clocks	64 clocks

Note 1) The non-overlap period is measured from the falling edge of the CL1.

SDT1-0: Sets the delay time of the source output timing from the falling edge of the gate output timing.

Table 10-15:

SDT1	SDT0	Source output delay period	
		System I/F Operation VSYNC I/F Operation (reference clock: internal oscillator)	RGB I/F Operation (reference clock: DOTCLK)
0	0	1 clock	8 clocks
0	1	2 clocks	16 clocks
1	0	3 clocks	24 clocks
1	1	4 clocks	32 clocks

ECS2-0: ECS period is sustained for the number of clock cycle which is set on ECS2-0. ECS function can be use only when VCOML is 0V(GND level).

Table 10-16:

ECS2	ECS1	ECS0	Equalizing Period	
			System I/F Operation VSYNC I/F Operation (reference clock: internal oscillator)	RGB I/F Operation (reference clock: DOTCLK)
0	0	0	No ECS	No ECS
0	0	1	2 clocks	8 clocks
0	1	0	4 clocks	16 clocks
0	1	1	6 clocks	24 clocks
1	0	0	8 clocks	32 clocks
1	0	1	10 clocks	40 clocks
1	1	0	12 clocks	48 clocks
1	1	1	14 clocks	56 clocks

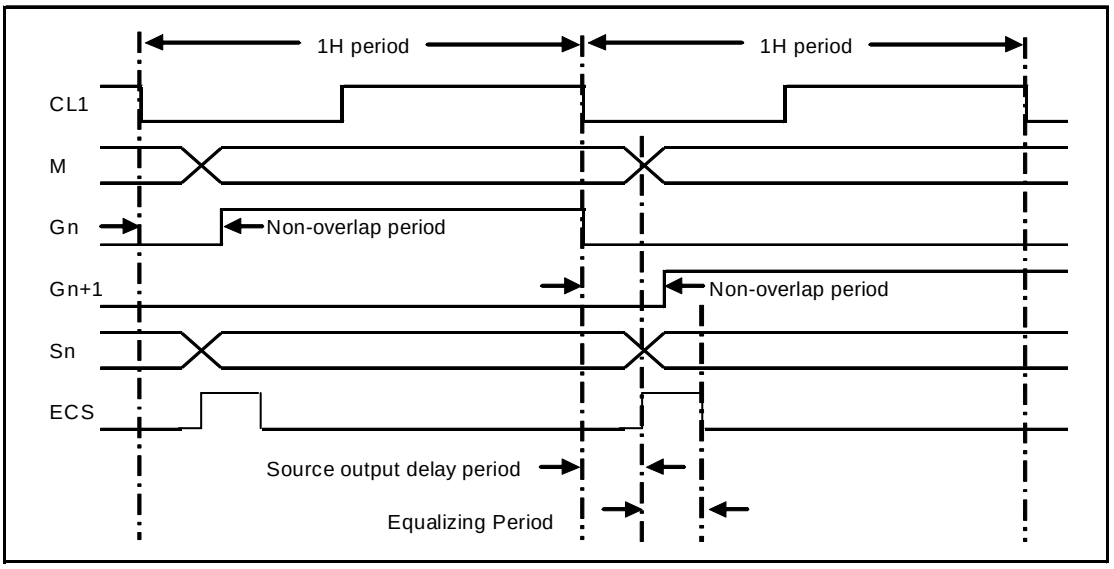


Figure 10-7: Non-overlap period of gate output, source output delay period and equalizing period

DIV1-0: The internal operation is synchronized with the clock divided by the division ratio, which is set with the DIV1-0 bits. Set the RTN and DIV bits to adjust the frame frequency. If the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. In RGB interface mode, the DIV1-0 bits are disabled.

Table 10-17:

DIV1	DIV0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

Note) fosc =Frequency of RC oscillation

$$\text{Frame frequency} = \frac{\text{fosc or DOTCLK}}{\text{Clock cycles per line x division ratio x (Line+BP+FP)}} \quad [\text{Hz}]$$

fosc: RC oscillation frequency (in the case of System interface or VSYNC interface)
DOTCLK: (in the case of RGB interface)
Clock cycles per line: R0Bh;RTN1-0 bits
Division ratio: R0Bh;DIV1-0 bits
Line: number of lines for driving liquid crystal (R01h;NL4-0 bits)
BP: R08h;BP3-0 bits, the number of lines for the back porch period
FP: R08h;FP3-0 bits, the number of lines for the front porch period

Figure 10-8: Formula for the frame frequency

DCR_EX: Input signal selection for external interface mode. ("0": internal operation clock, "1": DOTCLK)
Set DCR_EX bit for DOTCLK to be DCCLK (clock cycle for step-up circuits) source when external interface mode is in use (R0Ch;DM1-0 = "01").

DCR2-0: Set clock cycle for step-up circuits in external interface mode. Please set DCR_EX bit to "1" and DCR1-0 values when external interface is in use. In this case, DOTCLK must be input periodically and continuously.

Table 10-18:

DCR_EX	DCR2	DCR1	DCR0	Clock cycle for step-up circuits (DCCLK) in external interface mode
0	x	x	x	RTN1-0 setting
1	0	0	0	DOTCLK / 32
1	0	0	1	DOTCLK / 64
1	0	1	0	DOTCLK / 128
1	0	1	1	DOTCLK / 256
1	1	x	x	DOTCLK / 512

Note 1) If DOTCLK input cycle is variable or discontinuous, clock cycle for step-up circuits must be generated internally (DCR_EX ="0")
Note 2) x: don't care

RTN1-0: Set the 1H (1 line) period.

Table 10-19:

RTN1	RTN0	Horizontal clock frequency (CL1)	Clock frequency for step-up circuits (DCCLK)
0	0	INCLK / 16	fosc / 8
0	1	INCLK / 20	fosc / 10
1	0	INCLK / 24	fosc / 12
1	1	INCLK / 28	fosc / 14

10.2.11. RGB/VSYNC Interface (R0Ch)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

RM: Select the interface to access MC2TA7402's internal DDRAM. The DDRAM access is possible only via the interface selected with the RM bit. Set RM to "1" when writing display data via the RGB interface. The MC2TA7402 allows for setting the RM bit not constrained by the mode used for the display operation. This means it is possible to rewrite display data via the system interface by setting RM = "0" even while display operations are performed via the RGB interface.

Table 10-20: RM bit

RM	Interface for DDRAM Access
0	System interface / VSYNC interface
1	RGB interface

DM1-0: Select the display operation mode. The interface can be set based on the bits of DIM1-0.
This setting enables switching interface between internal operation and the external display interface.
Switching between two external display interface (RGB interface and VSYNC interface) should not be done.

Table 10-21: DM1-0 bits

DM1	DM0	Display Operation Mode	Clock for Display Operation
0	0	Internal clock operation (fosc)	fosc
0	1	RGB interface (DOTCLK)	DOTCLK
1	0	VSYNC interface (fosc)	fosc
1	1	Setting disabled	-

RIM1-0: Select RGB interface modes when the RGB interface mode is selected with the RM and DM1-0 bits.
Make this setting before starting a display operation via the RGB display interface.
Do not make changes to the setting while the display operation is being performed.

Table 10-22: RIM1-0 bits

RIM1	RIM0	RGB interface mode
0	0	18-bit RGB interface (1 transfer / dot)
0	1	16-bit RGB interface (1 transfer / dot)
1	0	6-bit RGB interface (3 transfer / dot)
1	1	Setting disabled

Note 1) Instructions are set only through the system interface.
Note 2) Make sure that data transfers and the dot clock input are performed in units of RGB pixels in 6-bit RGB interface mode.

As the following table shows, the optimum interface for each display state is selected by setting the RGB/VSYNC interface mode.

Table 10-23: RGB / VSYNC interface mode

Display State	Operation Mode	DDRAM Access (RM)	Display Operation Mode (DM1-0)
Still pictures	System interface	System interface (RM = "0")	System interface (DM1-0 ="00")
Moving pictures	RGB interface (1)	RGB interface (RM = "1")	RGB interface (DM1-0 ="01")
Rewrite still picture area while displaying moving pictures	RGB interface (2)	System interface (RM = "0")	RGB interface (DM1-0 = "01")
Moving pictures	VSYNC interface	VSYNC interface (RM =" "0)	VSYNC interface (DM1-0 = "10")

Note 1) Instructions can only be set through the system interface.
Note 2) Switching between RGB-I/F and the VSYNC-I/F are prohibited.
Note 3) RGB-I/F mode (RIM1-0) should not be changed during the RGB I/F is in operation.
Note 4) See the "15. VSYNC Interface" and "16. RGB Interface" sections for the mode transition flowcharts.

System interface mode

All display operation is controlled by the internal clock signals generated by RC oscillation in this mode.
None of inputs through the RGB/VSYNC interface are valid. The internal DDRAM is accessible only through the system interface.

RGB interface mode (1)

In RGB interface mode, display operation is controlled by the vertical synchronizing signal (VSYNC), the horizontal synchronizing signal (HSYNC), and the dot clocks (DOTCLK) in RGB interface mode. These signals must be supplied through a display period using the RGB interface.

Display data are transferred in units of pixels through the D17-0 pins. All display data are stored in the internal DDRAM. The window address function enables display of both the motion picture are and the internal DDRAM area simultaneously. In this method, data is only transferred when the screen is updated, which reduces the amount of data transferred.

The front porch (FP) and back porch (BP) periods, and the display duration period (NL) are automatically calculated in the MC2TA7402 by counting the number of horizontal synchronizing signal clocks (HSYNC) from the falling edge of the vertical synchronizing signal (VSYNC). Take this into consideration when transferring RGB data through the D17-0 pins.

RGB interface mode (2)

The MC2TA7402 enables rewriting DDRAM data via the system interface while the RGB interface is selected for display operation. In this case, make sure to write DDRAM data while display data are not being transferred via the RGB interface (ENABLE = High). To return to the display data transfer mode via the RGB interface, change the ENABLE first and then set a new address (R21h;AD15-0) in the address counter and the index register to "22"h.

VSYNC interface mode

In VSYNC interface mode, internal display operations are synchronized with the vertical synchronizing signal (VSYNC). In this mode, a moving picture can be displayed via the system interface by writing data to the internal DDRAM at a constant speed from the falling edge of the vertical synchronizing signal (VSYNC). In this case, there are constraints in the DDRAM writing speed and method. For details, see "15. VSYNC Interface".

No external signal input except the VSYNC inputs is accepted in VSYNC interface mode.

The timings and durations of the front porch (FP) and back porch (BP) periods and the display duration period (NL) are automatically calculated from the falling edge of the vertical synchronization signal (VSYNC) according to the instructions set in the relevant registers.

10.2.12. Power Control (1) (R10h)

10.2.13. Power Control (2) (R11h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	0	0	SAP2	SAP1	SAP0	BT2	BT1	BT0	DC2	DC1	DC0	0	0	0	SLP	STB
R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	0	0	GVD5	GVD4	GVD3	GVD2	GVD1	GVD0	0	0	0	0	0	VC2	VC1	VC0

SAP2-0: Adjust the constant current in the operational amplifier circuit for the source driver.

Setting a larger constant current stabilizes the operational amplifier circuit, but the current consumption also increases. Adjust the constant current taking the trade-off between the display quality and the current consumption into account. During a period showing no display, set R10h;SAP2-0 = "000" to halt the operational amplifier circuit for the source driver to reduce the current consumption.

Table 10-24: SAP2-0 bits

SAP2	SAP1	SAP0	Constant current in operational amplifier
0	0	0	Halt
0	0	1	small
0	1	0	medium low
0	1	1	medium
1	0	0	medium high
1	0	1	large
1	1	0	Setting disabled
1	1	1	Setting disabled

BT3-0: Change the rate applied to the step-up circuits 2. Adjust the step-up rate according to the voltage in use. To reduce the current consumption, set a smaller step-up rate.

Table 10-25: BT2-0 bits

BT2	BT1	BT0	Step-up circuit 1 (DDVDH)	Step-up circuit 2		Step-up circuit 3 (VCL)
				(VGH)	(VGL)	
0	0	0	VCI1 x 2	VCI1 x 4	VCI1 x -3	VCI1x-1
0	0	1	VCI1 x 2	VCI1 x 4	VCI1 x -4	VCI1x-1
0	1	0	VCI1 x 2	VCI1 x 5	VCI1 x -3	VCI1x-1
0	1	1	VCI1 x 2	VCI1 x 5	VCI1 x -4	VCI1x-1
1	0	0	VCI1 x 2	VCI1 x 5	VCI1 x -5	VCI1x-1
1	0	1	VCI1 x 2	VCI1 x 6	VCI1 x -3	VCI1x-1
1	1	0	VCI1 x 2	VCI1 x 6	VCI1 x -4	VCI1x-1
1	1	1	VCI1 x 2	VCI1 x 6	VCI1 x -5	VCI1x-1

Note 1) When using the DDVDH, VCL, VGH and VGL voltage levels, connect a capacitor to each connection pins.

Note 2) Set the following voltages within the limits:

- DDVDH = max. 5.5V,
- VCL = min. –3.3V,
- VGH = max. 16.5V,
- VGL = min. – 16.5V.
- VGH-VGL< 27.5V

DC2-0: Select the operating frequency of the step-up circuits. A higher step-up operating frequency enhances the driving capacity of the step-up circuit and the quality of display. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

Table 10-26: DC2-0 bits

DC2	DC1	DC0	Step-up circuit 1, 3 step-up frequency (fDCDC1/3)	Step-up circuit 2 step-up frequency (fDCDC2)
0	0	0	DCCLK / 1	DCCLK / 1
0	0	1	DCCLK / 1	DCCLK / 2
0	1	0	DCCLK / 1	DCCLK / 4
0	1	1	DCCLK / 2	DCCLK / 2
1	0	0	DCCLK / 2	DCCLK / 4
1	0	1	DCCLK / 4	DCCLK / 4
1	1	0	DCCLK / 4	DCCLK / 8
1	1	1	DCCLK / 4	DCCLK / 16

Note) DCCLK is clock frequency for step-up circuits.

SLP: When SLP = "1", the MC2TA7402 enters the sleep mode. In sleep mode, display operations are halted except for RC oscillation, thus reducing current consumption. During the sleep mode, the DDRAM data cannot be updated. Register set-up is maintained.

STB: When STB = "1", the MC2TA7402 enters the standby mode. In standby mode, display operations are completely halted, and all internal operations including internal RC oscillation are also halted. During standby mode, only the following instructions are accepted.

- to exit standby mode (R10h;STB="0")
- to start the oscillator (R00h)

The DDRAM data and instruction sets are susceptible to destruction and must be set again after exiting from the standby mode.

Table 10-27: Standby Mode

Level	Condition
VCOM	VSS(GND level)
Gate output	VGL
Source output	VSS(GND level)

VC2-0: Set the rate applied to VCILVL to generate a reference voltage for the VCI1 level.

Table 10-28: VC2-0 bits

VC2	VC1	VC0	VCI1 output voltage
0	0	0	0.68 x VCILVL
0	0	1	0.73 x VCILVL
0	1	0	0.83 x VCILVL
0	1	1	0.92 x VCILVL
1	0	0	1.00 x VCILVL
1	0	1	Setting disabled
1	1	0	Setting disabled
1	1	1	Setting disabled

Note: VCILVL = VCI. **Don't set any higher VCI1 level than 2.75V.**

GVD5-0: Select the VREG1OUT used for source of a gamma circuit. It allows to be amplified from 3.0V to 5.5V.

Formula: (2.0 / 63 x [GVD5-0] + 3) x VCILVL / 2.8

Table 10-29: VREG1OUT voltage (VCI=VCILVL=2.8V)

GVD5	GVD4	GVD3	GVD2	GVD1	GVD0	VREG1OUT voltage
0	0	0	0	0	0	3.00 V
0	0	0	0	0	1	3.03 V
0	0	0	0	1	0	3.06 V
0	0	0	0	1	1	3.09 V
0	0	0	1	0	0	3.12 V
0	0	0	1	0	1	3.16 V
0	0	0	1	1	0	3.19 V
0	0	0	1	1	1	3.22 V
0	0	1	0	0	0	3.25 V
0	0	1	0	0	1	3.28 V
0	0	1	0	1	0	3.31 V
0	0	1	0	1	1	3.35 V
0	0	1	1	0	0	3.38 V
0	0	1	1	0	1	3.41 V
0	0	1	1	1	0	3.44 V
0	0	1	1	1	1	3.47 V
0	1	0	0	0	0	3.51 V
0	1	0	0	0	1	3.54 V
0	1	0	0	1	0	3.57 V
0	1	0	0	1	1	3.60 V
0	1	0	1	0	0	3.63 V
0	1	0	1	0	1	3.66 V
0	1	0	1	1	0	3.70 V
0	1	0	1	1	1	3.73 V
0	1	1	0	0	0	3.76 V
0	1	1	0	0	1	3.79 V
0	1	1	0	1	0	3.82 V
0	1	1	0	1	1	3.86 V
0	1	1	1	0	0	3.89 V
0	1	1	1	0	1	3.92 V
0	1	1	1	1	0	3.95 V
0	1	1	1	1	1	3.98 V

GVD5	GVD4	GVD3	GVD2	GVD1	GVD0	VREG1OUT voltage
1	0	0	0	0	0	4.01 V
1	0	0	0	0	1	4.05 V
1	0	0	0	1	0	4.08 V
1	0	0	0	1	1	4.11 V
1	0	0	1	0	0	4.14 V
1	0	0	1	0	1	4.17 V
1	0	0	1	1	0	4.21 V
1	0	0	1	1	1	4.24 V
1	0	1	0	0	0	4.27 V
1	0	1	0	0	1	4.30 V
1	0	1	0	1	0	4.33 V
1	0	1	0	1	1	4.36 V
1	0	1	1	0	0	4.40 V
1	0	1	1	0	1	4.43 V
1	0	1	1	1	0	4.46 V
1	0	1	1	1	1	4.49 V
1	1	0	0	0	0	4.52 V
1	1	0	0	0	1	4.56 V
1	1	0	0	1	0	4.59 V
1	1	0	0	1	1	4.62 V
1	1	0	1	0	0	4.65 V
1	1	0	1	0	1	4.68 V
1	1	0	1	1	0	4.71 V
1	1	0	1	1	1	4.75 V
1	1	1	0	0	0	4.78 V
1	1	1	0	0	1	4.81 V
1	1	1	0	1	0	4.84 V
1	1	1	0	1	1	4.87 V
1	1	1	1	0	0	4.91 V
1	1	1	1	0	1	4.94 V
1	1	1	1	1	0	4.97 V
1	1	1	1	1	1	5.00 V

10.2.14. Power Control (3) (R13h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	0	0	0	0	0	0	0	0	0	PON	PON1	AON	0	0	0	0

PON: This is an operational starting bit for the step-up circuit 1 and 3.

"0": Step-up circuits 1 and 3 --- Stop

"1": Step-up circuits 1 and 3 --- Operate

PON1: This is an operational starting bit for the step-up circuit 2.

"0": Step-up circuits 2 --- Stop

"1": Step-up circuits 2 --- Operate

AON: This is an operational starting bit for Amplifier.

"0": Amplifier --- Stop

"1": Amplifier --- Operate

10.2.15. Power Control (4) (R14h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	0	VCMR	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	0	0	VML5	VML4	VML3	VML2	VML1	VML0

VCMR: "0": VCOMH is adjusted by VCM5-0 register.

VCOMR pin is used for monitoring the input voltage of the AMP which makes the VCOMH voltage.

"1": VCOMH voltage is adjusted by VCOMR voltage and VCM5-0 register setting is ignored.

VCOMR voltage is externally supplied. VCOMH = 2.5 x VCOMR

VCM5-0: Select the VCOMH voltage. **Formula: (2.0 / 63 x [VCM5-0] + 3) x VCILVL / 2.8**

Table 10-30: VCM5-0 bits (VCI=VCILVL=2.8V)

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH voltage
0	0	0	0	0	0	3.000V
0	0	0	0	0	1	3.032 V
0	0	0	0	1	0	3.063 V
0	0	0	0	1	1	3.095 V
0	0	0	1	0	0	3.127 V
0	0	0	1	0	1	3.159 V
0	0	0	1	1	0	3.190 V
0	0	0	1	1	1	3.222 V
0	0	1	0	0	0	3.254 V
0	0	1	0	0	1	3.286 V
0	0	1	0	1	0	3.317 V
0	0	1	0	1	1	3.349 V
0	0	1	1	0	0	3.381 V
0	0	1	1	0	1	3.413 V
0	0	1	1	1	0	3.444 V
0	0	1	1	1	1	3.476 V
0	1	0	0	0	0	3.508 V
0	1	0	0	0	1	3.540 V
0	1	0	0	1	0	3.571 V
0	1	0	0	1	1	3.603 V
0	1	0	1	0	0	3.635 V
0	1	0	1	0	1	3.667 V
0	1	0	1	1	0	3.698 V
0	1	0	1	1	1	3.730 V
0	1	1	0	0	0	3.762 V
0	1	1	0	0	1	3.794 V
0	1	1	0	1	0	3.825 V
0	1	1	0	1	1	3.857 V
0	1	1	1	0	0	3.889 V
0	1	1	1	0	1	3.921 V
0	1	1	1	1	0	3.952 V
0	1	1	1	1	1	3.984 V

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH voltage
1	0	0	0	0	0	4.016 V
1	0	0	0	0	1	4.048 V
1	0	0	0	1	0	4.079 V
1	0	0	0	1	1	4.111 V
1	0	0	1	0	0	4.143 V
1	0	0	1	0	1	4.175 V
1	0	0	1	1	0	4.206 V
1	0	0	1	1	1	4.238 V
1	0	1	0	0	0	4.270 V
1	0	1	0	0	1	4.302 V
1	0	1	0	1	0	4.333 V
1	0	1	0	1	1	4.365 V
1	0	1	1	0	0	4.397 V
1	0	1	1	0	1	4.429 V
1	0	1	1	1	0	4.460 V
1	0	1	1	1	1	4.492 V
1	1	0	0	0	0	4.524 V
1	1	0	0	0	1	4.556 V
1	1	0	0	1	0	4.587 V
1	1	0	0	1	1	4.619 V
1	1	0	1	0	0	4.651 V
1	1	0	1	0	1	4.683 V
1	1	0	1	1	0	4.714 V
1	1	0	1	1	1	4.746 V
1	1	1	0	0	0	4.778 V
1	1	1	0	0	1	4.810 V
1	1	1	0	1	0	4.841 V
1	1	1	0	1	1	4.873 V
1	1	1	1	0	0	4.905 V
1	1	1	1	0	1	4.937 V
1	1	1	1	1	0	4.968 V
1	1	1	1	1	1	5.000V

VML5-0: Select amplitude of VCOM voltage.

VCOML voltage is automatically adjusted by VCOM voltage and amplitude of VCOM voltage.

Formula:((2.4/63) x [VML5-0] + 3.6) x VCILVL / 2.8

Table 10-31: VML5-0 bits (VCI=VCILVL=2.8V)

VML5	VML4	VML3	VML2	VML1	VML0	amplitude of VCOM
0	0	0	0	0	0	3.600
0	0	0	0	0	1	3.638
0	0	0	0	1	0	3.676
0	0	0	0	1	1	3.714
0	0	0	1	0	0	3.752
0	0	0	1	0	1	3.790
0	0	0	1	1	0	3.829
0	0	0	1	1	1	3.867
0	0	1	0	0	0	3.905
0	0	1	0	0	1	3.943
0	0	1	0	1	0	3.981
0	0	1	0	1	1	4.019
0	0	1	1	0	0	4.057
0	0	1	1	0	1	4.095
0	0	1	1	1	0	4.133
0	0	1	1	1	1	4.171
0	1	0	0	0	0	4.210
0	1	0	0	0	1	4.248
0	1	0	0	1	0	4.286
0	1	0	0	1	1	4.324
0	1	0	1	0	0	4.362
0	1	0	1	0	1	4.400
0	1	0	1	1	0	4.438
0	1	0	1	1	1	4.476
0	1	1	0	0	0	4.514
0	1	1	0	0	1	4.552
0	1	1	0	1	0	4.590
0	1	1	0	1	1	4.629
0	1	1	1	0	0	4.667
0	1	1	1	0	1	4.705
0	1	1	1	1	0	4.743
0	1	1	1	1	1	4.781

VML5	VML4	VML3	VML2	VML1	VML0	amplitude of VCOM
1	0	0	0	0	0	4.819
1	0	0	0	0	1	4.857
1	0	0	0	1	0	4.895
1	0	0	0	1	1	4.933
1	0	0	1	0	0	4.971
1	0	0	1	0	1	5.010
1	0	0	1	1	0	5.048
1	0	0	1	1	1	5.086
1	0	1	0	0	0	5.124
1	0	1	0	0	1	5.162
1	0	1	0	1	0	5.200
1	0	1	0	1	1	5.238
1	0	1	1	0	0	5.276
1	0	1	1	0	1	5.314
1	0	1	1	1	0	5.352
1	0	1	1	1	1	5.390
1	1	0	0	0	0	5.429
1	1	0	0	0	1	5.467
1	1	0	0	1	0	5.505
1	1	0	0	1	1	5.543
1	1	0	1	0	0	5.581
1	1	0	1	0	1	5.619
1	1	0	1	1	0	5.657
1	1	0	1	1	1	5.695
1	1	1	0	0	0	5.733
1	1	1	0	0	1	5.771
1	1	1	0	1	0	5.810
1	1	1	0	1	1	5.848
1	1	1	1	0	0	5.886
1	1	1	1	0	1	5.924
1	1	1	1	1	0	5.962
1	1	1	1	1	1	6.000

Note) Set VCOML range from -2.25 V to 1.0 V.

10.2.16. DDRAM Address Set (R21h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

AD15–0: DDRAM addresses that are set in the AC (Address Counter) initially. The address in the AC is automatically updated in accordance with the AM and I/D1-0 bits as data are written to the internal DDRAM so that data are written consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal DDRAM.

1. It is not possible to set an address in the AC when the MC2TA7402 is in standby.
2. Make sure to set an address that is within the window address area.
3. When setting the gate scan start position register (R40h), the DDRAM address must be initialized in the address counter (AC).

Note 1) When the RGB interface is selected (RM = "1"), the addresses AD15-0 are set in the address counter every frame on the falling edge of VSYNC.

Note 2) When the system interface mode or the VSYNC interface mode is selected (RM = "0"), the address AD15-0 are set when executing an instruction.

Table 10-32: DDRAM Address Range

AD15-0	DDRAM Setting
"0000"h - "00AF"h	Bitmap data for G1
"0100"h - "01AF"h	Bitmap data for G2
"0200"h - "02AF"h	Bitmap data for G3
"0300"h - "03AF"h	Bitmap data for G4
:	:
"D800"h - "D8AF"h	Bitmap data for G217
"D900"h - "D9AF"h	Bitmap data for G218
"DA00"h - "DAAF"h	Bitmap data for G219
"DB00"h - "DBAF"h	Bitmap data for G220

10.2.17. DDRAM Data Write (R22h)

R/W	RS	DDRAM write data (WD17-0). The D17-0 pin assignment vaires according to the interface in use (see below).																
		D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	WD 17	WD 16	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0
RGB-I/F mode:																			

WD17-0: If data are less than 18 bits in a unit, the MC2TA7402 expands the data into 18 bits internally before writing to the internal DDRAM.

The grayscale level is selected according to the DDRAM data. The DDRAM address is automatically updated according to the AM and I/D1-0 bits as data are written to the internal DDRAM. In standby mode, no access to the internal DDRAM is allowed. When the 8- or 16- bit interface mode is selected, data are expanded into 18 bits internally by writing the MSBs of R and B pixels to the LSBs of R and B pixels respectively.

When writing data to the DDRAM through a system interface while using the RGB interface, make sure to avoid conflicts between writing operations via respective interfaces (RGB and system interfaces). When the18-bit RGB interface is selected, 18-bit data are written through the D17-0 pins and 262,144 colors are available. When the 16-bit RGB interface is selected, the MSBs of R and B pixels are also written to the LSBs of R and B pixels respectively, and 65,536 colors are available. Please refer to “8.1 Write data to DDRAM” section for more details.

Table 10-33: DDRAM data and LCD output level (on a normally-white panel)

DDRAM data setting RGB	Grayscale	
	Positive	Negative
000000	V0	V63
000001	V1	V62
000010	V2	V61
000011	V3	V60
000100	V4	V59
000101	V5	V58
000110	V6	V57
000111	V7	V56
001000	V8	V55
001001	V9	V54
001010	V10	V53
001011	V11	V52
001100	V12	V51
001101	V13	V50
001110	V14	V49
001111	V15	V48
010000	V16	V47
010001	V17	V46
010010	V18	V45
010011	V19	V44
010100	V20	V43
010101	V21	V42
010110	V22	V41
010111	V23	V40
011000	V24	V39
011001	V25	V38
011010	V26	V37
011011	V27	V36
011100	V28	V35
011101	V29	V34
011110	V30	V33
011111	V31	V32

DDRAM data setting RGB	Grayscale	
	Positive	Negative
100000	V32	V31
100001	V33	V30
100010	V34	V29
100011	V35	V28
100100	V36	V27
100101	V37	V26
100110	V38	V25
100111	V39	V24
101000	V40	V23
101001	V41	V22
101010	V42	V21
101011	V43	V20
101100	V44	V19
101101	V45	V18
101110	V46	V17
101111	V47	V16
110000	V48	V15
110001	V49	V14
110010	V50	V13
110011	V51	V12
110100	V52	V11
110101	V53	V10
110110	V54	V9
110111	V55	V8
111000	V56	V7
111001	V57	V6
111010	V58	V5
111011	V59	V4
111100	V60	V3
111101	V61	V2
111110	V62	V1
111111	V63	V0

DDRAM Access through RGB-I/F and System I/F

In RGB interface mode, the MC2TA7402 stores all display data in the internal DDRAM, enabling transferring only moving picture data only when updating the frames of a moving picture.

While the moving picture frames are not updated, it is possible to write data displayed in the area outside the moving picture area via the system interface.

In RGB interface mode, the MC2TA7402 writes data to the internal DDRAM in synchronization with DOTCLK while ENABLE = "Low". To access the internal DDRAM through the system interface while using the RGB interface for display operation, set ENABLE "High" to stop writing through the RGB interface. To start accessing the internal DDRAM through the RGB interface after accessing the DDRAM through the system interface, wait at least for a write/read bus cycle time. Data will not be written properly to the internal DDRAM when the write operations both via the RGB and system interfaces are conflicting.

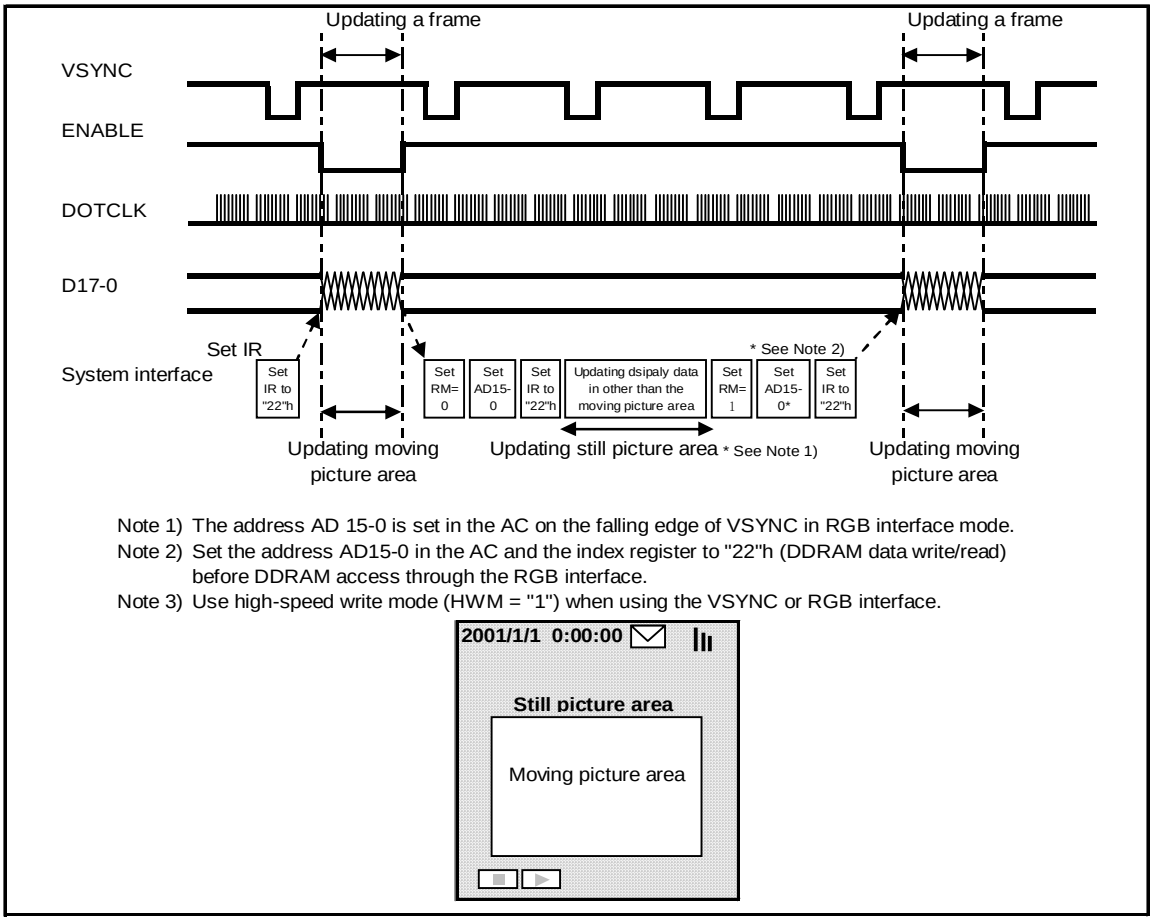


Figure 10-9: DDRAM Access through RGB-I/F and System I/F

10.2.18. DDRAM Data Read (R22h)

R/W	RS		DDRAM read data (RD17-0) The D17-0 pin assignment varies according to the interface in use.	
R	1			

RD17–0: Read 18-bit data from the DDRAM. The bit assignment between the data read out from the DDRAM and the D17-0 pins is different depending on the interface.

When data are read out from the DDRAM to the MPU, the first word that is read immediately after executing the DDRAM address set is taken into the internal read data latch and invalid data are sent to the data bus DB17-0. Valid data are sent to the data bus as the MC2TA7402 reads out the second word data from the internal DDRAM. When the 8- or 16-bit interface is selected, the LSBs of R and B pixels are not read out. Please refer to “8.2 Read data from DDRAM” section for more details.

Note) DDRAM read is not available with the RGB interface.

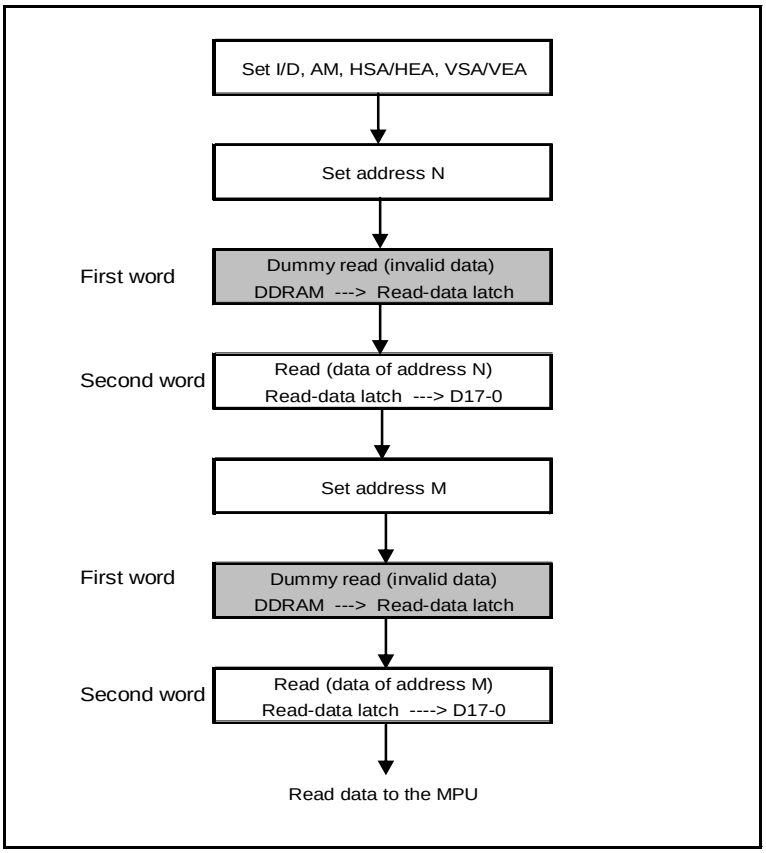


Figure 10-10: DDRAM read sequence

10.2.19. Gamma Control (R30h-R39h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
R30	W	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
R31	W	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
R32	W	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
R33	W	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
R34	W	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
R35	W	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
R36	W	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
R37	W	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
R38	W	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
R39	W	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

PKP5-0[2:0]: Gamma fine adjustment register bits for the positive polarity

PRP1-0[2:0]: Gamma gradient adjustment register bits for the positive polarity

PKN5-0[2:0]: Gamma fine adjustment register bits for the negative polarity

PRN1-0[2:0]: Gamma gradient adjustment register bits for the negative polarity

VRP0[3:0]/VRP1[4:0]: Amplitude adjustment register bits for the positive polarity

VRN0[3:0]/VRN1[4:0]: Amplitude adjustment register bits for the negative polarity

For details, see the "18. Gamma Correction Function" section.

10.2.20. Gate Scan Start Position (R40h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SCN

SCN: The MC2TA7402 allows for specifying the gate line for scanning start position.

Table 10-34:

SCN	Scanning start position			
	SM=0,GS=0	**SM=,GS=1**	**SM=1,GS=0**	**SM=1,GS=1**
0	G1	G220	G1	G220
1	Setting Disable	Setting Disable	Setting Disable	Setting Disable

Note) Regarding to Scanning direction, please refer to p41.

10.2.21. Vertical Scroll Control (R41h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

VL7-0: Set the amount of scrolling an image on the screen in the vertical direction. The scrolling amount can be set from 0 to 220 lines. The start position for displaying the image is shifted vertically by the number of lines set with the VL7-0 bits. The part of the image that is scrolled out from the end line (the 220th line) as a result of scrolling is displayed from the 1st line of the physical display. The VL7-0 bits are enabled when either the first display vertical scroll enable bit R07h;VLE1, or the second display vertical scroll enable bit R07h;VLE2 is set to "1". When R07h;VLE2-1="00", the fixed line display is enabled.

The vertical scrolling function is not available with the RGB/VSYNC interface.

Table 10-35:

VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scrolling lines
0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	1	0	2 lines
:	:	:	:	:	:	:	:	:
1	1	0	1	1	0	1	0	218 lines
1	1	0	1	1	0	1	1	219 lines

Note: Do not set a value that represents more than 219 lines ("DB"h).

10.2.22. First Screen Drive Position (R42h)

10.2.23. Second Screen Drive Position (R43h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

SE17-10: Set the position of the end line where the first display ends.
When R01h;IB9=GS=0, the gate driver ends the scan at the line of the number set with (SE17-10 bits) + 1.
When R01h;IB9=GS=1, the gate driver ends the scan at the line of the number set with 220 - (SE17-10 bits).

SS17-10: Set the position of the start line where the first display starts.
When R01h;IB9=GS=0, the gate driver starts the scan from the line of the number set with (SS17-10 bits) + 1.
When R01h;IB9=GS=1, the gate driver starts the scan from the line of the number set with 220 -(SS17-10 bits).

For instance, when SS17-10 = "07"h and SE17-10 = "10"h, the first display is shown on the gate lines from G8 to G17, and gate lines G1 to G7 and G18 thereafter are driven to show a blank screen. Make sure that SS17-10 ≤ SE17-10 ≤ "DB"h (when GS=0). For details, see the "20. Partial Display Function" section.

SE27-20: Set the position of the end line where the second display ends.
The second display is shown when R07h;SPT = "1".
When R01h;IB9=GS=0, the gate driver ends the scan at the line of the number set with (SE27-20 bits) + 1.
When R01h;IB9=GS=1, the gate driver ends the scan at the line of the number set with 220 - (SE27-20 bits).

SS27-20: Set the position of the start line where the second display starts.
When R01h;IB9=GS=0, the gate driver starts the scan from the line of the number set with (SS27-20 bits) + 1.
When R01h;IB9=GS=1, the gate driver starts the scan from the line of the number set with 220 -(SS27-20 bits).

Make sure that SS17-10 ≤ SE17-10 < SS27-20 ≤ SE27-20 ≤ "DB"h (When GS=0).
For details, see the "20. Partial Display Function" section.

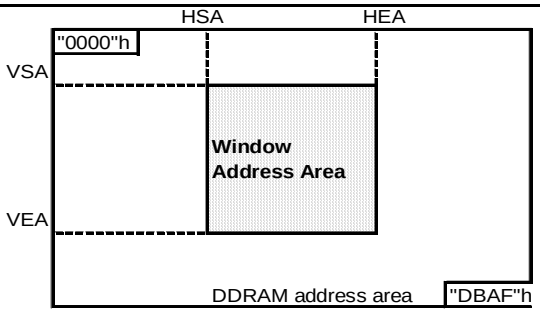
10.2.24. Horizontal DDRAM Address Position (R44h)

10.2.25. Vertical DDRAM Address Position (R45h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

HSA7-0/HEA7-0: HSA7-0 and HEA7-0 represent the respective addresses at the start and end of the window address area in the horizontal direction. By setting HSA and HEA bits, it is possible to limit the area on the DDRAM horizontally for writing data. The HSA and HEA bits must be set before starting the DDRAM write operation. In setting these bits, make sure "00"h ≤ HSA7-0≤ HEA7-0 ≤ "AF"h.

VSA7-0/VEA7-0: VSA7-0 and VEA7-0 represent the respective addresses at the start and end of the window address area in the vertical direction. By setting VSA and VEA bits, it is possible to limit the area on the DDRAM vertically for writing data. The VSA and VEA bits must be set before starting the DDRAM write operation. In setting, make sure "00"h ≤ VSA7-0 ≤ VEA7-0 ≤ "DB"h.



Note 1) Make a window address area within the DDRAM address area.
Note 2) Set a DDRAM start addresss within the window address area.
Note 3) When setting the DDRAM start address high-speed mode, set one within the window address area that includes the area for the dummy write operation.
Note 4) The DDRAM address register (R21h) must be set when the window address is specified.

If the setting of the R21h register is set out of the window address area, the DDRAM data write operation might not be performed.

Ex. When AM="0", I/D1-0="11"
It is set as: HSA7-0="10"h,
VSA7-0="22"h
Then the R21h;AD15-0 bits must be set as "2210"h.

Figure 10-11: DDRAM address and window address area

10.2.26. VCOMG Control (R53h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	XVCOMG

XVCOMG: When XCOMG=1, MC2TA7402 can output GND level for VCOM before display on operation, and GND level for VCOML during display on operation. (Make sure to set XVCOMG=1, if VCOM set to GND level before/after display on/off operation.)

When XVCOMG=0, MC2TA7402 can output a negative voltage for VCOM before display on operation, and a negative voltage for VCOML during display on operation.

10.2.27. VCOM EQ (R59h)

R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	ECV2	ECV1	ECV0

ECV2-0: When using VCOML< 0V, MC2TA7402 can be use VCOM EQ instead of ECS function for the low power consumption. Extend the period for the equalization mode than 1 clock for System, VCYNC I/F operation, or 8 clocks for RGB I/F operation mode. When using this function, M-pin must be connect to GND level.

Table 10-35:

ECV2	ECV1	ECV0	System I/F Operation VSNC I/F Operation (reference clock : Internal oscillator)	RGB I/F Operation (reference clock : DOTCLK)
0	0	0	No VCOM EQ	No VCOM EQ
0	0	1	1 clock	8 clocks
0	1	0	2 clocks	16 clocks
0	1	1	3 clocks	24 clocks
1	0	0	4 clocks	32 clocks
1	0	1	5 clocks	40 clocks
1	1	0	6 clocks	48 clocks
1	1	1	7 clocks	56clocks

10.2.28. STB Mode Selection(R5Ah)

STBM1-0: MC2TA7402 can select 2 kind of STB mode. One is the normal STB mode (STB current < 10uA). The other one is new STB mode (STB current is less than normal STB mode).

Table 10-36 :

STBM1	STBM0	VCI	Mode
0	0	2.5~3.3V	Normal STB
0	1	2.5~2.6V	New STB
1	0	2.6~3.1V	New STB
1	1	3.1~3.3V	New STB

11. Instruction List

Main Category		Sub Category		Upper code								Lower code							
Upper Index	Index		Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
-	index	-	Index	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status Read	-	Status Read	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
0*	Display Control	00h	Start Oscillation	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
			Device code Read	0	1	1	1	0	1	0	0	0	0	0	0	0	0	1	0
		01h	Driver Output Control	0	VSPL (0)	HSPL (0)	DPL (0)	EPL (0)	SM (0)	GS (0)	SS (0)	0	0	0	NL4 (1)	NL3 (1)	NL2 (0)	NL1 (1)	NL0 (1)
		02h	LCD Driver AC Control	0	0	0	0	FLD1 (0)	FLD0 (1)	B/C (0)	EOR (0)	0	0	0	0	0	0	0	0
		03h	Entry Mode	TRI (0)	DFM1 (0)	DFM0 (0)	BGR (0)	0	0	0	0	0	0	I/D1 (1)	I/D0 (1)	AM (0)	0	0	0
		07h	Display Control (1)	0	0	0	PT1 (0)	PT0 (0)	VLE2 (0)	VLE1 (0)	SPT (0)	0	0	0	GON (0)	CL (0)	REV (0)	D1 (0)	D0 (0)
		08h	Display Control (2)	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)
		09h	Display Control (3)	0	0	0	0	0	0	0	0	0	PTG2 (0)	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)
		0Bh	Frame Cycle Adjustment	NO1 (0)	NO0 (0)	SDT1 (0)	SDT0 (0)	ECS2 (0)	ECS1 (0)	ECS0 (0)	DIV1 (0)	DIV0 (0)	0	DCR_EX (0)	DCR2 (0)	DCR1 (0)	DCR0 (0)	RTN1 (0)	RTN0 (0)
		0Ch	External Display Interface	0	0	0	0	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)
1*	Power Control	10h	Power Control (1)	0	0	SAP2 (0)	SAP1 (0)	SAP0 (0)	BT2 (0)	BT1 (0)	BT0 (0)	DC2 (0)	DC1 (0)	DC0 (0)	0	0	0	SLP (0)	STB (0)
		11h	Power Control (2)	0	0	GVD5 (0)	GVD4 (0)	GVD3 (0)	GVD2 (0)	GVD1 (0)	GVD0 (0)	0	0	0	0	0	VC2 (1)	VC1 (0)	VC0 (0)
		13h	Power Control (3)	0	0	0	0	0	0	0	0	0	PON (0)	PON1 (0)	AON (0)	0	0	0	0
		14h	Power Control (4)	0	VCMR (0)	VCM5 (0)	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (0)	0	0	VML5 (0)	VML4 (0)	VML3 (0)	VML2 (0)	VML1 (0)	VML0 (0)
2*	DDRAM Access	21h	DDRAM Address Set	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)
		22h	DDRAM Data Write / Read	DDRAM Write data (WD17-0) DDRAM Read Data (RD17-0) *Bit assignment changes according to the interface in use.															
		23h 2Fh	Setting Disabled																
3*	Gamma Control	30h	Gamma Control (1)	0	0	0	0	0	PKP12 (0)	PKP11 (0)	PKP10 (0)	0	0	0	0	0	PKP02 (0)	PKP01 (0)	PKP00 (0)
		31h	Gamma Control (2)	0	0	0	0	0	PKP32 (0)	PKP31 (0)	PKP30 (0)	0	0	0	0	0	PKP22 (0)	PKP21 (0)	PKP20 (0)
		32h	Gamma Control (3)	0	0	0	0	0	PKP52 (0)	PKP51 (0)	PKP50 (0)	0	0	0	0	0	PKP42 (0)	PKP41 (0)	PKP40 (0)
		33h	Gamma Control (4)	0	0	0	0	0	PRP12 (0)	PRP11 (0)	PRP10 (0)	0	0	0	0	0	PRP02 (0)	PRP01 (0)	PRP00 (0)
		34h	Gamma Control (5)	0	0	0	0	0	PKN12 (0)	PKN11 (0)	PKN10 (0)	0	0	0	0	0	PKN02 (0)	PKN01 (0)	PKN00 (0)
		35h	Gamma Control (6)	0	0	0	0	0	PKN32 (0)	PKN31 (0)	PKN30 (0)	0	0	0	0	0	PKN22 (0)	PKN21 (0)	PKN20 (0)
		36h	Gamma Control (7)	0	0	0	0	0	PKN52 (0)	PKN51 (0)	PKN50 (0)	0	0	0	0	0	PKN42 (0)	PKN41 (0)	PKN40 (0)
		37h	Gamma Control (8)	0	0	0	0	0	PRN12 (0)	PRN11 (0)	PRN10 (0)	0	0	0	0	0	PRN02 (0)	PRN01 (0)	PRN00 (0)
		38h	Gamma Control (9)	0	0	0	VRP14 (0)	VRP13 (0)	VRP12 (0)	VRP11 (0)	VRP10 (0)	0	0	0	0	VRP03 (0)	VRP02 (0)	VRP01 (0)	VRP00 (0)
		39h	Gamma Control (10)	0	0	0	VRN14 (0)	VRN13 (0)	VRN12 (0)	VRN11 (0)	VRN10 (0)	0	0	0	0	VRN03 (0)	VRN02 (0)	VRN01 (0)	VRN00 (0)
4*	Coordinate Control	40h	Gate Scan Start Position	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SCN0 (0)
		41h	Vertical Scroll Control	0	0	0	0	0	0	0	0	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)
		42h	First Screen Drive Position	SE17 (1)	SE16 (1)	SE15 (1)	SE14 (0)	SE13 (1)	SE12 (1)	SE11 (1)	SE10 (1)	SS17 (0)	SS16 (0)	SS15 (0)	SS14 (0)	SS13 (0)	SS12 (0)	SS11 (0)	SS10 (0)
		43h	Second Screen Drive Position	SE27 (1)	SE26 (1)	SE25 (1)	SE24 (0)	SE23 (1)	SE22 (1)	SE21 (1)	SE20 (1)	SS27 (0)	SS26 (0)	SS25 (0)	SS24 (0)	SS23 (0)	SS22 (0)	SS21 (0)	SS20 (0)
		44h	Horizontal DDRAM Address Position	HEA7 (1)	HEA6 (0)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)
		45h	Vertical DDRAM Address Position	VEA7 (1)	VEA6 (0)	VEA5 (1)	VEA4 (0)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
5*		53h	VCOMG Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	XVCOMG (0)
		59h	VCOM EQ	0	0	0	0	0	0	0	0	0	0	0	0	0	ECV2 (0)	ECV1 (0)	ECV0 (0)
		5Ah	STB Mode Selection	0	0	0	0	0	0	0	0	0	0	0	0	0	0	STBM1 (1)	STBM0 (0)

Note) The undefined register bits are prohibited to set “1”.

12. Reset Function

The MC2TA7402 has the RESET pin for internal initialization. During the reset period, the MC2TA7402 is in a busy state and no access to instruction or to DDRAM data from the MPU is accepted. The reset period must be secured at least for 1ms. In case of power-on reset, wait until the frequency of RC oscillation stabilizes (for 10 ms). During this period, accessing the internal DDRAM and making an initial instruction setting are prohibited.

Initial state of instruction bits

See the "11. Instruction List" section.

Initial state of DDRAM data

DDRAM data are not automatically initialized with a RESET input. Initialize the internal DDRAM by software during a display-off period (R07h;D1-0 = "00").

Initial state of output pins

LCD driver (source outputs): All pins output the GND level

Oscillator : Oscillate

13. Interface Specifications

The MC2TA7402 has the system interface for making instruction setting and other settings, and the RGB/VSYNC interface for displaying a moving picture. The MC2TA7402 allows selecting an optimum interface for the display (moving or still picture) in order to transfer data efficiently.

In RGB interface mode, display operations are performed in synchronization with synchronizing signals (VSYNC, HSYNC, and DOTCLK). Display data are written to the DDRAM according to the polarity of the data enable signal (ENABLE) via the moving picture display data bus (DB17-0) in synchronization with VSYNC, HSYNC, and DOTCLK. All display data are stored in MC2TA7402's DDRAM to limit data transfers to only when switching the frames of a moving picture. By using the window address function, it is possible to limit the DDRAM area to be rewritten for displaying a moving picture and display both the moving picture and the data written on the DDRAM at a time.

In VSYNC interface mode, the internal display operations are synchronized with the vertical synchronization signal (VSYNC). The VSYNC interface enables a moving picture display via the system interface by writing data to the internal DDRAM at more than a designated speed in synchronization with the falling edge of VSYNC. In this case, there are constraints in the speed and methods to write data to the internal DDRAM.

The MC2TA7402 operates in one of the following 4 modes in line with the state of display.
When switching from one mode to the other, make sure to refer to the sequences mentioned in the sections of RGB and VSYNC interfaces.

Table 13-1: Operation Mode

Operation Mode	DDRAM Access Setting (R0Ch;RM)	Display Operation Mode (R0Ch;DM1-0)
System interface (Displaying still pictures)	System interface (RM = "0")	System interface (DM1-0 = "00")
RGB interface (1) (Displaying moving pictures)	RGB interface (RM = "1")	RGB interface (DM1-0 = "01")
RGB interface (2) (Rewriting still pictures while displaying moving pictures)	System interface (RM ="0 ")	RGB interface (DM1-0 = "01")
VSYNC interface (Displaying moving pictures)	System interface (RM ="0")	VSYNC interface (DM1-0 ="10")

Note 1) Instructions are set only via the system interface.

Note 2) The RGB-I/F and the VSYNC-I/F are not available at the same time.

Note 3) Do not make changes to the RGB-I/F mode (R0Ch;RIM1-0 bits) while the RGB I/F is in operation.

Note 4) See the sections of RGB and VSYNC interfaces for the sequences to switch from one mode to the other (Chapters 15 and 16).

14. System Interface

The following are the system interfaces available with the MC2TA7402. The interface is selected by setting the IM3/2/1/0 pins. The system interface is used for setting instructions and DDRAM access.

Table 14-1: Interface Selection by IM3-0 pins

IM3	IM2	IM1	IM0	Interface Mode		data pin	Colors
0	0	0	0	68-system	16-bit interface	D17-10, D8-1	65,536
0	0	0	1	68-system	8bit interface	D17-10	262,144 / 65,536
0	0	1	0	80-sytem	16-bit interface	D17-10, D8-1	65,536
0	0	1	1	80-system	8-bit interface	D17-10	262,144 / 65,536
0	1	0	*	Serial Peripheral Interface (SPI)		SDI, SDO	262,144 / 65,536
0	1	1	*	Setting disabled		-	-
1	0	0	0	68-system	18-bit interface	D17-0	262,144
1	0	0	1	68-system	9-bit interface	D17-9	262,144
1	0	1	0	80-system	18-bit interface	D17-0	262,144
1	0	1	1	80-system	9-bit interface	D17-9	262,144
1	1	*	*	Setting disabled		-	-

14.1. 80-/68-system 18-bit Interface

The 80-/68-system 18-bit parallel system interface is selected by setting the IM3/2/1/0 pins.

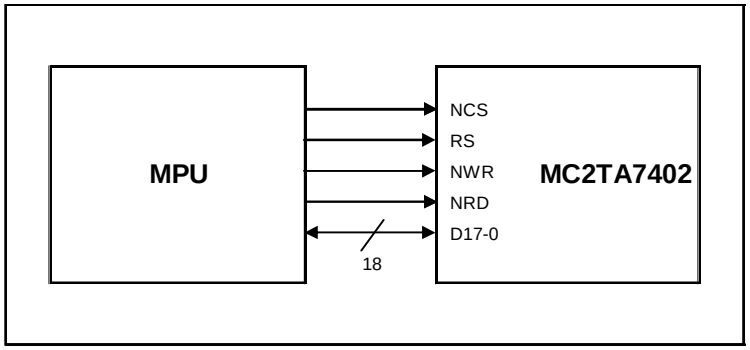


Figure 14-1: 18-bit MPU and the MC2TA7402

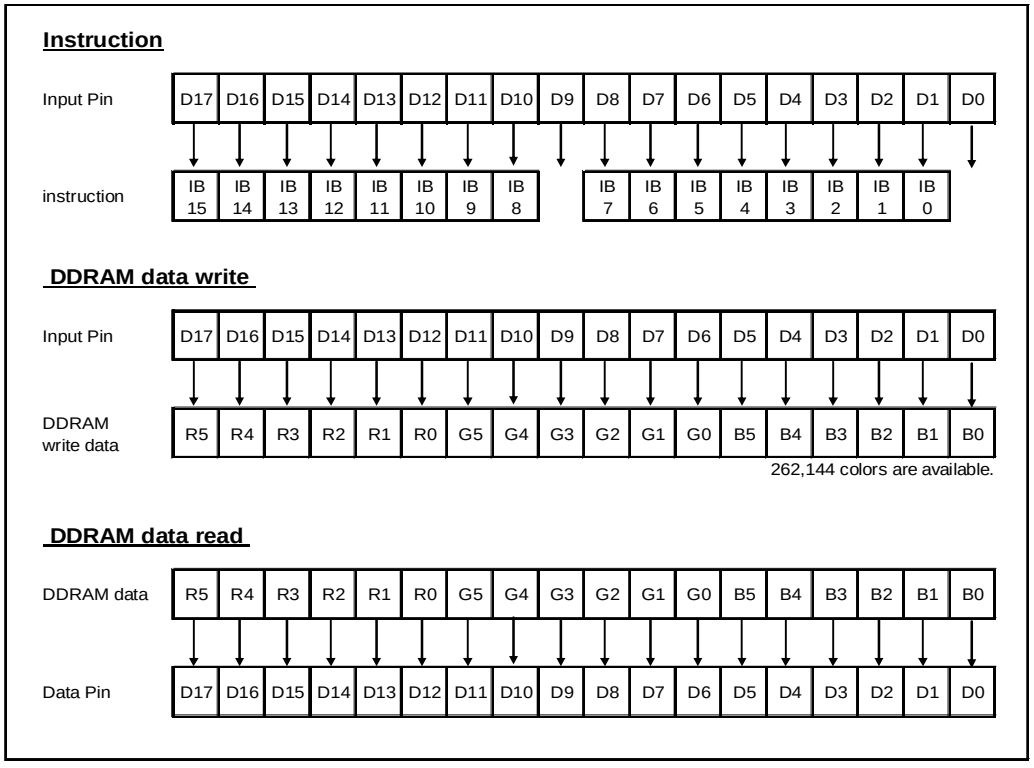


Figure 14-2: Data format for 18-bit interface

14.2. 80-/68-system 16-bit Interface

The 80-/68-system 16-bit parallel system interface is selected by setting the IM3/2/1/0 pins.

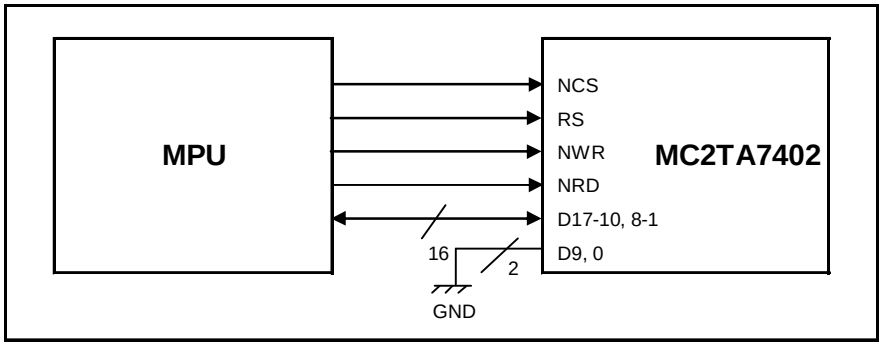


Figure 14-3: 16-bit MPU and the MC2TA7402

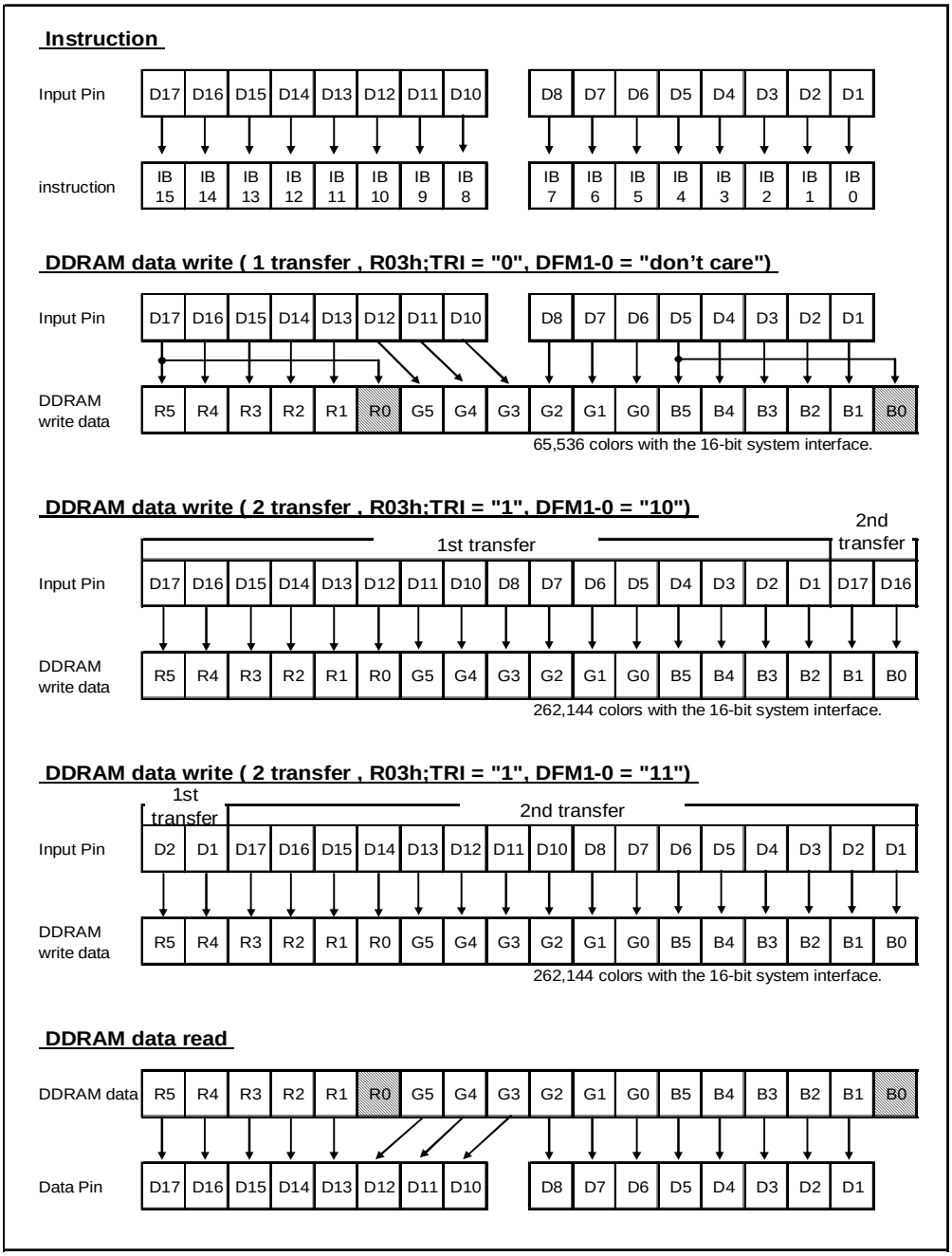


Figure 14-4: Data format for 16-bit interface

14.3. 80-/68-system 9-bit Interface

The 80-/68-system 9-bit parallel system interface using the D17-9 pins is selected by setting the IM3/2/1/0 pins. When transferring a 16-bit instruction, it is divided into upper and lower 8 bits (the LSB is not used), and the upper 8 bits are transferred first. The DDRAM write data are also divided into the upper and lower 9 bits, and the upper bits are transferred first. The unused D8-0 pins must be fixed either at the IOVCC or GND level. When writing the index register, the upper byte (8 bits) must be written.

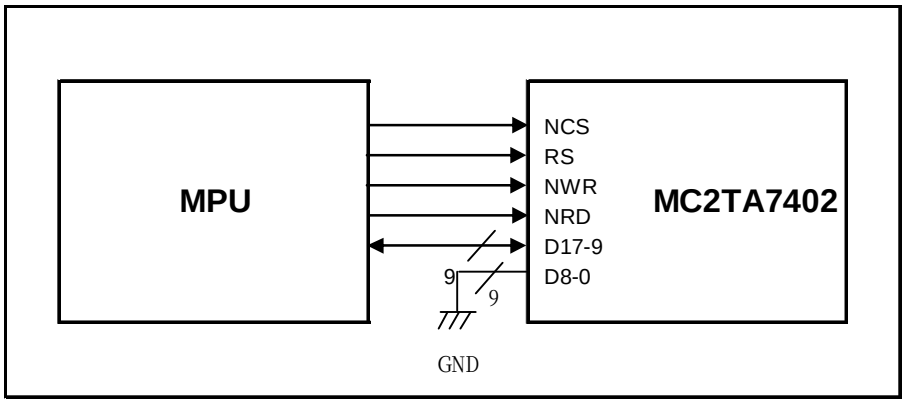


Figure 14-5: 9-bit MPU and the MC2TA7402

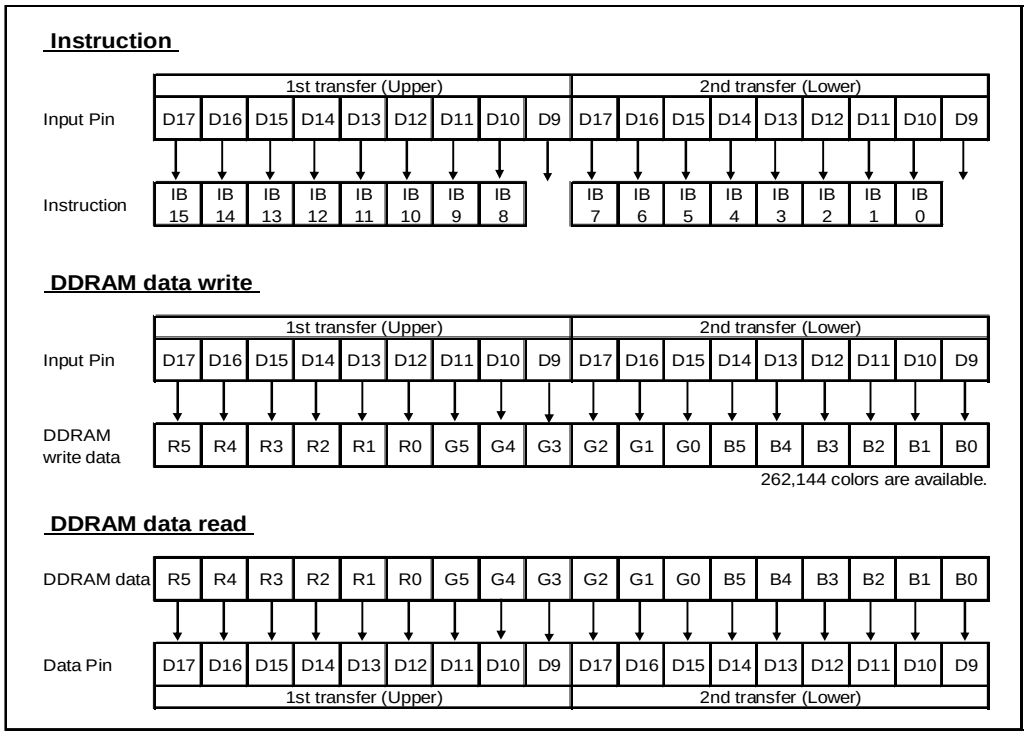


Figure 14-6: Data format for 9-bit interface

14.4. Data Transfer Synchronization in 9-bit Bus Interface Mode

The MC2TA7402 supports a data transfer synchronization function to reset the upper and lower counters that count the number of transfers of upper and lower 9 bits in 9-bit bus interface mode. If a mismatch arises in the numbers of transfers between the upper and lower 9-bit counters due to noise, etc., the "00"h instruction is written 4 times consecutively to reset the upper and lower counters so that data transfers will restart with the transfer of upper 9 bits. This synchronization function, when executed periodically, can effectively prevent the display system from running out of control.

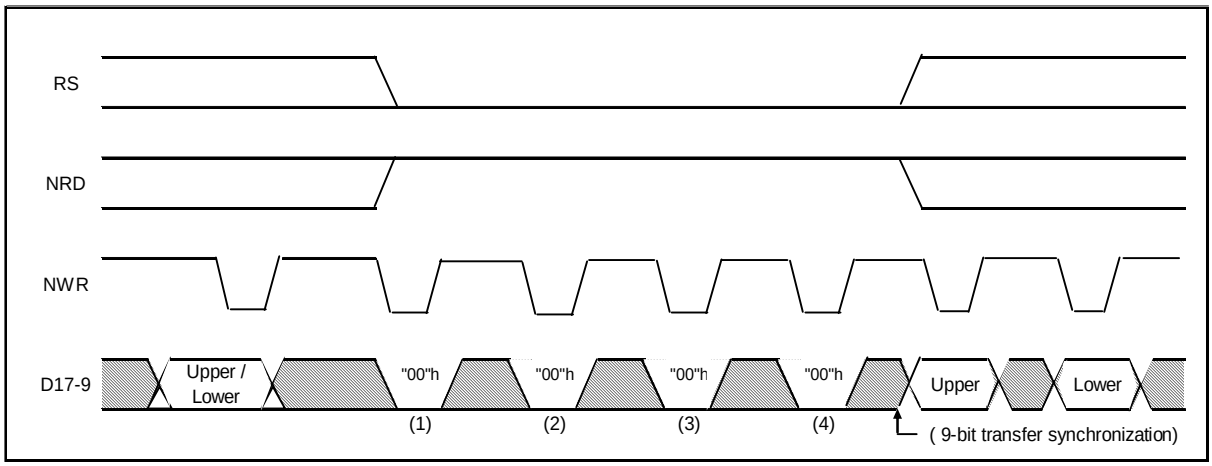


Figure 14-7: 9-bit data transfer synchronization

14.5. 80-/68-system 8-bit Interface

The 80-/68-system 8-bit parallel system interface is selected by setting the IM3/2/1/0 pins. When transferring a 16-bit instruction, it is divided into upper and lower 8 bits and the upper 8 bits are transferred first. The DDRAM data is also divided into the upper and lower 8 bits, and the upper bits are transferred first. The DDRAM write data are expanded into 18 bits internally. The unused pins DB9-0 must be fixed either at the IOVCC or GND level. When writing the index register, the upper byte (8 bits) must be written.

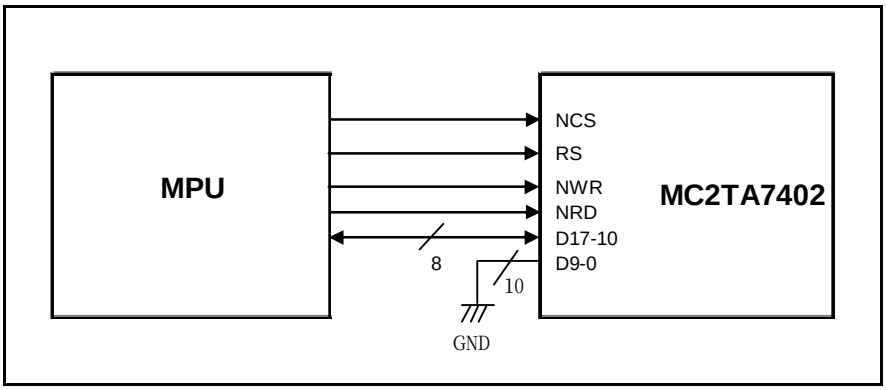
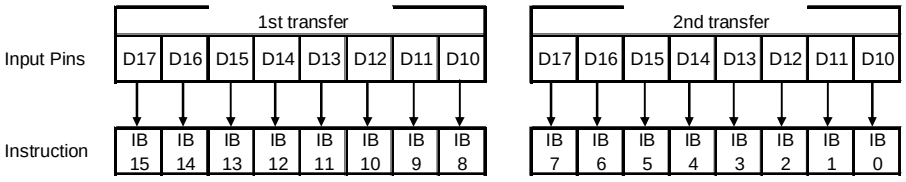
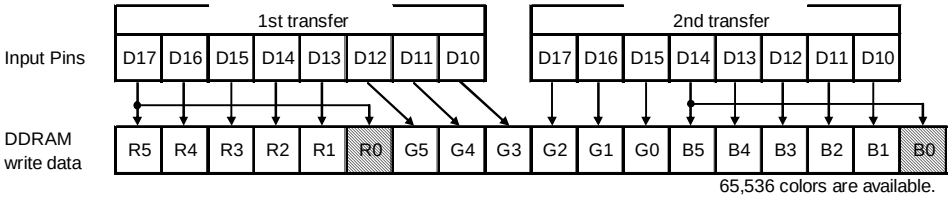


Figure 14-8: 8-bit MPU and the MC2TA7402

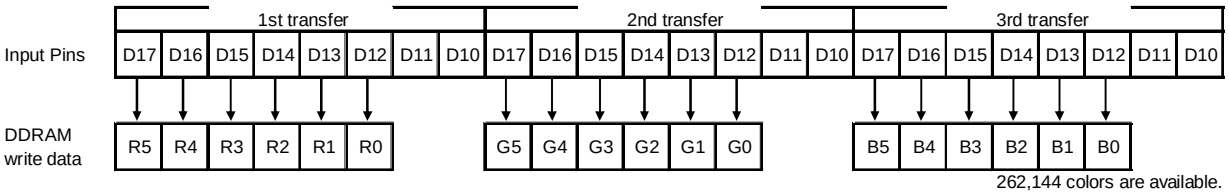
Instruction



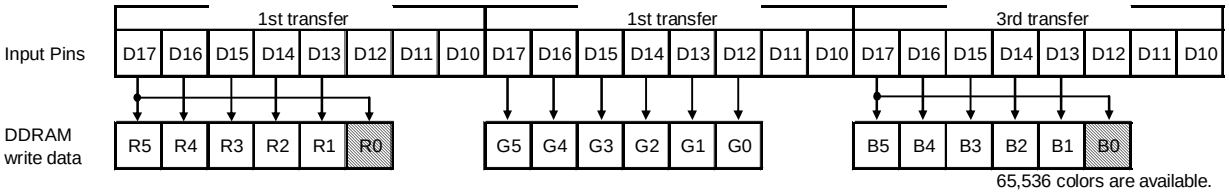
DDRAM data write (2 transfers: R03h;TRI="0", R03h;DFM1-0= don't care)



DDRAM data write (3 transfer mode: R03h;TRI="1", R03h;DFM1-0="10")



DDRAM data write (3 transfer mode: R03h;TRI="1", R03h;DFM1-0="11")



DDRAM data read

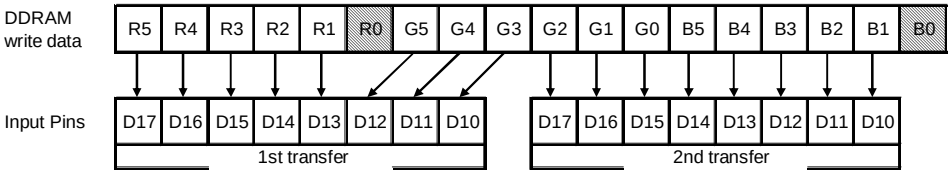


Figure 14-9: Data format for 8-bit interface

14.6. Data Transfer Synchronization in 8-bit Bus Interface Mode

The MC2TA7402 supports a data transfer synchronization function to reset upper and lower counters that count the number of transfers of upper and lower 8 bits in 8-bit bus interface mode. If a mismatch arises in the numbers of transfers between the upper and lower 8-bit counters due to noise, etc., the "00"h instruction is written 4 times consecutively to reset the upper and lower counters so that data transfers will restart with the transfer of upper 8 bits. This synchronization function, when executed periodically, can effectively prevent the display system from running out of control.

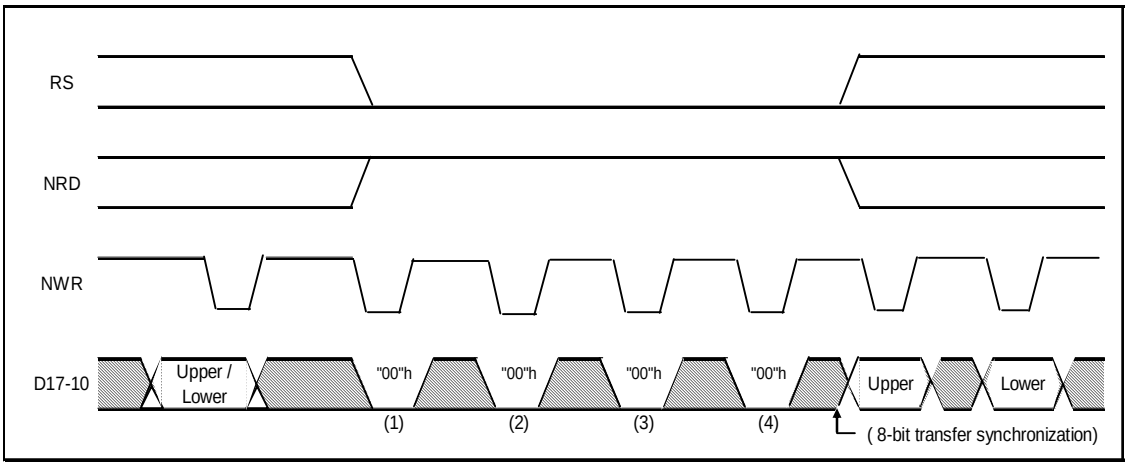


Figure 14-10: 8-bit data transfer synchronization

14.7. Serial Peripheral interface (SPI)

The Serial Peripheral Interface (SPI) is selected by setting the IM3/2/1 pins. The SPI is available through the chip select line (NCS), the serial transfer clock line (SCL), the serial data input (SDI), and the serial data output (SDO). In SPI mode, the IM0/ID pin functions as the ID and the D17-0 pins which are not be used, must be fixed either at the IOVCC or GND level.

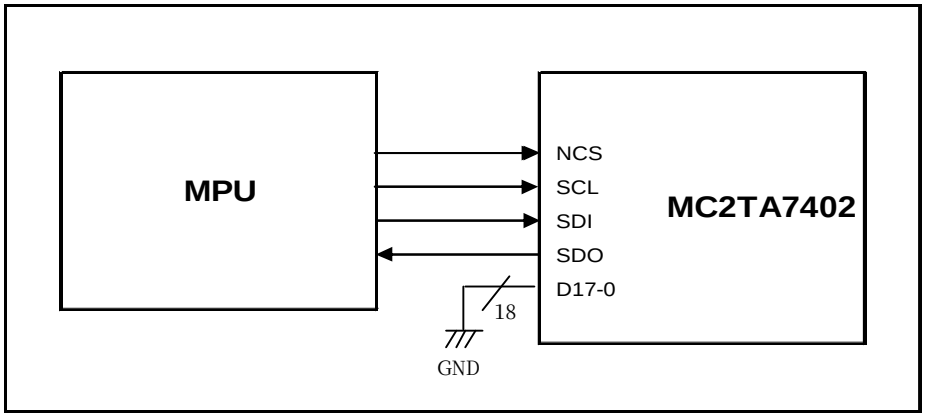


Figure 14-11: SPI MPU and the MC2TA7402

The MC2TA7402 recognizes the start of data transfer on the falling edge of the NCS input and transfers the start byte. It recognizes the end of data transfer on the rising edge of the NCS input. The MC2TA7402 is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the MC2TA7402 correspond as a result of comparison. When selected, the MC2TA7402 starts taking the subsequent data. The ID pin sets the LSB of the identification code. Send "01110" to the identification code that is the five upper bits of the start byte. Two different chip addresses must be assigned to the MC2TA7402 because the seventh bit of the start byte is assigned to the register select bit (RS). When RS = "0", either the index register write operation or the status read operation is executed. When RS = "1", either the instruction write operation or the DDRAM read/write operation is executed. The eighth bit of the start byte is to select either the read or write operation (R/W bit). Data are received when the R/W bit is "0", and are transferred when the R/W bit is "1".

After receiving the start byte, the MC2TA7402 starts transferring or receiving data in units of bytes. Data transfers are executed from the MSB. All instructions of the MC2TA7402 take the 16-bit format and are executed internally after transferring two bytes (DB15-0) from the MSB. DDRAM write data are internally expanded into 18 bits. After receiving the start byte, the MC2TA7402 takes the first and the second bytes as the upper and the lower eight bits of a 16-bit instruction, respectively.

In SPI mode, invalid data are sent to the data bus until 5-byte data are read out from the internal DDRAM after the start byte. Valid data are read out as the MC2TA7402 reads out the 6th byte data from the internal DDRAM.

Table 14-2: Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note 1) The ID bit is selected by setting the IM0/ID pin.

Table 14-3:

RS	RW	Function
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction of DDRAM data
1	1	Read an instruction or DDRAM data

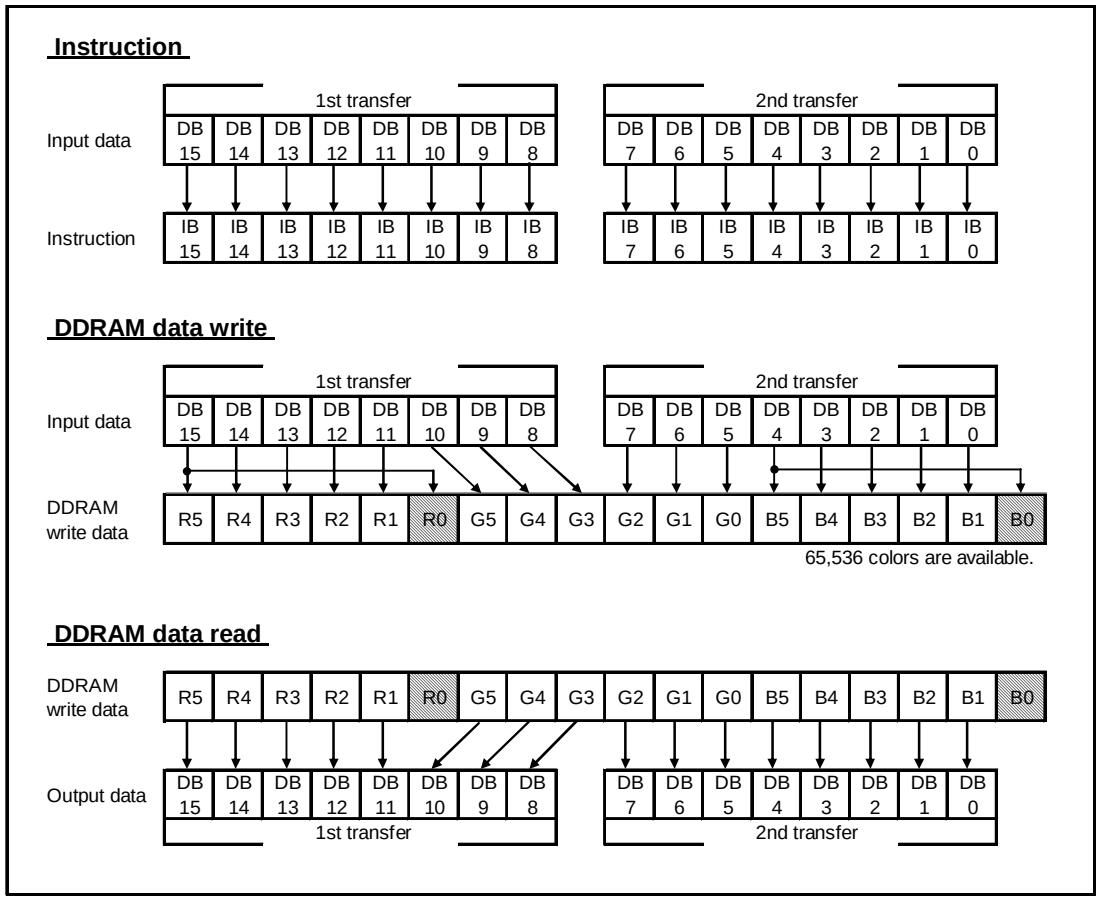
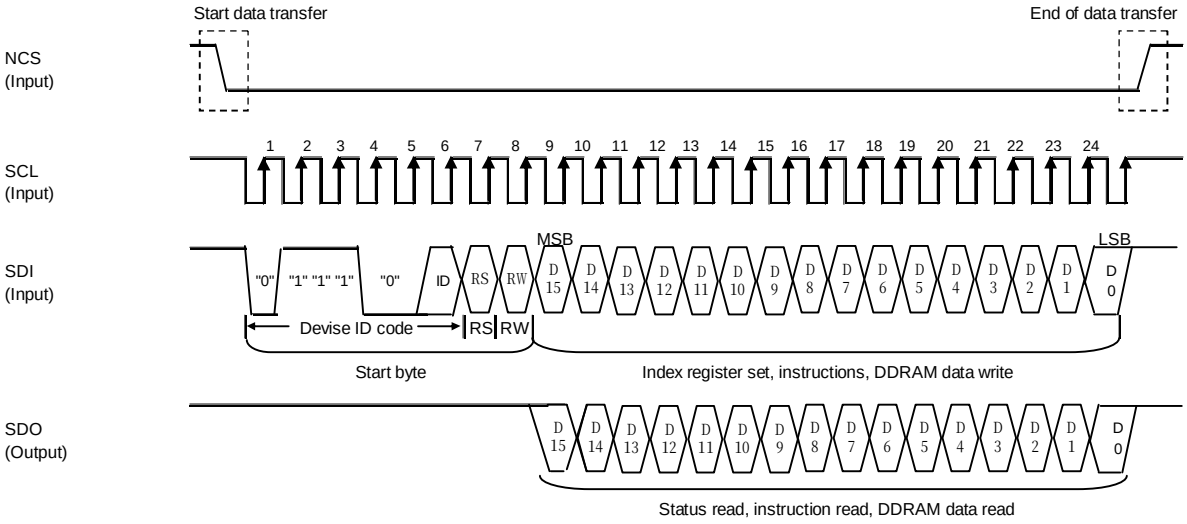
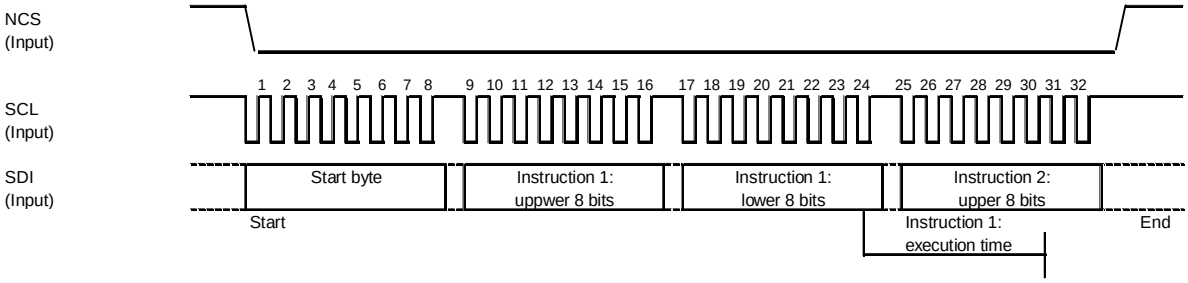


Figure 14-12: Data format for SPI

A) Basic data transfers through SPI

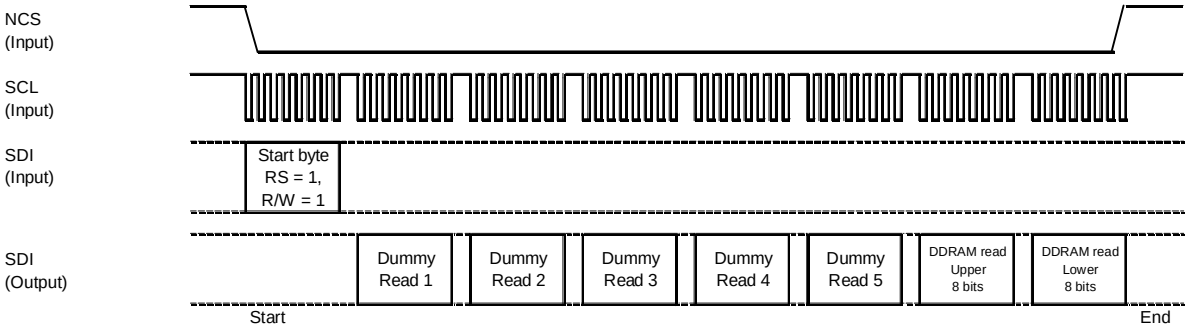


B) Consecutive data transfers through SPI



Note: The start byte transfer is always followed by the transfer of upper byte of an instruction.

C) DDRAM data read transfers through SPI



Note: Invalid data are sent to the data bus until the 5th byte data are read out from the internal DDRAM.
Valid data are sent to the data bus as the MC2TA7402 starts reading the 6th data from the internal DDRAM.

Figure 14-13: Data transmission through SPI (1)

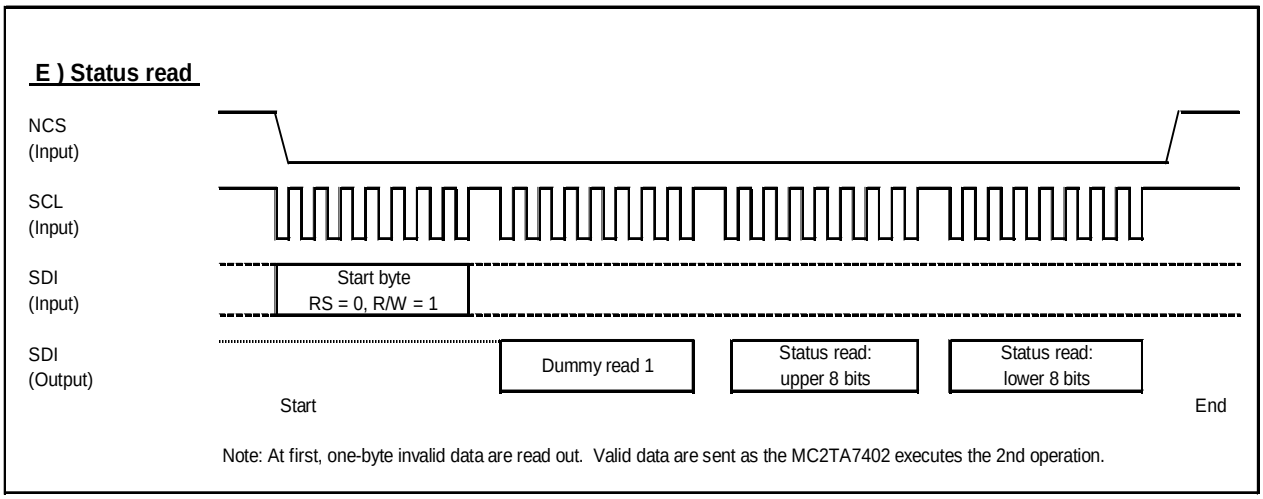


Figure 14-14: Data transmission through SPI (2)

15. VSYNC Interface

The MC2TA7402 has the VSYNC interface that enables moving picture display with the system interface in synchronization with the vertical synchronizing signal (VSYNC). The VSYNC interface enables the system interface to display a moving picture with minimum modification.

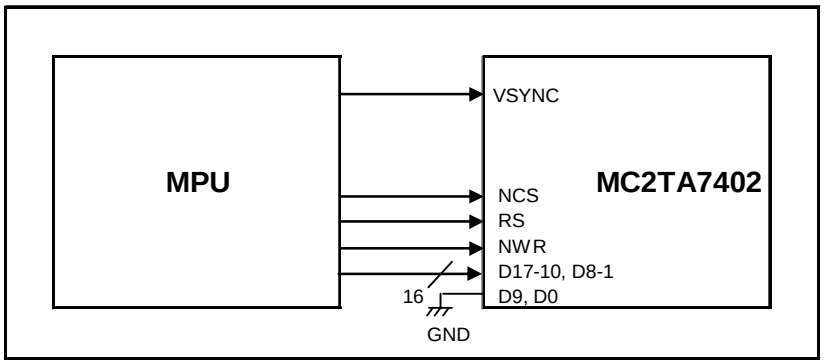


Figure 15-1: VYSNC interface (in case of 16 bits)

The VSYNC interface is selected by setting R0Ch;DM1-0 = "10" and R0Ch;RM = "0". In VSYNC interface mode, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal DDRAM through the system interface at a certain speed higher than that of internal display operation, the VSYNC interface enables moving picture display through the system interface and a screen rewriting operation without flicker.

The display operation in VSYNC mode is executed in synchronization with the internal clock generated from internal oscillators and the VSYNC input. All display data are stored in the internal DDRAM to limit the data to be transferred to those overwritten on the moving picture DDRAM area. Also the total data transfers required for moving picture display are minimized. By using this method the MC2TA7402 can access the internal DDRAM with less power consumption in VSYNC interface mode.

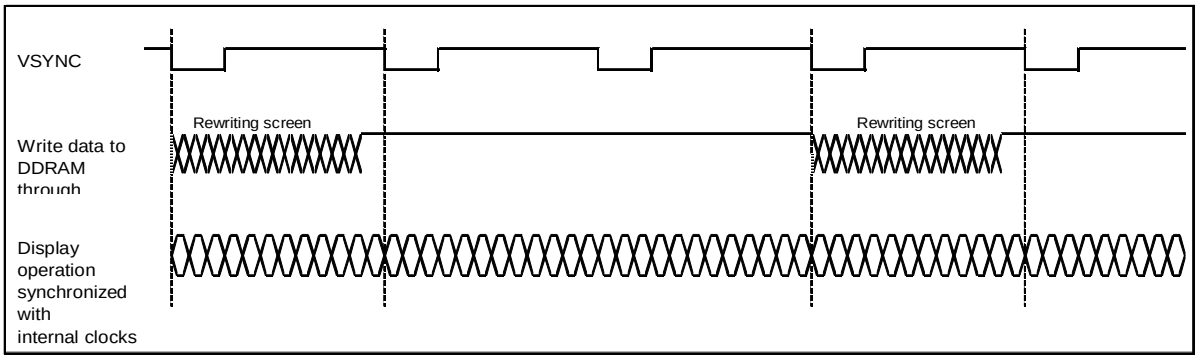


Figure 15-2: Moving picture data transfers via VSYNC interface

VSYNC interface requires taking the minimum speed for RAM writing via the system interface and the frequency of the internal clock into consideration. RAM writing should be performed with higher speed than the result obtained from the calculation shown below. The internal memory write address counter is reset by VSYNC. So, insure interval time between VSYNC falling and GRAM data writing.

Internal clock frequency (fosc) [Hz]
=Frame Frequency x (DisplayLines(NL)+Frontporch(FP)+BackPorch(BP)) x 16(clocks) x variance

$$\textit{DDRAM Write Speed (min.)[Hz]} > \frac{\textit{176 x Display Lines (NL)}}{\textit{\{(Display Lines(NL)+Backporch(BP)+Frontporch(FP)-Margin) x 16(Clocks) x (1/fosc)\}}}$$

Note) When the DDRAM write operation does not start on the falling edge of the VSYNC input, the time from the falling edge of the VSYNC input until the start of the DDRAM write operation must also be taken into account.

An example of the minimum DDRAM writing speed and the internal clock frequency in VSYNC interface mode is as follows.

[Example]

Display size:	176 RGB × 220 lines
Lines	220 lines
Back Front porch	14/2 lines (R08h;BP3-0= "1110" / FP3-0 = "0010")
Frame frequency	60 Hz
1H period	16 clock (R0Bh;RTN1-0 = "00" = INCLK / 16

Internal clock frequency (fosc) [Hz]= 60 Hz × (220 + 14 + 2) lines × 16 clocks × 1.1 / 0.9 = 277 kHz

Note1) When setting the internal clock frequency, possible causes of variances must also be taken into consideration. In this example, the calculated internal clock frequency with the above register setting allows for a margin of ±10% for variances and ensures to complete the display operation within one VSYNC cycle.

Note2) In this example, variances attributed to the fabrication process of LSI and room temperature are counted in. Other possible causes of variances, such as voltage changes are not in consideration. It is necessary to allow for an enough margin for these factors to be incorporated.

Minimum speed for DDRAM writing [Hz] > 176 × 220 / {((14 + 220 - 2) lines × 16 clock) / 277 kHz} = 2.89 MHz

Note3) The above theoretical value is calculated on the premise that the MC2TA7402 starts writing data to the internal DDRAM on the falling edge of the VSYNC input.

Note4) There must be at least a margin of 2 lines between the physical display line where the display operation is performed and the DDRAM line address where the data write operation is performed.

The DDRAM write speed of 2.89MHz or more on the falling edge of the VSYNC input will guarantee the completion of the DDRAM write operation before the MC2TA7402 starts displaying the DDRAM data on the screen, enabling rewriting the entire screen without flicker.

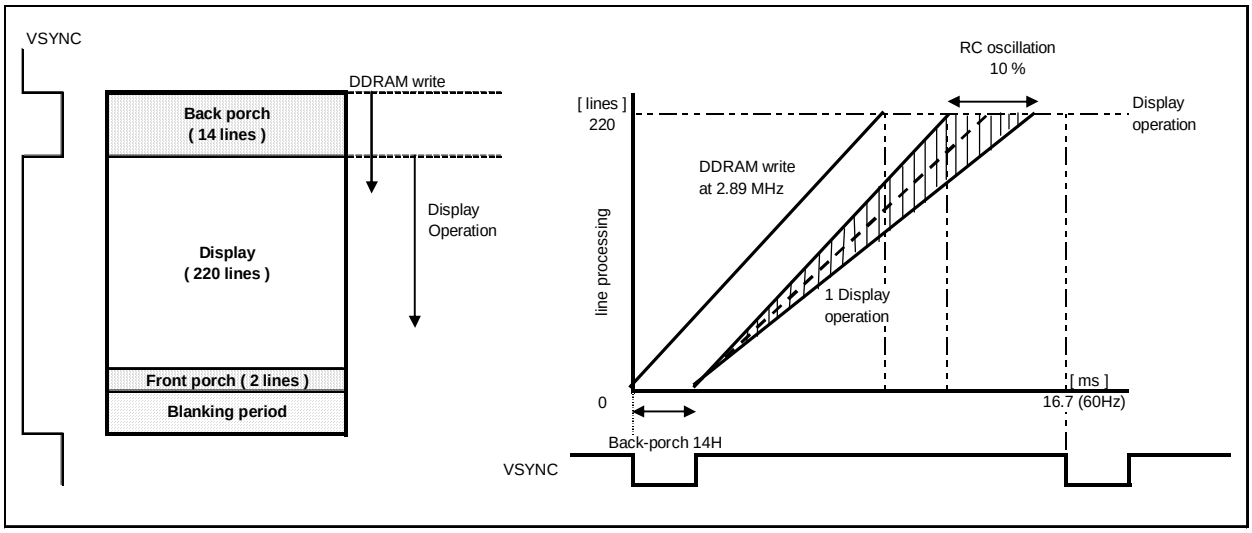


Figure 15-3: Write/display operation timing via VSYNC interface

Notes in using the VSYNC interface

The above calculation example gives a theoretical value. At time of setting, other possible causes of variances that are not counted in the above example (such as differences in internal oscillators) should also be taken into consideration. It is strongly recommended to allow for an enough margin in setting a DDRAM writing speed.

The above calculation example gives the minimum value in case of rewriting the entire screen. If the moving picture display area is smaller than that, the range for setting the minimum DDRAM writing speed can have extra margins.

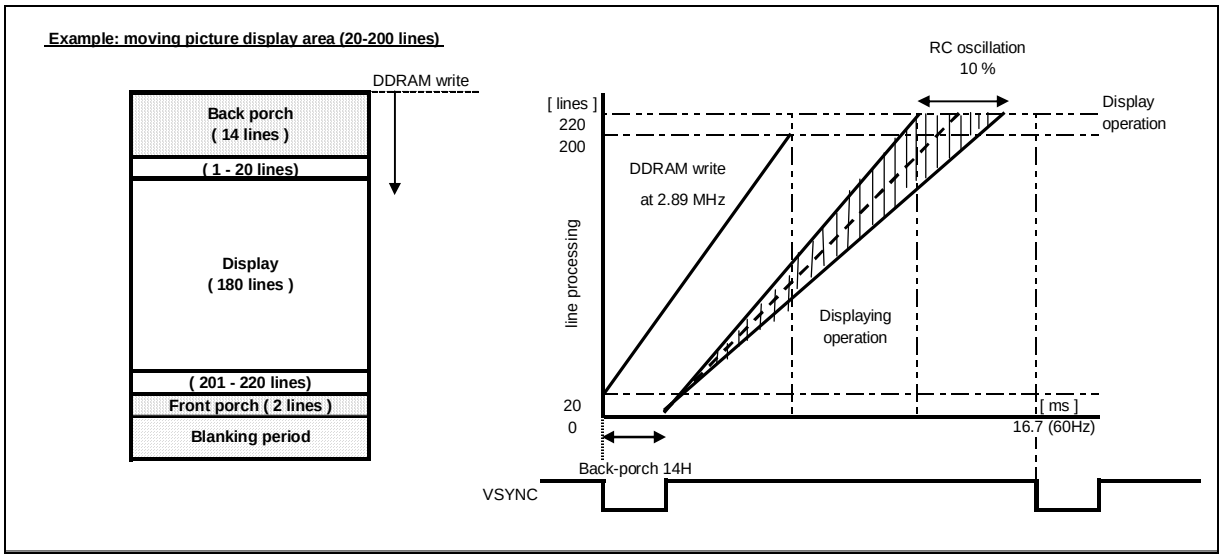


Figure 15-4: DDRAM write margin

1. After drawing a frame, a front porch period continues until the next VSYNC input is detected.
2. When switching from the system interface mode (DM1-0 = "00") to the VSYNC interface mode or vice versa, the new interface mode is enabled from the next VSYNC cycle. For example, the new interface is enabled after completing the display of the frame that the MC2TA7402 was internally processing when switching modes.
3. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.
4. In VSYNC interface mode, set the AM bit to "0" to transfer display data in the method mentioned above.

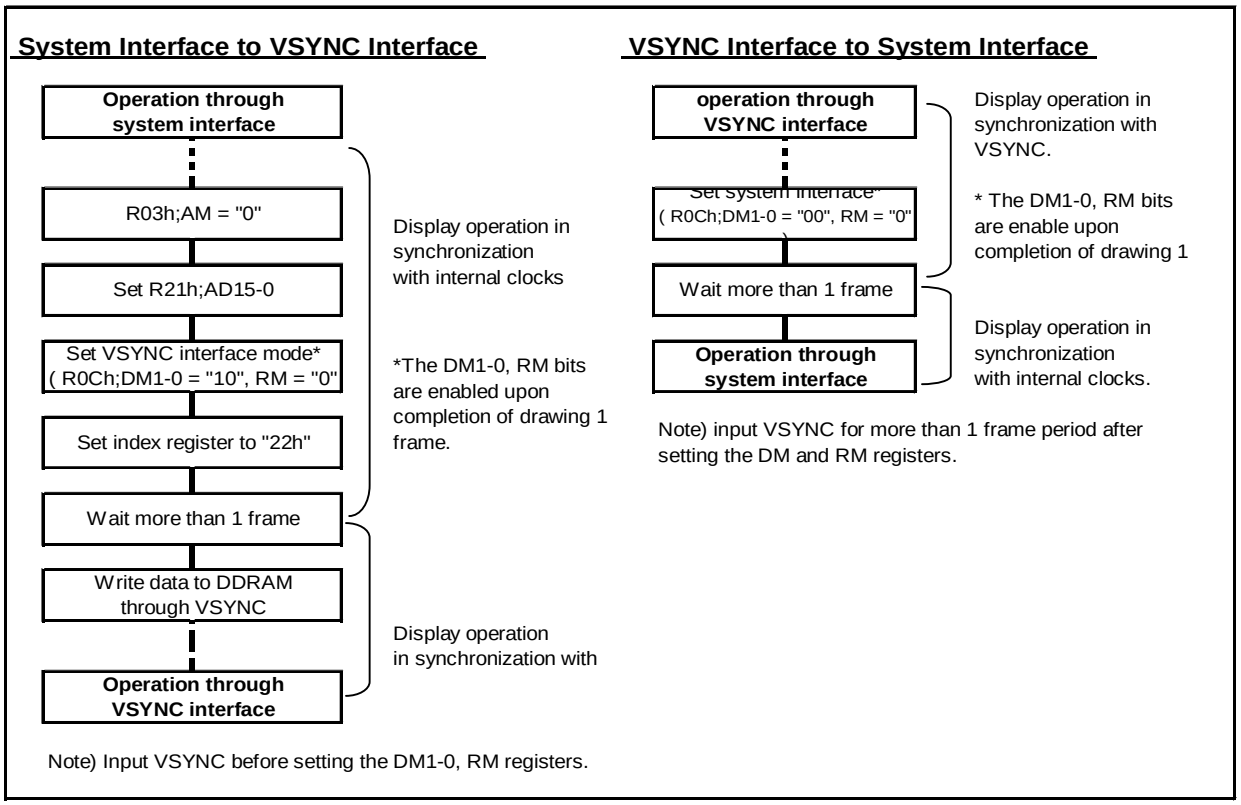


Figure 15-5: VSYNC/system interface mode switching sequences

16. RGB Interface

16.1. RGB Interface

The following table shows the RGB interface available with the MC2TA7402 . The interface is selected by setting the R0Ch;RIM1-0 bits as follows. The RGB interface is used to access the DDRAM.

Table 16-1:

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-13, 11-1
1	0	6-bit RGB interface	DB17-12
1	1	Setting disabled	

Note 1) Multiple RGB interfaces cannot be used at the same time.

The display operation via the RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. The RGB interface enables transferring the minimum necessary data and rewriting the DDRAM area to be overwritten with the use of the window address function. In RGB interface mode, it is necessary to set back and front porch periods before and after a display period, respectively.

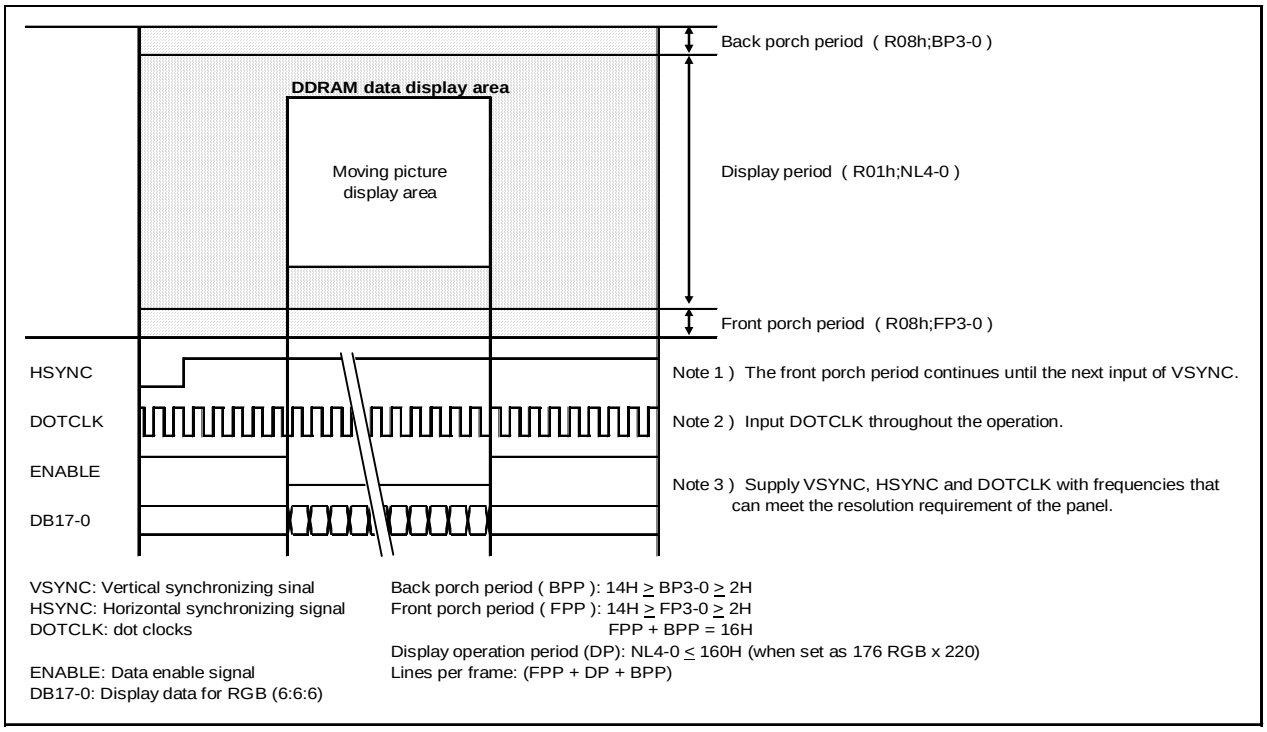


Figure 16-1: RGB interface

16.2. RGB Interface Timing

The timing chart of signals in the 16-/18-bit RGB interface mode is as follows.

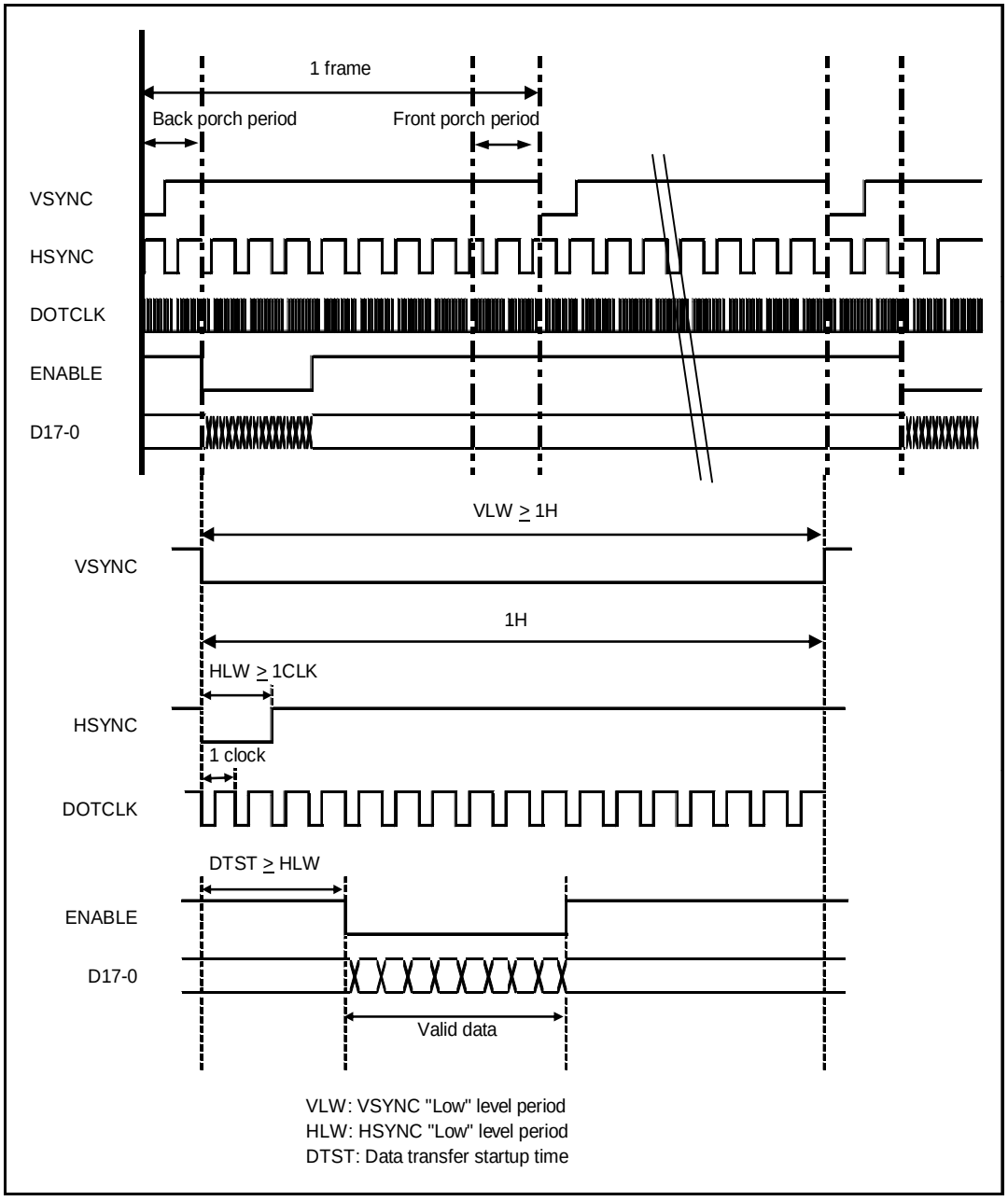
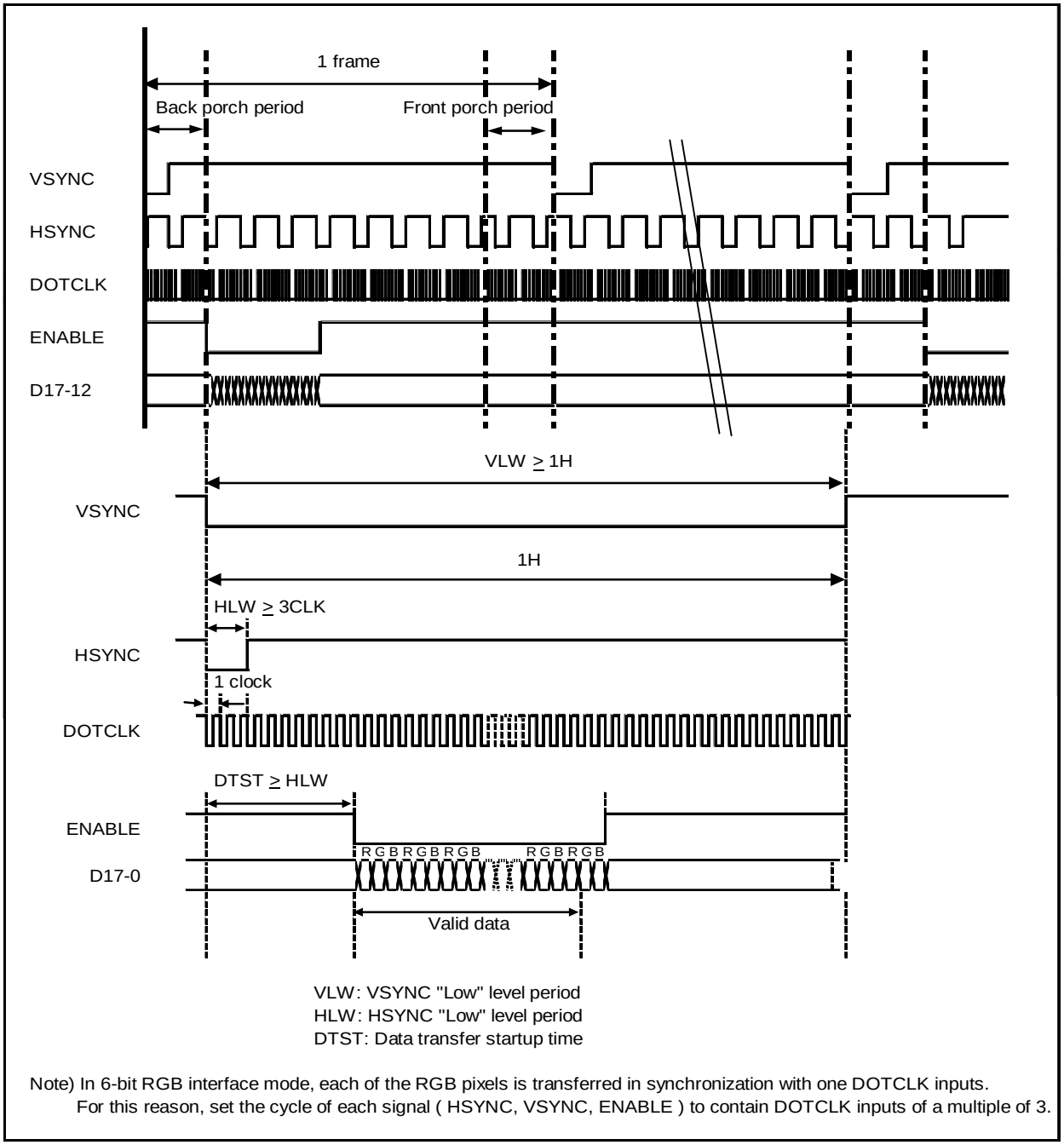


Figure 16-2: 16-/18-bit RGB Interface Timing

The timing chart of signals in the 6-bit RGB interface mode is as follows.



Note) In 6-bit RGB interface mode, each of the RGB pixels is transferred in synchronization with one DOTCLK inputs.
For this reason, set the cycle of each signal (HSYNC, VSYNC, ENABLE) to contain DOTCLK inputs of a multiple of 3.

Figure 16-3: 6-bit RGB Interface Timing

16.3. Moving Picture Display

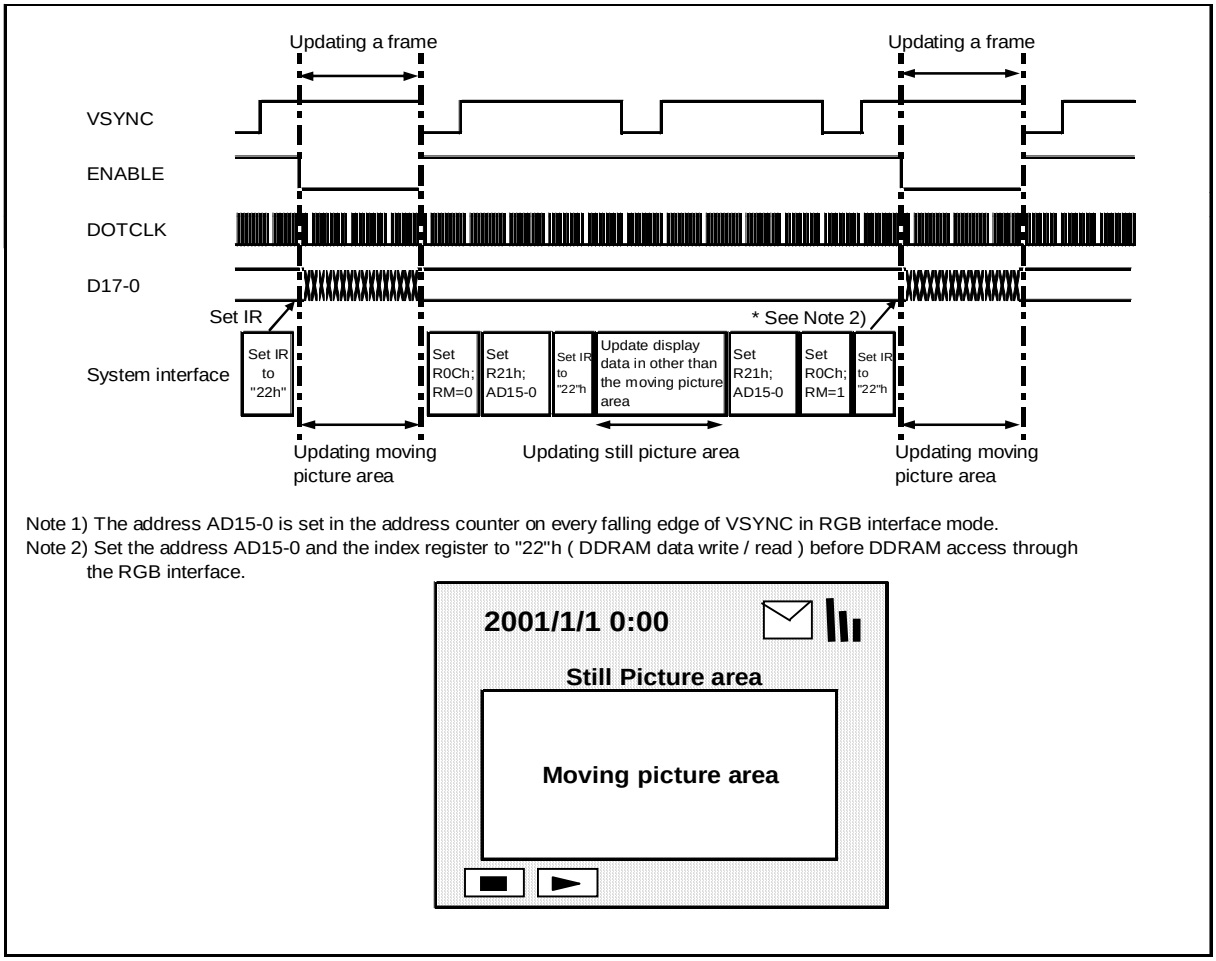
The MC2TA7402 has the RGB interface that is dedicated to display moving picture display. The MC2TA7402 also has the DDRAM for storing data for a moving picture. In this way, the MC2TA7402 has the following benefit in displaying a moving picture.

- The window address function enables transferring the minimum necessary data to be written to the moving picture DDRAM area
- Data are transferred only to the moving picture DDRAM area.
- The reduction in data transfers contributes to reduce the power consumption by the entire system.
- By using the system interface, it is possible to rewrite data in a still picture DDRAM area (icons, etc.) even when displaying a moving picture.

16.4. DDRAM Access through a System Interface in RGB-I/F Mode

The MC2TA7402 allows DDRAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal DDRAM in synchronization with DOTCLK while the ENABLE is “Low”. Set the ENABLE "High" to stop writing data via the RGB interface during writing data to the internal DDRAM via the system interface. Then set R0Ch;RM = "0" to make the DDRAM accessible via the system interface. At the time to restart the DDRAM access in RGB interface mode, wait for a read/write bus cycle time. Then, set R0Ch;RM = "1" and the index register to "22"h to start accessing the DDRAM via the RGB interface. When conflicts between DDRAM accesses via those two interfaces occur, the DDRAM write data is not guaranteed.

The following figure illustrates the operation of the MC2TA7402 when displaying a moving picture via the RGB interface and rewriting data in the still picture DDRAM area via the system interface.



Note 1) The address AD15-0 is set in the address counter on every falling edge of VSYNC in RGB interface mode.
Note 2) Set the address AD15-0 and the index register to "22"h (DDRAM data write / read) before DDRAM access through the RGB interface.

Figure 16-4:

16.5. 6-bit RGB Interface

The 6-bit RGB interface is selected by setting the R0Ch;RIM1-0 bits to "10". The display operation is synchronized with the VSYNC, HSYNC, and DOTCLK signals. According to the data enable signal (ENABLE), display data are transferred to the internal DDRAM in synchronization with the display operation through the 6-bit RGB data bus (D17-12). Unused pins (D11-0) must be fixed at either the IOVCC or GND level.

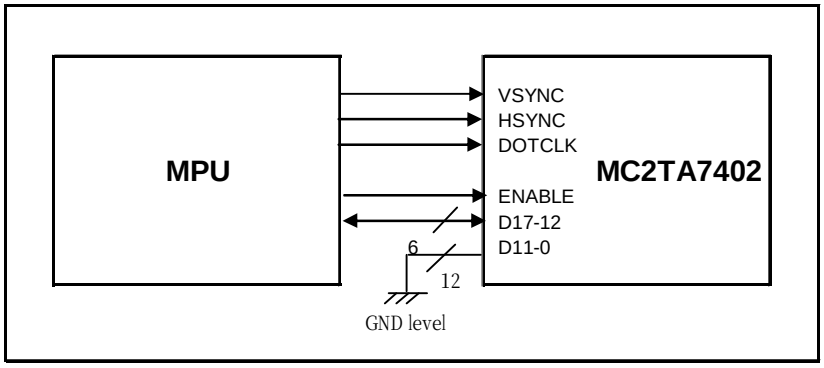


Figure 16-5: 6-bit RGB interface

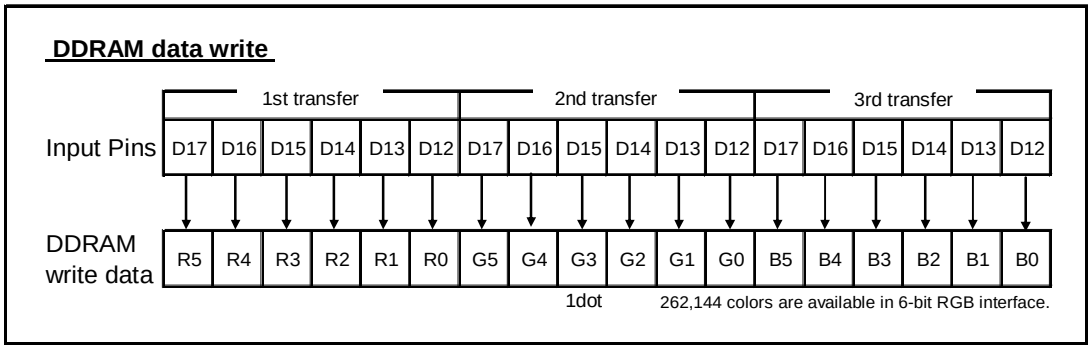


Figure 16-6: Data format for 6-bit interface

16.6. Data Transfer Synchronization in 6-bit RGB Interface Mode

The MC2TA7402 has data transfer counters for counting the first, second and third data transfers in 6-bit RBG interface mode. The transfer counters are always reset to the state of the first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counters are reset to the state of the first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is useful for moving picture display. This function enables the system to return to the normal state with the minimum effects from failed transfers in transferring data consecutively (displaying a moving picture, etc.).

Note that the internal display operations are performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one-frame period must be a multiple of 3 to complete data transfers correctly. Otherwise the display on the screen will be affected.

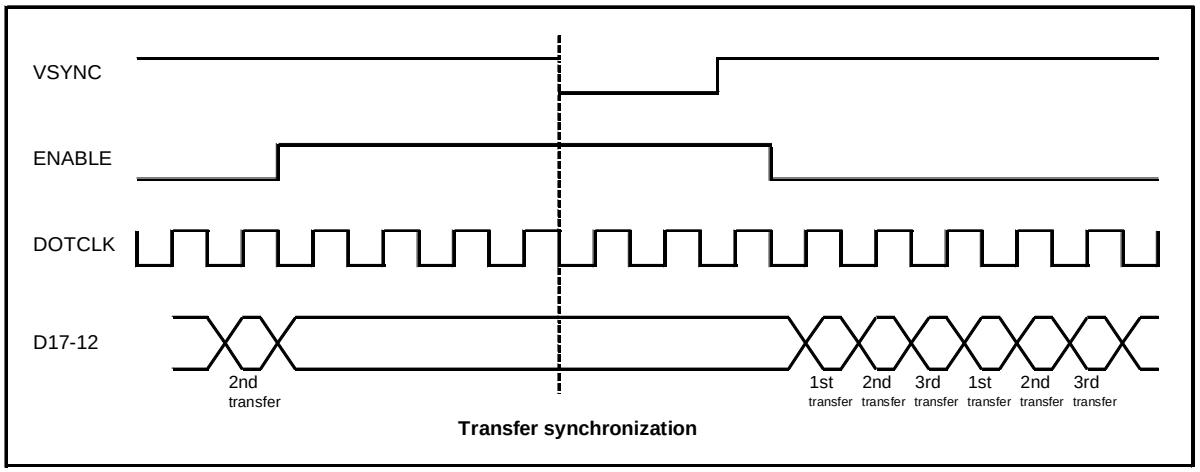


Figure 16-7: 6-bit data transfer synchronization

16.7. 16-bit RGB Interface

The 16-bit RGB interface is selected by setting the R0Ch;RIM1-0 bits to "01". The display operation is synchronized with the VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal DDRAM in synchronization with the display operation through the 16-bit RGB data bus (D17-13, D11-1) according to the data enable signal (ENABLE). Instructions are set only through the system interface.

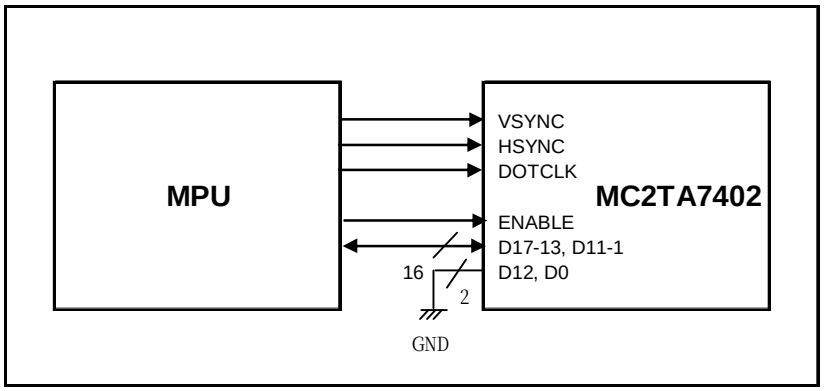


Figure 16-8: 16-bit RGB interface

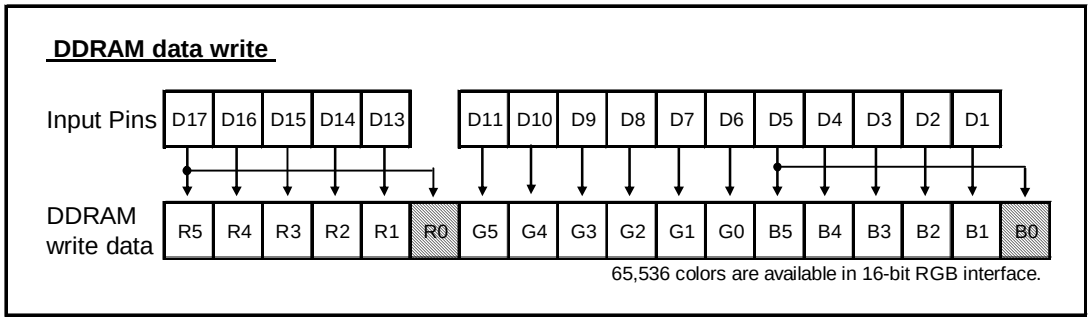


Figure 16-9: Data format for 16-bit interface

16.8. 18-bit RGB Interface

The 18-bit RGB interface is selected by setting the R0Ch;RIM1-0 bits to "00". The display operation is synchronized with the VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal DDRAM in synchronization with the display operation through the 18-bit RGB data bus (D17-0) according to the data enable signal (ENABLE).

Instructions are set only through the system interface.

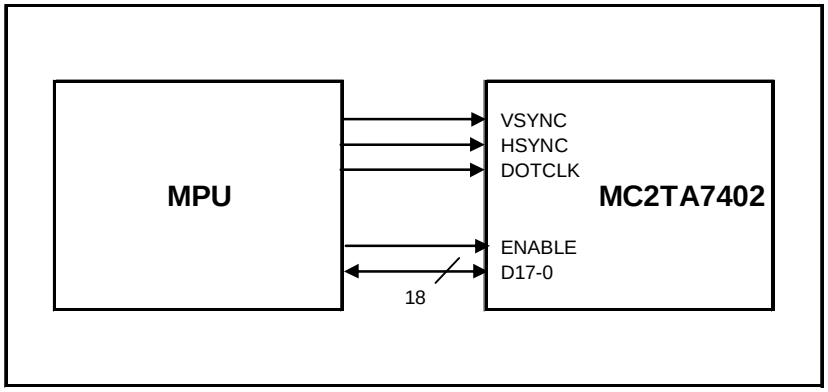


Figure 16-10: 18-bit RGB interface

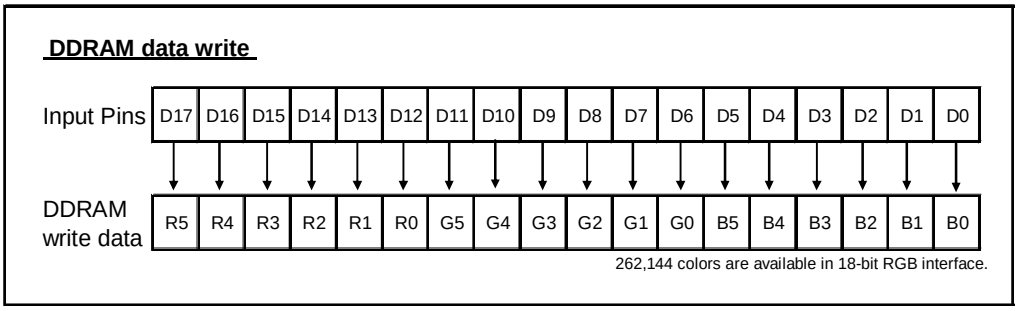


Figure 16-11: Data format for 18-bit interface

16.9. Notes in Using the RGB Interface

The following are the unavailable functions in RGB interface mode.

Table 16-2:

Function	RGB Interface	VSYNC Interface	System Interface
Partial display	Not available	Not available	Available
Scroll function	Not available	Not available	Available
Interlaced scan	Not available	Not available	Available

1. The VSYNC, HSYNC, and DOTCLK signals must be supplied throughout a display operation period.
2. The periods set with the R0Bh;NO1-0 bits (gate output non-overlap period), R0Bh;SDT1-0 bits (source output delay period) and R0Bh;ECS2-0(Equalizing period) are not based on the internal clock but based on DOTCLK in RGB interface mode.
3. In 6-bit RGB interface mode, each of the RGB pixels is transferred in synchronization with a DOTCLK input. In other words, it takes 3 DOTCLK inputs to transfer one-dot data. Make sure to complete data transfers in units of 3 DOTCLK inputs in 6-bit RGB interface mode.
4. In 6-bit RGB interface mode, one-dot data, which consist of the RGB dots, are transferred in units of 3 DOTCLK inputs. Accordingly, set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC ENABLE, D17-0) to contain the DOTCLK inputs of a multiple of 3 to complete data transfers in a dot unit.
5. When switching from the system interface mode to the RGB/VSYNC interface mode, or vice versa, follow the sequence on Figure 16-12 and Figure 16-13.
6. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
7. In RGB interface mode, a DDRAM address (R21h;AD15-0) is set in the address counter every frame on the falling edge of VSYNC.

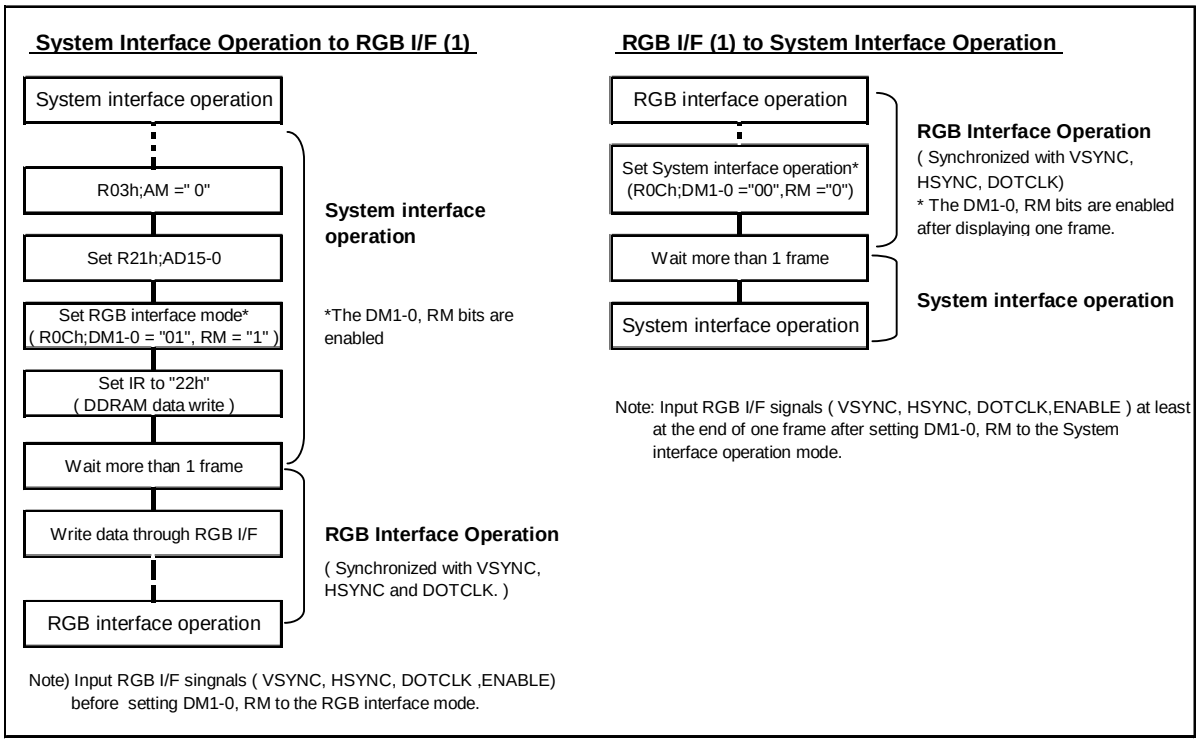


Figure 16-12: System interface/RGB interface mode switching sequence

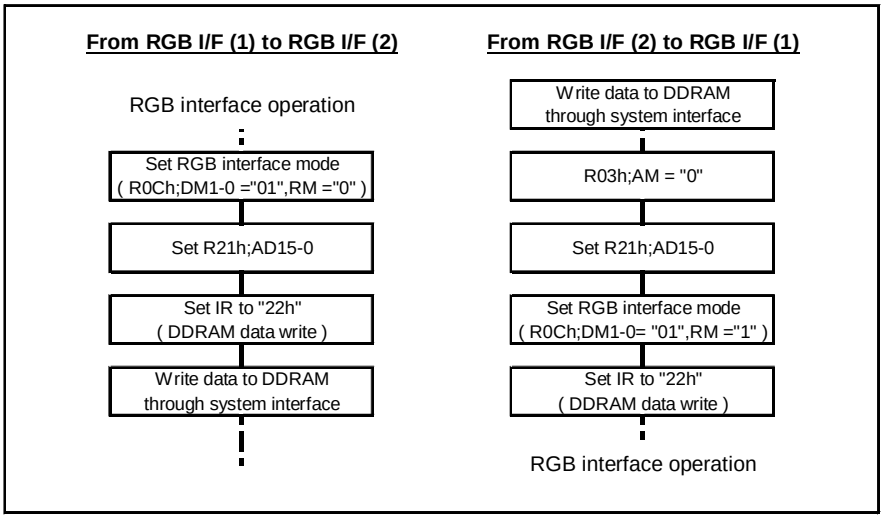


Figure 16-13: Switching DDRAM access modes
(between RGB interface (1) and RGB interface (2) modes)

17. Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) on the internal DDRAM. The window address area is created by setting the horizontal address register (start: R44h;HSA7-0, end: HEA 7-0) and the vertical address register (start: R45h;VSA7-0, end: VEA7-0).

The R03h;AM bit sets the transition direction of a DDRAM address (either increment or decrement). These bits enables the MC2TA7402 to write data including image data consecutively not taking data wrap positions into account.

The window address area must be made within the DDRAM address map area. Also, the R21h; AD15-0 bits (DDRAM address set register) must be an address within the window address area.

[Window address setting area]

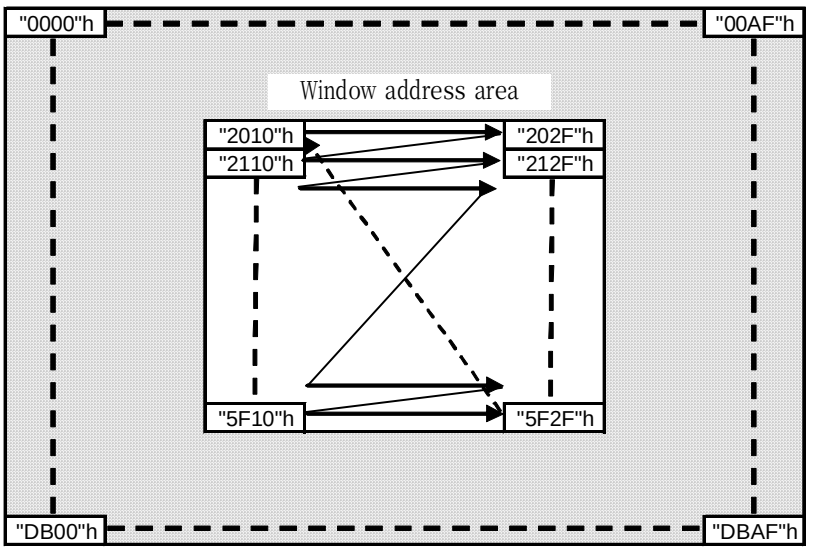
(Horizontal direction) "00"h ≤ HSA7-0 ≤ "AF"h (When set as 176 RGB x 220)

(Vertical direction) "00"h ≤ VSA7-0 ≤ "DB"h

[DDRAM address, AD15-0 (an address within a window address area)]

(DDRAM address) HSA7-0 ≤ AD7-0 ≤ HEA7-0

VSA7-0 ≤ AD15-8 ≤ VEA7-0



Window address setting area

R44h;HSA7-0 = "10"h, R44h;HEA7-0 = "2F"h R03h;I/D = 1 (increment)

R45h;VSA7-0 = "20"h, R45h;VEA7-0 = "5F"h R03h;AM = 0 (horizontal writing)

Figure 17-1

18. Gamma Correction Function

The MC2TA7402 has the gamma-correction function to display in 262,144 colors simultaneously. The gamma-correction is performed with 4 groups of registers determining eight reference grayscale levels, gradient adjustment, amplitude adjustment, reference adjustment and micro adjustment registers. Each register group further consists of register groups of positive and negative polarities. Each register group is set independently to other register groups, making the MC2TA7402 available with liquid crystal display panels of various characteristics.

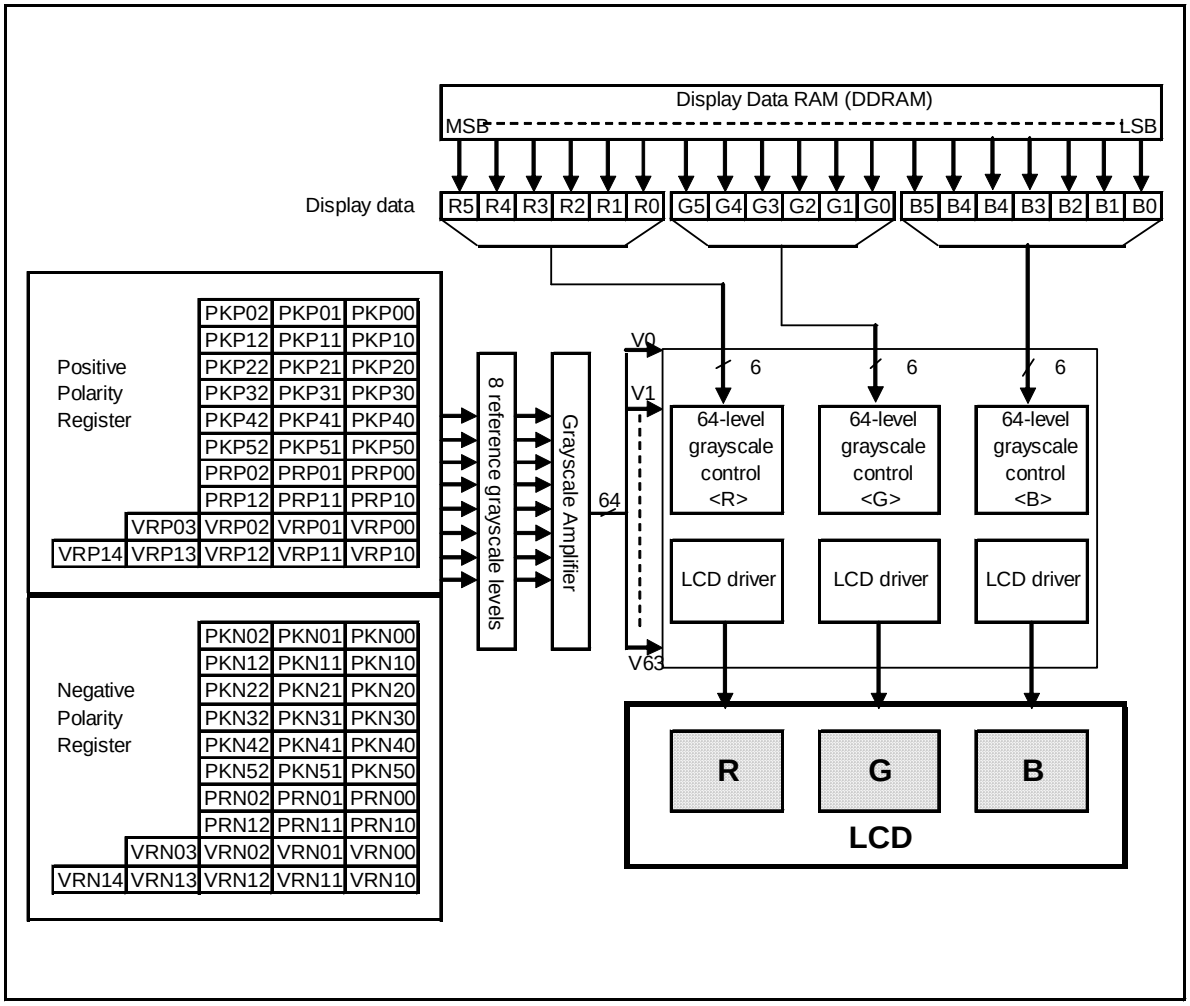


Figure 18-1

18.1. Grayscale Amplifier Unit Configuration

The following figure illustrates the grayscale amplifier unit of the MC2TA7402. To generate 64 grayscale voltages (V0 to V63), the MC2TA7402 first generates eight reference grayscale voltages (VINP0-7/VINN0-7). The grayscale amplifier unit then divides eight reference grayscale voltages with the built-in ladder resistors.

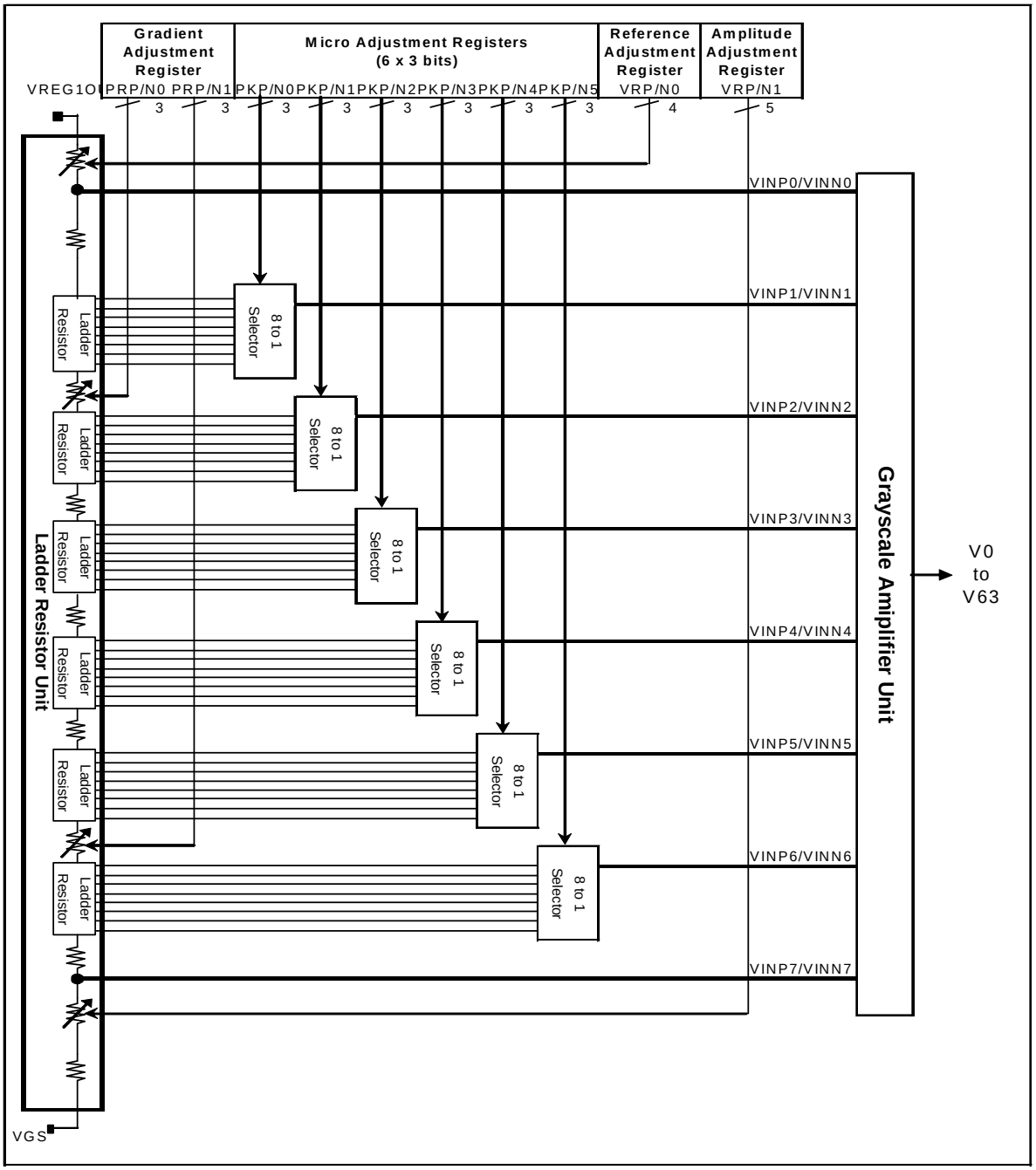


Figure 18-2: Grayscale amplifier unit

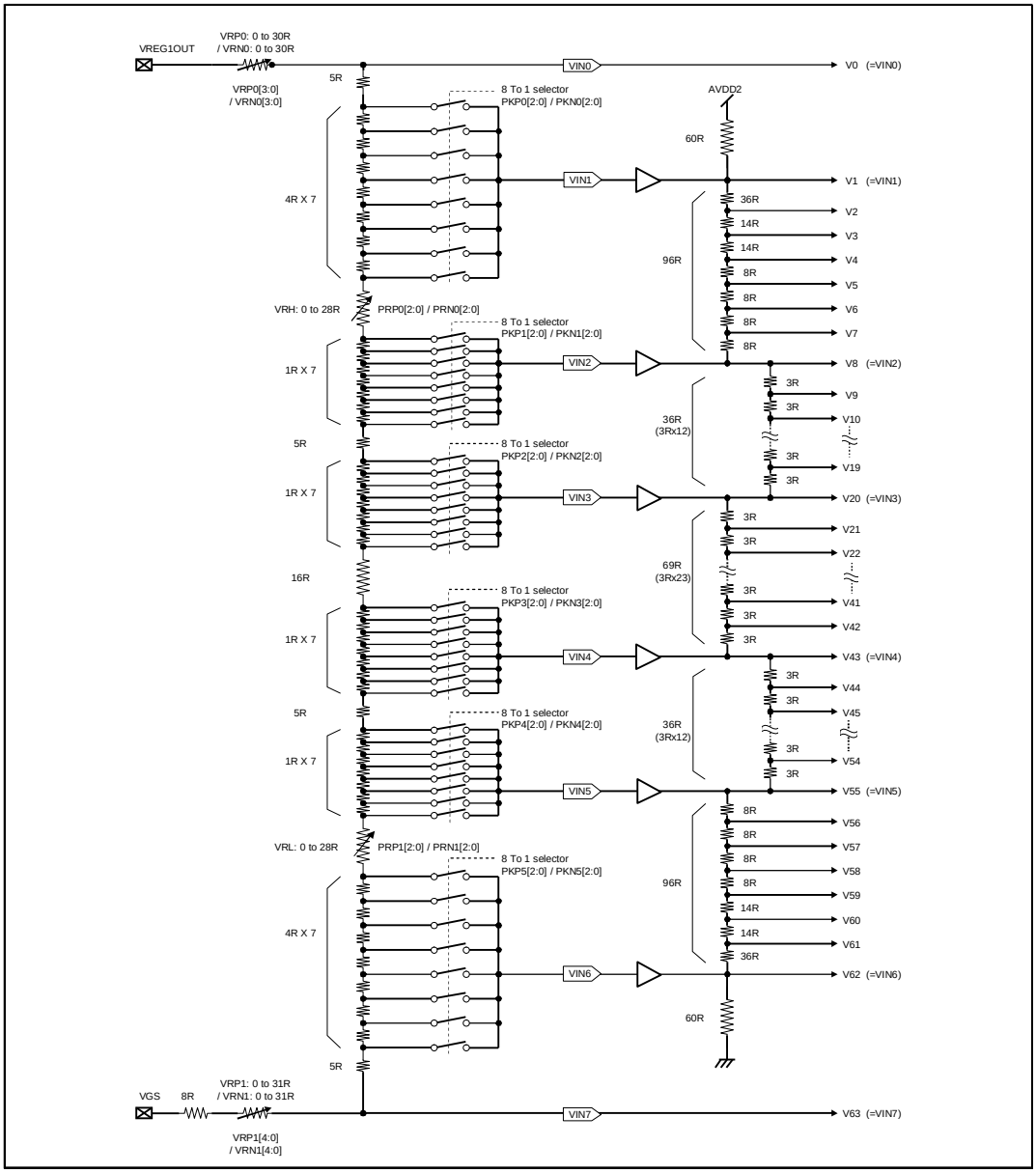


Figure 18-3: Reference voltage generating block (ladder resistor units and 8-to-1 selectors)

18.2. Gamma Correction Register

The gamma-correction registers of the MC2TA7402 consist of gradient adjustment, amplitude adjustment, reference adjustment and micro adjustment registers. Each register has registers of positive and negative polarities. Each register group can be set independently to others, enabling adjustment of grayscale voltage levels in relation to grayscales set optimally for gamma-characteristics of a liquid crystal panel. These gamma-correction register settings and the reference levels of the 64 grayscales to which each of the three adjustments (bold lines in the following figure) is made are common to all RGB pixels.

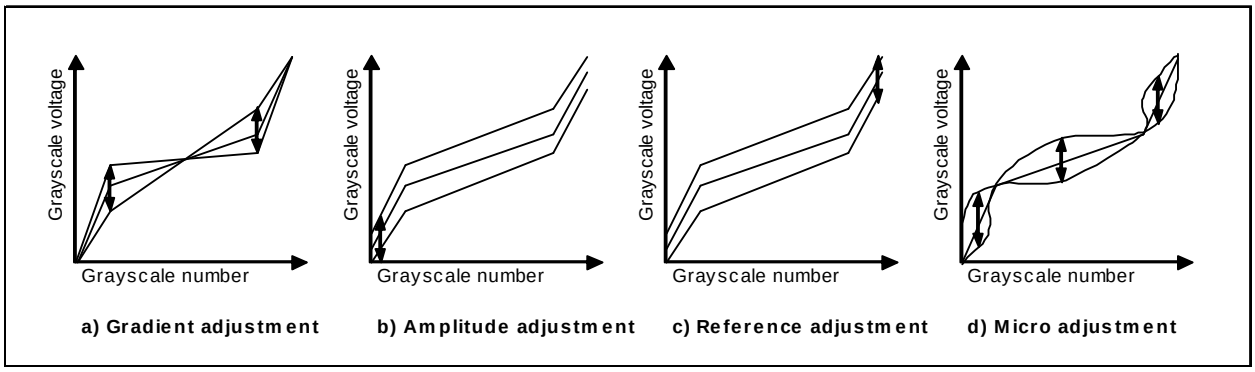


Figure 18-4:

a) Gradient adjustment resistor

The gradient adjustment resistors are used to adjust the gradient in the middle of the grayscale characteristics for the voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistor (VRHP (N) / VRLP (N)) of the ladder resistor for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

b) Amplitude adjustment resistor

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP (N)) of the ladder resistor for the grayscale voltage generator located at lower side of the ladder resistor. (Adjust upper side by input VREG1OUT level.) Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

c) Reference adjustment resistor

The Reference-adjusting resistor is to adjust reference of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP(N)0) of the ladder resistor for the grayscale voltage generator located at upper side of the ladder resistor.

d) Micro adjustment resistor

The micro adjustment resistor is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls the each reference voltage level by the 8 to 1 selector towards the 8-leveled reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

Table 18-1:

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0 [2:0]	PRN0 [2:0]	Variable resister VRHP (N)
	PRP1 [2:0]	PRN1 [2:0]	Variable resister VRLP (N)
Amplitude adjustment	VRP1 [3:0]	VRN0 [3:0]	Variable resister VRP (N) 1
Reference adjustment	VRP0 [4:0]	VRN1 [4:0]	Variable resister VRP (N) 0
Micro adjustment	PKP0 [2:0]	PKN0 [2:0]	8-to-1 selector (voltage level of grayscale 1)
	PKP1 [2:0]	PKN1 [2:0]	8-to-1 selector (voltage level of grayscale 8)
	PKP2 [2:0]	PKN2 [2:0]	8-to-1 selector (voltage level of grayscale 20)
	PKP3 [2:0]	PKN3 [2:0]	8-to-1 selector (voltage level of grayscale 43)
	PKP4 [2:0]	PKN4 [2:0]	8-to-1 selector (voltage level of grayscale 55)
	PKP5 [2:0]	PKN5 [2:0]	8-to-1 selector (voltage level of grayscale 62)

18.3. Ladder Resistors and 8-to-1 Selector

Block configuration

As Figure 18-3 shows, the reference voltage generating unit consists of a ladder resistor unit that can switch 4R. The ladder resistor unit includes variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the gamma correction registers. This unit has pins to connect a volume resistor externally to compensate the differences in characteristics of various panels.

18.4. Variable Resistors

The MC2TA7402 uses variable resistors of the following three types: gradient adjustment (VRHP(N)/VRLP(N)), amplitude adjustment (1) (VRP(N)0), and the amplitude adjustment (2) (VRP(N)1). The resistance values of these variable resistors are set by the gradient adjustment registers and amplitude adjustment registers as follows.

Table 18-2:

Gradient adjustment	
Register Value PRP(N) 0/1 [2:0]	Resistance VRHP (N) VRLP (N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 18-3:

Amplitude adjustment	
Register Value VRP(N) 1 [3:0]	Resistance VRP (N) 1
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

Table 18-4:

Reference adjustment	
Register Value VRP(N) 0 [4:0]	Resistance VRP (N) 0
0000	0R
0001	2R
0010	4R
:	:
:	:
1101	26R
1110	28R
1111	30R

18.5. 8-to-1 selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register, and output the selected voltage level as a reference grayscale voltage (VINP(N)1 to VINP(N 6).
The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

Table 18-5: Micro adjustment registers and selected voltage

The value of Register PKP (N) [2:0]	Selected Voltage					
	VINP (N) 1	VINP (N) 2	VINP (N) 3	VINP (N) 4	VINP (N) 5	VINP (N) 6
000	KVP (N) 1	KVP (N) 9	KVP (N) 17	KVP (N) 25	KVP (N) 33	KVP (N) 41
001	KVP (N) 2	KVP (N) 10	KVP (N) 18	KVP (N) 26	KVP (N) 34	KVP (N) 42
010	KVP (N) 3	KVP (N) 11	KVP (N) 19	KVP (N) 27	KVP (N) 35	KVP (N) 43
011	KVP (N) 4	KVP (N) 12	KVP (N) 20	KVP (N) 28	KVP (N) 36	KVP (N) 44
100	KVP (N) 5	KVP (N) 13	KVP (N) 21	KVP (N) 29	KVP (N) 37	KVP (N) 45
101	KVP (N) 6	KVP (N) 14	KVP (N) 22	KVP (N) 30	KVP (N) 38	KVP (N) 46
110	KVP (N) 7	KVP (N) 15	KVP (N) 23	KVP (N) 31	KVP (N) 39	KVP (N) 47
111	KVP (N) 8	KVP (N) 16	KVP (N) 24	KVP (N) 32	KVP (N) 40	KVP (N) 48

The grayscale voltage levels for V0-V64 grayscales are calculated from the following formulae.

Table 18-6: Formulae for calculating voltage (Positive polarity)

Pins	Formula	Micro adjustment register value	Reference voltage
KVP0	VREG1OUT-ΔV*VRP0/SUMRP	-	VINP0
KVP1	VREG1OUT-ΔV*(VRP0+5R)/SUMRP	PKP0[2:0] = “000”	VINP1
KVP2	VREG1OUT-ΔV*(VRP0+9R)/SUMRP	PKP0[2:0] = “001”	
KVP3	VREG1OUT-ΔV*(VRP0+13R)/SUMRP	PKP0[2:0] = “010”	
KVP4	VREG1OUT-ΔV*(VRP0+17R)/SUMRP	PKP0[2:0] = “011”	
KVP5	VREG1OUT-ΔV*(VRP0+21R)/SUMRP	PKP0[2:0] = “100”	
KVP6	VREG1OUT-ΔV*(VRP0+25R)/SUMRP	PKP0[2:0] = “101”	
KVP7	VREG1OUT-ΔV*(VRP0+29R)/SUMRP	PKP0[2:0] = “110”	
KVP8	VREG1OUT-ΔV*(VRP0+33R)/SUMRP	PKP0[2:0] = “111”	
KVP9	VREG1OUT-ΔV*(VRP0+33R+VRHP)/SUMRP	PKP1[2:0] = “000”	VINP2
KVP10	VREG1OUT-ΔV*(VRP0+34R+VRHP)/SUMRP	PKP1[2:0] = “001”	
KVP11	VREG1OUT-ΔV*(VRP0+35R+VRHP)/SUMRP	PKP1[2:0] = “010”	
KVP12	VREG1OUT-ΔV*(VRP0+36R+VRHP)/SUMRP	PKP1[2:0] = “011”	
KVP13	VREG1OUT-ΔV*(VRP0+37R+VRHP)/SUMRP	PKP1[2:0] = “100”	
KVP14	VREG1OUT-ΔV*(VRP0+38R+VRHP)/SUMRP	PKP1[2:0] = “101”	
KVP15	VREG1OUT-ΔV*(VRP0+39R+VRHP)/SUMRP	PKP1[2:0] = “110”	
KVP16	VREG1OUT-ΔV*(VRP0+40R+VRHP)/SUMRP	PKP1[2:0] = “111”	
KVP17	VREG1OUT-ΔV*(VRP0+45R+VRHP)/SUMRP	PKP2[2:0] = “000”	VINP3
KVP18	VREG1OUT-ΔV*(VRP0+46R+VRHP)/SUMRP	PKP2[2:0] = “001”	
KVP19	VREG1OUT-ΔV*(VRP0+47R+VRHP)/SUMRP	PKP2[2:0] = “010”	
KVP20	VREG1OUT-ΔV*(VRP0+48R+VRHP)/SUMRP	PKP2[2:0] = “011”	
KVP21	VREG1OUT-ΔV*(VRP0+49R+VRHP)/SUMRP	PKP2[2:0] = “100”	
KVP22	VREG1OUT-ΔV*(VRP0+50R+VRHP)/SUMRP	PKP2[2:0] = “101”	
KVP23	VREG1OUT-ΔV*(VRP0+51R+VRHP)/SUMRP	PKP2[2:0] = “110”	
KVP24	VREG1OUT-ΔV*(VRP0+52R+VRHP)/SUMRP	PKP2[2:0] = “111”	
KVP25	VREG1OUT-ΔV*(VRP0+68R+VRHP)/SUMRP	PKP3[2:0] = “000”	VINP4
KVP26	VREG1OUT-ΔV*(VRP0+69R+VRHP)/SUMRP	PKP3[2:0] = “001”	
KVP27	VREG1OUT-ΔV*(VRP0+70R+VRHP)/SUMRP	PKP3[2:0] = “010”	
KVP28	VREG1OUT-ΔV*(VRP0+71R+VRHP)/SUMRP	PKP3[2:0] = “011”	
KVP29	VREG1OUT-ΔV*(VRP0+72R+VRHP)/SUMRP	PKP3[2:0] = “100”	
KVP30	VREG1OUT-ΔV*(VRP0+73R+VRHP)/SUMRP	PKP3[2:0] = “101”	
KVP31	VREG1OUT-ΔV*(VRP0+74R+VRHP)/SUMRP	PKP3[2:0] = “110”	
KVP32	VREG1OUT-ΔV*(VRP0+75R+VRHP)/SUMRP	PKP3[2:0] = “111”	
KVP33	VREG1OUT-ΔV*(VRP0+80R+VRHP)/SUMRP	PKP4[2:0] = “000”	VINP5
KVP34	VREG1OUT-ΔV*(VRP0+81R+VRHP)/SUMRP	PKP4[2:0] = “001”	
KVP35	VREG1OUT-ΔV*(VRP0+82R+VRHP)/SUMRP	PKP4[2:0] = “010”	
KVP36	VREG1OUT-ΔV*(VRP0+83R+VRHP)/SUMRP	PKP4[2:0] = “011”	
KVP37	VREG1OUT-ΔV*(VRP0+84R+VRHP)/SUMRP	PKP4[2:0] = “100”	
KVP38	VREG1OUT-ΔV*(VRP0+85R+VRHP)/SUMRP	PKP4[2:0] = “101”	
KVP39	VREG1OUT-ΔV*(VRP0+86R+VRHP)/SUMRP	PKP4[2:0] = “110”	
KVP40	VREG1OUT-ΔV*(VRP0+87R+VRHP)/SUMRP	PKP4[2:0] = “111”	
KVP41	VREG1OUT-ΔV*(VRP0+87R+VRHP+VRLP)/SUMRP	PKP5[2:0] = “000”	VINP6
KVP42	VREG1OUT-ΔV*(VRP0+91R+VRHP+VRLP)/SUMRP	PKP5[2:0] = “001”	
KVP43	VREG1OUT-ΔV*(VRP0+95R+VRHP+VRLP)/SUMRP	PKP5[2:0] = “010”	
KVP44	VREG1OUT-ΔV*(VRP0+99R+VRHP+VRLP)/SUMRP	PKP5[2:0] = “011”	
KVP45	VREG1OUT-ΔV*(VRP0+103R+VRHP+VRLP)/SUMRP	PKP5[2:0] = “100”	
KVP46	VREG1OUT-ΔV*(VRP0+107R+VRHP+VRLP)/SUMRP	PKP5[2:0] = “101”	
KVP47	VREG1OUT-ΔV*(VRP0+111R+VRHP+VRLP)/SUMRP	PKP5[2:0] = “110”	
KVP48	VREG1OUT-ΔV*(VRP0+115R+VRHP+VRLP)/SUMRP	PKP5[2:0] = “111”	
KVP49	VREG1OUT-ΔV*(VRP0+120R+VRHP+VRLP)/SUMRP	-	VINP7

SUMRP: Total of the positive polarity ladder resistance = VRP0 + 128R + VRHP + VRLP + VRP1

SUMRN: Total of the negative polarity ladder resistance = VRN0 + 128R + VRHN + VRLN + VRN1

ΔV: Electric potential difference between VREG1OUT and VGS = VREG1OUT*[SUMRP(N)/([SUMRP(N)+EXVR])

Table 18-7: Formulae for calculating voltage (Positive polarity)

Grayscale voltage	Formula
V0	VINP0
V1	VINP1
V2	V8+(V1-V8)*(30/48)
V3	V8+(V1-V8)*(23/48)
V4	V8+(V1-V8)*(16/48)
V5	V8+(V1-V8)*(12/48)
V6	V8+(V1-V8)*(8/48)
V7	V8+(V1-V8)*(4/48)
V8	VINP2
V9	V20+(V8-V20)*(11/12)
V10	V20+(V8-V20)*(10/12)
V11	V20+(V8-V20)*(9/12)
V12	V20+(V8-V20)*(8/12)
V13	V20+(V8-V20)*(7/12)
V14	V20+(V8-V20)*(6/12)
V15	V20+(V8-V20)*(5/12)
V16	V20+(V8-V20)*(4/12)
V17	V20+(V8-V20)*(3/12)
V18	V20+(V8-V20)*(2/12)
V19	V20+(V8-V20)*(1/12)
V20	VINP3
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VINP4
V44	V55+(V43-V55)*(11/12)
V45	V55+(V43-V55)*(10/12)
V46	V55+(V43-V55)*(9/12)
V47	V55+(V43-V55)*(8/12)
V48	V55+(V43-V55)*(7/12)
V49	V55+(V43-V55)*(6/12)
V50	V55+(V43-V55)*(5/12)
V51	V55+(V43-V55)*(4/12)
V52	V55+(V43-V55)*(3/12)
V53	V55+(V43-V55)*(2/12)
V54	V55+(V43-V55)*(1/12)
V55	VINP5
V56	V62+(V55-V62)*(44/48)
V57	V62+(V55-V62)*(40/48)
V58	V62+(V55-V62)*(36/48)
V59	V62+(V55-V62)*(32/48)
V60	V62+(V55-V62)*(25/48)
V61	V62+(V55-V62)*(18/48)
V62	VINP6
V63	VINP7

Note: The following relations must be retained: V63-VSS(GND level)>0.3V, V0<VREG1OUT-0.3V.

Table 18-8: Formulae for calculating voltage (Negative polarity)

Pins	Formula	Micro adjustment register value	Reference Voltage
KVN0	VREG1OUT-ΔV*VRN0/SUMRN	-	VINN0
KVN1	VREG1OUT-ΔV*(VRN0+5R)/SUMRN	PKN0[2:0] = “000”	VINN1
KVN2	VREG1OUT-ΔV*(VRN0+9R)/SUMRN	PKN0[2:0] = “001”	
KVN3	VREG1OUT-ΔV*(VRN0+13R)/SUMRN	PKN0[2:0] = “010”	
KVN4	VREG1OUT-ΔV*(VRN0+17R)/SUMRN	PKN0[2:0] = “011”	
KVN5	VREG1OUT-ΔV*(VRN0+21R)/SUMRN	PKN0[2:0] = “100”	
KVN6	VREG1OUT-ΔV*(VRN0+25R)/SUMRN	PKN0[2:0] = “101”	
KVN7	VREG1OUT-ΔV*(VRN0+29R)/SUMRN	PKN0[2:0] = “110”	
KVN8	VREG1OUT-ΔV*(VRN0+33R)/SUMRN	PKN0[2:0] = “111”	
KVN9	VREG1OUT-ΔV*(VRN0+33R+VRHN)/SUMRN	PKN1[2:0] = “000”	VINN2
KVN10	VREG1OUT-ΔV*(VRN0+34R+VRHN)/SUMRN	PKN1[2:0] = “001”	
KVN11	VREG1OUT-ΔV*(VRN0+35R+VRHN)/SUMRN	PKN1[2:0] = “010”	
KVN12	VREG1OUT-ΔV*(VRN0+36R+VRHN)/SUMRN	PKN1[2:0] = “011”	
KVN13	VREG1OUT-ΔV*(VRN0+37R+VRHN)/SUMRN	PKN1[2:0] = “100”	
KVN14	VREG1OUT-ΔV*(VRN0+38R+VRHN)/SUMRN	PKN1[2:0] = “101”	
KVN15	VREG1OUT-ΔV*(VRN0+39R+VRHN)/SUMRN	PKN1[2:0] = “110”	
KVN16	VREG1OUT-ΔV*(VRN0+40R+VRHN)/SUMRN	PKN1[2:0] = “111”	
KVN17	VREG1OUT-ΔV*(VRN0+45R+VRHN)/SUMRN	PKN2[2:0] = “000”	VINN3
KVN18	VREG1OUT-ΔV*(VRN0+46R+VRHN)/SUMRN	PKN2[2:0] = “001”	
KVN19	VREG1OUT-ΔV*(VRN0+47R+VRHN)/SUMRN	PKN2[2:0] = “010”	
KVN20	VREG1OUT-ΔV*(VRN0+48R+VRHN)/SUMRN	PKN2[2:0] = “011”	
KVN21	VREG1OUT-ΔV*(VRN0+49R+VRHN)/SUMRN	PKN2[2:0] = “100”	
KVN22	VREG1OUT-ΔV*(VRN0+50R+VRHN)/SUMRN	PKN2[2:0] = “101”	
KVN23	VREG1OUT-ΔV*(VRN0+51R+VRHN)/SUMRN	PKN2[2:0] = “110”	
KVN24	VREG1OUT-ΔV*(VRN0+52R+VRHN)/SUMRN	PKN2[2:0] = “111”	
KVN25	VREG1OUT-ΔV*(VRN0+68R+VRHN)/SUMRN	PKN3[2:0] = “000”	VINN4
KVN26	VREG1OUT-ΔV*(VRN0+69R+VRHN)/SUMRN	PKN3[2:0] = “001”	
KVN27	VREG1OUT-ΔV*(VRN0+70R+VRHN)/SUMRN	PKN3[2:0] = “010”	
KVN28	VREG1OUT-ΔV*(VRN0+71R+VRHN)/SUMRN	PKN3[2:0] = “011”	
KVN29	VREG1OUT-ΔV*(VRN0+72R+VRHN)/SUMRN	PKN3[2:0] = “100”	
KVN30	VREG1OUT-ΔV*(VRN0+73R+VRHN)/SUMRN	PKN3[2:0] = “101”	
KVN31	VREG1OUT-ΔV*(VRN0+74R+VRHN)/SUMRN	PKN3[2:0] = “110”	
KVN32	VREG1OUT-ΔV*(VRN0+75R+VRHN)/SUMRN	PKN3[2:0] = “111”	
KVN33	VREG1OUT-ΔV*(VRN0+80R+VRHN)/SUMRN	PKN4[2:0] = “000”	VINN5
KVN34	VREG1OUT-ΔV*(VRN0+81R+VRHN)/SUMRN	PKN4[2:0] = “001”	
KVN35	VREG1OUT-ΔV*(VRN0+82R+VRHN)/SUMRN	PKN4[2:0] = “010”	
KVN36	VREG1OUT-ΔV*(VRN0+83R+VRHN)/SUMRN	PKN4[2:0] = “011”	
KVN37	VREG1OUT-ΔV*(VRN0+84R+VRHN)/SUMRN	PKN4[2:0] = “100”	
KVN38	VREG1OUT-ΔV*(VRN0+85R+VRHN)/SUMRN	PKN4[2:0] = “101”	
KVN39	VREG1OUT-ΔV*(VRN0+86R+VRHN)/SUMRN	PKN4[2:0] = “110”	
KVN40	VREG1OUT-ΔV*(VRN0+87R+VRHN)/SUMRN	PKN4[2:0] = “111”	
KVN41	VREG1OUT-ΔV*(VRN0+87R+VRHN+VRLN)/SUMRN	PKN5[2:0] = “000”	VINN6
KVN42	VREG1OUT-ΔV*(VRN0+91R+VRHN+VRLN)/SUMRN	PKN5[2:0] = “001”	
KVN43	VREG1OUT-ΔV*(VRN0+95R+VRHN+VRLN)/SUMRN	PKN5[2:0] = “010”	
KVN44	VREG1OUT-ΔV*(VRN0+99R+VRHN+VRLN)/SUMRN	PKN5[2:0] = “011”	
KVN45	VREG1OUT-ΔV*(VRN0+103R+VRHN+VRLN)/SUMRN	PKN5[2:0] = “100”	
KVN46	VREG1OUT-ΔV*(VRN0+107R+VRHN+VRLN)/SUMRN	PKN5[2:0] = “101”	
KVN47	VREG1OUT-ΔV*(VRN0+111R+VRHN+VRLN)/SUMRN	PKN5[2:0] = “110”	
KVN48	VREG1OUT-ΔV*(VRN0+115R+VRHN+VRLN)/SUMRN	PKN5[2:0] = “111”	
KVN49	VREG1OUT-ΔV*(VRN0+120R+VRHN+VRLN)/SUMRN	-	VINN7

SUMRP: Total of the positive polarity ladder resistance = VRP0 + 128R + VRHP + VRLP + VRP1

SUMRN: Total of the negative polarity ladder resistance = VRN0 + 128R + VRHN + VRLN + VRN1

ΔV: Electric potential difference between VREG1OUT and VGS = VREG1OUT*[SUMRP(N)/([SUMRP(N)+EXVR)]

Table 18-9: Formulae for calculating voltage (Negative polarity)

Grayscale voltage	Formula
V0	VINN0
V1	VINN1
V2	V8+(V1-V8)*(30/48)
V3	V8+(V1-V8)*(23/48)
V4	V8+(V1-V8)*(16/48)
V5	V8+(V1-V8)*(12/48)
V6	V8+(V1-V8)*(8/48)
V7	V8+(V1-V8)*(4/48)
V8	VINN2
V9	V20+(V8-V20)*(11/12)
V10	V20+(V8-V20)*(10/12)
V11	V20+(V8-V20)*(9/12)
V12	V20+(V8-V20)*(8/12)
V13	V20+(V8-V20)*(7/12)
V14	V20+(V8-V20)*(6/12)
V15	V20+(V8-V20)*(5/12)
V16	V20+(V8-V20)*(4/12)
V17	V20+(V8-V20)*(3/12)
V18	V20+(V8-V20)*(2/12)
V19	V20+(V8-V20)*(1/12)
V20	VINN3
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VINN4
V44	V55+(V43-V55)*(11/12)
V45	V55+(V43-V55)*(10/12)
V46	V55+(V43-V55)*(9/12)
V47	V55+(V43-V55)*(8/12)
V48	V55+(V43-V55)*(7/12)
V49	V55+(V43-V55)*(6/12)
V50	V55+(V43-V55)*(5/12)
V51	V55+(V43-V55)*(4/12)
V52	V55+(V43-V55)*(3/12)
V53	V55+(V43-V55)*(2/12)
V54	V55+(V43-V55)*(1/12)
V55	VINN5
V56	V62+(V55-V62)*(44/48)
V57	V62+(V55-V62)*(40/48)
V58	V62+(V55-V62)*(36/48)
V59	V62+(V55-V62)*(32/48)
V60	V62+(V55-V62)*(25/48)
V61	V62+(V55-V62)*(18/48)
V62	VINN6
V63	VINN7

Note: The following relations must be retained: V63-VSS(GND level)>0.3V, V0<VREG1OUT-0.3V.

18.6. Relationship between DDRAM Data and Voltage Output Levels

The relationship between DDRAM data and source output voltage levels is as follows.
(In case of a normally-white panel)

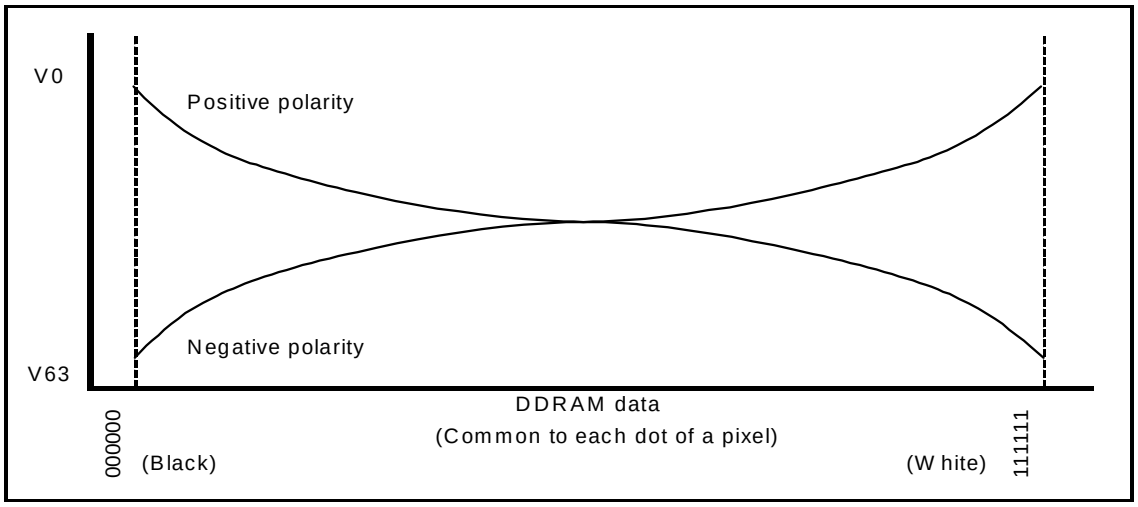


Figure 18-5: DDRAM data and the output voltage

19. 8-Color Display Mode

The MC2TA7402 has a function to display in 8 colors. In 8-color mode, the available grayscale levels are V0 and V63, and the power supplies of other grayscales (V1-V62) are halted to reduce the power consumption.

The gamma-correction registers, PKP0-PKP5 and PKN0-PKN5, are disabled in 8-color display mode. Since power supplies for V1-V62 are halted, the RGB data in the internal DDRAM should be rewritten to either "000000" or "111111" to select either the V0 or V63 level before setting this mode.

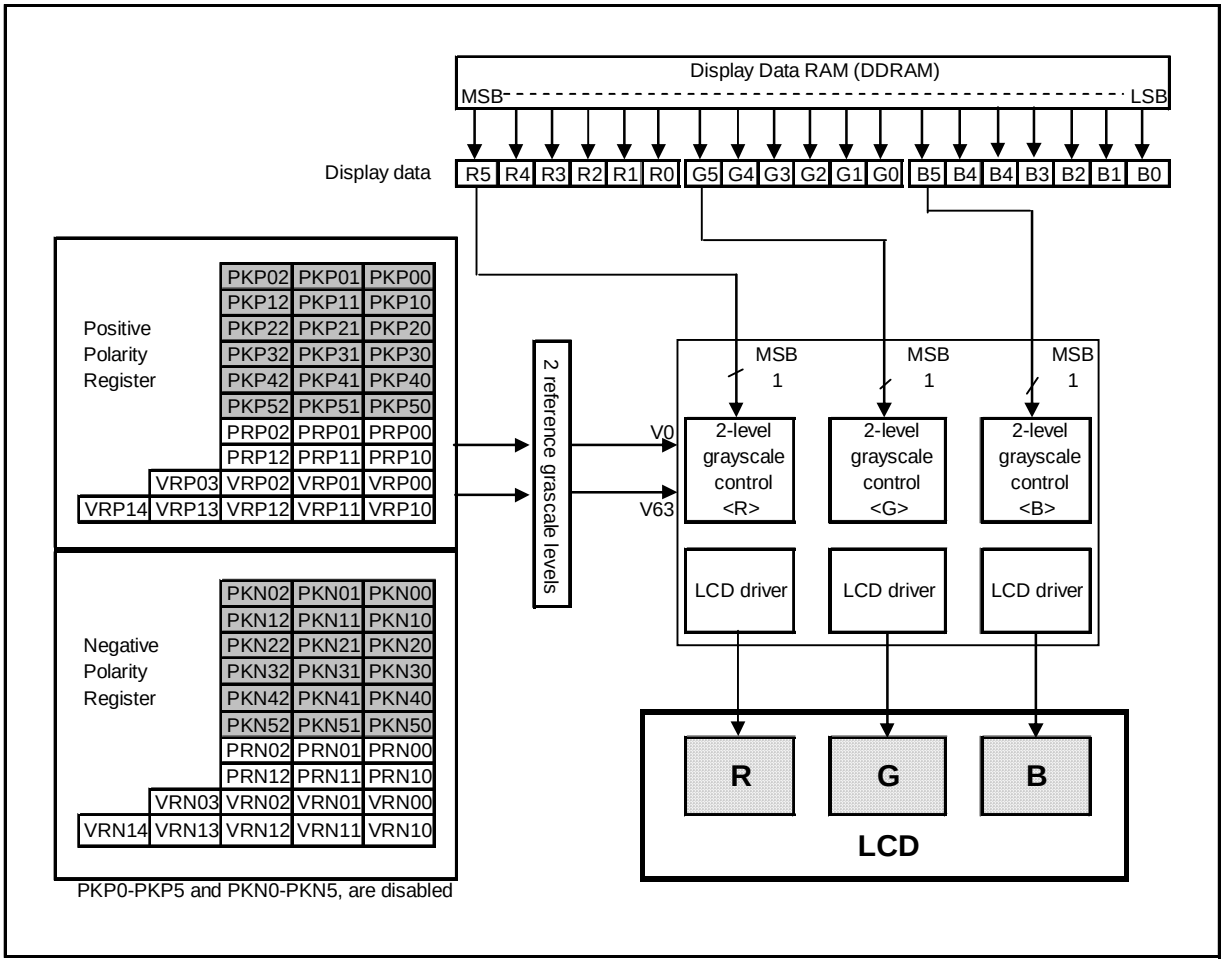


Figure 19-1:

To switch between the 262, 144-color and 8-color modes, follow the sequences below.

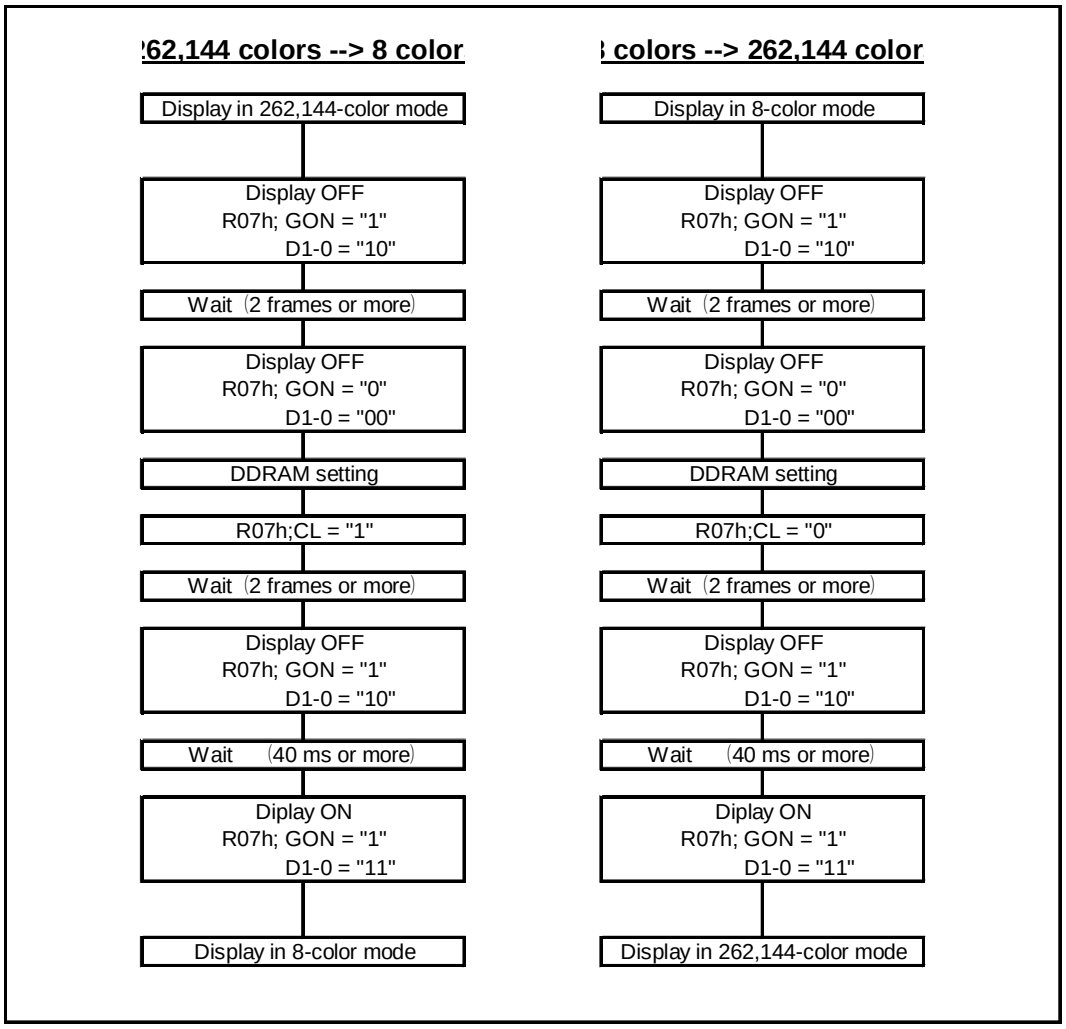


Figure 19-2:

20. Partial Display Function

The MC2TA7402 allows selectively driving two images on the screen at arbitrary positions set in the screen-drive position registers (R42h and R43h). Only the lines for displaying two images are selectively driven in order to reduce the current consumption.

The first display drive position register (R42h) includes the start line setting bits (SS17-10) and the end line setting bits (SE17-10) for displaying the first image. The second display drive position register (R43h) includes the start line setting bits (SS27-20) and the end line setting bits (SE27-20) for displaying the second image. The second display control is effective when the R07h;SPT bit is set to "1". The total number of lines driven for displaying the first and second displays must be less than the number of lines set with the R01h;NL4-0 bits.

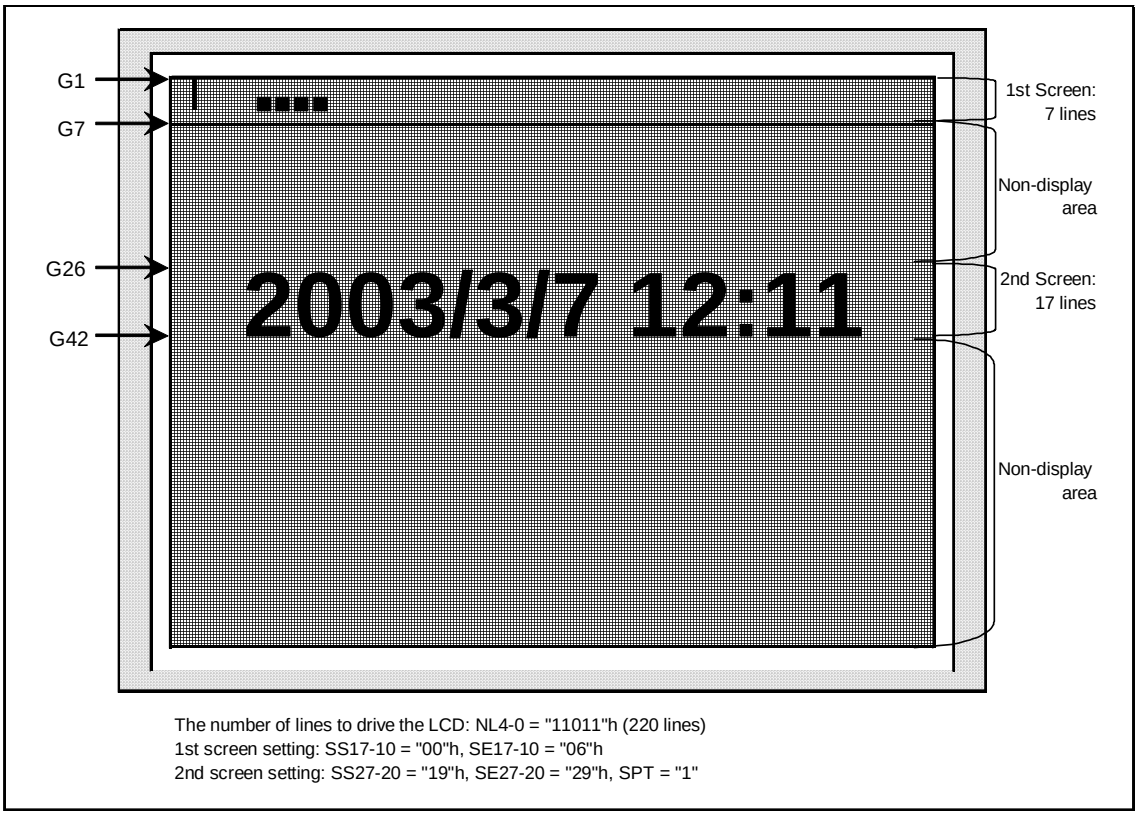


Figure 20-1:

20.1. Constraints in Setting the 1st/2nd Screen Drive Position Resister

When setting the start line setting bits (SS17-10) and the end line setting bits (SE17-10) of the first display drive position register (R42h), and the start line setting bits (SS27-20) and the end line setting bits (SE27-20) of the second display drive position register (R43h), it is necessary to satisfy the following conditions to display screens correctly.

Table 20-1: One Screen Drive (R07h;SPT = "0")

Register Settings	Display Operation
R42h;(SE17-10) - (SS17-10) = NL	Full screen display The area of (SE17-10) - (SS17-10) is normally displayed.
R42h;(SE17-10) - (SS17-10) < NL	Partial screen display
The area of (SE17-10) - (SS17-10) is normally displayed. The rest of the area is a white display irrespective of the data in the DDRAM.	
R42h;(SE17-10) - (SS17-10) > NL	Setting disabled

Note 1) SS17-10 ≤ SE17-0 ≤ “DB”h (when the gate is 220).
Note 2) SS27-20 and SE27-20 are disabled when SPT = "0".
Note 3) LCD drive lines set by the R01h;NL4-0 bits

Table 20-2: Two Screen Drive (R07h;SPT = "1")

Register Settings	Display Operation
((SE17-10) - (SS17-10)) + ((SE27-20) - (SS27-20)) = NL	Full screen display The area of (SE27-20) - (SS17-10) is normally displayed.
((SE17-10) - (SS17-10)) + ((SE27-20) - (SS27-20)) < NL	Partial screen display The area of (SE17-10) - (SS17-10) is normally displayed. The area of (SE27-10) - (SS27-20) is normally displayed. The rest of the area is a white display irrespective of the data in the DDRAM.
((SE17-10) - (SS17-10)) + ((SE27-20) - (SS27-20)) > NL	Setting disabled

Note 1) SS17-10 ≤ SE17-10 < SS27-20 ≤ SE27-20 ≤ "DB"h (when the gate is 220)
Note 2) Make sure that ((SE27-20) - (SS17-10)) ≤ NL.

The outputs from the source driver in non-display areas of the partial display can be changed as follows by setting the R07h;PT1-0 bits. Select the appropriate kind of source outputs according to the characteristics of the display panel.

Table 20-3: Source outputs in non-display areas

PT1	PT0	Source Output		VCOM Output				Gate Output
				R09h; PTG2=0		R09h; PTG2=1		
		Positive	Negative	Positive	Negative	Positive	Negative	
0	0	VSS(GND level)	VSS(GND level)	VSS(GND level)	VSS(GND level)	Keep the final level of display area		R09h; PTG1-0 setting
0	1	V63	V0	VCOMH	VCOML			
1	0	V0	V63	VCOMH	VCOML			
1	1	Hi-Z	Hi-Z	VSS(GND level)	VSS(GND level)			

Follow the sequences below when using the partial display function.

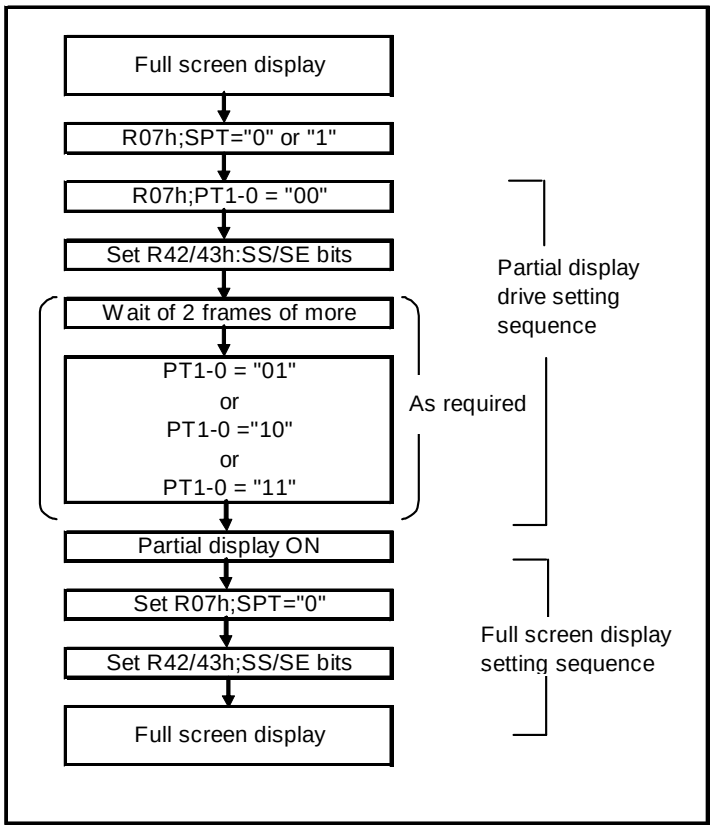


Figure 20-2:

21. Liquid Crystal AC Drive Function

The MC2TA7402 supports three kinds of liquid crystal AC drive function. It is defined by setting LCD driver AC control register (R02h) as Table 21-1.

Table 21-1:

FLD1-0	B/C	EOR	Operation
01	0	x	Frame Reversed AC driving
	1	1	1-line Reversed AC driving
11	0	x	3-field Interlaced driving

Note) x: don't care

21.1. Frame Reversed AC Drive Function

The MC2TA7402 supports the frame reversed AC drive function. In frame reversed AC driving, the polarity of liquid crystal is inverted in each frame.

21.2. 1-line Reversed AC Drive Function

In addition to the frame reversed AC drive function, the MC2TA7402 supports the 1-line reversed AC drive function. In 1-line reversed AC driving, the polarity of liquid crystal is inverted in each line. The 1-line reversed AC drive function is for overcoming problems associated with the quality of display.

Note that setting 1-line reversed AC drive function will raise the frequency of liquid crystal polarity inversion and increase charging/discharging current on liquid crystal cells.

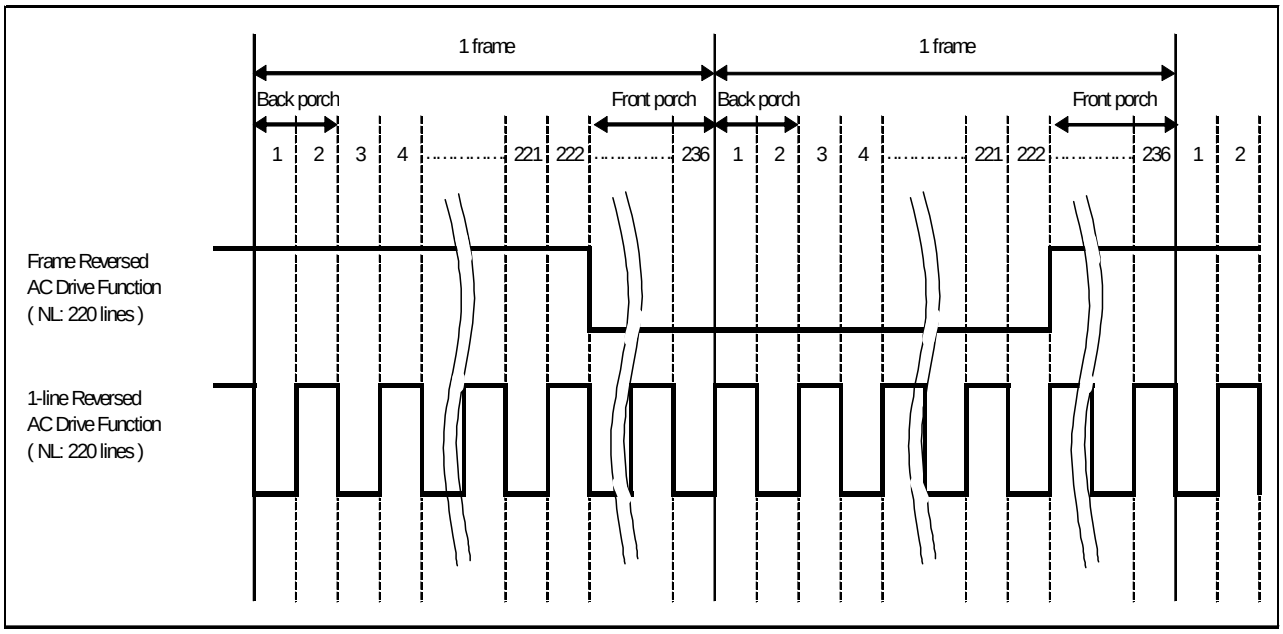


Figure 21-1:

21.3. 3-field Interlaced Scan

The MC2TA7402 supports the interlaced scan function for driving a frame by splitting it into n fields in order to prevent flicker. The following tables show the scan (gate) lines in each field. When FLD1-0="01", the number of fields in a frame is one. When FLD1-0="11", the number of fields in a frame is three. The figure illustrates the output waveforms of the 3-field interlaced scan.

Table 21-2: Gate=220

GS = "0"

FLD1-0		01	11		
Gate \ Field		-	1	2	3
G1		o	o		
G2		o		o	
G3		o			o
G4		o	o		
G5		o		o	
G6		o			o
G7		o	o		
G8		o		o	
G9		o			o
:		:	:	:	:
G217		o			o
G218		o	o		
G219		o		o	
G220		o			o

GS = "1"

FLD1-0		01	11		
Gate \ Field		-	1	2	3
G220		o	o		
G219		o		o	
G218		o			o
G217		o	o		
G216		o		o	
G215		o			o
G214		o	o		
G213		o		o	
G212		o			o
:		:	:	:	:
G4		o			o
G3		o	o		
G2		o		o	
G1		o			o

Note) o: Scanned gate lines

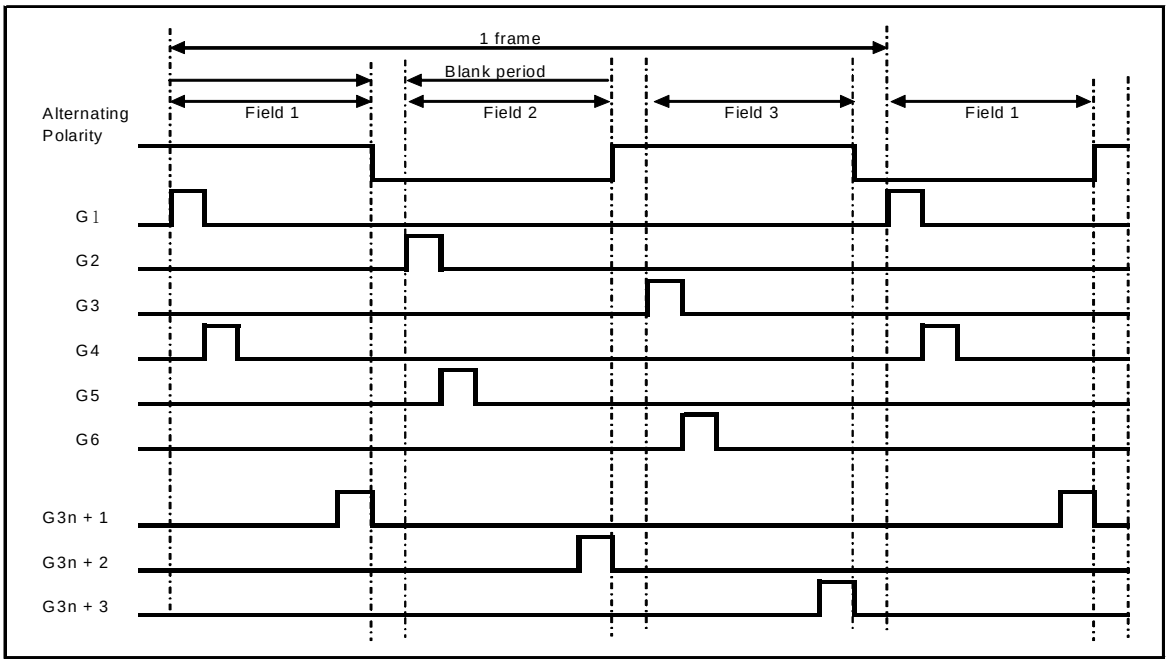


Figure 21-2: Gate output timing of 3-field interlaced scan

22. Alternating Timing

The following figure illustrates the timing of liquid crystal polarity inversion in different driving formulas. In case of the frame-inversion AC drive, the polarity is inverted after drawing one frame, followed by a blank period that lasts for a 16H period. In the blank period, all outputs from the gate lines become the VGL level. In case of the 3-field interlaced scan, the polarity is inverted after drawing one field, followed by a blank period that adds up to a 16H period in one frame. In case of the 1-line inversion AC drive, the polarity is inverted as drawing 1 line, and a blank period that lasts for a 16H period is inserted after drawing one frame.

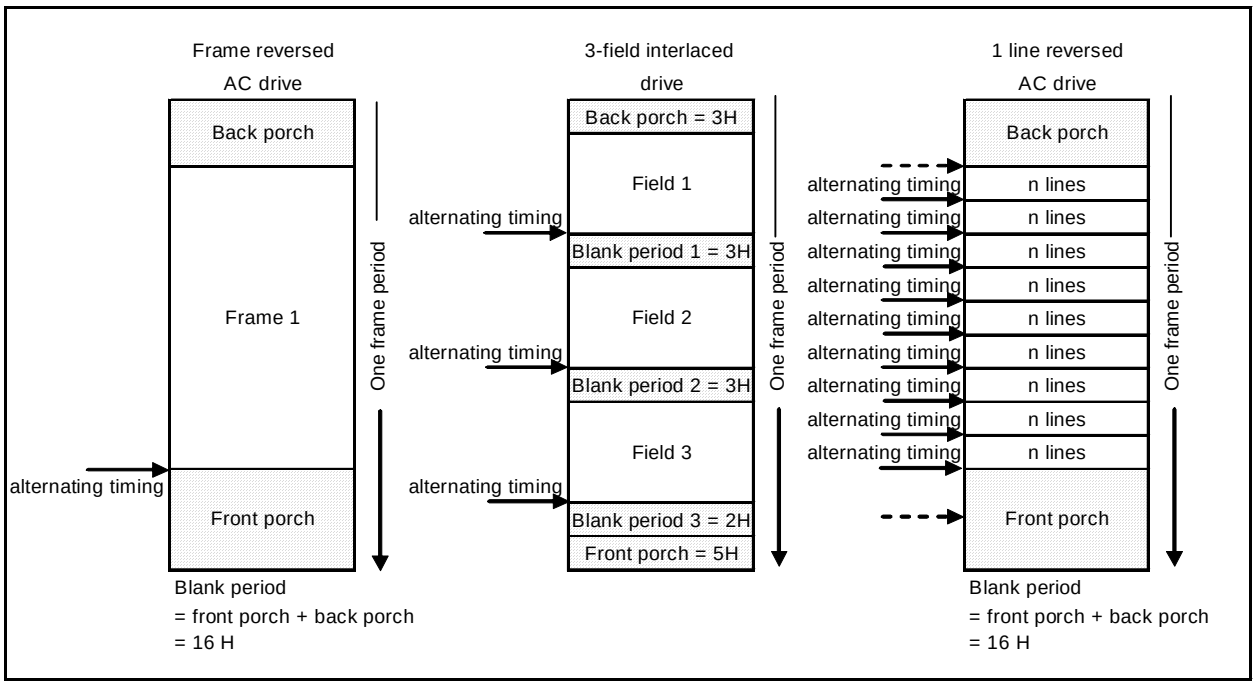


Figure 22-1:

23. Frame- Frequency Adjustment Function

The MC2TA7402 has a frame frequency adjustment function. The frame frequency for driving LCDs can be adjusted by instructions (using the R0Bh;DIV, RTN bits) without changing the oscillation frequency.
To switch frame frequencies between when displaying a moving picture and when displaying a still picture, set a high oscillation frequency in advance. By doing so, it becomes possible to set a low frame frequency when displaying a still picture for saving the power consumption and to set a high frame frequency when displaying a moving picture.

Relationship between Liquid Crystal Drive Duty and Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated from the following formula. The frame frequency is adjusted by instructions using the 1H period adjustment bits (RTN bits) and the operation clock division bits (DIV bits).

Formula to calculate frame frequency:

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per line x division ratio x (Line + BP + FP)}} \quad [\text{Hz}]$$

fosc: frequency of RC oscillation
Line: number of lines for driving liquid crystal (NL bits)
Division ratio: DIV bits
Clock cycles per line: RTN bits
FP: the number of lines for the front porch period
BP: the number of lines for the back porch period

Example of Calculation: when the maximum frame frequency = 60 Hz

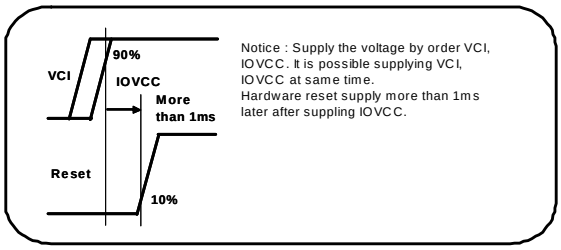
Number of lines to drive the LCD: 220 lines
1H period: 16 clock cycles (R0Bh;RTN1-0 = "00")
Operational clock division ratio: fosc / 1 (R0Bh; DIV1-0 = “00”)
Back/Front porch: 14 lines / 2 lines (R08h;BP3-0 = “1110”, FP3-0 = “0010”)

fosc = 60 Hz × 16 clock × 1/1 × (220 + 14 + 2) lines = 227 (kHz)

In this case, the RC oscillation frequency becomes 227 kHz. The external resistance value of the RC oscillator must be adjusted to be 227 kHz.

24. Power Supply Setting

As for power supply setting, follow the sequence below. The setting time for oscillators, step-up circuits and operational amplifiers depends on the panel's wiring resistance, ACF connection resistance, used capacitance and panel's load. Set according to the actual LCD module.



Power ON sequence

Step	Register	Register Value	Waiting time	Operation
1	Power-on		50ms	Power-on (VCI and IOVCC power supply start)
2	Hardware Reset		10ms	Intializing LSI by using NRESET pin.
User Setting				
3	R01h	xxxxh	-	Driver Output Control (VSPL,HSPL,DPL,EPL,SM,GS,SS,NL4-0)
4	R02h	xxxxh	-	LCD Driver AC Cntrol (FLD1-0,BC, EOR)
5	R03h	xxxxh	-	Entry Mode (TR1,DFM1-0,BGR,I/D1-0,AM)
6	R07h	xx0xh	-	Display Cntrol (1) (PT1-0,VLE1-0,SPT,GON=0,CL,REV, D1-0=00)
7	R08h	xxxxh	-	Display Control (2) (FP3-0,BP3-0)
8	R09h	xxxxh	-	Display Control (3) (PTG2-0,ISC3-0)
9	R0Bh	xxxxh	-	Frame Cycle Adjustment (NO1-0,SDT1-0,ECS2-0,DIV1-0,DCR EX,DCR2-0,RTN1-0)
10	R0Ch	xxxxh	-	RGB/VSYNC Interface (RM,DM1-0,RIM1-0)
11	R21h	xxxxh	-	DDRAM Addess Set (AD15-0)
12	R30h	xxxxh	-	Gamma Control (PKP12-10,PKP02-00)
13	R31h	xxxxh	-	Gamma Control (PKP32-30,PKP22-20)
14	R32h	xxxxh	-	Gamma Control (PKP52-50,PKP42-40)
15	R33h	xxxxh	-	Gamma Control (PRP12-10,PRP02-00)
16	R34h	xxxxh	-	Gamma Control (PKN12-10,PKN02-00)
17	R35h	xxxxh	-	Gamma Control (PKN32-30,PKN22-20)
18	R36h	xxxxh	-	Gamma Control (PKN52-50,PKN42-40)
19	R37h	xxxxh	-	Gamma Control (PRN12-10,PRN02-00)
20	R38h	xxxxh	-	Gamma Control (VRP14-10,VRP03-00)
21	R39h	xxxxh	-	Gamma Control (VRN14-10,VRN03-00)
22	R40h	xxxxh	-	Gate Scan Start Position (SCN)
23	R42h	xxxxh	-	First Screen Drive Position (SE17-10, SS17-10)
24	R43h	xxxxh	-	Second Screen Drive Position (SE27-20,SS27-20)
25	R44h	xxxxh	-	Horizontal DDRAM Address Position (HEA7-0,HSA7-0)
26	R45h	xxxxh	-	Vertical DDRAM Address Position (VEA7-0, VSA7-0)
Initial Power Control Sequence (fosc=285kHz±10%) VCI=VCILVL=2.8V				
27	R11h	2F04h	-	VREG1OUT, VCI1 Setting (GVD5-0=2F, VC1-0=100)
28	R14h	xxxxh	10ms	Power Control (4) (VCMR, VCM5-0,VML5-0)
29	R10h	0580h	-	Power Control (1) (SAP[2:0]=000,BT[2:0]=101,DC[2:0]=100,SLP=0,STB=0)
30	R13h	0040h	40ms	CP1/CP3 ON (PON=1,PON1=0,AON=0)
31	R13h	0060h	40ms	CP2 ON (PON=1, PON1=1,AON=0)
32	R13h	0070h	20ms	AMP ON (PON=1,PON1=1,AON=1)
User Setting for Power Control Registers				
33	R11h	xx04h	10ms	GVD5-0,VC1-0=100
34	R10h	xxx0h	-	Power Control (1) (SAP[2:0],BT[2:0],DC[2:0],SLP=0,STB=0) SAP setting
Start transfering display image data Display ON sequence				
35	R07h	081xh	40ms	PT[1:0]=01,VLE[2:1]=00,SPT=0,GON=1,CL,REV, D[1:0]=10
36	R07h	081xh	40ms	PT[1:0]=01,VLE[2:1]=00,SPT=0,GON=1,CL,REV, D[1:0]=11

"x"stands for "user preference"

Note1) Waiting time on the list is for reference. (variable depending on penel's wiring resistance, ACF conection resistance, FPC wiring
Note2) "Initial Power Control" should not be changed.
Note3) Set the following voltage within the limits : DDVDH=max. 5.5V, VCL=min. -3.3V, VGH=max. 16.5V, VGL=min. -16.5V, VGH-VGL<2

Table 24-1: Power ON Sequence

Power Off sequence

Step	Register	Register Value	Waiting time	Operation
Display OFF sequnce				
1	R07h	081xh	40ms	Display On (PT[1:0]=01,VLE[2:1]=00,SPT=0,GON=1,CL,REV, D[1:0]=10)
2	R07h	080xh	40ms	Display On- Normaly Color (PT[1:0]=01,VLE[2:1]=00,SPT=0,GON=0,CL,REV, D[1:0]=10)
3	R07h	080xh	-	Display Off (PT[1:0]=01,VLE[2:1]=00,SPT=0,GON=0,CL,REV, D[1:0]=00)
Power Off sequence				
4	R10h	0xxxh	-	Source Amp Off (SAP[2:0]=000(halt),BT[2:0], DC[2:0], SLP, STB)
5	R13h	0060h	5ms	CP2 Off (PON=1, PON1=1, AON=0)
6	R13h	0040h	5ms	CP1/CP3 Off (PON=1, PON1=0, AON=0)
7	R13h	0000h	5ms	Amp Off (PON=0, PON1=0, AON=0)

"x"stands for "user preference"

Note) Waiting time on the list is for reference. (variable depending on penel's wiring resistance, ACF conection resistance, FPC wi

Table 24-2: Power OFF Sequence

25. Instruction Setting

When setting the following instructions, follow the sequences below.

25.1. Display ON / OFF

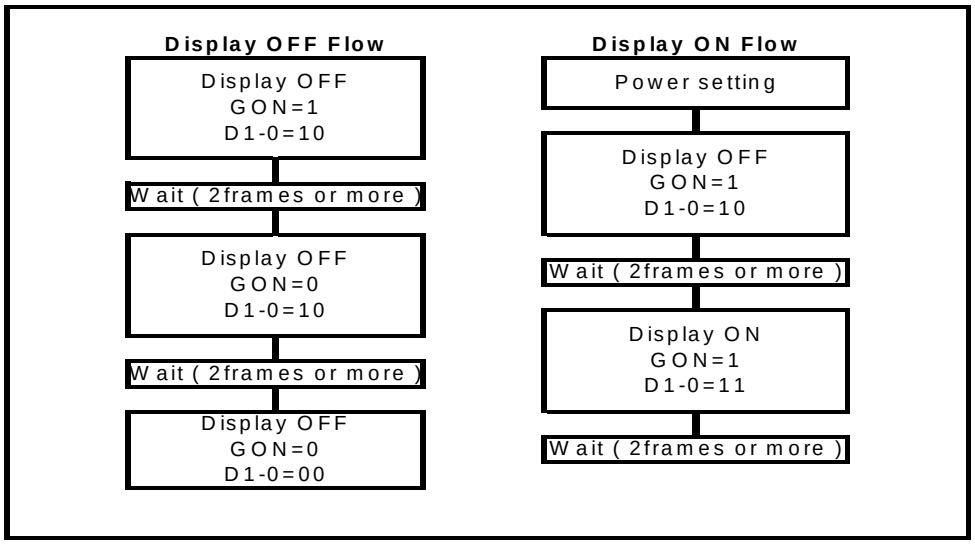


Figure 25-1: Display ON/OFF flowchart

25.2. Standby Mode

Standby-in sequence

Step	Register	Register Value	Waiting time	Operation
1	R07h	081xh	40ms	Display On (PT[1:0]=01,VLE[2:1]=00,SPT=0,GON=1,CL,REV, D[1:0]=10)
2	R07h	080xh	40ms	Display On- Normaly Color (PT[1:0]=01,VLE[2:1]=00,SPT=0,GON=0,CL,REV, D[1:0]=10)
3	R07h	080xh	-	Display Off (PT[1:0]=01,VLE[2:1]=00,SPT=0,GON=0,CL,REV, D[1:0]=00)
4	R10h	0xx0h	-	Source Amp Off (only SAP[2:0]=000,BT[2:0], DC[2:0], SLP=0, STB=0)
5	R13h	0060h	5ms	AMP Off (PON=1, PON1=1, AON=0)
6	R13h	0040h	5ms	CP2 Off (PON=1, PON1=0, AON=0)
7	R13h	0000h	5ms	CP1/CP3 Off (PON=0, PON1=0, AON=0)
8	R5Ah	0002h	-	Standby setting (STBM[1:0]=010) VCI=2.75V
9	R10h	0001h	(30ms)	Standby in (SAP[2:0]=000,BT[2:0]=000, DC[2:0]=000, SLP=0, STB=1)

"x"stands for "user preference"

Note) Waiting time on the list is for reference. (variable depending on penel's wiring resistance, ACF conection resistance, FPC wiring

Standby -release sequence

Step	Register	Register Value	Waiting time	Operation
1	R00h	0001h	10ms	OSC Satat- in Standby Mode
2	R10h	0000h	10ms	Standby out (SAP[2:0]=000,BT[2:0]=000, DC[2:0]=000, SLP=0, STB=0)
3				Execute from step 3 to 36 of "Power-on sequence"

"x"stands for "user preference"

Note) Waiting time on the list is for reference. (variable depending on penel's wiring resistance, ACF conection resistance, FPC wiring

Table 25-1: Standby Mode sequence

25.3. Sleep Mode

Standby-> Sleep Sequence

Step	Register	Register Value	Waiting time	Operation
1	R00h	0001h	10ms	OSC Start- in Standby Mode
2	R10h	0000h	5ms	Standby out (SAP[2:0]=000,BT[2:0]=000, DC[2:0]=000, SLP=0, STB=0)
3	R10h	0002h	30ms	Sleep in (SAP[2:0]=000,BT[2:0]=000, DC[2:0]=000, SLP=1, STB=0)

"x"stands for "user preference"

Note) Waiting time on the list is for reference. (variable depending on penel's wiring resistance, ACF conection resistance, FPC wi

Table 25-3: Sleep-in sequence

26. Pattern Diagram for Voltage Setting

The pattern diagram for setting the voltages and the waveforms of the voltages of the MC2TA7402 is as follows.

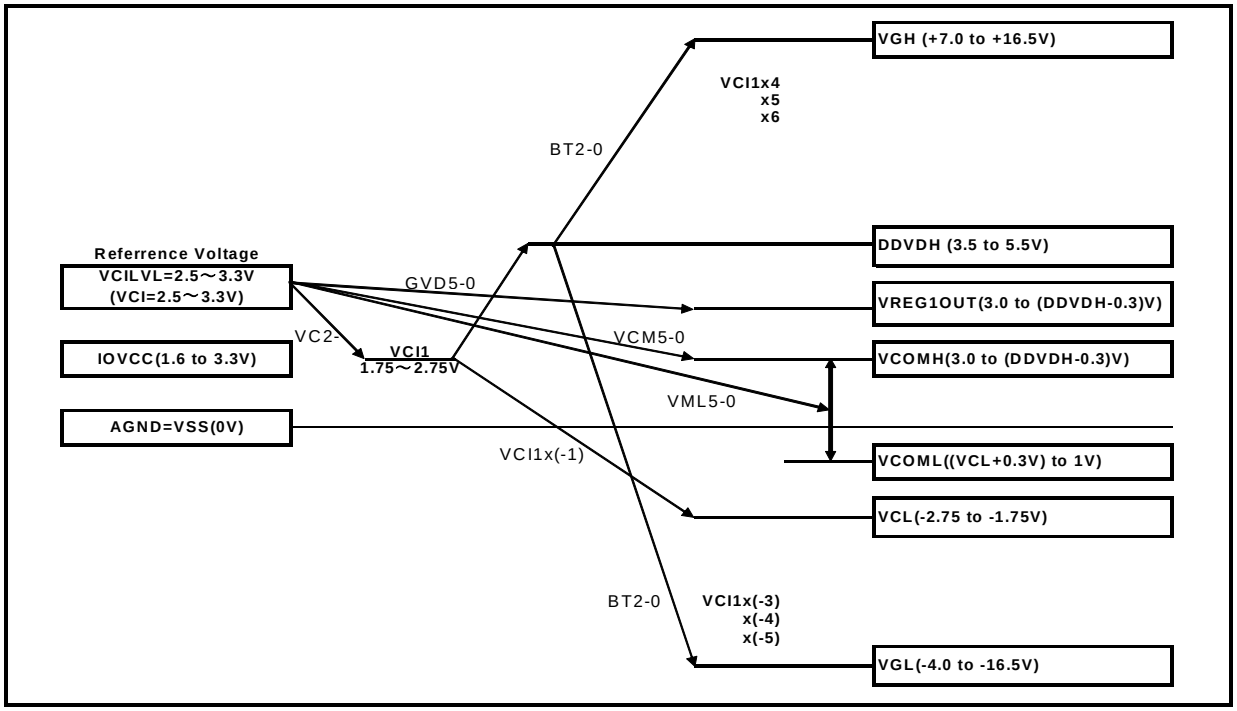


Figure 26-1: Pattern diagram for voltage setting

Note: The DDVDH, VGH, VGL, and VCL output voltage levels are lower than their theoretical levels (ideal voltage levels) due to the current consumption at respective outputs.

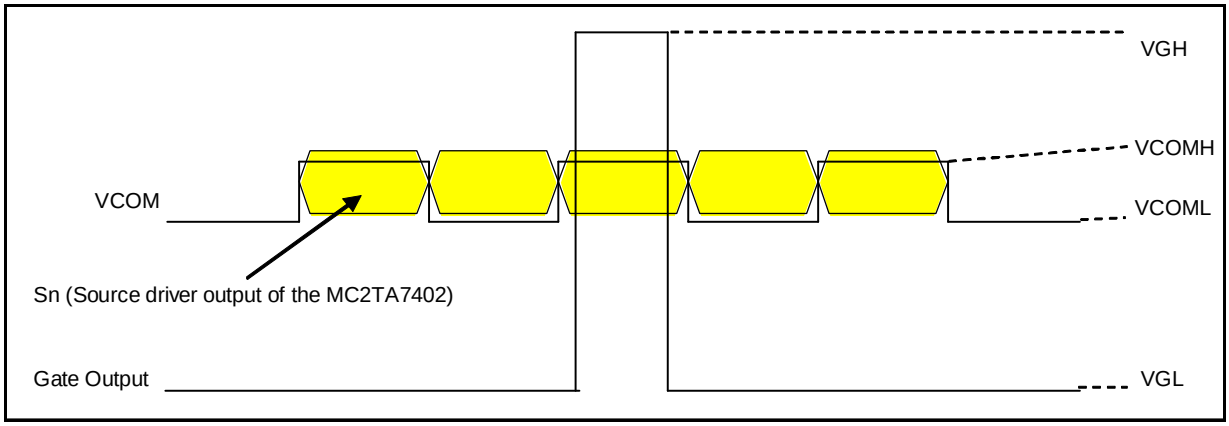


Figure 26-2: Applied voltage to the TFT display

27. Oscillation Circuit

The MC2TA7402 can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor. Note that in R-C oscillation, the oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decrease, the oscillation frequency decreases.

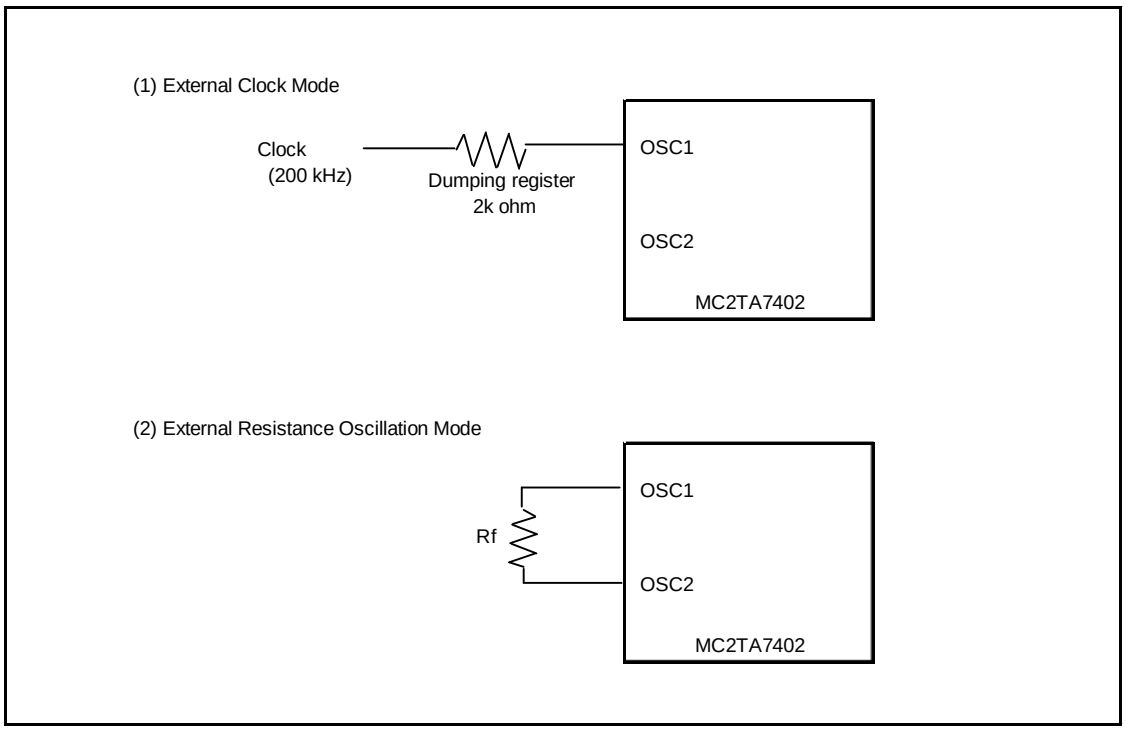
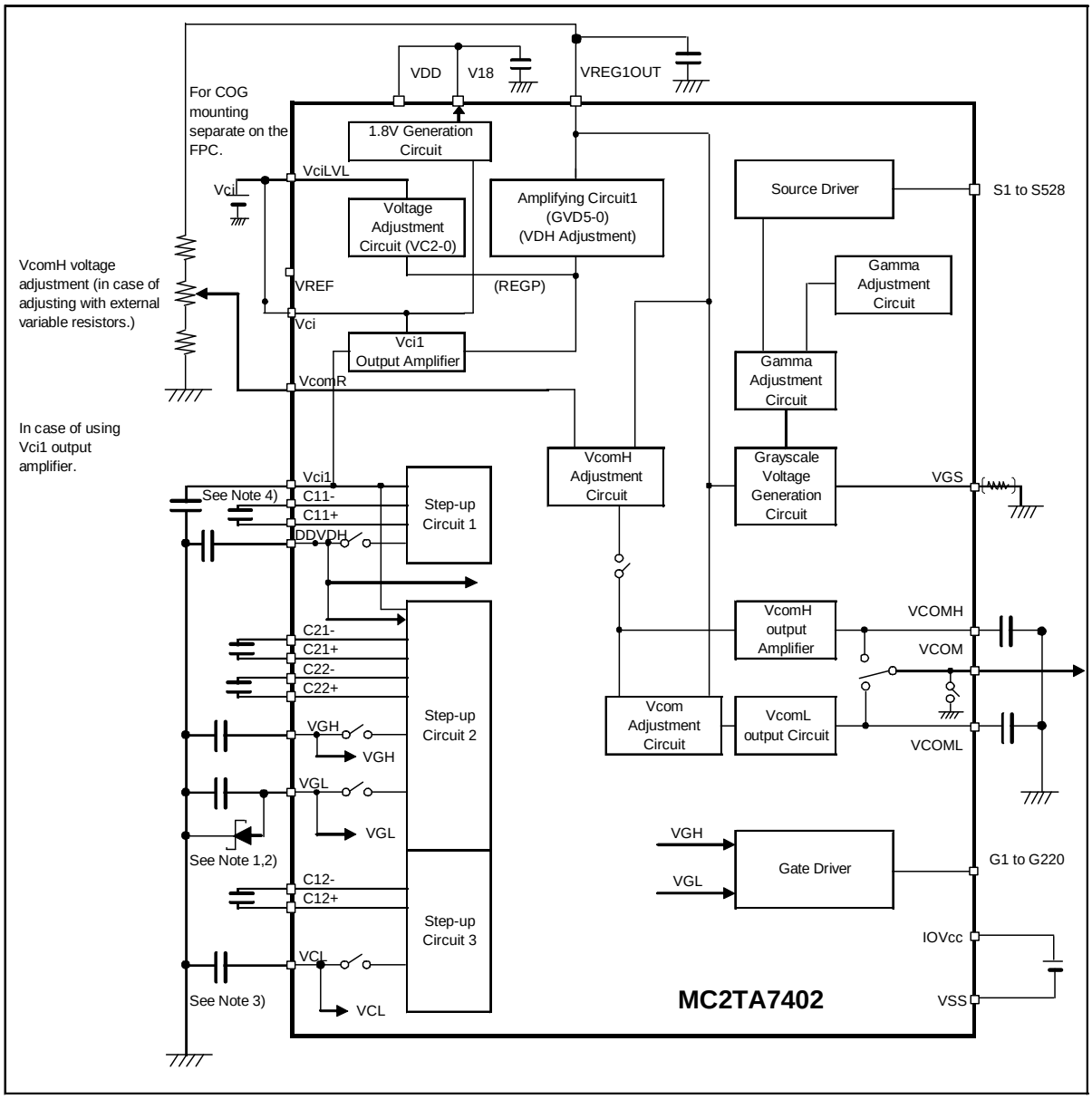


Figure 27-1: Oscillation Circuit

28. Configuration of Power Supply Circuit

The following figure shows the configuration of the power supply circuit in the MC2TA7402 for generating supply voltages to drive a liquid crystal panel.



Note 1) Place a schottky barrier diode (VF = (about) 0.4 / 20mA, VR > 30V).
Note 2) The wiring resistance between GND or VGL and the schottky barrier diode must be 10 ohm or less.
Note 3) Capacitor connection is not required when using with VCOMG = 0 (VcomL = GND).
Note 4) When directly inputting Vci to Vci1, set the VC2-0 bits to "000".
In this case, capacitor connection to the Vci1 pin is not required.

Figure 28-1:

29. Specification of External Elements Connected to MC2TA7402 Power Supply

The following tables show specifications of the external elements connected to the MC2TA7402's power supply circuit.

Table 22-1: Capacitor

Capacity	Recommended voltage	Pin connection
1 uF (B characteristics)	6.3V	V18
	10V	VREG1OUT, VCI1, VCL VCOMH, VCOML C11P/M, C12P/M
	16V	DDVDH, C21P/M, ,
	25V	VGL, VGH ,C22P/M

Table 22-2: Schottky diode

Feature	Pin connection
VF < 0.4V / 20mA at 25 degrees C, VR ≥ 30V (Recommended diode: HSC226)	GND level - VGL

Table 22-3: Variable resistor

Feature	Pin connection
> 200kohm	VCOMR

30. Absolute Maximum Ratings

Table 30-1:

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	VDD – GND level	V	-0.3 to +2.2	1, 2, 8
	IOVCC – GND level		-0.3 to +4.6	
Power supply voltage (2)	VCI, VCILVL – GND level	V	-0.3 to +4.6	1, 3
Power supply voltage (3)	DDVDH – GND level	V	-0.3 to +6.0	1, 4
Power supply voltage (4)	GND level - VCL	V	-0.3 to +4.6	1,
Power supply voltage (5)	DDVDH - VCL	V	-0.3 to +9.0	1, 5
Power supply voltage (6)	VGH – GND level	V	-0.3 to +18.5	1, 6, 8
Power supply voltage (7)	GND level - VGL	V	-0.3 to +18.5	1, 7, 8
Power supply voltage (8)	VGHmax-VGLmin	V	<32V	1,6,7,9
Input signal voltage	Vt	V	-0.3 to IOVCC + 0.3	1
Operating temperature	Topr	Degrees C	-40 to +85	1
Storage temperature	Tstg	Degrees C	-55 to +110	1

Note 1) If used beyond the absolute maximum ratings, the LSI may be permanently damaged. It is strongly recommended to use the LSI at a condition within the electrical characteristics for normal operation. Exposure to a condition not within the electrical characteristics may affect device's reliability.

Note 2) Make sure: VDD $\geq$ GND level, IOVCC $\geq$ GND level.

Note 3) Make sure: VCI $\geq$ GND level.

Note 4) Make sure: DDVDH $\geq$ GND level.

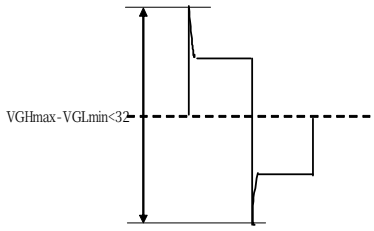
Note 5) Make sure: DDVDH $\geq$ VCL.

Note 6) Make sure: VGH $\geq$ GND level.

Note 7) Make sure: GND level $\geq$ VGL.

Note 8) "GND level" symbolizes "AGND" and "VSS".

Note 9) Not over than absolute maximum voltage including the panel in On/Off and the ripple voltage of wave pattern.



31. Electric Characteristics

31.1. DC Characteristics (VCI=2.5V to 3.3V, Ta=-40 to +85 degrees C)

The all guarantee value is a value when contact and metal resistance of COG/FOG are less than 15 ohm / function (After reliability test it is 25 ohm /function).

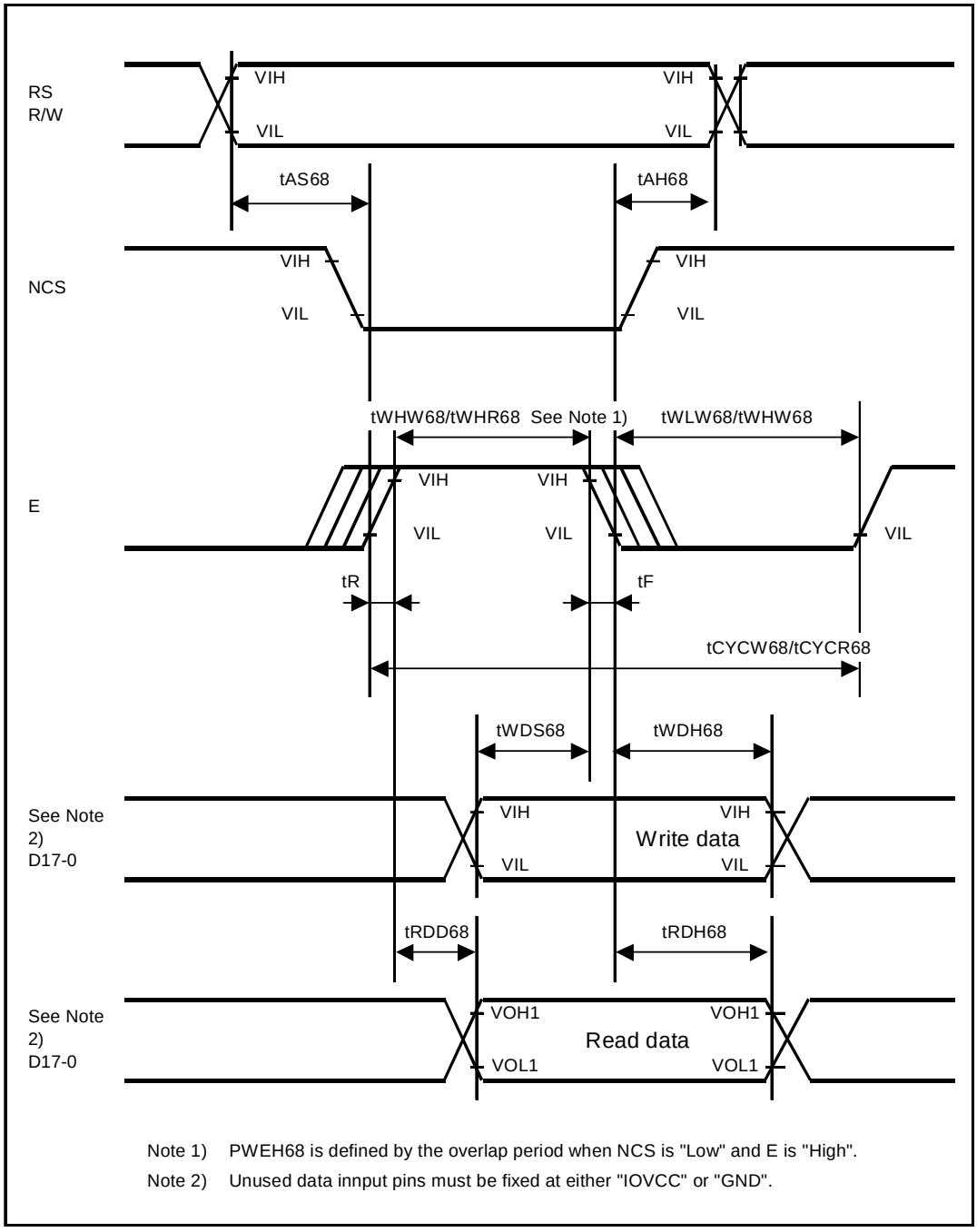
Item		Symbol	Unit	Test Condition	Min.	Typ.	Max.
Input high voltage		VIH	V	IOVCC=1.6V to 3.3V	0.8IOVCC	-	IOVCC
Input low voltage		VIL	V	IOVCC=1.6V to 3.3V	0.0	-	0.2IOVCC
Output high voltage (D17-D0)		VOH1	V	IOVCC=1.6V to 3.3V, IOH=-0.1mA	0.8IOVCC	-	-
Output low voltage (D17- D0)		VOL1	V	IOVCC=1.6V to 3.3V, IOL=0.1mA	-	-	0.2IOVCC
I/O leakage current		ILI	uA (Note)	Vin=0 to IOVCC	-1	-	1
Current consumption (VCI, IOVCC -GND level)	Normal operation mode	IOP1	mA	Ta=25 degrees C, 262,144-color display, VCI=VCILVL=2.8V IOVCC=2.8V 1 line reverse RC Oscillation: fosc=270kHz (220 lines) GVD[5:0]=2F,VC[2:0]=010,SAP[2:0]=011,BT[2:0]=111,DC[2:0]=100 With Tester load	-	-	4.2

Item		Symbol	Unit	Test Condition	Min.	Typ.	Max.
Current consumption (VCI, IOVCC -GND level)	8-color/ partial display mode	IOP2	mA	The test condition is almost same as the normal mode except for the following: CL=1,SPT=1, With Tester load	-	-	1.0
Current consumption (VCI, IOVCC-GND level)	Standby mode	IST	uA	Ta=25 degrees C VCI=VCILVL=IOVCC=2.8V STB=1, STBM[1-0]=10	-	-	1.0

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.
Step-up output voltage	DDVDH	V	VCI=VCILVL =2.8V IOVCC= 2.8V fosc=270kHz, Ta=25 degrees C. VC=010, AP=000, SAP=000, BT=111 (VCI1 x 2), DC=100, C11=C12=C21=C22=C23=1uF/B characteristics DDVDH=VGH=VGHL=VCL=1uF/B characteristics No panel load, Iload=-1mA	4.0	4.5	-
	VGH	V	VCI=VCILVL =2.8V IOVCC= 2.8V fosc=270KHz., Ta=25 degrees C. VC=010, AP=000, SAP=000, BT=111 (VCI1 x 2), DC=100, C11=C12=C21=C22=C23=1uF/B characteristics DDVDH=VGH=VGHL=VCL=1uF/B characteristics No panel load, Iload=-100uA	11.5	13.5	-
	VGL	V	VCI=VCILVL =2.8V IOVCC= 2.8V fosc=270KHz., Ta=25 degrees C. VC=010, AP=000, SAP=000, BT=111 (VCI1 x 2), DC=100, C11=C12=C21=C22=C23=1uF/B characteristics DDVDH=VGH=VGHL=VCL=1uF/B characteristics No panel load, Iload=+100uA	-	-11.3	-9.3
	VGH -VGL	V	Please use even a mode to be at the time of movement within max value.	-	-	27.5
	VCL	V	VCI=VCILVL =2.8V IOVCC= 2.8V fosc=270KHz., Ta=25 degrees C. VC=010, AP=000, SAP=000, BT=111 (VCI1 x 2), DC=100, C11=C12=C21=C22=C23=1uF/B characteristics DDVDH=VGH=VGHL=VCL=1uF/B characteristics No panel load, Iload=+200uA	-	-2.3	-2.1

31.2. AC Characteristics

68-system bus interface operation

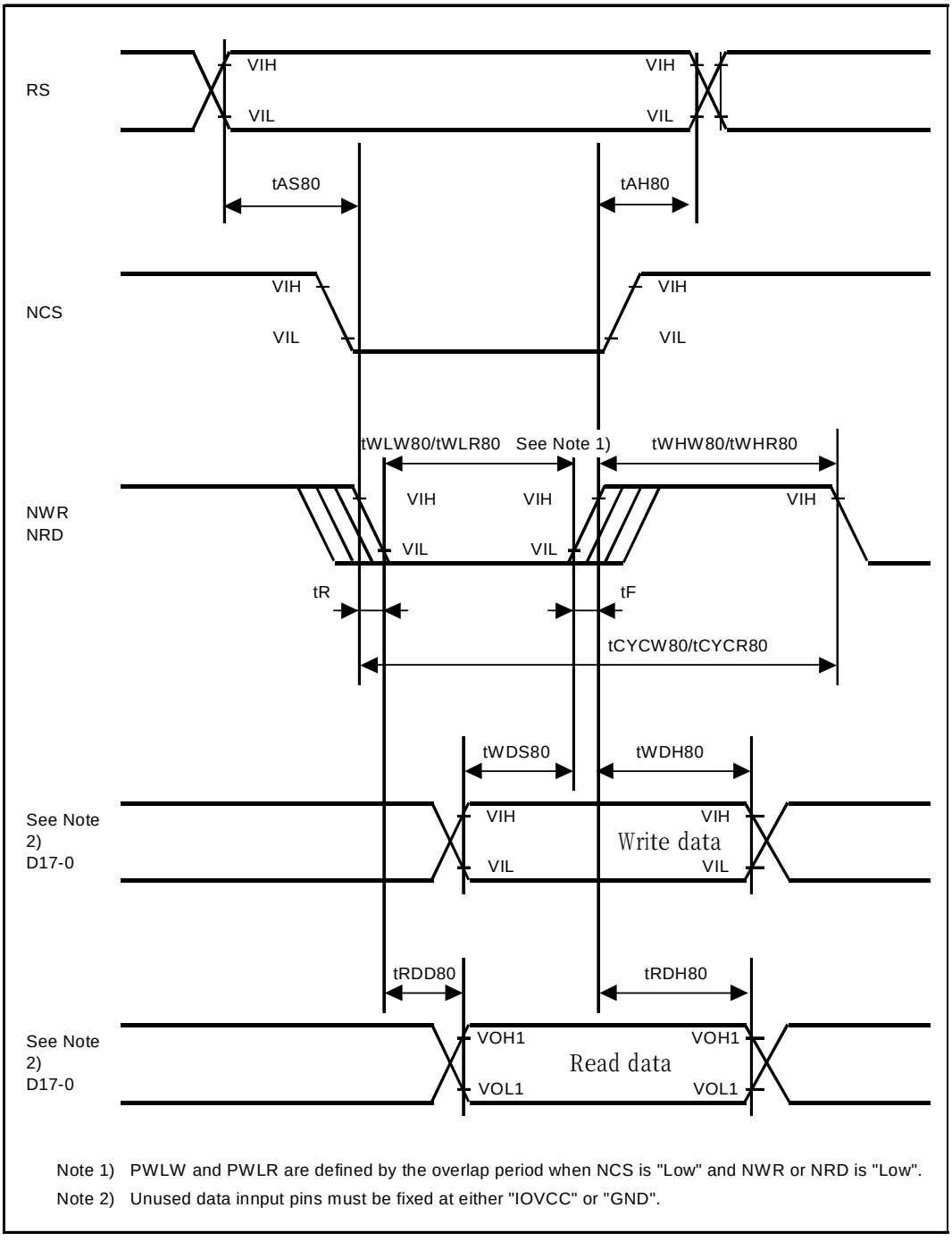


Note 1) PWEH68 is defined by the overlap period when NCS is "Low" and E is "High".

Note 2) Unused data innput pins must be fixed at either "IOVCC" or "GND".

Figure 31-1:

80-systems bus interface operation



Note 1) PWLW and PWLR are defined by the overlap period when NCS is "Low" and NWR or NRD is "Low".

Note 2) Unused data innput pins must be fixed at either "IOVCC" or "GND".

Figure 31-2:

Serial Peripheral Interface operation

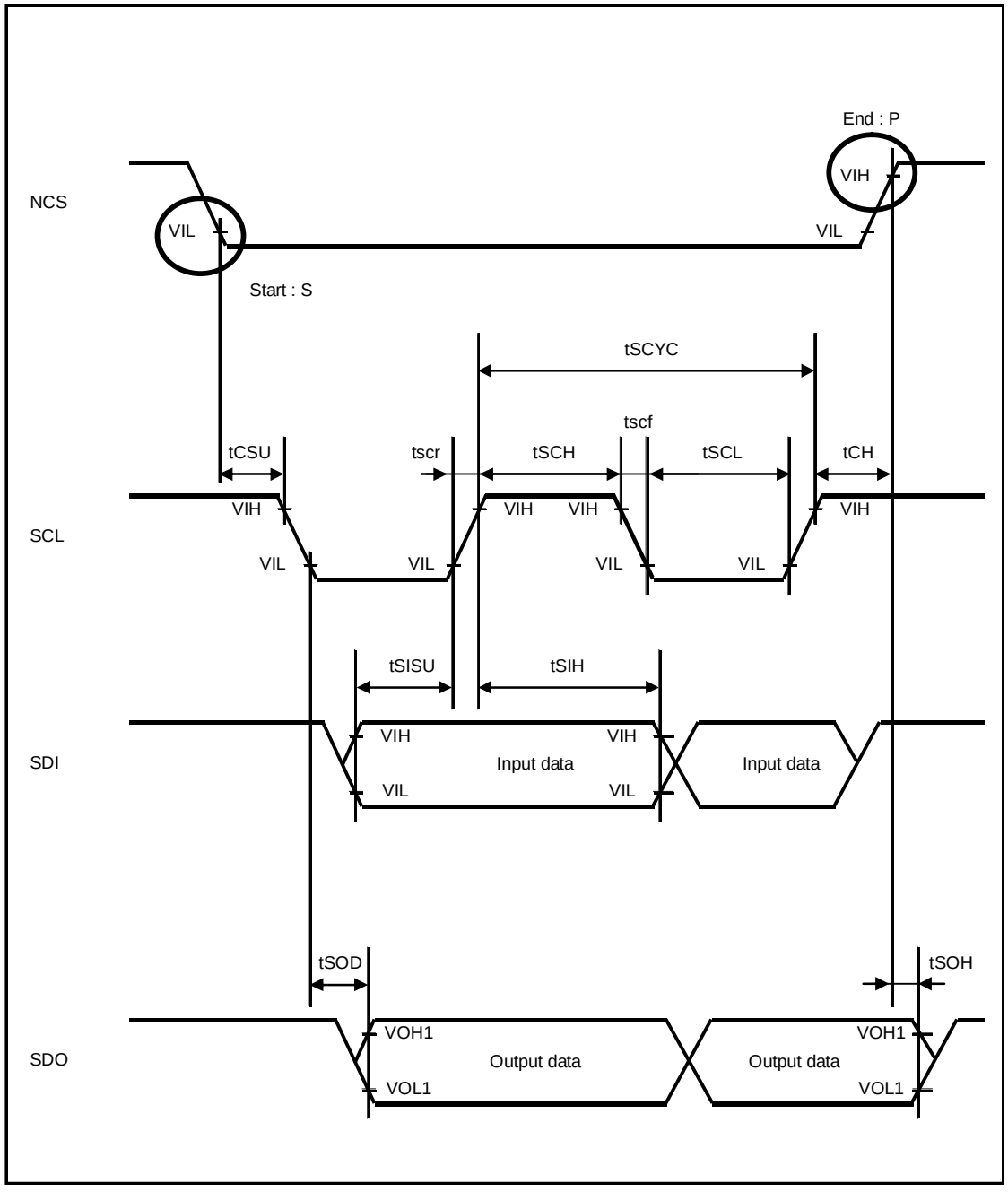


Figure 31-3:

Reset operation

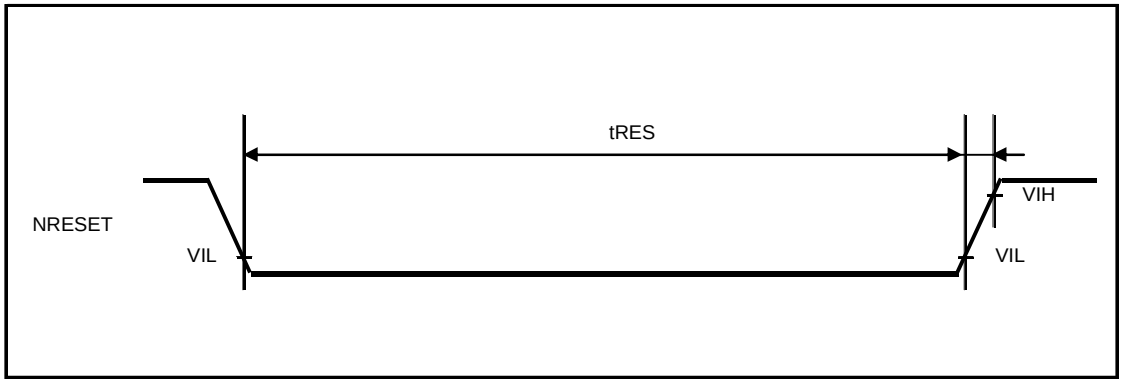


Figure 31-4:

RGB interface

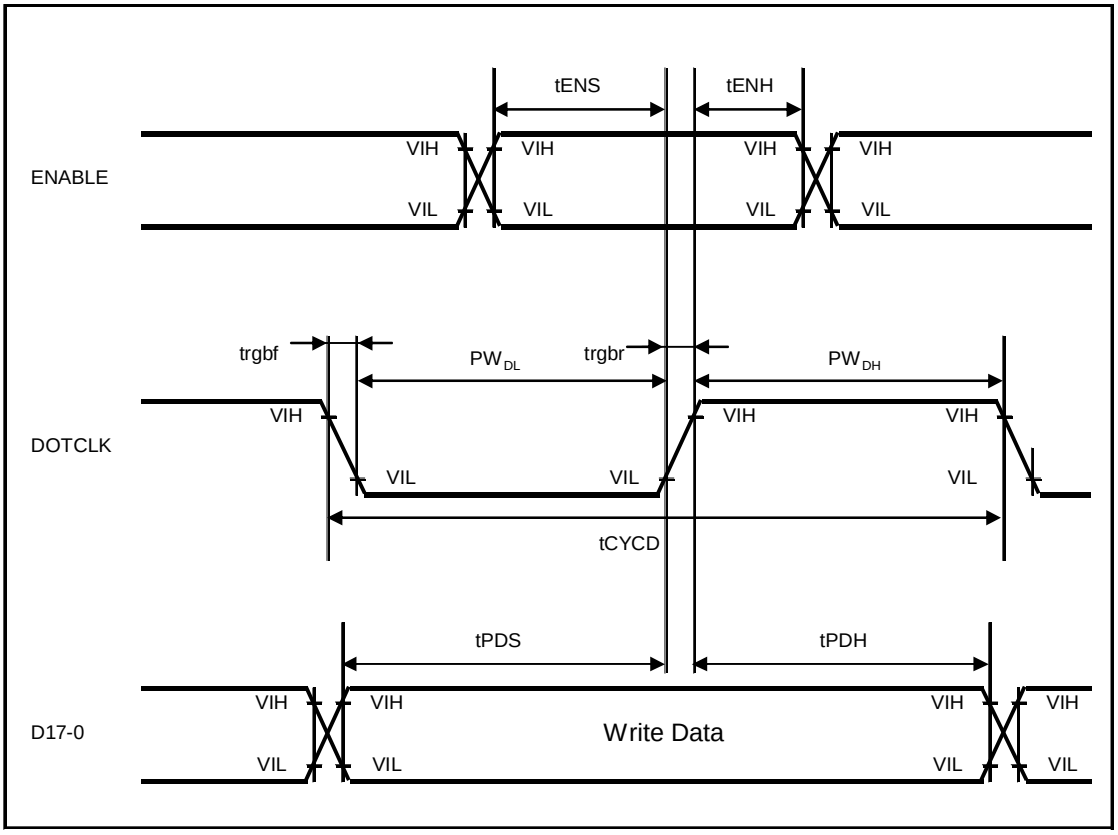


Figure 31-5:

Table 31-1: Clock Characteristics, Rf=135k ohm, VCI=2.8V

Item	Symbol	Unit	Min	Typ	Max
RC Oscillation clock	tosc	kHz	257	285.	313

Note) Above value is defined on tester condition. Actual value in module depends on FPC.

Table 31-2: 68-system bus interface operation (Figure 31-1), IOVCC=1.6 to 3.3V, VCI=2.5V to 3.3V

Item		Symbol	Unit	Min	Typ	Max
Cycle time	Write	tCYCW68	ns	100 *1	-	-
	Read	tCYCR68	ns	500		
Pulse rise/fall time		tR,tF	ns		-	25
E pulse width high	Write	tWHW68	ns	40	-	-
	Read	tWHR68	ns	250		
E pulse width low	Write	tWLW68	ns	40	-	-
	Read	tWLR68	ns	200		
RW,RS and CSB setup time		tAS68	ns	10	-	-
RW,RS and CSB hold time		tAH68	ns	2	-	-
Write data setup time		tWDS68	ns	60		
Write data hold time		tWDH68	ns	15		
Read data delay time		tRDD68	ns			200
Read data hold time		tRDH68	ns	5		

Note *1) If you set the horizontal dot's number "odd", the Min of tCYCW will be 200nS

Table 31-3: 80-system bus interface operation (Figure 31-2), IOVCC=1.6 to 3.3V, VCI=2.5V to 3.3V

Item		Symbol	Unit	Min	Typ	Max
Cycle time	Write	tCYCW80	ns	100 *1	-	-
	Read	tCYCR80		500	-	-
Pulse width low	Write	tWLW80	ns	40	-	-
Read "Low" level pulse width	Read	tWLR80		250	-	-
Pulse width high	Write	tWHW80	ns	40	-	-
Read "High" level pulse width	Read	tWHR80		200	-	-
Pulse rise/fall time		tR, tF	ns	-	-	25
RW,RS and CSB setup time		tAS80	ns	10	-	-
RW,RS and CSB hold time		tAH80		0	-	-
			ns	2	-	-
Write data setup time		tWOS80	ns	60	-	-
Write data hold time		tWDH80	ns	15	-	-
Read data delay time		tRDD80	ns	-	-	200
Read data hold time		tRDH80	ns	5	-	-

Note *1) If you set the horizontal dot's number "odd", the Min of tCYCW will be 200nS

Table 31-4: Serial Peripheral Interface operation (Figure 31-3), IOVCC=1.6 to 3.3V, VCI=2.5V to 3.3V

Item		Symbol	Unit	Min	Typ	Max
Serial clock cycle time	Write (Received)	tSCYC	ns	76	-	-
	Read (Transmitted)			350	-	-
Serial clock "High" level pulse width	Write (Received)	tSCH	ns	40	-	-
	Read (Transmitted)			150	-	-
Serial clock "Low" level pulse width	Write (Received)	tSCL	ns	35	-	-
	Read (Transmitted)			150	-	-
Serial clock rise/fall time		tscr, tscf	ns	-	-	20
Chip select setup time		tCSU	ns	20	-	-
Chip select hold time		tCH		60		
Serial input data setup time		tSISU	ns	30	-	-
Serial input data hold time		tSIH	ns	30	-	-
Serial output data delay time		tSOD	ns	-	-	130
Serial output data hold time		tSOH	ns	5	-	-

Note *1) If you set the horizontal dot's number "odd", the Min of tCYCW will be 200nS.

Table 31-5: Reset operation (Figure 31-4), IOVCC=1.6 to 3.3V,VCI=2.5V to 3.3V

Item	Symbol	Unit	Min	Typ	Max
NRESET "Low" level width	tRES	μs	1	-	-
NRESET rise time	trRES	ns	-	-	10

Table 31-6: RGB interface (Figure 31-5), IOVCC=1.6 to 3.3V, VCI=2.5V to 3.3V

Item	Symbol	Unit	Min	Typ	Max
ENABLE setup time	tENS	ns	10	-	-
ENABLE hold time	tENH	ns	20	-	-
DOTCLK "Low" level pulse width	PWDL	ns	40	-	-
DOTCLK "High" level pulse width	PWDH	ns	40	-	-
DOTCLK cycle time	tCYCD	ns	100	-	-
Data setup time	tPDS	ns	10	-	-
Data hold time	tPDH	ns	40	-	-
DOTCLK,VSYNC,HSYNC rise/fall time	trgbr, trgbf	ns	-	-	25

When changing the interface, please follow "A" to "D" in the figure below.

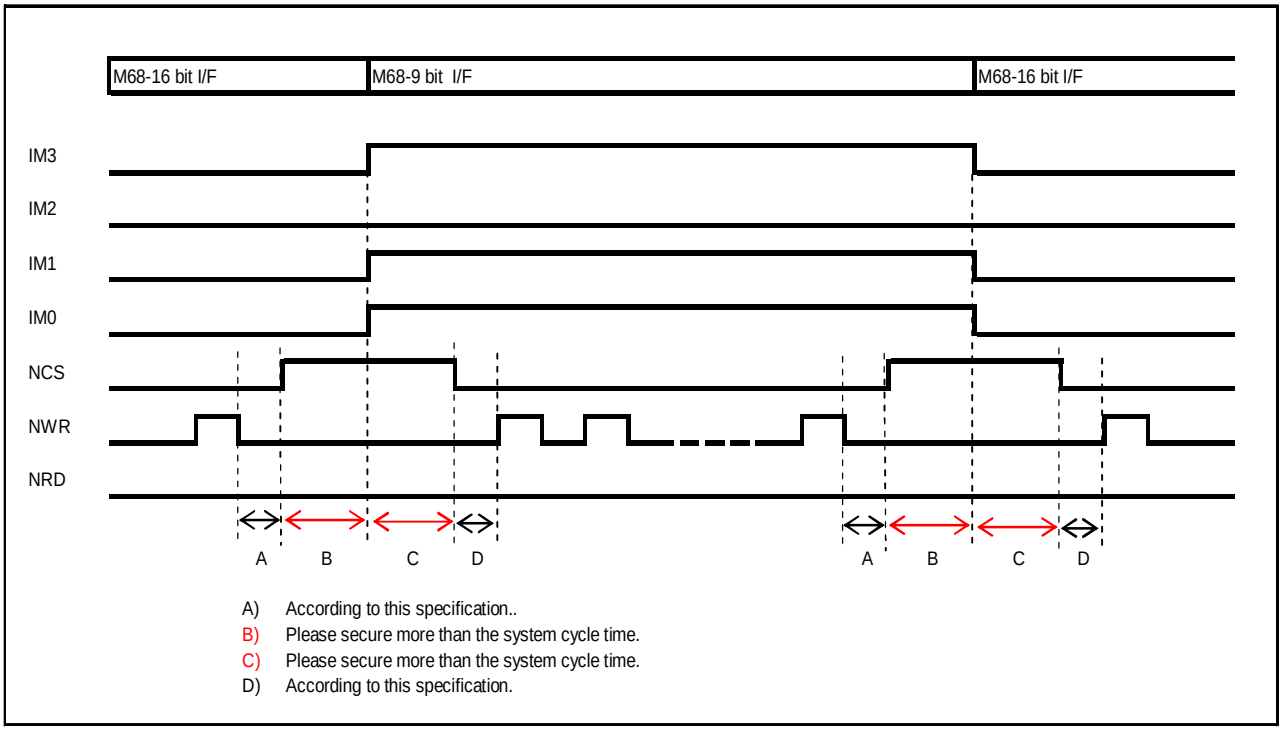


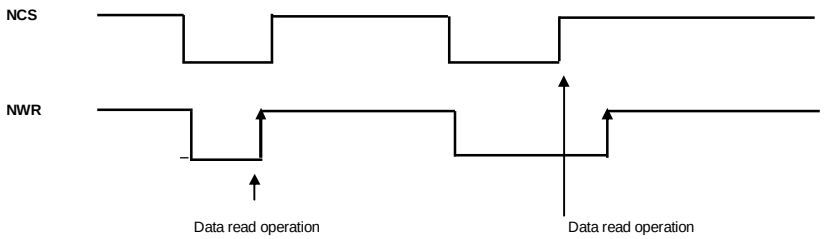
Figure 31-6:

32. Instructions and Directions for Using Magna Chip's Driver IC for TFT Mobile Phones

1. About NCS

- NCS operates as shown below. Please fix NCS at the "High" level when data is not written to the driver.

If the rising edge of NCS comes before the rising edge of NWR, data read operation starts at the rising edge of NCS.



2. Overshoot and/or Undershoot of Handset Main LSI's Output

- The output voltage of the handset main LSI originally has large overshoot and/or undershoot due to the recent movie function.
- Make consideration on the FPC so that the overshoot and/or undershoot do(es)n't exceed the absolute maximum rating of the input signal of this driver IC.

3. GND Electrode on the FPC

- Modules for handsets usually receive ESD test at 10+ kV. Test results sometimes vary depending on the shape of the GND electrodes on the FPC. Please carefully study the shape of the GND electrodes at the design and development stage.

4. Contact and metal pattern Resistance of COG/FOG

- As for contact and metal pattern resistance of the GND pin, input voltage pins and step-up circuit pins, the total of the resistance must be less than 15(ohm)/function.

Resistance: metal pattern resistance on the FPC, ACF contact resistance at the time of FOG, metal pattern resistance on the TFT panel, ACF resistance at the time of COG.

Please keep the above condition in mind at the time of design.

(After reliability test, the total of the resistance must be 25(ohm)/function.)

(LSIs are designed with the premise that the designated voltage is supplied to the LSIs. If the contact and metal pattern resistance is high, the designated voltage can't be supplied and unexpected failure might occur.)

(Each step-up circuit is designed with the premise that the contact and metal pattern resistance are less than 50(ohm)/function. If the contact and metal pattern resistance is 500hm/function or more, the step-up operation might not be performed.)

5. FPC and TFT panel Pattern for Measuring contact and metal pattern Resistance

- As for the GND pin, input voltage pins and step-up circuit pins, please design the FPC and TFT panel pattern so that the contact and metal pattern resistance can be measured.

6. Power Supply Voltage of Each Step-up Voltage

- The step-up circuits in this driver IC for TFT mobile phones use the Charge-pump method. If the panel's load is large, enough driving operation might not be performed.
- When using a TFT LCD display panel using the 1-line inversion AC driving method, whose current consumption is large, study carefully the possible values of each step-up power supply voltages.
- Depending on the panel's current consumption, we recommend using an external power supply.

7. Setting the Frequency for Each Step-up Power Supply

- The efficiency of each step-up circuit depends on the contact and metal pattern resistance and frequency for each step-up power supply. At the time of module designing, please study carefully how each step-up circuit can generate the maximum efficiency.

8. Step-up Sequence

- The appropriate sequence varies according to the module design. Please note that the listed sequence in this specification is for your reference.

9. Countermeasures Against ESD in the Process.

- Manufacturing sites of TFT modules must pay attention to the static electricity more so than the manufacturing sites of C-STNs.
- Static electricity must be less than 50V in general. This condition can vary depending on the TFT LCD display panel used.

10. Migration

- Bumps on the driver IC is made of gold and the space between bumps are extremely narrow.
  Please design modules and control processes to prevent "Migration".

33. Note

The followings should be noted when this LSI specification is used.

1. The information in this document is subject to change without notice for the purpose of product improvement and technical progress. So please make sure that the information in your specification is the latest. (However, after the Delivery Specification is provided officially, any changes to the specification will be made after discussion and agreement by both sides.)
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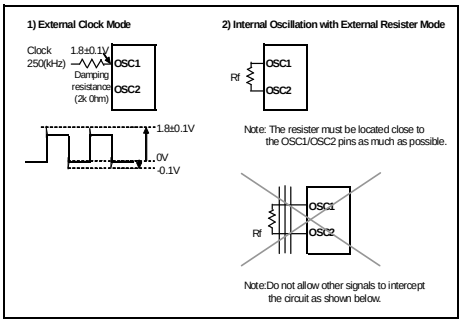
34. Revision History

Page/Chapter	Ver.0.0	Ver.0.1
P78,79,81,86	MA2TA7402	MC2TA7402
P106	<B>	<G>
P109	GVDD level	VREG1OUT level
P114	GVDD	VREG1OUT
P129	VREG1OUT(3 to (DDVDH-0.5)V)	VREG1OUT(3 to (DDVDH-0.3)V)
P131	VREFI	VREG1OUT
P63	Value of Table10-30,31	Please, show Table10-30,31(after Ver.0.1)
P143	Table31-2	Same to Table31-3 and replace to 68-system's name.
P27/C6.5	S384-S1	S528-S1
P27/C6.5	G2-G160,G159,-G1	G2-G220,G219-G1
P134	VIL2 : Min=-0.3	VIL : Min=0.0V
P134	VIH Min=0.7xIOVCC, VIL Max=0.3xIOVCC	VIH Min=0.8xIOVCC, VIL Max=0.2xIOVCC
P122	Table21-1 NM5-0	Delete NW5-0
P132	Table30-1	Insert VGHmax-VGLmin<32
P54,135		Insert VGH-VGL<27.5V
P3	IOVCC=1.65V to 3.3V	IOVCC=1.6V to 3.3V
P129/Fig26-1	IOVCC=1.8V to 3.3V	IOVCC=1.6V to 3.3V
P24	NWR : Inputs an ENABLE signal for **triggering** a data read/write operation in 68-system interface mode. NRD : Inputs an ENABLE signal for **selecting** a data read/write operation in 68-system interface mode	NWR : Inputs an ENABLE signal for **selecting** a data read/write operation in 68-system interface mode. NRD : Inputs an ENABLE signal for **triggering** a data read/write operation in 68-system interface mode.
P24	Vci1 : The Vci1 output ----- VDC2-0bits.	Vci1 : The Vci1 output ----- VC2-0bits.

34.1. Revision from Ver.0.0 to Ver0.1

34.2. Revision from Ver.0.1 to Ver0.2

Page/Chapter	Ver.0.1	Ver.0.2

P24	VREG1OUT : VREG1OUT is used for (1)a source driver grayscale reference voltage (2)a VCOM level reference voltage (3)a VCOM amplitude reference voltage Connect to a stabilizing capacitor.	VREG1OUT : VREG1OUT is used for a source driver grayscale reference voltage. Connect to a stabilizing capacitor.
P58	Table10-26 : (fDCDC1)	(fDCDC1/3)
P58	Table10-26 : (fDCDC2/3)	(fDCDC2)
P29		Insert below figure 
P13/C5.5	Bump No 74 : B8, Bump No 75 : DB8	Bump No 74 : D8, Bump No 75 : D8
P53/ Table10-19	RTN=01 : DCCLK=fosc/16	RTN=01 : DCCLK=fosc/10
P128/ Figure16-1	Vci1→VCOMH, Vci1→VREG1OUT	VciLVL→VOMH, VciLVL→VREG1OUT
P128/ Figure16-1	VGH : VCL x4,5,6 , VGL : VCL x(-3),(-4),(-5)	VGH : Vci1 x4,5,6 , VGL : Vci1 x(-3),(-4),(-5)
P140		Delete the figure of VSYNC, HSYNC
P142		Delete VSYNC/HSYNC setup time
P51	ECS2-0=101 Sys./ V IF OP=12, RGB IF OP=48 ECS2-0=110 Sys./V IF OP=14, RGB IF OP=56 ECS2-0=111 Sys./V IF OP=Setting disable, RGB IF=Setting disable	ECS2-0=101 Sys./ V IF OP=10, RGB IF OP=40 ECS2-0=110 Sys./V IF OP=12, RGB IF OP=48 ECS2-0=111 Sys./V IF OP=14, RGB IF=56

34.3. Revision from Ver.0.2to Ver0.21

Page/Chapter	Ver.0.2	Ver.0.21
P10	Chip X size=19.242mm(after dicing) Chip Y size=1.270mm(after dicing)	Chip X size= 19.202mm(after dicing) Chip Y size=1.230mm(after dicing)
P12	Chip size : 19.242mmx1.27mm	Chip size : 19.202mmx1.23mm

34.4. Revision from Ver.0.21to Ver0.22

Page/Chapter	Ver.0.21	Ver.0.22
P22	VSS: Power supply GND for-----.	VSS: Power supply GND level for-----.
	AGND: Power supply GND for------.	AGND: Power supply GND level for-------.
P23	VCOMR : ----------VREG1OUT and GND.	VCOMR: ----------VREG1OUT and VSS(GND level.)
	VGS(Connect to) : GND or resistor	VGS (Connect to) : VSS(GND level)or resistor
P24	IM3-0(Connect to) : GND/IOVCC	IM3-0(Connect to) : VSS (GND level)/ IOVCC
	IM3-0 Function (Amplitude) : IOVCC/GND	IM3-0 Function (Amplitude) : IOVCC/VSS (GND level)).
	NRESET Function (Amplitude : IOVCC/GND)	NRESET Function (Amplitude) : IOVCC / VSS (GND level))
	NCS Function (Amplitude) : IOVCC/GND	NCS Function (Amplitude) : IOVCC/ VSS(GND level)).
	RS Function (Amplitude) : IOVCC/GND	RS Function (Amplitude) : IOVCC/VSS(GND level)).
	RS (Unused pins) : GND/IOVCC	RS (Unused pins) : VSS(GND level/IOVCC)
	NWR Function (Amplitude): IOVCC/GND	NWR Function (Amplitude) : IOVCC/VSS(GND level)).
	NWR (Unused pins) : GND/IOVCC	NWR (Unused pins) : VSS(GND level)/IOVCC
	NRD Function (Amplitude): IOVCC/GND	NWR Function (Amplitude) : IOVCC/VSS(GND level)).
	NRD (Unused pins) : GND/IOVCC	NRD (Unused pins) : VSS(GND level)/IOVCC
	ENABLE Function (Amplitude): IOVCC/GND	ENABLE Function (Amplitude) : IOVCC/VSS(GND level)).
	ENABLE (Unused pins) : GND/IOVCC	ENABLE (Unused pins) : VSS(GND level)/IOVCC
	VSYNC Function (Amplitude): IOVCC/GND	VSYNC Function (Amplitude) : IOVCC/VSS(GND level)).
	VSYNC (Unused pins) : GND/IOVCC	VSYNC (Unused pins) : VSS(GND level)/IOVCC
	HSYNC Function (Amplitude): IOVCC/GND	HSYNC Function (Amplitude) : IOVCC/VSS(GND level)).
	HSYNC (Unused pins) : GND/IOVCC	HSYNC (Unused pins) : VSS(GND level)/IOVCC
P25	DOTCLK Function (Amplitude): IOVCC/GND	DOTCLK Function (Amplitude) : IOVCC/VSS(GND level)).
	DOTCLK (Unused pins) : GND/IOVCC	DOTCLK (Unused pins) : VSS(GND level)/IOVCC
	D0~17 Function (Amplitude): IOVCC/GND	D0~17 Function (Amplitude) : IOVCC/VSS(GND level)).
	D0~17 (Unused pins) : GND/IOVCC	D0~17 (Unused pins) : VSS(GND level)/IOVCC

	SDI Function (Amplitude): IOVCC/GND	SDI Function (Amplitude) : IOVCC/VSS(GND level)).
	SDI (Unused pins) : GND/IOVCC	SDI (Unused pins) : VSS(GND level)/IOVCC
	SCL Function (Amplitude): IOVCC/GND	SCL Function (Amplitude) : IOVCC/VSS(GND level)).
	SCL (Unused pins) : GND/IOVCC	SCL (Unused pins) : VSS(GND level)/IOVCC
P26	-	<Insert> VCOM5~10
	FLM Function (Amplitude): IOVCC/GND	FLM Function (Amplitude) : IOVCC/VSS(GND level)).
	FLM (Unused pins) : GND/IOVCC	FLM (Unused pins) : VSS(GND level)/IOVCC
	TEST1,2(Connect to) : GND/IOVCC	TEST1,2(Connect to) : VSS (GND level)/ IOVCC
	TEST1,2 (Unused pins) : GND	TEST1,2 (Unused pins) : VSS(GND level)
	DUMMY3~6(Connect to) : GND	DUMMY3~6(Connect to) : VSS (GND level)
P46	Table10-5 : GND	Table10-5 : AGND (GND level)
P47	GON : ------becomes GND.	GON : -------becomes VSS(GND level).
	D1-0 : ------at the GND level.	D1-0 : -------at the VSS(GND level).
	Table10-9, Source Output, VCOM Output : GND	Table10-9, Source Output, VCOM Output : VSS(GND level).
P58	Table10-27, Source Output, VCOM Output : GND	Table10-27, Source Output, VCOM Output : VSS(GND level).
P74	Initial state of output pins LCD driver (source outputs): All pins output the GND level.	Initial state of output pins LCD driver (source outputs): All pins output the VSS(GND level).
P112	Table 18-7, Note : ---------V63-GND>0.3V,-----	Table 18-7, Note : --------- V63 - AGND(GND level) > 0.3V, ------
P114	Table 18-9, Note : ---------V63-GND>0.3V,-----	Table 18-9, Note : ---------V63- AGND(GND level)>0.3V, ------
P119	Table20-3 : GND	Table20-3 : AGND(GND level)
P129	Figure27-1 : OSC1, OSC2	Figure27-1 : OSC1→OSC2, OSC2→OSC1
P130	Figure28-1 : GND	Figure28-1 : VSS
P131	Table22-2 : Schottky Diode, Pin connection GND-VGL	Table22-2 : Schottky Diode, Pin connection VSS(GND level)-VGL
P133	31.1 DC Characteristics (Normal operation mode) : Current consumption (VCI,IOVCC-GND)	31.1 DC Characteristics (Normal operation mode) : Current consumption (VCI,IOVCC – VSS (GND level))
P134	31.1 DC Characteristics (8-color/partial display mode) : Current consumption (VCI,IOVCC-GND)	31.1 DC Characteristics (8-color/ partial display mode) : Current consumption (VCI,IOVCC – VSS (GND level))

	31.1 DC Characteristics (Standby mode) : Current consumption (VCI,IOVCC-GND)	31.1 DC Characteristics (Standby mode) : Current consumption (VCI,IOVCC – VSS (GND level))
P136	Figure31-1 : Note 2) : ----------"IOVCC" or "GND "	Figure31-1 : Note 2) : ----------"IOVCC" or "VSS(GND level) "
P137	Figure31-2 : Note 2) : ----------"IOVCC" or "GND"	Figure31-2 : Note 2) : ----------"IOVCC" or "VSS(GND level) "
P144	4.. ----------resistance of the GND pin,-------	4.----------resistance of the VSS and AGND pins,--------
	5.-As for the GND pin,-------	5- As for the VSS and AGND pin,--------

34.5. Revision from Ver.0.22to Ver0.23

Page/Chapter	Ver.0.22	Ver0.23
P4/4,5.1~5.5,6	(TBD)	Delete

34.6. Revision from Ver.0.23to Ver0.24

Page/Chapter	Ver.0.23	Ver0.24
P50	IB9:ESC0	IB9 : ECS0
P127	Step-up Chart : VCI1→VGH/VGL	DDVDH→VGH/VGL
P125~127		Recommended sequence add.
P133~140		Spec value add.

34.7. Revision from Ver.0.24to Ver0.25

Page/Chapter	Ver.0.24	Ver0.25
P129	In Fig27-1 OSC1, OSC2	OSC1←→OSC2

34.8. Revision from Ver.0.25to Ver0.26

Page/Chapter	Ver.0.25	Ver0.26
P9	In the figure, left side alignment Mark is ◎, and right side Mark is ○.	Left side Mark is ○, right side Mark is ◎.

34.9. Revision from Ver.0.26to Ver0.27

Page/Chapter	Ver.0.26	Ver0.27
P9,10	In the figure, left side alignment Mark is ○, and right side Mark is ◎.	Left side Mark is ◎, right side Mark is ○.

34.10. Revision from Ver.0.27to Ver0.28

Page/Chapter	Ver.0.27	Ver0.28
P10	-	Add alignment coordinates
P69(Ver0.27)	Table 10-34 : Scanning Start Position SCN=1, GS=0 → G220, SCN=1, GS=1 →G1	.SCN=1 : Setting Disable. SCN=0 : SM=0, GS=0 → G1, SM=0, GS=1 →G220, SM=1, GS=0 → G1, SM=1, GS=1 → G220
P73~74(Ver0.28)	-	Add : 10.2.26 VCOMG Control (R53h) 10.2.27 VCOM EQ (R59h) 10.2.28 STB mode selection (R5Ah)
P75(Ver0.28)	-	Add to Instruction Table : R53h,R59h,R5Ah
P127~129(Ver0.28)	Fig 24-1,Fig24-2, Fig25-2, Fig25-3	Table24-1,Table24-2, Table25-1, Table25-2
P127~129(Ver0.28)	At Table24-1, Table24-2, Table25-1, Table25-2 Resister : Rxx	 Resister : Rxxh

34.11. Revision from Ver.0.28to Ver0.29

Page/Chapter	Ver.0.28	Ver0.29
P74	Table10-36: STBM1-0=01 : VCI=2.5V STBM1-0=10 : VCI=2.8V STBM1-0=11 : VCI=3.3V	Table10-36 STBM1-0=01 : VCI=2.5~2.6V STBM1-0=10 : VCI=2.6~3.1V STBM1-0=11 : VCI=3.1~3.3V
P143	Table31-5 : NRESET "Low" level width (tRES) Min : , Typ : , Max :	Table31-5 : NRESET "Low" level width (tRES) Min : 1 , Typ : -, Max : -

34.12. Revision from Ver.0.29to Ver0.30

Page/Chapter	Ver.0.29	Ver0.30
P32	80-System 16-bit Interface (2 transfers/pixel, 65,536 colors) (R03h;TRI = "1", DFM1-0 = "11")	80-System 16-bit Interface (2 transfers/pixel, 262,144 colors) (R03h;TRI = "1", DFM1-0 = "11")
P143	Table31-5 : NRESET ”Low” level width (tRES) Unit : ms	Table31-5 : NRESET ”Low” level width (tRES) Unit : μs

34.13. Revision from Ver.0.30to Ver0.31

Page/Chapter	Ver.0.30	Ver0.31
P10	Right side + alignment mark coordinate (-9446,460)	Right side + alignment mark coordinate (9446,460)
P153	-	Add into P10 Item into Revision history.

34.14. Revision from Ver.0.31to Ver0.32

Page/Chapter	Ver.0.31	Ver0.32
P127, Table24.1	Initial power control sequence (fosc=200kHz----) and, step11 R14h and others	Initial power control sequence (fosc=285kHz-----) and step 28 R14h and others
P127, Table24-2	4:R10h-----Source AMP Off SAP2-0=000,-----.	4:R10h-----Source AMP Off only SAP2-0=000 change.-------.
P142,Table31-1	Tosc=min:244kHz, typ:272kHz, Max=299kHz	Tosc=min::257kHz,typ: 285kHz,Max=313kHz

34.15. Revision from Ver.0.32to Ver1.00

Page/Chapter	Ver.0.32	Ver1.00
P23 6.3.Logic I/O Pins	IM3=0,IM2=0,IM1=1,IM0=0 Colors : 65,536	IM3=0,IM2=0,IM1=1,IM0=0 Colors : 262,144 / 65,536
P27 Table7-1	IM3=0,IM2=0,IM1=1,IM0=0 Colors : 65,536	IM3=0,IM2=0,IM1=1,IM0=0 Colors : 262,144 / 65,536
P127	-	Insert power supply timing.
P135	Power supply voltage(1) VDD-GND level -0.3 to 2.8	Power supply voltage(1) VDD-GND level -0.3 to 2.2
All page	Preliminary	-

34.16. Revision from Ver.1.00to Ver1.01

Page/Chapter	Ver.1.00	Ver1.01
P8	In Block Diagram, DDRAM I/F line number are 16, 64.	18,72
P8	In Block Diagram, Gamma line areV0-V31.	V0-V63
P11	'-	Notation of wafer thickness.
P12	Chip size: 19.202mmX1.230mm	Chip size(after dicing):19.202mmX1.230mm
P22 6.1.	VCI: No of pins:5 VCILVL: No of pins:1 IOVCC: Bump No:108,109, No of pins 2 VSS: Bump No: 118~125, No of pins :8	VCI: No of pins:6 VCILVL: No of pins:2 IOVCC: Bump No:40,44108,109, No of pins 2 VSS: Bump No:38.42,73,118~125, No of pins :11
P22 6.2	VDD: No of pins:4	VDD: No of pins:6
P25 6.5.	S528~S1: No of pins:384 G2~G220,G219~G2: No of pins:160	S528~S1: No of pins:528 G2~G220,G219~G2: No of pins:220

P36 Table9-2.	S1,DB=[17:12],S2,DB=[11:6],S3,DB=[5,0]------- S526,DB=[17:12],S527DB=[11:6],S528DB=[5:0]	S1,DB=[5:0],S2,DB=[11:6],S3,DB=[17,12]------- S526,DB=[5:0],S527DB=[11:6],S528DB=[17:12]
P127	Power supply order IOVCC→VCI	Power supply order VCI→IOVCC

34.17. Revision from Ver.1.01to Ver1.02

Page/Chapter	Ver.1.01	Ver1.02
P23	No of pins:IM3,IM2,IM1,IM0:1,2,2,1	No of pins:IM3,IM2,IM1,IM0:1,2,2,1
P51	ECS2-0:-------. When VCOML>0,set these bits as “000” to prevent the abnormal function.	ECS2-0:-------. ECS function can be use only when VCOML is 0V(GND level).
P155	Chapter 6.5 of Revision History: Ver1.01: S528~S1: No of pins:384	S528~S1: No of pins:528

34.18. Revision from Ver.1.02to Ver1.03

Page/Chapter	Ver.1.02	Ver1.03
P136 /Standby current	Ta=25degreeC,VCI=VCILVL=IOVCC=2.75	Ta=25degreeC,VCI=VCILVL=IOVCC=2.8,STB=1, STBM[1-0]=10