MC33304

Low Voltage Rail-To-Rail Sleep-Mode™ Operational Amplifier

The MC33304 is a monolithic bipolar operational amplifier. This low voltage rail–to–rail amplifier has both a rail–to–rail input and output stage, with high output current capability. This amplifier also employs Sleep–Mode technology. In sleepmode, the micropower amplifier is active and waiting for an input signal. When a signal is applied, causing the amplifier to source or sink ≥200 μA (typically) to the load, it will automatically switch to the awakemode (supplying up to 70 mA to the load). When the output current drops below 90 μA, the amplifier automatically returns to the sleepmode.

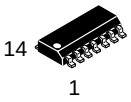
Excellent performance can be achieved as an audio amplifier. This is due to the amplifier's low noise and low distortion. A delay circuit is incorporated to prevent crossover distortion.

- Ideal for Battery Applications
- Full Output Signal (No Distortion) for Battery Applications Down to ±0.9 VDC.
- Single Supply Operation (+1.8 to +12 V)
- Rail–To–Rail Performance on Both the Input and Output
- Output Voltages Swings Typically within 100 mV of Both Rails (R_L = 1.0 mΩ)
- Two States: "Sleepmode" (Micropower, I_D = 110 μA/Amp) and "Awakemode" (High Performance, I_D = 1200 μA/Amp)
- Automatic Return to Sleepmode when Output Current Drops Below Threshold, Allowing a Fully Functional Micropower Amplifier
- Independent Sleepmode Function for Each Amplifier
- No Phase Reversal on the Output for Overdriven Input Signals
- High Output Current (70 mA typically)
- 600 Ω Drive Capability
- Standard Pinouts; No Additional Pins or Components Required
- Drop–In Replacement for Many Other Quad Operational Amplifiers
- Similar to MC33201, MC33202 and MC33204 Family
- The MC33304 Amplifier is Offered in the Plastic DIP or SOIC Package (P and D Suffixes)

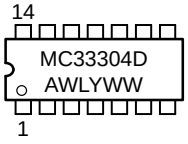
ON Semiconductor

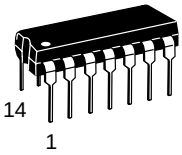
http://onsemi.com

MARKING DIAGRAMS

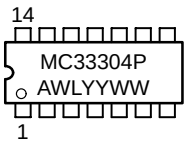


SO–14
D SUFFIX
CASE 751A



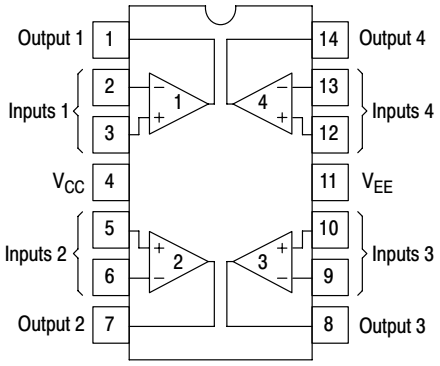


PDIP–14
P SUFFIX
CASE 646



A = Assembly Location
WL = Wafer Lot
YY, Y = Year
WW = Work Week

PIN CONNECTIONS



(Quad, Top View)

ORDERING INFORMATION

Device	Package	Shipping
MC33304D	SO–14	55 Units/Rail
MC33304DR2	SO–14	2500 Tape & Reel
MC33304P	PDIP–14	25 Units/Rail

TYPICAL DC ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	V_{CC} = 2.0 V	V_{CC} = 3.3 V	V_{CC} = 5.0 V	Unit
Input Offset Voltage $V_{IO(max)}$ MC33304	 ±10	 ±10	 ±10	mV
Output Voltage Swing V_{OH} (R_L = 600 Ω) V_{OL} (R_L = 600 Ω)	 1.85 0.15	 3.10 0.15	 4.75 0.15	 V_{min} V_{max}
Power Supply Current per Amplifier (I_D) Awakemode Sleepmode	 1.625 140	 1.625 140	 1.625 140	 mA μA

Specifications are for reference only and not necessarily guaranteed. V_{EE} = Gnd.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+16	V
ESD Protection Voltage at Any Pin Human Body Model	V_{ESD}	 2000	V
Voltage at Any Device Pin (Note 2.)	V_{DP}	$V_S \pm 0.5$	V
Input Differential Voltage Range	V_{IDR}	(Notes 1. and 2.)	V
Output Short Circuit Duration	t_s	Indefinite (Note 3.)	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Maximum Power Dissipation	P_D	(Note 5.)	mW

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage Single Supply Split Supplies	V_S	 1.8 ±0.9	 – –	 12 ±6.0	V
Input Voltage Range, Sleepmode and Awakemode	V_{ICR}	V_{EE}	–	V_{CC}	V
Ambient Operating Temperature Range	T_A	–40	–	+105	°C

1. The differential input voltage of each amplifier is limited by two internal diodes. The diodes are connected across the inputs in parallel and opposite to each other. For more differential input voltage range, use current limiting resistors in series with the input pins.
2. The common–mode input voltage range of each amplifier is limited by diodes connected from the inputs to both power supply rails. Therefore, the voltage on either input must not exceed supply rail by more than ±500 mV.
3. Simultaneous short circuits of two or more amplifiers to the positive or negative rail can exceed the power dissipation ratings and cause eventual failure of the device.
4. Rail–to–rail performance is achieved at the input of the amplifier by using parallel NPN–PNP differential stages. When the inputs are near the negative rail (V_{EE} < V_{CM} < 800 mV), the PNP stage is on. When the inputs are above 800 mV (i.e. 800 mV < V_{CM} < V_{CC}), the NPN stage is on. This switching of the input pairs will cause a reversal of input bias current. Slight changes in the input offset voltage will be noted between the NPN and PNP pairs. Cross–coupling techniques have been used to keep this change to a minimum.
5. Power dissipation must be considered to ensure maximum junction (T_J) is not exceeded. (See Figure 2)
6. When connected as a voltage follower and used in transient conditions, a current limiting resistor may be needed between the output and the inverting input. This is because of the back to back diodes clamped across the inputs. The value of this resistor should be between 1.0 kΩ and 10 kΩ. If the amplifier does not become slew rate limited and is processing low frequency waveforms, then no resistor would be necessary. (The output could be tied directly to the negative input.)

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

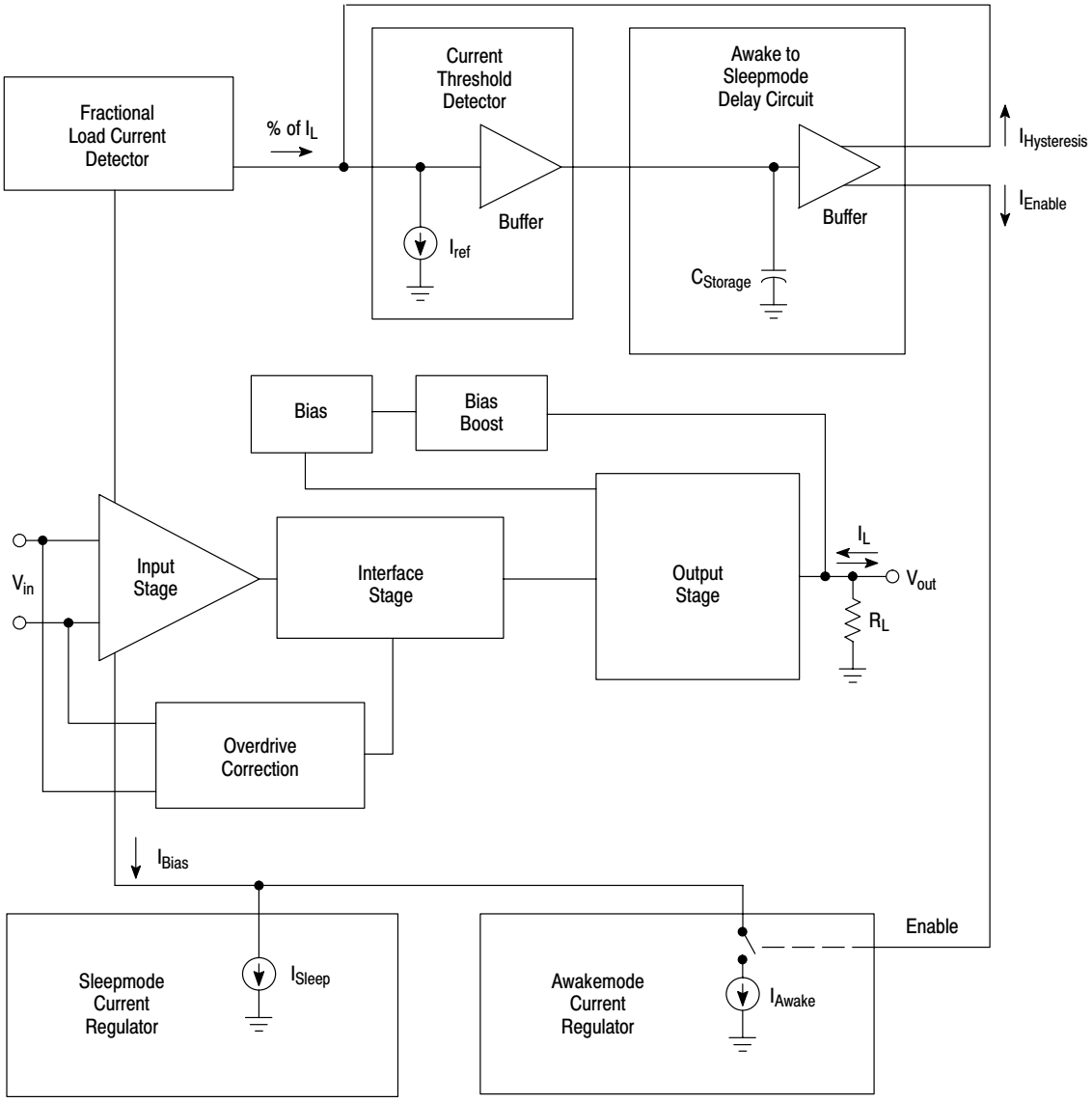
Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} = 0 V, V_O = 0 V) (Note 4.)	V_{IO}				mV
Sleepmode and Awakemode					
T_A = 25°C		–10	0.7	+10	
T_A = –40° to +105°C		–13	–	+13	
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$				μV/°C
(R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)					
T_A = –40° to +105°C, Sleepmode and Awakemode		–	2.0	–	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) (Note 4.)	$\|I_{IB}\|$				nA
Awakemode					
T_A = 25°C		–	90	+200	
T_A = –40° to +105°C		–	–	+500	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V) (Note 4.)	$\|I_{IO}\|$				nA
Awakemode					
T_A = 25°C		–	3.1	+50	
T_A = –40° to +105°C		–	–	+100	
Large Signal Voltage Gain (V_{CC} = +5.0 V, V_{EE} = –5.0 V)	A_{VOL}				dB
Awakemode, R_L = 600 Ω					
T_A = 25°C		90	116	–	
T_A = –40° to +105°C		85	–	–	
Power Supply Rejection Ratio, Awakemode	PSRR	65	90	–	dB
Output Short Circuit Current (Awakemode)	I_{SC}				mA
(V_{ID} = ±0.2 V)					
Source		–200	–89	–50	
Sink		+50	+89	+200	
Output Transition Current, Source/Sink					μA
Sleepmode to Awakemode, V_{CC} = +1.0 V, V_{EE} = –1.0 V	$\|I_{TH1}\|$	–	–	200	
Awakemode to Sleepmode, V_{CC} = +5.0 V, V_{EE} –5.0 V	$\|I_{TH2}\|$	90	–	–	
Output Voltage Swing (V_{ID} = ±0.2 V)					V
Sleepmode					
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 1.0 MΩ	V_{OH}	4.90	4.97	–	
V_{CC} = 0 V, V_{EE} = –5.0 V, R_L = 1.0 MΩ	V_{OL}	–	–4.96	–4.90	
V_{CC} = +2.0 V, V_{EE} = 0 V, R_L = 1.0 MΩ	V_{OH}	1.90	1.98	–	
V_{CC} = 0 V, V_{EE} = –2.0 V, R_L = 1.0 MΩ	V_{OL}	–	–1.97	–1.90	
Awakemode					
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 600 Ω	V_{OH}	4.75	4.86	–	
V_{CC} = 0 V, V_{EE} = –5.0 V, R_L = 600 Ω	V_{OL}	–	–4.85	–4.75	
V_{CC} = +2.0 V, V_{EE} = 0 V, R_L = 600 Ω	V_{OH}	1.85	1.91	–	
V_{CC} = 0 V, V_{EE} = –2.0 V, R_L = 600 Ω	V_{OL}	–	–1.90	–1.85	
V_{CC} = +2.5 V, V_{EE} = –2.5 V, R_L = 600 Ω	V_{OH}	–	2.41	–	
V_{CC} = +2.5 V, V_{EE} = –2.5 V, R_L = 600 Ω	V_{OL}	–	–2.40	–	
Common Mode Rejection Ratio	CMRR	60	90	–	dB
Power Supply Current (per Amplifier)	I_D				μA
Sleepmode					
V_{CC} = +2.0 V, V_{EE} = 0 V T_A = +25°C		–	85	–	
V_{CC} = +2.5 V, V_{EE} = –2.5 V T_A = +25°C		–	110	140	
T_A = –40° to +105°C		–	–	150	
V_{CC} = +12 V, V_{EE} = 0 V T_A = +25°C		–	125	–	
Awakemode					
V_{CC} = +2.5 V, V_{EE} = –2.5 V T_A = +25°C		–	1200	1625	
T_A = –40° to +105°C		–	–	1750	
Thermal Resistance	θ_{JA}				°C/W
SOIC		–	145	–	
Plastic DIP		–	75	–	

4. Rail–to–rail performance is achieved at the input of the amplifier by using parallel NPN–PNP differential stages. When the inputs are near the negative rail (V_{EE} < V_{CM} < 800 mV), the PNP stage is on. When the inputs are above 800 mV (i.e. 800 mV < V_{CM} < V_{CC}), the NPN stage is on. This switching of the input pairs will cause a reversal of input bias current. Slight changes in the input offset voltage will be noted between the NPN and PNP pairs. Cross–coupling techniques have been used to keep this change to a minimum.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 V, V_{EE} = –6.0 V, R_L = 600 Ω, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{CC} = +2.5 V, V_{EE} = –2.5 V, A_V = +1.0) (Note 6.) Awakemode	SR	 0.5	 0.89	 –	V/μs
Gain Bandwidth Product (f = 100 kHz) Awakemode	GBW	 –	 2.2	 –	MHz
Gain Margin (C_L = 0 pF) Awakemode Sleepmode (R_L = 1.0 kΩ)	A_m	 – –	 6.0 9.0	 – –	dB
Phase Margin (R_L = 1.0 kΩ, V_O = 0 V, C_L = 0 pF) Awakemode Sleepmode	ϕ_m	 – –	 40 60	 – –	Deg
Sleepmode to Awakemode Transition Time R_L = 600 Ω R_L = 10 k	t_{tr1}	 – –	 4.0 12	 – –	μsec
Awakemode to Sleepmode Transition Time	t_{tr2}	–	1.5	–	sec
Channel Separation (f = 1.0 kHz) Awakemode	CS	 –	 100	 –	dB
Power Bandwidth (V_O = 4.0 V_{pp}, R_L = 2.0 kΩ, THD ≤ 1.0%) Awakemode	BW_p	 –	 28	 –	kHz
Distortion (V_O = 2.0 V_{pp}, A_V = +1.0) Awakemode (f = 10 kHz) Sleepmode (f = 1.0 kHz, R_L = Infinite)	THD	 – –	 0.009 0.007	 – –	%
Open Loop Output Impedance (V_O = 0 V, f = 2.0 MHz, A_V = +10, I_Q = 10 μA) Awakemode Sleepmode	$\|Z_O\|$	 – –	 100 1000	 – –	Ω
Differential Input Impedance (V_{CM} = 0 V) Awakemode Sleepmode	R_{IN}	 – –	 200 1300	 – –	kΩ
Differential Input Capacitance (V_{CM} = 0 V) Awakemode Sleepmode	C_{IN}	 – –	 8.0 0.4	 – –	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz) Awakemode Sleepmode	e_n	 – –	 15 60	 – –	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz) Awakemode Sleepmode	i_n	 – –	 0.22 0.20	 – –	$pA/\sqrt{Hz}$

6. When connected as a voltage follower and used in transient conditions, a current limiting resistor may be needed between the output and the inverting input. This is because of the back to back diodes clamped across the inputs. The value of this resistor should be between 1.0 kΩ and 10 kΩ. If the amplifier does not become slew rate limited and is processing low frequency waveforms, then no resistor would be necessary. (The output could be tied directly to the negative input.)



There are 515 active components for the entire quad device.

Figure 1. Equivalent Circuit Block Diagram (Each Amplifier)

DEVICE DESCRIPTION

The MC33304 will begin to function at power supply voltages as low as $V_S = \pm 0.8$ V. The device has the ability to swing rail–to–rail on both the input and the output. Since the common mode input voltage range extends from V_{CC} to V_{EE}, it can be operated with either single or split voltage supplies. The MC33304 is guaranteed not to latch up or phase reverse over the entire common mode range. However, the output could go into phase reversal state if input voltage is set higher than $+V_{CC}$ or $-V_{EE}$.

When power is initially applied, the part may start to operate in the awakemode. This occurs because of bias currents being generated from the charging of the internal capacitors. When this occurs, the user will have to wait approximately 1.5 seconds before the device will switch back to the sleepmode.

The amplifier is designed to switch from sleepmode to awakemode whenever the output current exceeds a preset current threshold (I_{TH}) of approximately 200 μA. As a result, the output switching threshold voltage (V_{ST}) is controlled by the output loading resistance (R_L). Large valued load resistors require a large output voltage to switch, but reduce unwanted transitions to the awakemode.

Most of the transition time is consumed slewing in the sleepmode until V_{ST} is reached, therefore, small values of R_L allow rapid transition to the awakemode. The output switching threshold voltage (V_{ST}) is higher for the larger values of R_L, requiring the amplifier to slew longer in the slower sleepmode state before switching to the awakemode.

Although typically 200 μA, I_{TH} varies with supply voltage, temperature and the load resistance. Generally, any current loading on the ouput which causes a current greater than I_{TH} to flow will switch the amplifier into the awakemode. This includes transition currents like those generated by charging load capacitances. In fact, the maximum capacitance that can be driven while attempting to remain in the sleepmode is approximately 300 pF.

The awakemode to sleepmode transition time is controlled by an internal delay circuit, which is necessary to prevent the amplifier from going to sleep during every zero crossing of the output waveform. This delay circuit also eliminates the crossover distortion commonly found in micropower amplifiers.

The MC33304 rail–to–rail sleepmode operational amplifier is unique in its ability to swing rail–to–rail on both the input and output using a bipolar design. This offers a low noise and wide common mode input voltage range. Since the common mode input voltage range extends from V_{CC} to V_{EE}, it can be operated with either single or split voltage supplies.

Rail–to–rail performance is achieved at the input of the amplifiers by using parallel NPN–PNP differential input stages. When the inputs are within 800 mV of the negative rail, the PNP stage is on. When the inputs are more than 800 mV above V_{EE}, the NPN stage is on. This switching of input pairs will cause a reversal of input bias currents. Also, slight differences in offset voltage may be noted between the NPN and PNP pairs. Cross–coupling techniques have been used to keep this change to a minimum.

In addition to the rail–to–rail performance, the output stage is current boosted to provide enough output current to drive 600 Ω loads. Because of this high current capability, care should be taken not to exceed the 150°C maximum junction temperature specification.

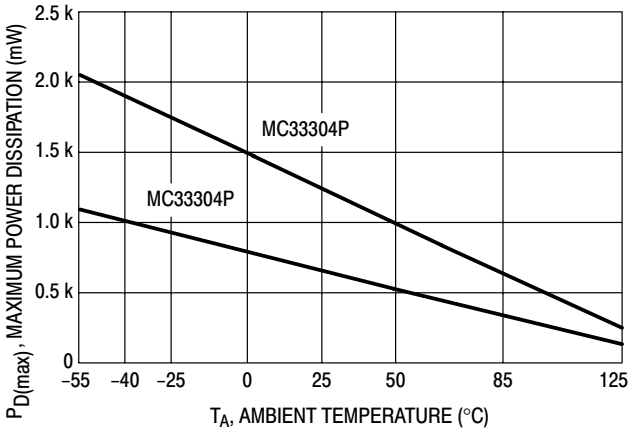


Figure 2. Maximum Power Dissipation versus Temperature

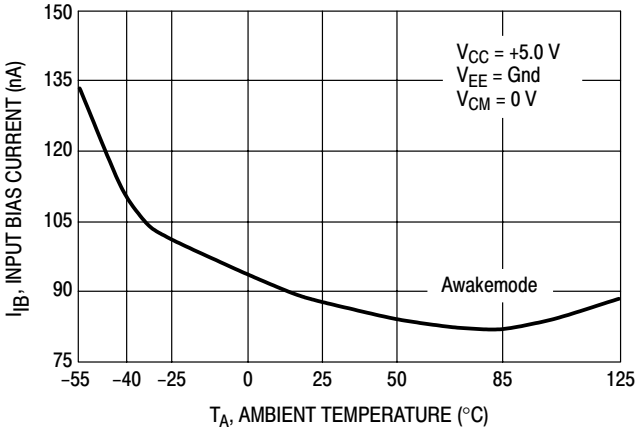


Figure 3. Input Bias Current versus Temperature

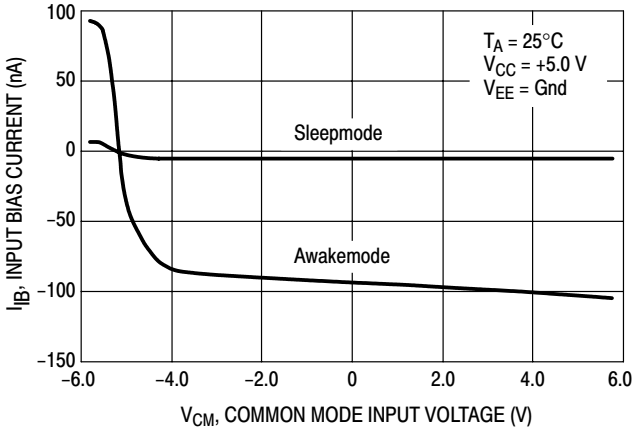


Figure 4. Input Bias Current versus Common Mode Input Voltage

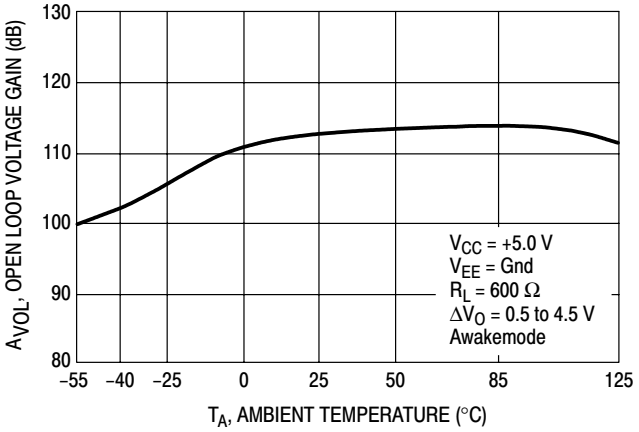


Figure 5. Open Loop Voltage Gain versus Temperature

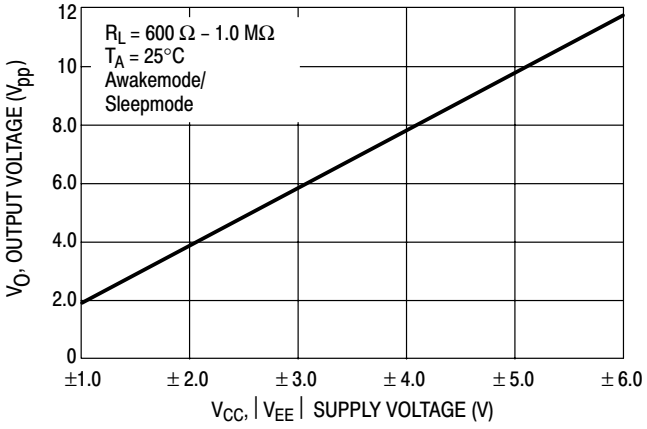


Figure 6. Output Voltage Swing versus Supply Voltage

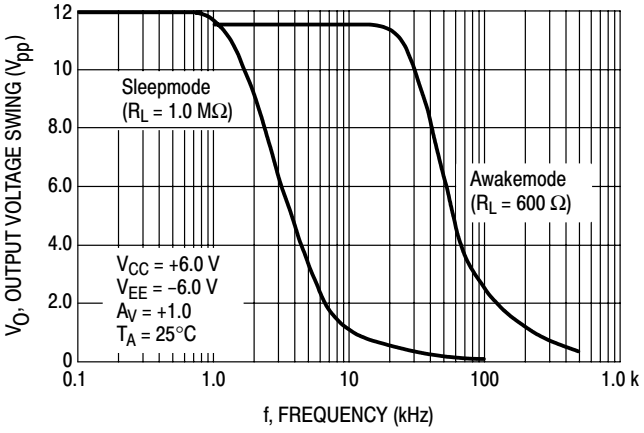


Figure 7. Output Voltage versus Frequency

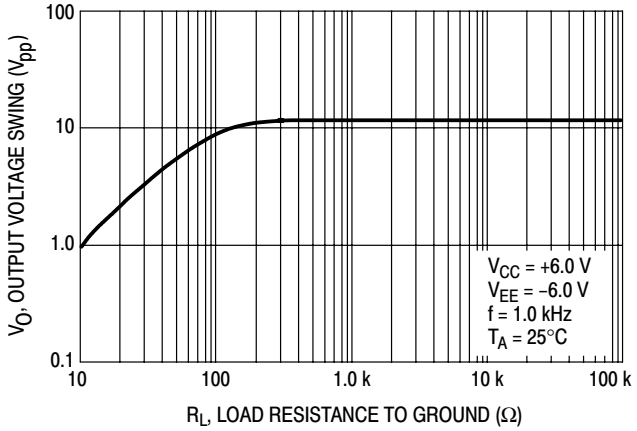


Figure 8. Maximum Peak−to−Peak Output Voltage Swing versus Load Resistance

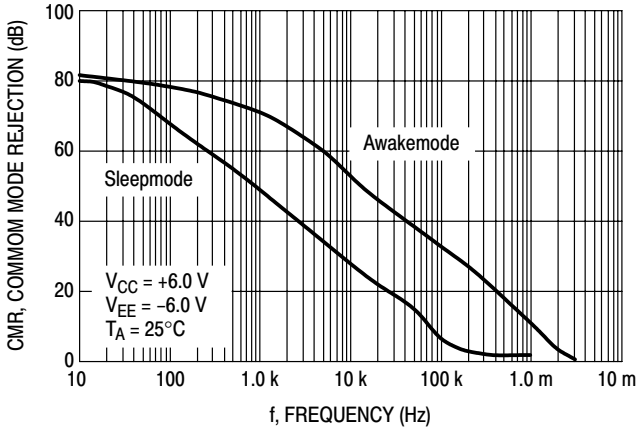


Figure 9. Common Mode Rejection versus Frequency

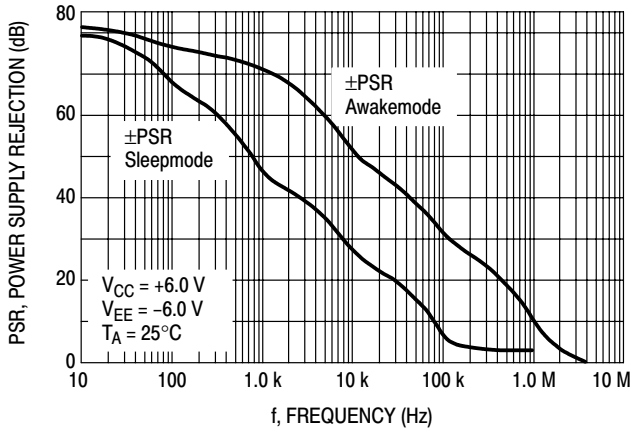


Figure 10. Power Supply Rejection versus Frequency

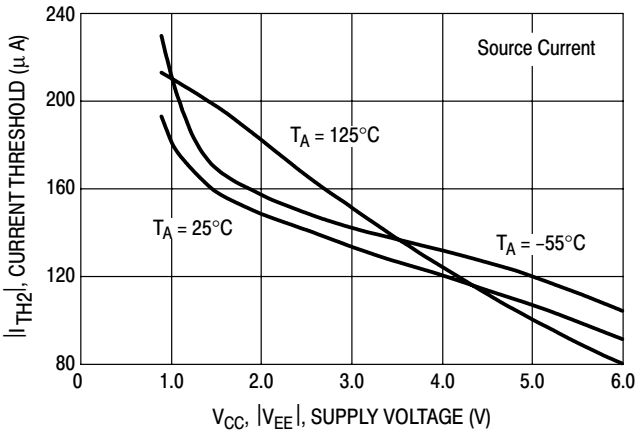


Figure 11. Awakemode to Sleepmode Current Threshold versus Supply Voltage

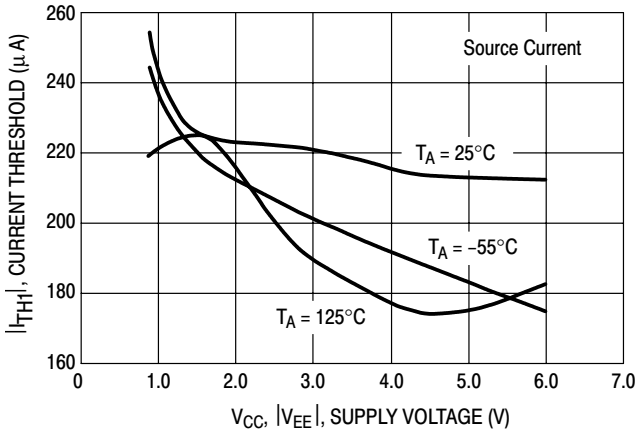


Figure 12. Sleepmode to Awakemode Current Threshold versus Supply Voltage

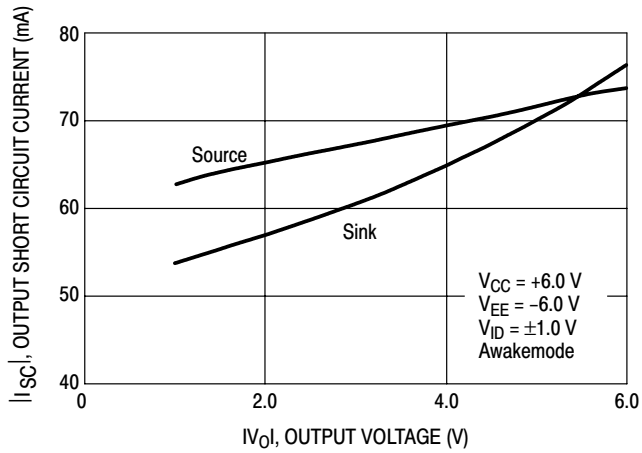


Figure 13. Output Short Circuit Current versus Output Voltage

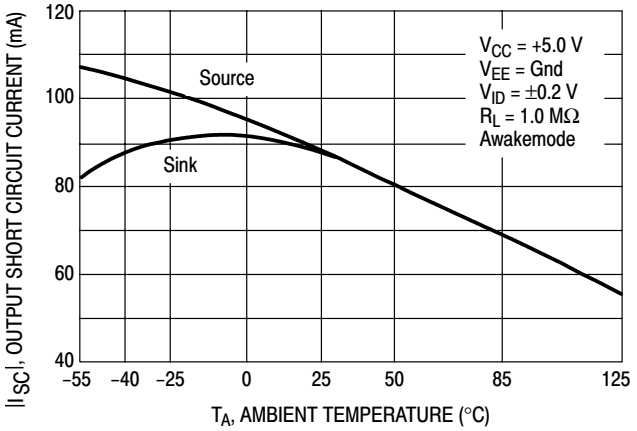


Figure 14. Output Short Circuit Current versus Temperature

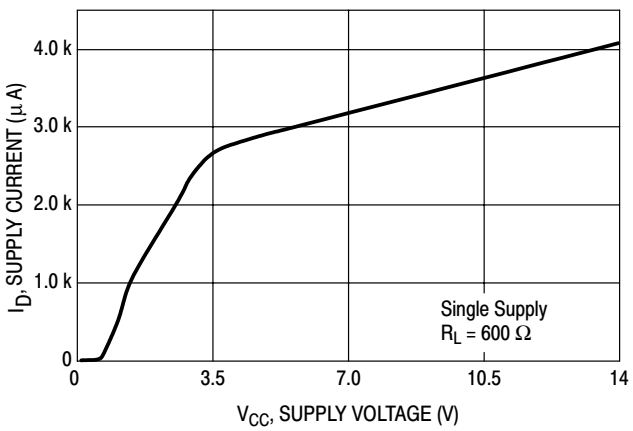


Figure 15. Supply Current versus Supply Voltage with Load

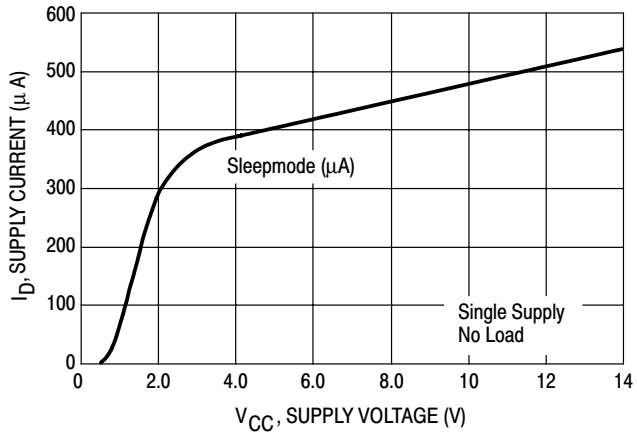


Figure 16. Supply Current versus Supply Voltage

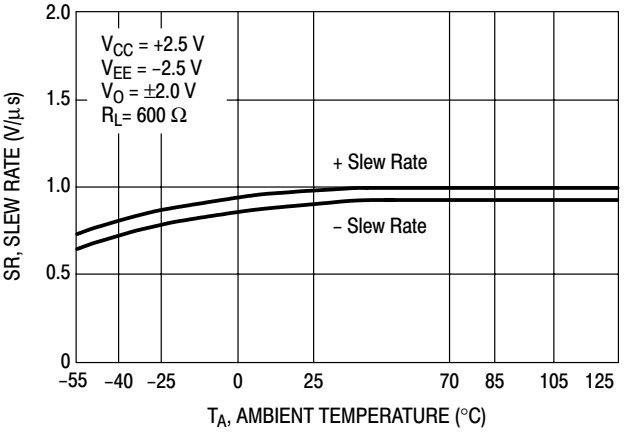


Figure 17. Slew Rate versus Temperature

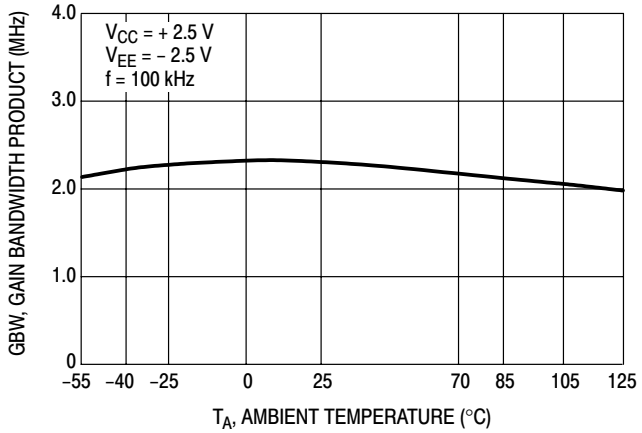


Figure 18. Gain Bandwidth Product versus Temperature

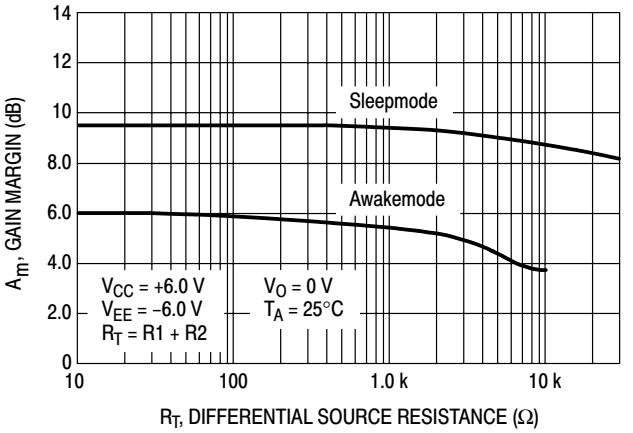


Figure 19. Gain Margin versus Differential Source Resistance

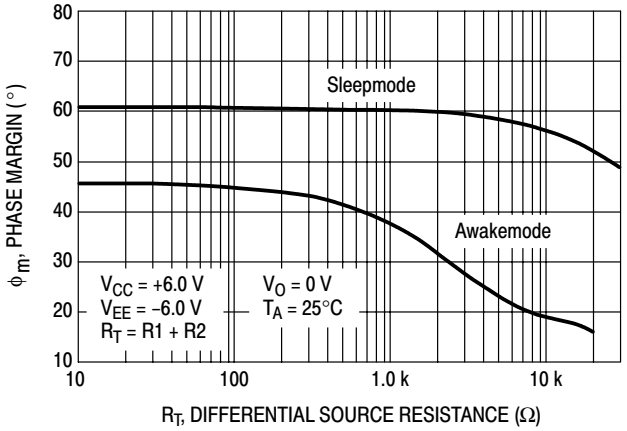


Figure 20. Phase Margin versus Differential Source Resistance

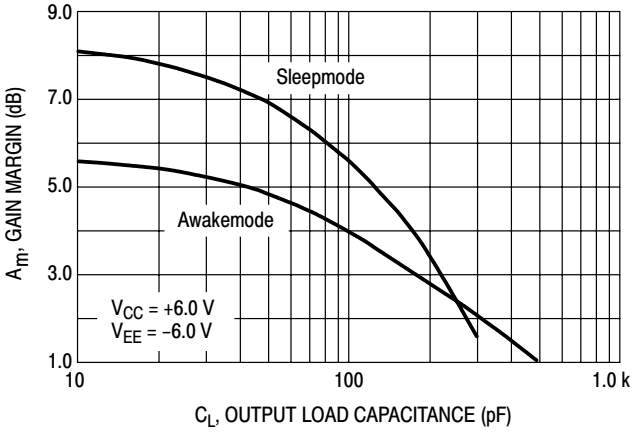


Figure 21. Gain Margin versus Output Load Capacitance

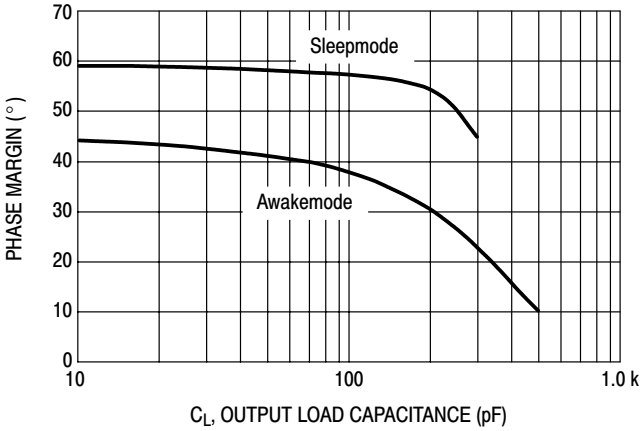


Figure 22. Phase Margin versus Output Load Capacitance

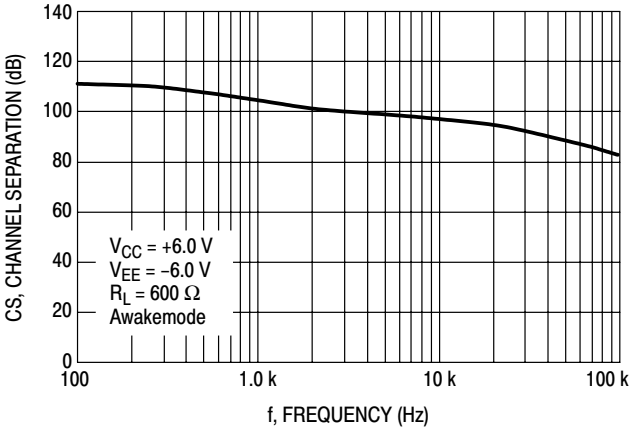


Figure 23. Channel Separation versus Frequency

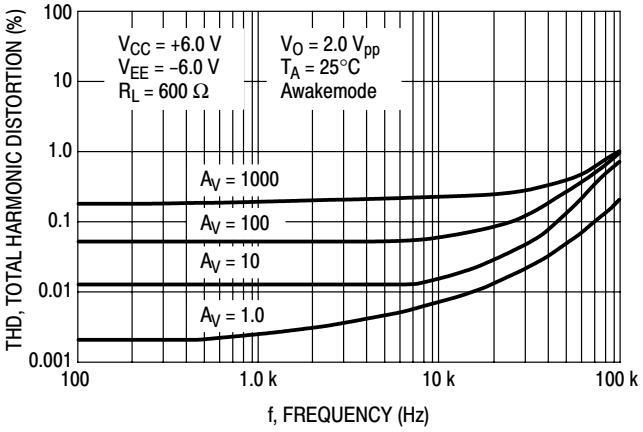


Figure 24. Total Harmonic Distortion versus Frequency

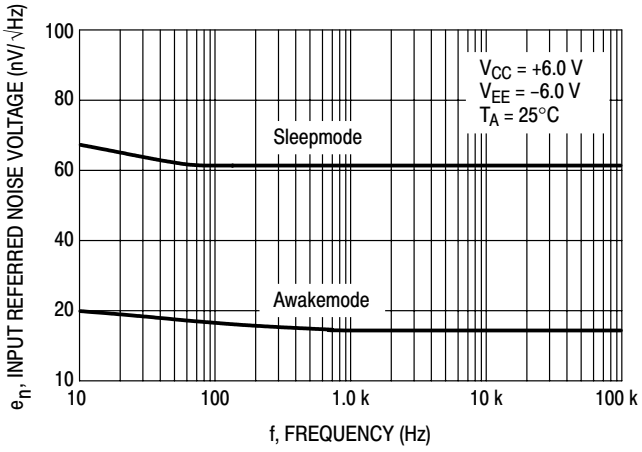


Figure 25. Input Referred Noise Voltage versus Frequency

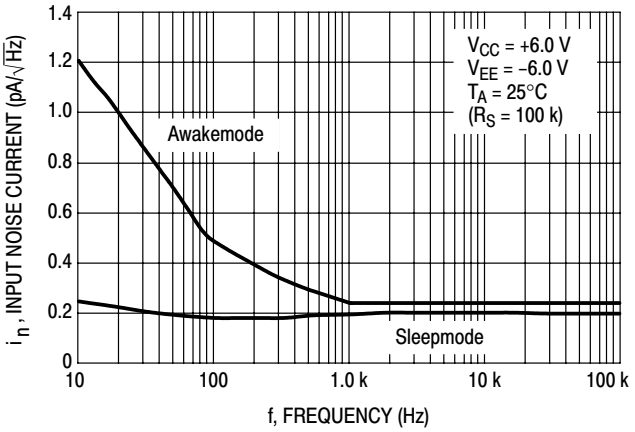


Figure 26. Current Noise versus Frequency

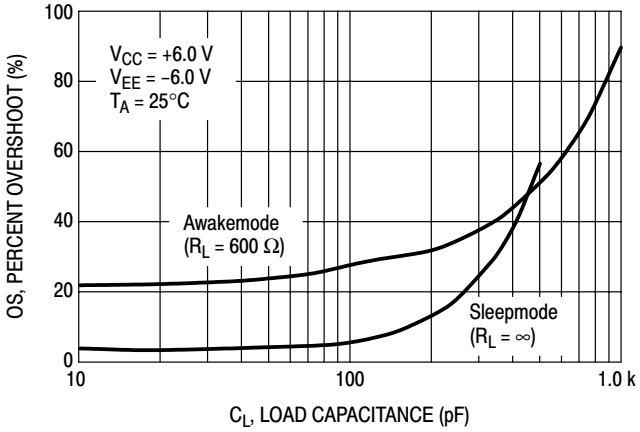
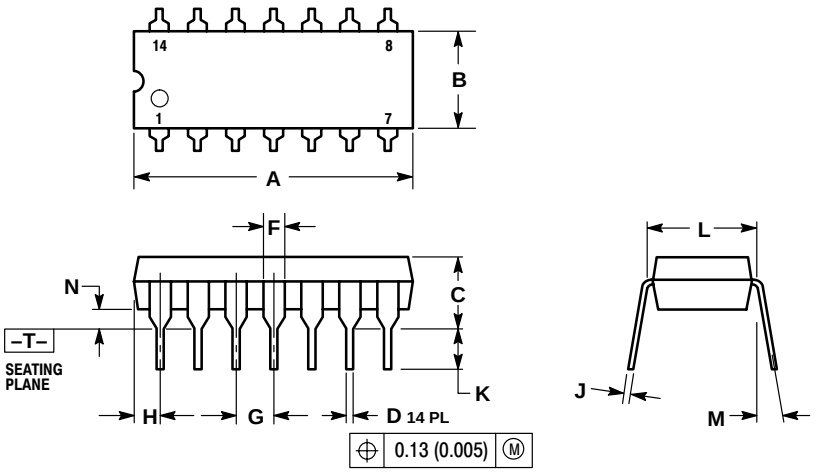


Figure 27. Percent Overshoot versus Load Capacitance

PACKAGE DIMENSIONS

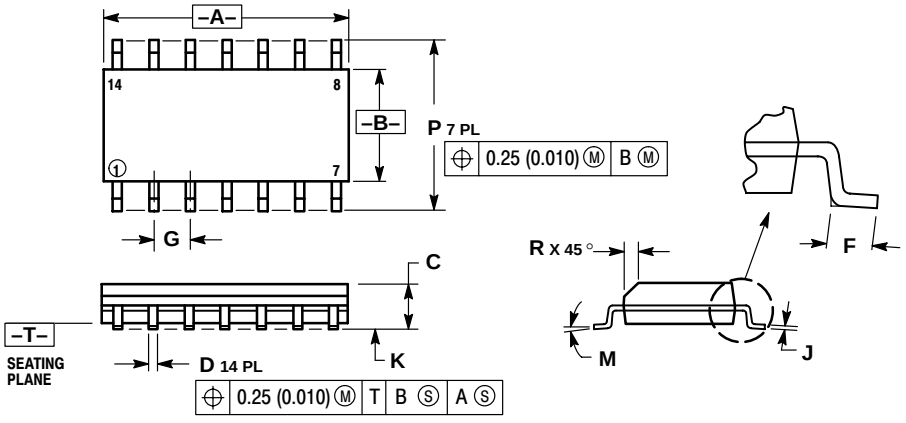
PDIP–14
P SUFFIX
CASE 646–06
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

SO–14
D SUFFIX
CASE 751A–03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

Notes

Notes

Notes

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