Order this document by MC33351A/D

MOTOROLA

MC33351A

Advanced Information

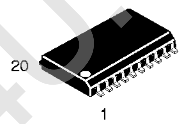
Lithium Battery Protection Circuit for Three or Four Cell Battery Packs

LITHIUM BATTERY PROTECTION CIRCUIT FOR THREE OR FOUR CELL SMART BATTERY PACKS

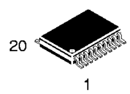
SEMICONDUCTOR TECHNICAL DATA

The MC33351A is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of three or four cell rechargeable battery packs. Cell protection features include a selectable charge interrupt, voltage sensing mode for precise cell voltage measurements, programmable overvoltage delay, choice of discharge current limit sensing elements consisting of either a low–side resistor or the high–side MOSFET switches, programmable discharge current limit threshold and shutdown delay, selectable cell voltage balancing, and a virtually zero current sleepmode state when the cells are discharged. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. The MC33351A is available in standard and low profile 20 lead surface mount packages.

- Selectable Charge Interrupt Voltage Sensing Mode for Precise Cell Voltage Measurements
- Programmable Overvoltage Delay
- Choice of Discharge Current Limit Sensing Elements consisting of either Low–Side Resistor or High–Side MOSFET Switches
- Programmable Discharge Current Limit Threshold and Shutdown Delay
- Selectable Cell Voltage Balancing
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Programmable for Three or Four Cell Applications
- Minimum External Components for Inclusion within the Battery Pack
- Available in Standard and Low Profile Surface Mount Package

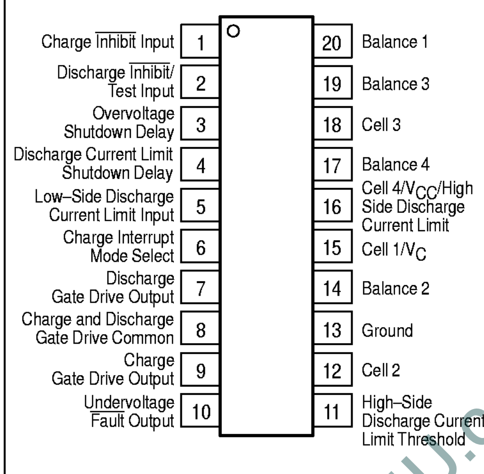


DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)



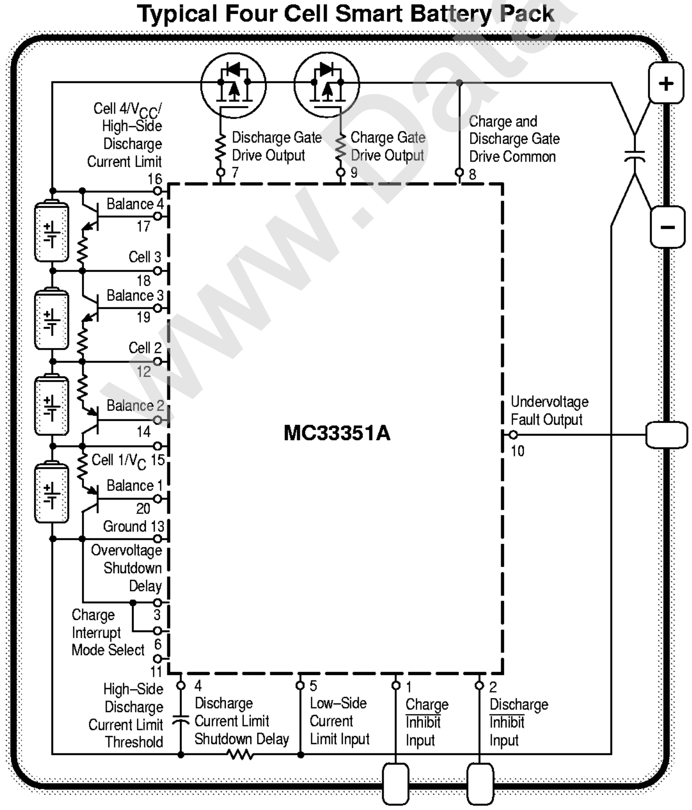
DTB SUFFIX
PLASTIC PACKAGE
CASE 948E
(TSSOP–20)

PIN CONNECTIONS



(Top View)

Typical Four Cell Smart Battery Pack



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33351ADW	T_J = –40° to +85°C	SO–20L
MC33351ADTB		TSSOP–20

This document contains information on a new product. Specifications and information are subject to change without notice.

 Rev 0

Four Cell Smart Battery Pack with Low–Side Discharge Current Sensing, Charge Interrupt Voltage Sensing, and Cell Voltage Balancing

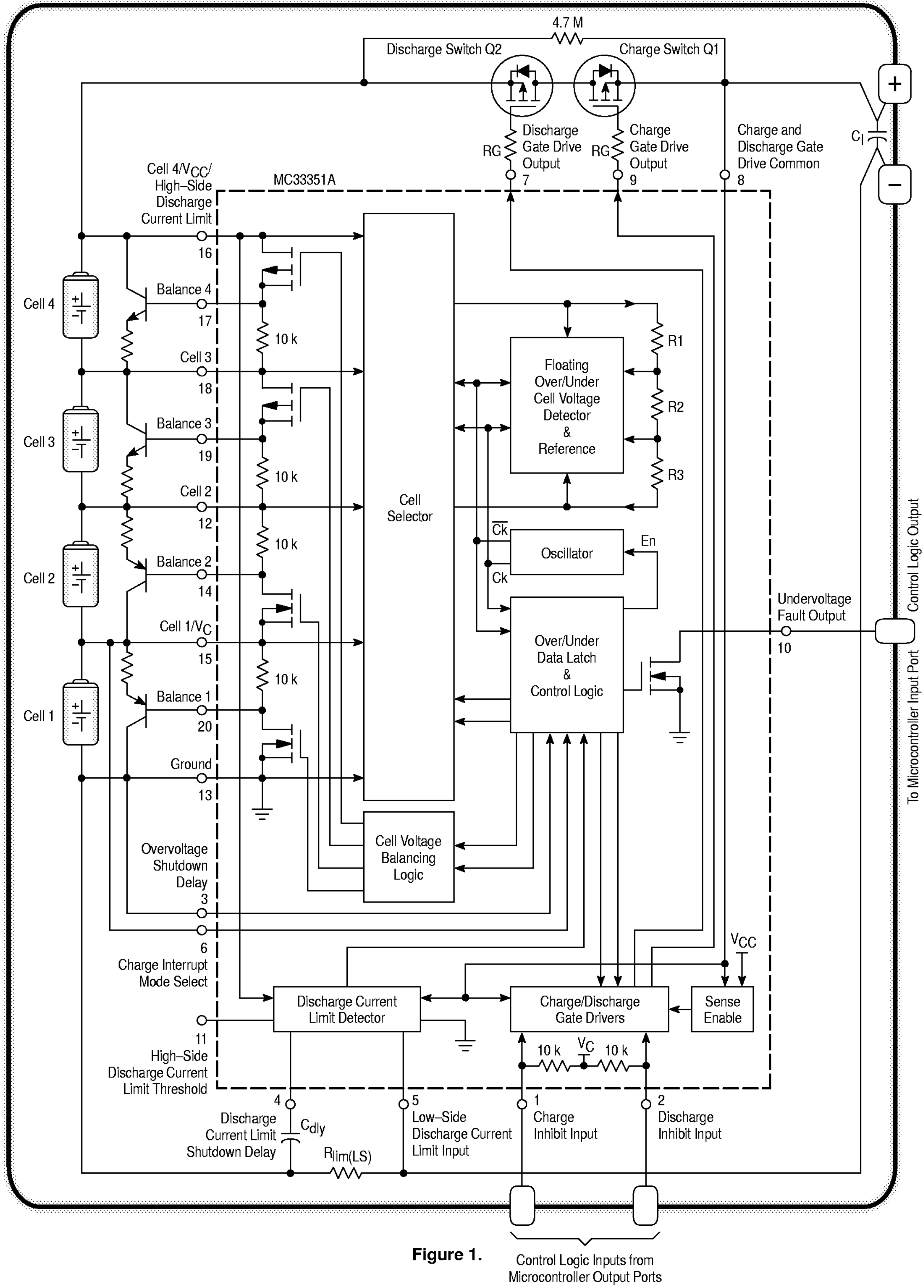


Figure 1.

Three Cell Smart Battery Pack with High–Side Discharge Current Sensing

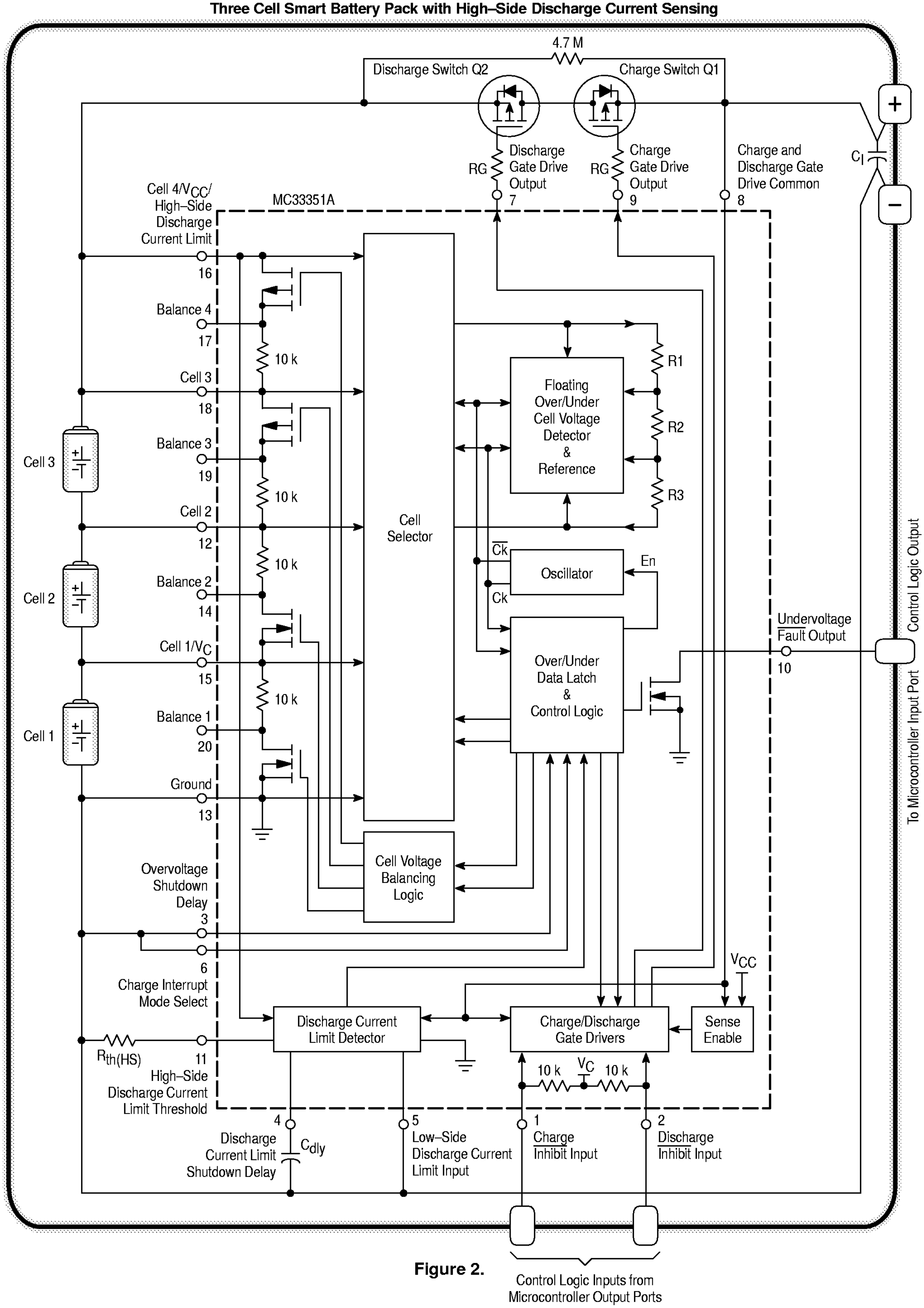


Figure 2.

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Input Voltage (Measured with respect to Ground, Pin 13)	V_{IR}		V
Cell 1/Vc (Pin 15)		7.5	
Cell 2 (Pin 12)		10	
Cell 3 (Pin 18)		18	
Cell 4/ Vcc/ High Side Discharge Current Limit (Pin 16)		20	
Charge Inhibit Input (Pin 1)		7.5	
Discharge Inhibit Input (Pin 2)		7.5	
Overvoltage Shutdown Delay (Pin 3)		7.5	
Discharge Current Limit Shutdown Delay (Pin 4)		20	
Low–Side Discharge Current Limit Input (Pin 5)		7.5	
Voltage Sampling Mode Select (Pin 6)		7.5	
Discharge Gate Drive Output (Pin 7)		18	
Charge Gate Drive Common (Pin 8)		20	
Charge Gate Drive Output (Pin 9)		18	
Undervoltage Fault Output (Pin 10)		20	
High–Side Current Limit Threshold (Pin 11)		7.5	
Cell Balancing Current (Note 1)	I_{bal}		mA
Balance 3, Balance 4 Source Current (Pin 19, 17)		50	
Balance 1, Balance 2 Sink Current (Pin 20, 14)		50	
Undervoltage Fault Output Sink Current (Pin 10)	I_{flt}	10	mA
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$		°C/W
DTB Suffix, TSSOP Plastic Package, Case 948E		135	
DW Suffix, SO–20L Plastic Package, Case 751D		105	
Operating Junction Temperature (Note 1, 2)	T_J	–40 to 150	°C
Storage Temperature	T_{stg}	–55 to 150	°C

ELECTRICAL CHARACTERISTICS (V_{cc} (Pin 16) = 14V, $V_{cell\ 3}$ (Pin 18) = 10.5V, $V_{cell\ 2}$ (Pin 12) = 7.0V, $V_{cell\ 1}$ (Pin 15) = 3.5V, C_{dly} (Pin 4) = 1000 pF, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE SENSING					
Cell Charging Cutoff (Pin 15 to 13, 12 to 15, 18 to 12, 16 to 18)					
Overvoltage Threshold, V_{Cell} Increasing MC33351A–1,3	$V_{th(OV)}$	4.2075		4.2925	V
MC33351A–2,4		4.3065		4.3935	
Overvoltage Hysteresis, V_{Cell} Decreasing	V_H	50	125	200	mV
Delay	$t_{dly(OV)}$				
One Overvoltage Sample (Pin 3 = Gnd)		0	–	1.2	s
Two Consecutive Overvoltage Samples (Pin 3 = Vc)		1.0	–	2.1	s
Cell Discharging Cutoff MC33351A–1,2	$V_{th(UV)}$	2.185	2.3	2.415	V
MC33351A–3,4		1.900	2.0	2.100	
Undervoltage Threshold, V_{Cell} Decreasing					
Input Bias Current During Cell Voltage Sampling	I_{IB}	–	28	–	µA
Cell Voltage Sampling Rate	$t_{(smpl)}$	–	1.0	–	s
Charge Interrupt	$V_{th(Intrrpt)}$				V
Input Voltage Range (Pin 6)					
Enabled		–	(V_c/2+0.2 to V_c)	–	
Disabled		–	(0 to V_c/2–0.2)	–	
Enabled Charge Interrupt Time	t_{Intrrp}	–	20	–	ms
Cell Program Input Voltage Range (Pin 18 to 16)	$V_{th(3/4)}$				V
Three Cell Mode Enabled		–	0 to 0.3	–	
Four Cell Mode Enabled		–	0.7 to $V_{cell\ 4}$	–	
CELL VOLTAGE BALANCING					
Internal Balancing MOSFET On–Resistance	$R_{DS(on)}$				Ω
Balance 3, Balance 4 (Pin 19, 17)		–	100	–	
Balance 1, Balance 2 (Pin 20, 14)		–	50	–	

NOTE: 1 Maximum package power dissipation limits must be observed.
2. Tested ambient temperature range for the MC33351A:
T_{low} = –25°C T_{high} = +85°C

ELECTRICAL CHARACTERISTICS (V_{cc} (Pin 16) = 14V, $V_{cell\ 3}$ (Pin 18) = 10.5V, $V_{cell\ 2}$ (Pin 12) = 7.0V, $V_{cell\ 1}$ (Pin 15) = 3.5V, C_{dly} (Pin 4) = 1000 pF, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSING					
High–Side Discharge Current Limit (Pin 16 to Pin 8)					
Threshold Voltage	$V_{th(HSdschg)}$				
$R_{pin\ 11}$ = 1.0 MΩ		200	280	350	mV
$R_{pin\ 11}$ = 2.0 MΩ		100	170	200	mV
Delay					
Overcurrent Detect (V_{sense} = 250 mV)	$t_{dly(HSdschg)}$	3.0		6.0	ms
Short Circuit Detect (V_{sense} = 1.0 V)		0.5		2.5	ms
Low–Side Discharge Current Limit (Pin 13 to Pin 5)					
Threshold Voltage	$V_{th(LSdschg)}$	48	50	58	mV
Delay					
Overcurrent Detect (V_{sense} = 50 mV)	$t_{dly(LSdschg)}$	3.0		6.0	ms
Short Circuit Detect (V_{sense} = 200 mV)		0.3		0.4	ms
LOGIC					
Charge and Discharge Inhibit Inputs (Pin 1, 2)					
Threshold Voltage	$V_{th(inhbt)}$	–	$V_C/2$	–	V
Propagation Delay to Respective Gate Drive Output	$t_{PL/H}$	–	100	–	µs
Undervoltage Fault Output (Pin 10)					
Low State Sink Resistance		–	100	–	Ω
Off State Leakage Current (V_{drain} = 16V)		–	100	–	nA
Detection Delay Time Before Discharge MOSFET Turn Off		–	16	–	s
Charge and Discharge Gate Drive Outputs (Pin 9, 7)					Ω
High State Source Resistance	$R_{DS(source)}$	–	100	–	
Low State Sink Resistance	$R_{DS(sink)}$	–	100	–	
TOTAL DEVICE					
Average Cell Current	I_{CC}				
Four Cell Mode					
Operating (V_{CC} = 16 V)		–	15	20	µA
Sleepmode (V_{CC} = 8.0 V)		–	5.0	50	nA
Three Cell Mode					
Operating (V_{CC} = 12 V)		–	15	20	µA
Sleepmode (V_{CC} = 6.0 V)		–	5.0	50	nA
Minimum Operating Cell Voltage	V_{CC}				V
Programmed for Three, or Four, Cell Operation					
Cell 1 Voltage		1.5	1.8	–	
Cell 2, Cell 3, or Cell 4 Voltage		0.7	0.8	–	

NOTE: 1 Maximum package power dissipation limits must be observed.
2. Tested ambient temperature range for the MC33351A:
T_{low} = –25°C T_{high} = +85°C

Figure 3. Over Voltage Threshold versus Temperature

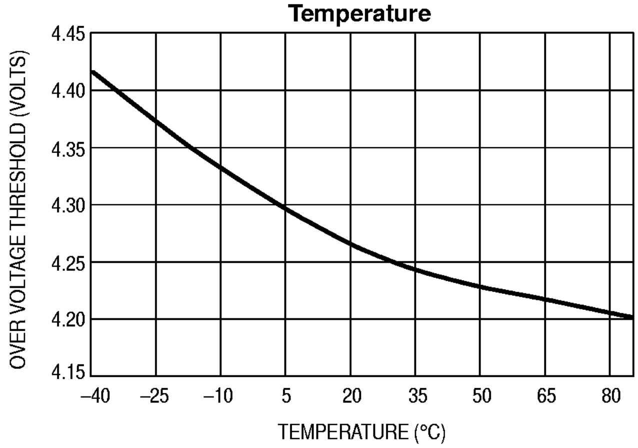


Figure 4. Charge ON Voltage Threshold versus Temperature

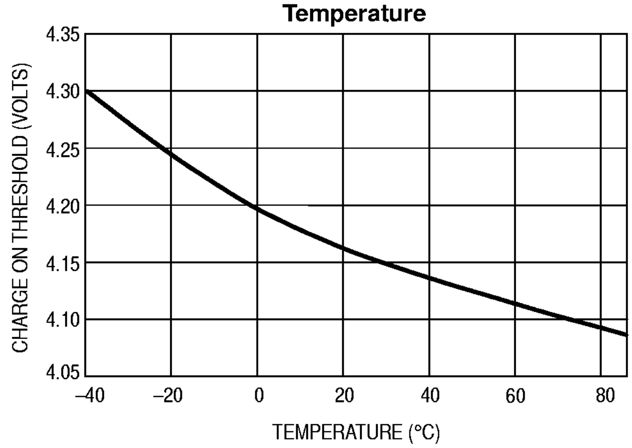


Figure 5. Undervoltage Threshold versus Temperature

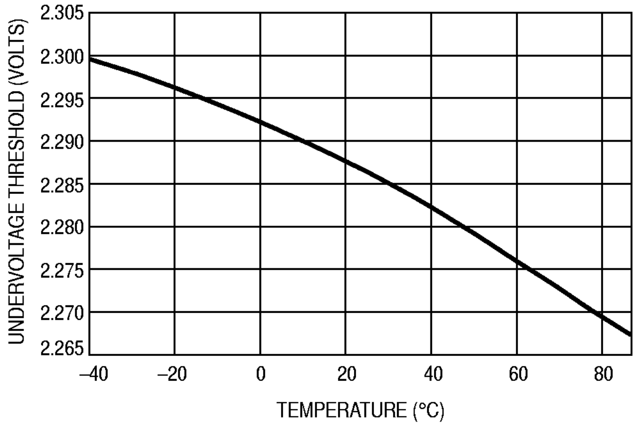


Figure 6. Discharge Current (Low Side) versus Temperature

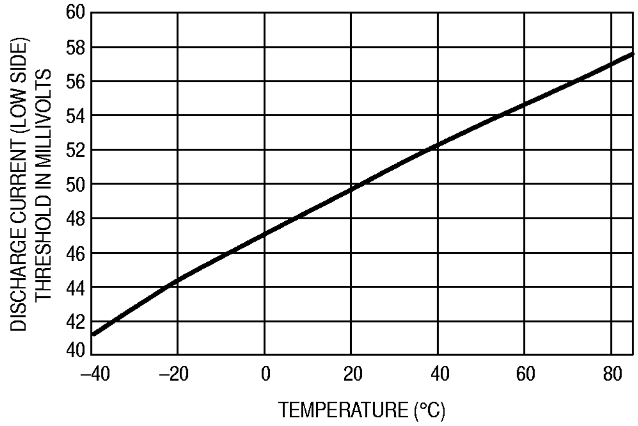


Figure 7. Discharge Current (High Side) Threshold versus Temperature (R11 = 1.5 mOhms)

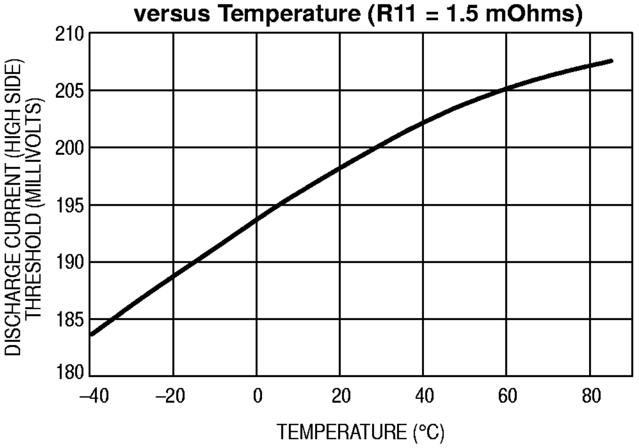


Figure 8. Discharge Current (High Side) versus Resistance

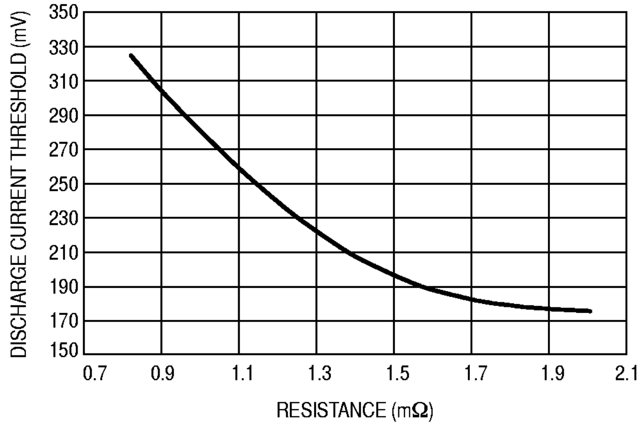


Figure 9. V_{CC} versus I_{EE} (No Load)

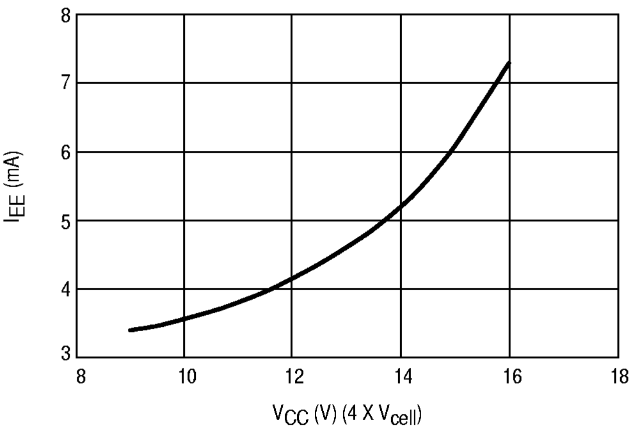
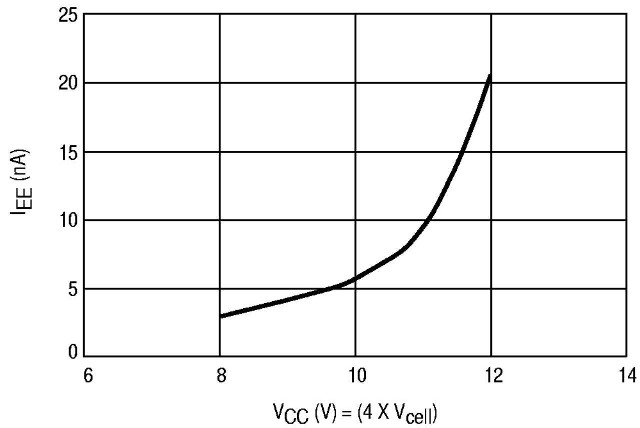


Figure 10. V_{CC} versus I_{EE} (Sleep–Mode)



PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	Charge $\overline{\text{Inhibit}}$ Input	A logic low level at this input will disable battery pack charging. A 10 k internal pull–up resistor connects from this pin to V_C.
2	Discharge $\overline{\text{Inhibit}}$ Input	A logic low level at this input will disable battery pack discharging. A 10 k internal pull–up resistor connects from this pin to V_C.
3	Overvoltage Shutdown Delay	This input controls the required number of cell overvoltage events that must be detected before charge switch Q1 is turned off. With a logic level low at this input, charge switch Q1 turns off after a single overvoltage event is detected. With a logic level high, charge switch Q1 turns off after two successive overvoltage events are detected.
4	Discharge Current Limit Shutdown Delay	A capacitor connects from this pin to ground and is used to program a time delay from when the discharge current limit is exceeded to when discharge switch Q2 is turned off.
5	Low–Side Discharge Current Limit Input	This pin is used to monitor the load induced voltage drop that appears across current sensing resistor $R_{lim(LS)}$. This voltage drop is sensed by pins 13 and 5.
6	Charge Interrupt Mode Select	The logic level that is applied to this input determines if the charge current will be interrupted during the cell voltage sampling period. The charge current is interrupted when this input is connected to V_C, and not interrupted when connected to ground, pin 13.
7	Discharge Gate Drive Output	This output connects to the gate of discharge switch Q2 allowing it to enable or disable battery pack discharging.
8	Charge and Discharge Gate Drive Common	This pin provides a gate turn–off path for charge switch Q1. The charge switch source and the battery pack positive terminal connect to this point.
9	Charge Gate Drive Output	This output connects to the gate of charge switch Q1 allowing it to enable or disable battery pack charging. Also, connecting this pin to 3.0V above V_C the internal logic is held in reset state and both MOSFET switches are turned on.
10	Undervoltage $\overline{\text{Fault}}$ Output	This is an open drain output that is active low when an undervoltage fault limit has been exceeded. Discharge switch Q2 will turn off 16 seconds after the $\overline{\text{Fault}}$ goes low.
11	High–Side Discharge Current Limit Threshold	A resistor connects from this pin to ground and is used to program the high–side discharge current limit threshold. The programmed threshold voltage is sensed by pins 16 and 8.
12	Cell 2	This pin connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 2 and the negative terminal of Cell 3.
13	Ground	This is the protection IC ground and all voltage ratings are with respect to this pin.
14	Balance 2	This pin is used if cell balancing is desired. It connects to the drain of an internal N–channel MOSFET and is active low during the balancing of Cell 2.
15	Cell 1/V_C	This is a multi–function pin that connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 1 and the negative terminal of Cell 2. This pin also provides bias for the internal logic.
16	Cell 4/V_{CC}/High–Side Discharge Current Limit	This is a multi–function pin that connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 4 and to provide positive supply voltage for the protection IC. This pin can also be used for high–side discharge current limit protection by monitoring the load induced voltage drop that appears across the on–resistance of switches Q2 and diode of Q1. This voltage drop is sensed by pins 16 and 8.
17	Balance 4	This pin is used if cell balancing is desired. It connects to the drain of an internal P–channel MOSFET and is active high during the balancing of Cell 4.
18	Cell 3	This pin connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 3 and the negative terminal of Cell 4.
19	Balance 3	This pin is used if cell balancing is desired. It connects to the drain of an internal P–channel MOSFET and is active high during the balancing of Cell 3.
20	Balance 1	This pin is used if cell balancing is desired. It connects to the drain of an internal N–channel MOSFET and is active low during the balancing of Cell 1.

PROTECTION CIRCUIT OPERATING MODE TABLE

Input Conditions Cell Status	Circuit Operation Battery Pack Status	Outputs: MOSFET Switches (Note 1) Charge Q1	Outputs: MOSFET Switches (Note 1) Discharge Q2	Outputs: Cell Balancing Balancing Outputs
CELL CHARGING/DISCHARGING				
Storage or Nominal Operation: No current or voltage faults	Both Charge MOSFET Q1 and Discharge MOSFET Q2 are on. The battery pack is available for charging or discharging.	On	On	Active
CELL CHARGING FAULT/RESET				
Charge Voltage Limit Fault: $V_{Cell} \geq V_{th(OV)}$ for $t_{dly(OV)}$ $t_{dly(OV)}$ = 0 to 1.2 s, Pin 3 to 13 1.0 to 2.1 s, Pin 3 to 15	Charge MOSFET Q1 is latched off and the cells are disconnected from the charging source. An internal hysteresis voltage is generated when the overvoltage cell is sensed. The shutdown delay is programmable for either one or two successive overvoltage events by the state of Pin 3. The battery pack is available for discharging.	On to Off	On	Active
Charge Voltage Limit Reset: $V_{Cell} < (V_{th(OV)} - V_H)$ for 1.2 s	Charge MOSFET Q1 will turn on when the voltage across the overvoltage cell falls sufficiently to overcome the internal hysteresis voltage. This can be accomplished by applying a load to the battery pack.	Off to On	On	Active
CELL DISCHARGING FAULT/RESET				
Discharge Current Limit Fault: $V_{Pin\ 16} \geq (V_{Pin\ 8} + Vth_{(HS\ dschg)}$ for $t_{dly(HS\ dschg)}$ or $V_{Pin\ 5} \geq (V_{Pin\ 13} + V_{th(LS\ dschg)}$ for $t_{dly(LS\ dschg)}$	Discharge MOSFET Q2 is latched off and the cells are disconnected from the load. Q2 will remain in the off state as long as $V_{Pin\ 16}$ exceeds $V_{Pin\ 8}$ by $\approx V_{TH(HSdschrg)}$. A discharge current limit fault can be activated by either high–side or a low–side current sensing methods. The battery pack is available for charging.	On	On to Off	Active
Discharge Current Limit Reset: $V_{Pin\ 16} - V_{Pin\ 8} < V_{TH(HSdschrg)}$ $V_{Pin\ 5} - V_{Pin\ 13} < V_{TH(LSdschrg)}$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 16}$ no longer exceeds $V_{Pin\ 8}$ by 2.0 V. This can be accomplished by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger.	On	Off to On	Active
Discharge Voltage Limit Fault: $V_{Cell} \leq V_{th(UV)}$ for 2.1 s	Undervoltage Fault Output (Pin 10) is driven low after two successive undervoltage events are detected. After a 16 second delay, discharge MOSFET Q2 is latched off, the cells are disconnected from the load, and the protection circuit enters a low current sleepmode state. The battery pack is available for charging.	On	On to Off after 16 s (Note 2)	Disabled
Discharge Voltage Limit Reset: $V_{Pin\ 8} > (V_{Pin\ 16} + 0.6\ V)$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 8}$ exceeds $V_{Pin\ 16}$ by 0.6 V. This can be accomplished by connecting the battery pack to the charger.	On	Off to On	Active
FAULTY CELL				
Simultaneous Charge and Discharge Voltage Limit Faults	This condition can happen if there is a defective cell in the battery pack. The protection circuit will remain in the sleepmode state until the battery pack is connected to a charger. If Cell 2, 3, or 4 is faulty and a charger is connected, the protection circuit will cycle in and out of sleepmode. If Cell 1 is faulty (<1.5 V) the protection circuit logic will not function and the battery pack cannot be charged.	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty

NOTE: 1 Charge switch Q1 and discharge switch Q2 can be selectively turned off via the appropriate $\overline{\text{inhibit}}$ input except during the sleepmode state.
2. The 16 s delay time can be reduced by strobing the Discharge $\overline{\text{Inhibit}}$ input low immediately after the Undervoltage $\overline{\text{Fault}}$ Output goes low.

OPERATING DESCRIPTION

INTRODUCTION

The demand for smaller lightweight portable electronic equipment has dramatically increased the requirements of battery performance. Today's most attractive chemistries include lithium–polymer, lithium–ion, and lithium–metal. Each of these chemistries require electronic protection in order to constrain cell operation to within the manufacturers limits.

Rechargeable lithium–based cells require precise charge and discharge termination limits for both voltage and current in order to maximize cell capacity, cycle life, and to protect the end user from a catastrophic event.

The MC33351A features internally–fixed cell voltage limits, programmable cell voltage balancing, low operating current, a virtually zero current sleepmode state, and requires few external components.

OPERATING DESCRIPTION

The MC33351A is specifically designed to be placed in the battery pack where it can be continuously powered from either three or four lithium cells. In order to maintain cell operation within specified limits, the protection circuit senses both cell voltage and discharge current, and correspondingly controls the state of two P–channel MOSFET switches. These switches, Q1 and Q2, are placed within the series path of the positive terminal of cell 4 and the positive terminal of the battery pack. For lowside current limit sense, a resistor is placed within the series path of the negative terminal of Cell 1 and the negative terminal of the battery pack. This configuration allows the protection circuit to interrupt the appropriate charge or discharge path FET in the event that a programmed voltage or current limit for any cell has been exceeded.

A functional description of the protection circuit blocks follows. Refer to the detailed block diagram shown in Figure 1.

Voltage Sensing

Individual cell voltage sensing is accomplished by the use of the Cell Selector in conjunction with the Floating Over/Under Voltage Detector and Reference block. The Cell Selector applies the voltage of each cell across an internal resistor divider string. The voltage at each of the tap points is sequentially polled and compared to an internal reference. If a limit has been exceeded, the result is stored in the Over/Under Data Latch and Control Logic block. The Cell Selector is gated on for a 4.0 ms period at a fixed one second repetition rate. This low duty cycle sampling technique reduces the average load current that the divider presents across each cell, thus extending the useful battery pack capacity. When programmed for four cell operation, the cells are sensed in the following sequence:

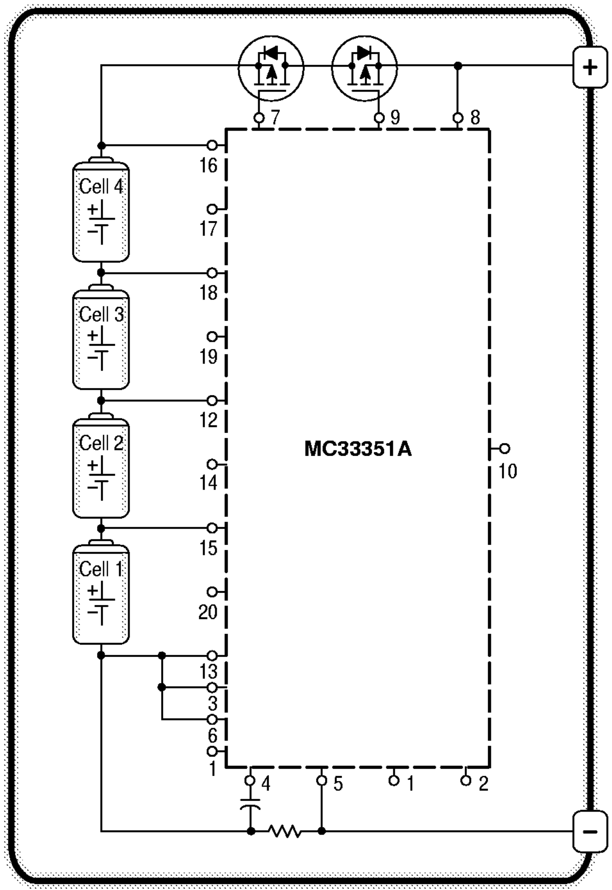


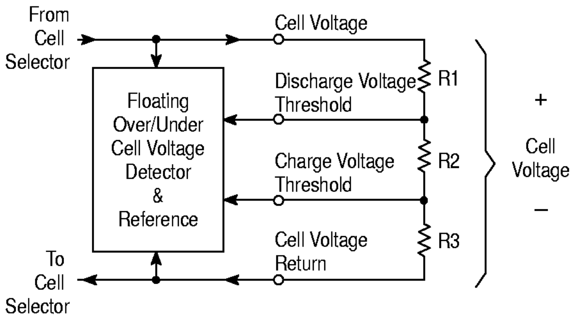
Figure 11. Simplified Four Cell Smart Battery Pack

Cell Sensing Sequence

Polling Sequence	Time (ms)	Cell Sensed	Tested Limit
1	0.25	Cell 1	Overvoltage
2	0.25	Cell 2	Overvoltage
3	0.25	Cell 3	Overvoltage
4	0.25	Cell 4	Overvoltage
5	0.25	Cell 1	Undervoltage
6	0.25	Cell 2	Undervoltage
7	0.25	Cell 3	Undervoltage
8	0.25	Cell 4	Undervoltage

By incorporating this polling technique with a single floating comparator and voltage divider, a significant reduction of circuitry and trim elements is achieved. This results in a smaller die size, lower cost, and reduced operating current.

Figure 12. Cell Voltage Limit ***Sampling vs. Programming***



The cell charge and discharge voltage limits are controlled by the values selected for the internal resistor divider string. As the battery pack reaches full charge, the Cell Voltage Detector will sense an overvoltage fault condition on the first cell that exceeds the pre–set overvoltage limit. The fault information is stored in a data latch and charge MOSFET Q1 is turned off, disconnecting the battery pack from the charging source. An internal current source pull–up is then applied to the lower tap of the divider when the overvoltage cell is again sensed. This creates an input hysteresis voltage with divider resistors R1 and R2. As a result of an overvoltage fault, the battery pack is available for discharging only.

The overvoltage fault is reset by applying a load to the battery pack. As the voltage across the highest voltage cell falls below the hysteresis level, charge MOSFET Q1 will turn on and the current source pull–up will turn off. The battery pack will now be available for charging or discharging.

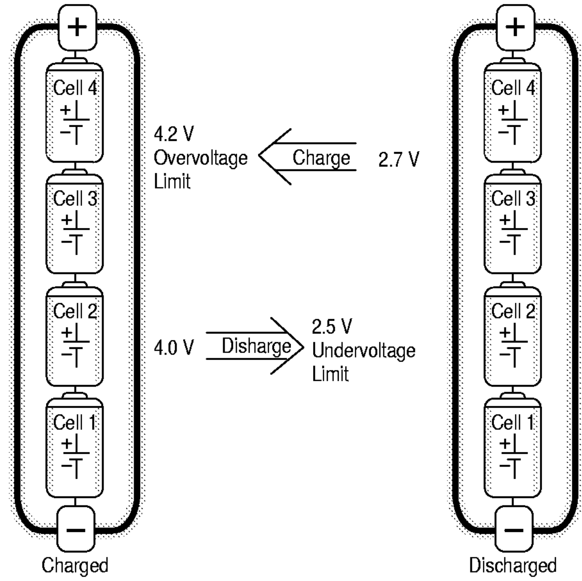
As the load eventually depletes the battery pack charge, the Cell Voltage Detector will sense an undervoltage fault condition on the first cell that falls below the designed undervoltage limit. After an undervoltage cell is detected, discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. The protection circuit will now enter a low current sleepmode state drawing less than 15.0 nA typically, thus preventing any further cell discharging. As a result of the undervoltage fault, the battery pack is available for charging only.

The undervoltage fault is reset by applying charge current to the battery pack. When the voltage on Pin 8 exceeds Pin 16 by 0.6 V, discharge MOSFET Q2 will be turned on. The battery pack will now be available for charging or discharging.

Cell Voltage Balancing

With series connected cells, successive charge and discharge cycles can result in a significant difference in cell voltage with a corresponding degradation of battery pack capacity. Figure 13 illustrates the operation of an unbalanced four cell pack. As the cells become unbalanced, the full battery pack capacity is not realized. This is due to the requirement that charging must terminate when the highest voltage cell reaches the overvoltage limit, and discharging must terminate when the lowest voltage cell reaches the undervoltage limit. By employing a method of keeping the cell voltages equal, each of the cells can be charged and discharged to their specified limits, thus attaining the maximum possible capacity.

Figure 13. Unbalanced Battery Pack Operation



The MC33351A contains a Cell Voltage Balancing Logic circuit that controls four internal MOSFETs. These MOSFETs are connected to an external transistor and resistor combination across the individual cells. The circuit samples the voltage of each cell during the polling period. If all of the cells are below the programmed overvoltage fault limit, no cell balancing takes place. If one or more cells reach the overvoltage fault limit, a specific latch is set for each cell. At the end of the polling period, charge MOSFET Q1 is turned off and the latches are interrogated. If all of the latches were set, no cell balancing takes place. If one, two, or three latches were set, the required cell balancing MOSFETs are then activated. The overvoltage cells are discharged to the pre–set level. As each cell attains this level, the balancing MOSFETs successively turn off. Upon completion of cell balancing, charge MOSFET Q1 is turned on. Cell voltage balancing can be active during charging and discharging, but is disabled during the low current sleepmode state.

Cell Programming

The protection circuit can be programmed for operation with either three or four cell battery pack. If three cells are required, the input for the empty cell position must be connected to V_{CC}, (connect pin #18 to pin #16). Refer to the Cell Programming table shown below and the specific application figure.

Cell Programming

Number of Cells	Program (Pin 18–>Pin 16)	Application Figure
3	0V – 0.3V	2
4	0.7V – VCell4	1

Test Mode

A test option is provided to speed up device and battery pack testing. By connecting Pin 9 to 3.0 V above V_C the internal logic is held in a reset state and both MOSFET switches are turned on. Upon release, the Control Logic becomes active and the cell are polled within 4.0 ms.

Discharge Current Sensing

Discharge current limit protection can be selectively added to the battery pack with the addition of a sense resistor $R_{lim(dschg)}$ on the Low–Side or by monitoring the voltage drop across the series FETs on the High–Side.

Sense resistor – low–side

The sense resistor $R_{lim(dschg)}$ is placed in series with the negative terminal of Cell 1 and the negative terminal of the battery pack, Refer to Figure 1.

As the battery pack discharges, Pins 5 and 13 sense the voltage drop across $R_{Lim(dschg)}$.

A discharge current limit fault is detected if the voltage at Pin 5 is greater than Pin 13 by ***50 mV for more than 3.0 ms.*** The fault information is stored in a data latch and discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. As a result of the discharge current fault, the battery pack is available for charging only. The discharge current limit is given by:

$$I_{Lim(dschg)} = \frac{V_{th(dschg)}}{R_{Lim(dschg)}} = \frac{50\ mV}{R_{Lim(dschg)}}$$

Voltage across FETs – high–side

A 1MΩ or 2MΩ resistor connected from pin# 11 to ground is used to program the high–side discharge current limit threshold.

The discharge current fault is reset by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger. When the voltage on Pin 16 no longer exceeds Pin 8 by approximately 2.0 V, the Sense Enable circuit will turn on discharge MOSFET Q2. Discharge current sensing can be disabled by connecting Pin 16 to Pin 8.

The discharge current protection ***circuit contains a built in response delay of 3.0 ms. This helps to prevent fault activation when the battery pack is subjected to pulsed currents during charging or discharging.***

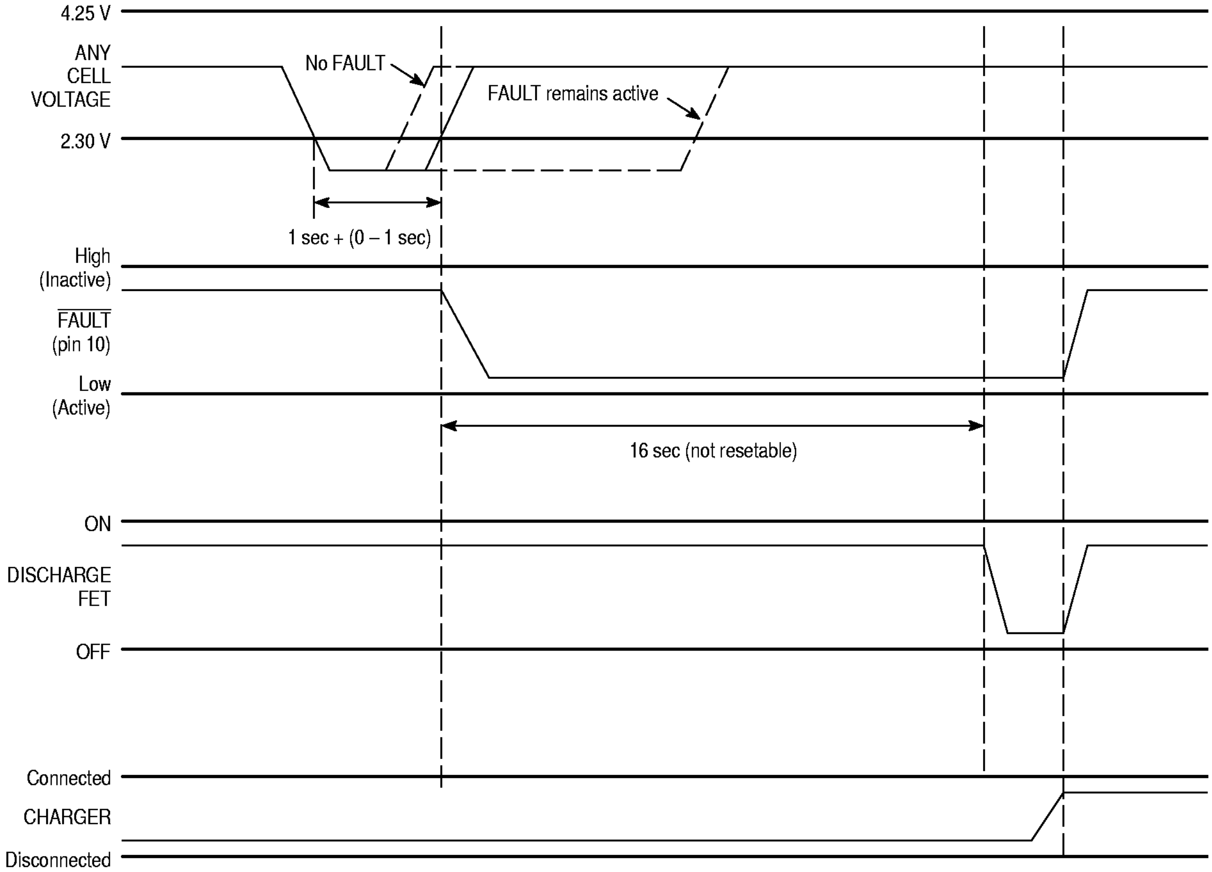
Battery Pack Application

Each of the application figures show a capacitor labeled C_l that connects directly across the battery pack terminals, and two resistors labeled R_g that are placed in series with the charge and discharge gate drive outputs. These components prevent excessive currents from flowing into the MC33351A when the battery pack terminals are shorted or arced and are **mandatory**. Capacitor C_l is ***a 1.0 µF ±20% ceramic leaded or surface mount type.*** It must be placed directly across the battery pack plus and minus terminals with extremely short lead lengths (≤1/16”) and as close to the IC as possible. The gate drive output resistors for both Q1 and Q2 are ***10 k***Ω ±5.o% carbon film type.

In applications where inordinately low leakage MOSFETs are used, the protection circuit may take several seconds to reset from an overcurrent fault after the load is removed. If desired, this situation can be remedied by providing a small leakage path for charging C_l, thus allowing Pin 8 to rapidly rise, so that it no longer exceeds Pin 16 by approximately 2.0 V. A 4.7 MΩ resistor placed across the MOSFET switches accomplishes this task with a minimum increase in cell discharge current when the battery pack is connected to the load.

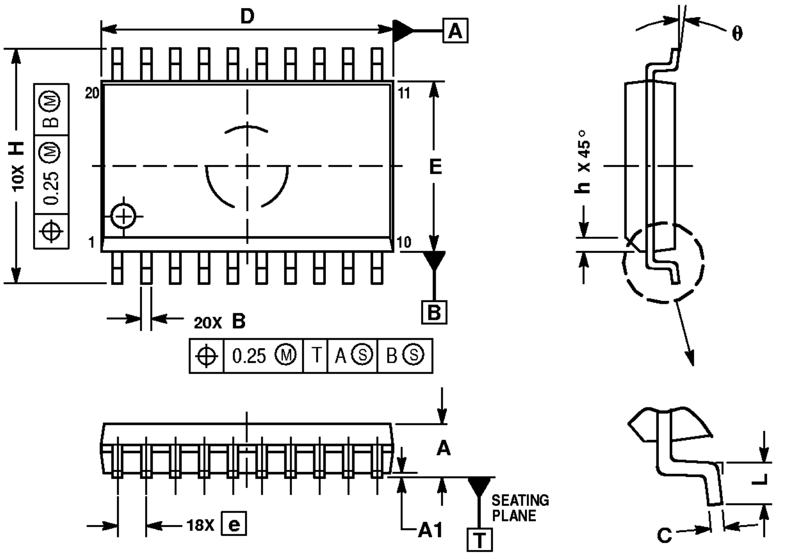
Upon assembly of the battery pack, it is imperative that Cell 1 be connected first so that V_C is properly biased. The remaining cells can then be connected in any order. This assembly method prevents forward biasing the protection IC substrate which can result in overheating and non–functionality.

MC33351A – Cell Voltage versus Undervoltage Fault



OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC PACKAGE
CASE 751D–05
(SO–20L)
ISSUE F

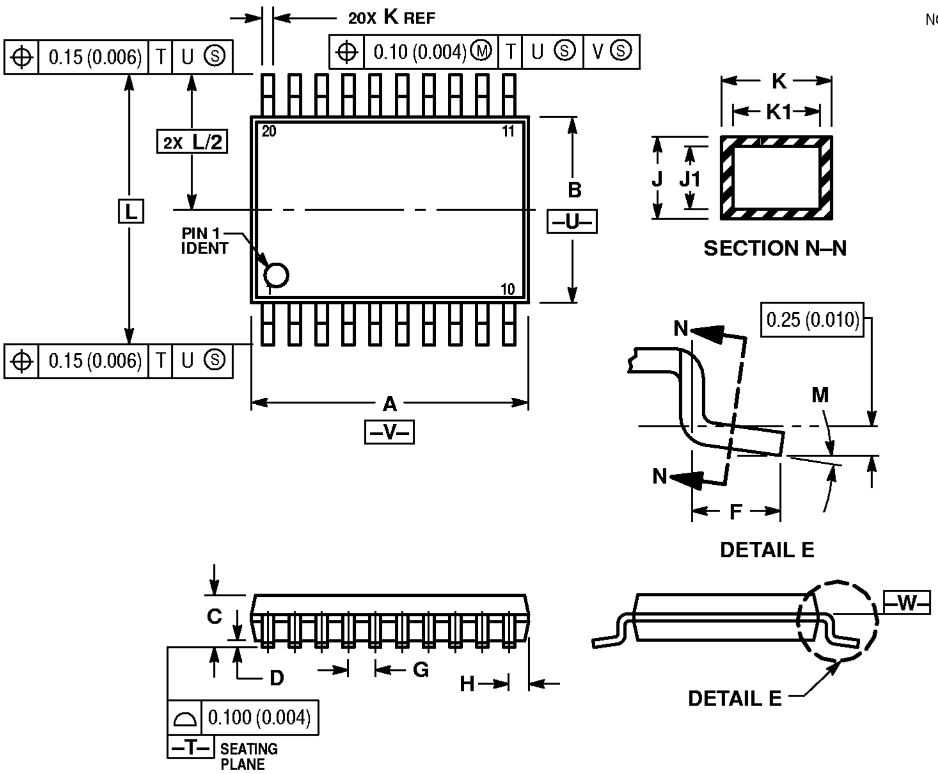


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

OUTLINE DIMENSIONS

DTB SUFFIX
PLASTIC PACKAGE
CASE 948E–02
(TSSOP–20)
ISSUE A



NOTES:
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION: MILLIMETER.
3 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°