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MOTOROLA

MC33369 thru MC33374

High Voltage Power Switching Regulator

HIGH VOLTAGE OFF–LINE POWER SWITCHING REGULATOR

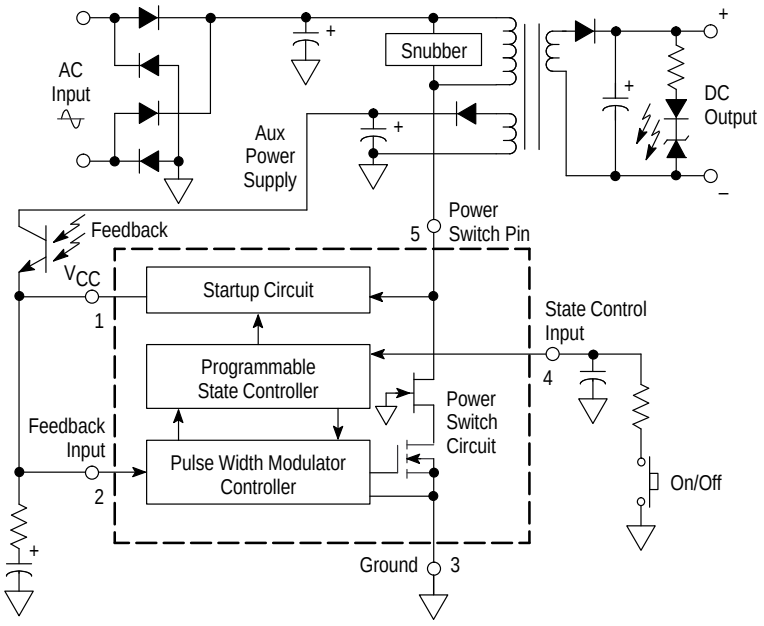
SEMICONDUCTOR TECHNICAL DATA

The MC33369 through MC33374 are monolithic high voltage power switching regulators that combine the required converter functions with a unique programmable state controller, allowing a simple and economical powersystem solution for office automation, consumer, and industrial products. These devices are designed to operate directly from a rectified AC line source, and in flyback converter applications are capable of providing an output power in excess of 150 W with a fixed AC input of 100 V, 115 V, or 230 V, and in excess of 90 W with a variable AC input that ranges from 85 V to 265 V.

This device series features a programmable state controller, an on–chip 700 V SENSEFET™ power switch circuit, 700 V active off–line startup circuit including a high voltage JFET and a low voltage MOSFET, auto restart logic, fixed frequency duty cycle controlled oscillator, current limiting comparator with leading edge blanking, latching pulse width modulator for double pulse suppression, and a high gain amplifier with a bandgap reference. Protective features include cycle–by–cycle current limiting, input undervoltage lockout with hysteresis, and a non–latching thermal shutdown. These devices are available in economical 8–pin dual–in–line and five pin TO–220 style packages.

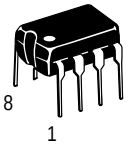
- Programmable State Controller
- On–Chip 700 V SENSEFET Power Switch Circuit
- Rectified AC Line Source Operation from 85 V to 265 V
- On–Chip 700 V Active Off–Line Start–Up Circuit
- Latching PWM for Double Pulse Suppression
- Cycle–By–Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Non–Latching Internal Thermal Shutdown
- Enhanced Functionality Over TOP200 and TOP221 Series

Typical Application



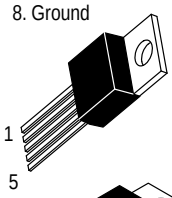
This device contains 391 active transistors.

P SUFFIX
PLASTIC PACKAGE
CASE 626

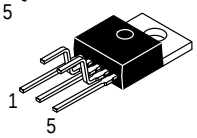


Pin 1. V_{CC}
2. Feedback Input
3. Ground
4. State Control Input
5. Power Switch Pin
6. Ground
7. Ground
8. Ground

T SUFFIX
PLASTIC PACKAGE
CASE 314D



TV SUFFIX
PLASTIC PACKAGE
CASE 314E



Pin 1. V_{CC}
2. Feedback Input
3. Ground
4. State Control Input
5. Power Switch Pin

Heatsink surface connected to Pin 3

ORDERING INFORMATION

Device	Power Switch Circuit		Package
	On Resistance (Ω)	Peak Current (A)	
MC33369P	12	0.5	Plastic DIP–8
MC33370P	12	0.9	
MC33371P	6.8	1.5	
MC33372P	4.8	2.0	
MC33373AP	4.0	2.5	
MC33369T	12	0.5	Straight Lead
MC33370T	12	0.9	
MC33371T	6.8	1.5	
MC33372T	4.8	2.0	
MC33373T	3.8	2.7	
MC33374T	3.0	3.3	
MC33369TV	12	0.5	Vertical Mount
MC33370TV	12	0.9	
MC33371TV	6.8	1.5	
MC33372TV	4.8	2.0	
MC33373TV	3.8	2.7	
MC33374TV	3.0	3.3	

Rev 3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Switch and Start–Up Circuit (Pin 5)			
Voltage Range Pin 5	V_5	–0.3 to 700	V
Current Peak During Transformer Saturation	$I_{5(pk)}$	2.0 I_{lim} Max	A
Power Supply Voltage Range (Pin 1)	V_{CC}	–0.3 to 10	V
Feedback Input (Pin 2)			
Voltage Range	$V_{IR(fb)}$	–0.3 to 10	V
Current	I_{fb}	100	mA
State Control Input Current (Pin 4)	I_{st}	50	mA
Thermal Characteristics			°C/W
P Suffix, Plastic Package Case 626			
Junction–to–Lead	$R_{\theta JC}$	5.0	
Junction–to–Air, 2.0 oz. printed circuit copper clad	$R_{\theta JA}$		
0.36 sq. inch		45	
1.0 sq. inch		35	
T and TV Suffix, Plastic Package Case 314			
Junction–to–Case		2.0	
Junction–to–Air		65	
Operating Junction Temperature	T_J	–40 to +150	°C
Storage Temperature	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (Pin 1 connected to Pin 2, for typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (I_{fb} = 4.0 mA)	f_{OSC}				kHz
T_J = 25°C		90	100	110	
T_J = T_{low} to T_{high}		70	–	115	
AMPLIFIER and PWM COMPARATOR (Pin 2)					
Feedback Input Shunt Regulation (I_{fb} = 4.0 mA, T_J = T_{low} to T_{high})					
Voltage	$V_{reg(fb)}$	8.3	8.6	8.9	V
Voltage Temperature Coefficient	$\Delta V_{reg(fb)}$	–	0.005	–	%/°C
Feedback Input (I_{fb} = 3.5 mA to 4.5 mA)					
Resistance (T_J = 25°C)	R_I	14	19	23	Ω
Resistance Temperature Coefficient (T_J = T_{low} to T_{high})	ΔR_I	–	0.3	–	%/°C
Feedback Input Current at Threshold of Duty Cycle Reduction	$I_{th(PWM)}$				mA
MC33369, MC33370		1.2	1.6	2.1	
MC33371		1.3	1.8	2.3	
MC33372		1.4	2.0	2.4	
MC33373A, MC33373		1.5	2.1	3.0	
MC33374		1.6	2.2	3.2	
Amplifier/PWM Gain (I_{fb} = 3.5 mA to 4.5 mA)					
Gain (T_J = 25°C)	A_V	–10	–14	–18	%/mA
Gain Temperature Coefficient (T_J = T_{low} to T_{high})	ΔA_V	–	–0.05	–	%/°C
PWM Duty Cycle					%
Maximum (I_{fb} = I_{CC1})	$D_{(max)}$	71	74	77	
Minimum (I_{fb} = 10 mA)	$D_{(min)}$	0.5	0.9	2.0	
SHUTDOWN LATCH					
External Shutdown Activation, Current into Pin 2 to Set Latch	I_{sd}	30	70	150	mA
Power–Up Reset Threshold, Pin 1 Voltage to Reset Latch	V_{rst}	2.5	3.7	5.0	V
STATE CONTROL (Pin 4)					
Input Open Circuit Voltage (I_{fb} = 4.0 mA)	$V_{oc(st)}$	3.2	3.55	3.8	V
Set Comparator (V_{CC} = $V_{reg(fb)}$)					
Threshold Voltage	$V_{th(st)}$	4.1	4.4	4.7	V
Input Clamp Voltage (I_{in} = 0.5 mA)	$V_{clmp(st)}$	5.0	5.5	6.5	V
Input Clamp Current (V_{in} = 8.6 V)	$I_{in(st)}$	–	1.0	–	mA
Toggle Comparator (V_{CC} = $V_{reg(fb)}$)					
Threshold Voltage (V_{in} Decreasing)	$V_{th(tg)}$	1.6	1.8	2.0	V
Hysteresis (V_{in} Increasing)	$V_{H(tg)}$	–	200	–	mV
Input Current (V_{in} = 0.2 V)	$I_{in(tog)}$	–	–40	–	µA
Input Reset Current (V_{CC} < V_{rst}, V_{st} = 1.1 V)	$I_{rst(st)}$	1.0	3.7	7.0	mA

ELECTRICAL CHARACTERISTICS (continued) (Pin 1 connected to Pin 2, for typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SWITCH CIRCUIT (Pin 5)					
On Resistance Pin 5 to Pin 3	$R_{5,3(on)}$				Ω
MC33369, MC33370 (I_5 = 50 mA)					
T_J = 25°C		–	12	13.5	
T_J = 125°C		–	21	30	
MC33371 (I_5 = 100 mA)					
T_J = 25°C		–	6.8	7.5	
T_J = 125°C		–	13	14.5	
MC33372 (I_5 = 150 mA)					
T_J = 25°C		–	4.8	5.5	
T_J = 125°C		–	8.0	9.0	
MC33373A (I_5 = 175 mA)					
T_J = 25°C		–	4.0	5.0	
T_J = 125°C		–	7.2	9.5	
MC33373 (I_5 = 200 mA)					
T_J = 25°C		–	3.8	4.5	
T_J = 125°C		–	6.8	8.5	
MC33374 (I_5 = 250 mA)					
T_J = 25°C		–	3.0	3.5	
T_J = 125°C		–	5.4	6.5	
Breakdown Voltage Pin 5 ($I_{5(off)}$ = 100 μA, T_A = 25°C)	$V_{(BR)5}$	700	–	–	V
Off–State Leakage Current Pin 5 (V_5 = 700 V)	$I_{5(off)}$				μA
T_J = 25°C		–	28	50	
T_J = 125°C		–	100	200	
Switching Characteristics (V_5 = 50 V, R_L set for I_5 = 0.7 I_{lim})					ns
Turn–on Time (90% to 10%)	t_{on}	–	10	–	
Turn–off Time (10% to 90%)	t_{off}	–	15	–	
CURRENT LIMIT AND THERMAL PROTECTION					
Current Limit Threshold (Note 4, T_J = 25°C)	I_{lim}				A
MC33369		0.44	0.5	0.56	
MC33370		0.8	0.9	1.0	
MC33371		1.3	1.5	1.7	
MC33372		1.8	2.0	2.2	
MC33373A		2.2	2.5	2.8	
MC33373		2.4	2.7	3.0	
MC33374		2.9	3.3	3.7	
Propagation Delay, Current Limit Threshold to Power Switch Circuit Output Pin 5 (Leading Edge Blanking plus Current Limit Delay)	t_{PLH}	–	280	–	ns
Thermal Protection (Note 1, 3)					°C
Shutdown (Junction Temperature Increasing)	t_{sd}	140	157	–	
Hysteresis (Junction Temperature Decreasing)	t_H	–	15	–	

ELECTRICAL CHARACTERISTICS (continued) (Pin 1 connected to Pin 2, for typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
STARTUP CONTROL (Pin 1)					
Undervoltage Lockout					V
Start–Up Threshold (V_{CC} Increasing)	$V_{CC(on)}$	8.2	8.5	8.8	
Minimum Operating Voltage After Turn–On	$V_{CC(min)}$	7.2	7.5	7.8	
Hysteresis	V_H	0.8	1.0	1.2	
Start–Up Circuit Pin 1 Output Current (Pin 5 = 50 V)	I_{start}				mA
V_{CC} = 0 V		1.2	2.0	2.5	
V_{CC} = 8.0 V		0.5	1.4	2.5	
Auto Restart ($C_{Pin\ 1}$ = 47 µF, Pin 5 = 50 V)					
Duty Cycle	D_{rst}	–	5.0	–	%
Frequency	f_{rst}	–	1.2	–	Hz
TOTAL DEVICE (Pin 1)					
Power Supply Current After UVLO Turn–On					mA
Power Switch Circuit Enabled	I_{CC1}				
MC33369, MC33370		0.5	1.2	1.7	
MC33371		0.65	1.4	1.8	
MC33372		0.8	1.5	1.9	
MC33373A, MC33373		0.95	1.7	2.1	
MC33374		1.1	1.8	2.2	
Power Switch Circuit Disabled	I_{CC2}	0.6	1.0	1.2	

NOTES: 1. Maximum Package power dissipation limits must be observed.
2. Tested junction temperature range for the MC33370 series:
T_{low} = –40°C T_{high} = +125°C
3.Guaranteed by design only.
4.Adjust di/dt to reach I_{lim} in 5.0 µs.

Figure 1. Oscillator Frequency Change versus Temperature

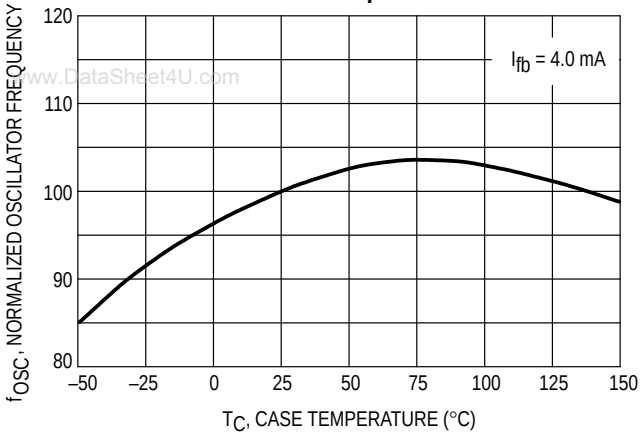


Figure 2. State Control Input Current versus Input Voltage

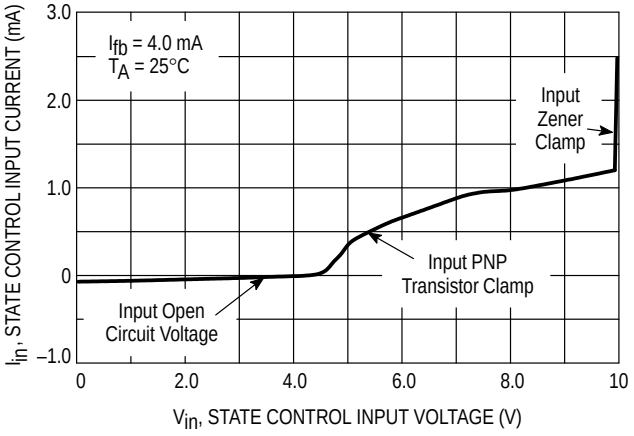


Figure 3. State Control Input Threshold Voltage versus Temperature

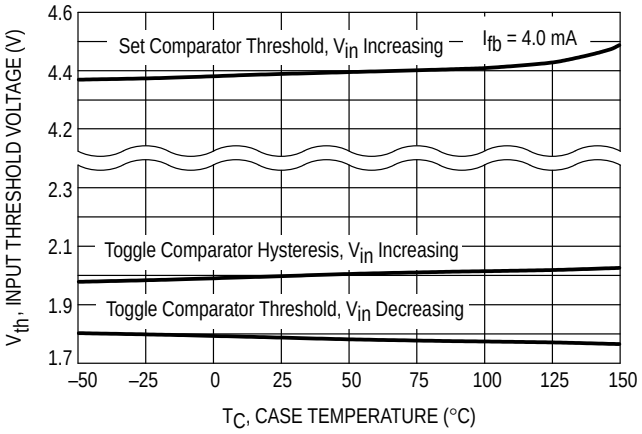


Figure 4. State Control Input Open Circuit and Clamp Voltages versus Temperature

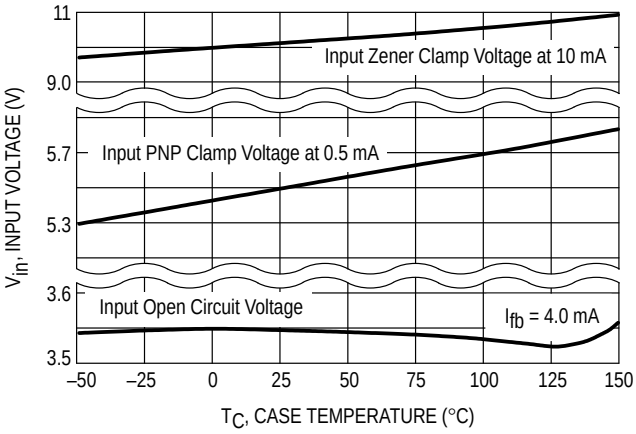


Figure 5. Power Switch Circuit Output Duty Cycle versus Feedback Input Current

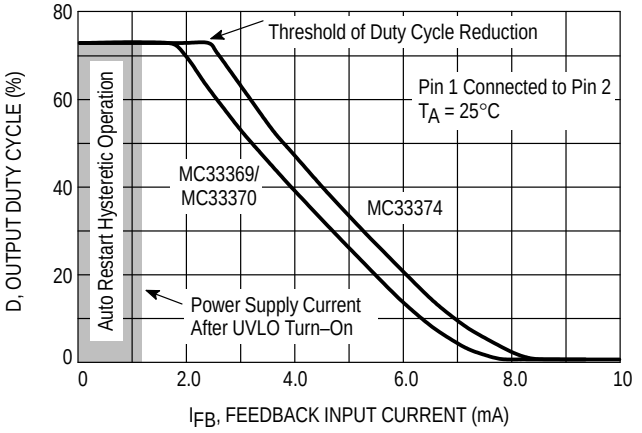


Figure 6. Feedback Input Current versus Input Voltage

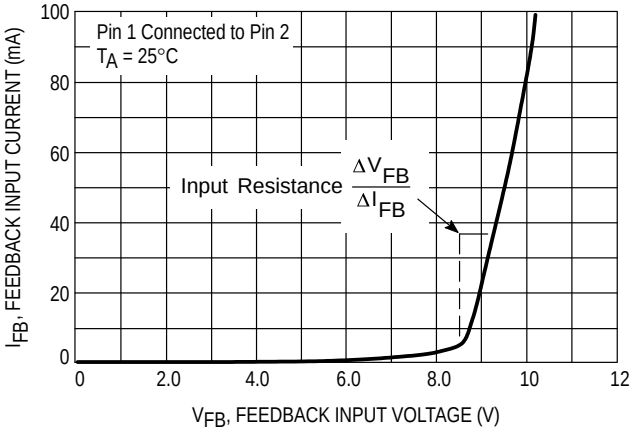


Figure 7. Feedback Input Shunt Regulation Voltage and Current versus Temperature

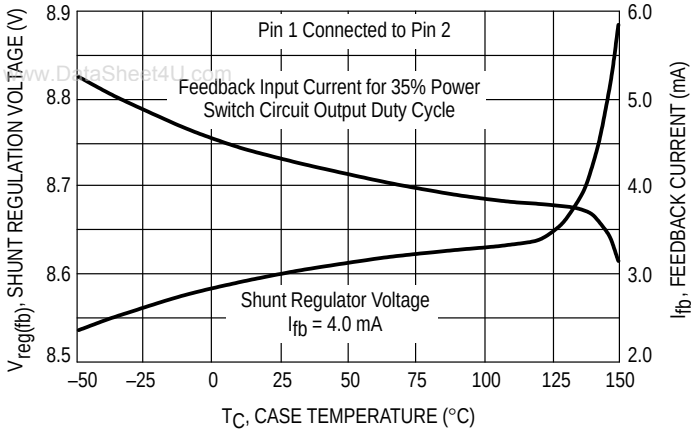


Figure 8. Undervoltage Lockout Thresholds versus Temperature

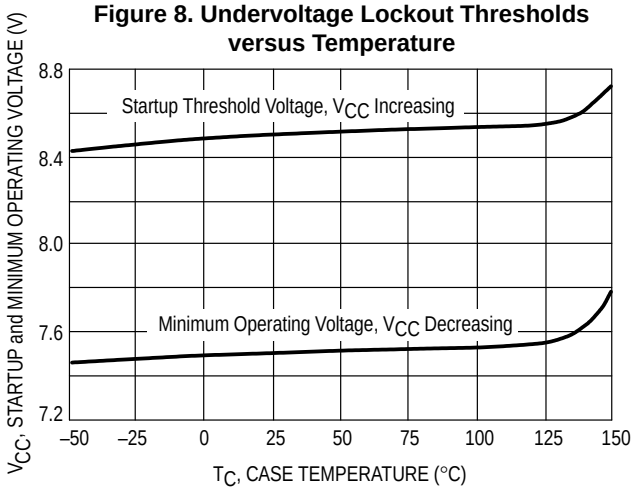


Figure 9. Start–Up Circuit Current versus Pin 5 Voltage

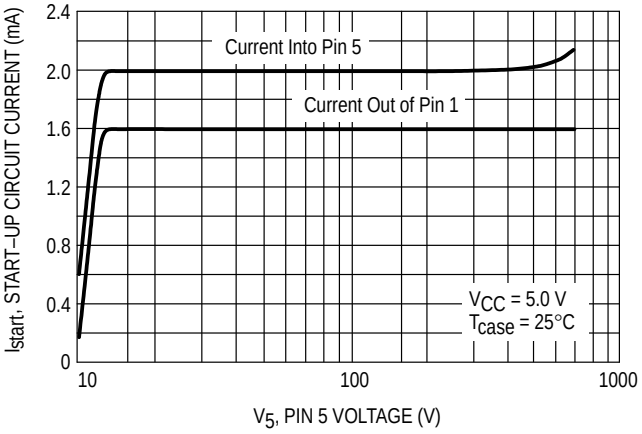


Figure 10. Start–Up Circuit Current versus Power Supply Voltage

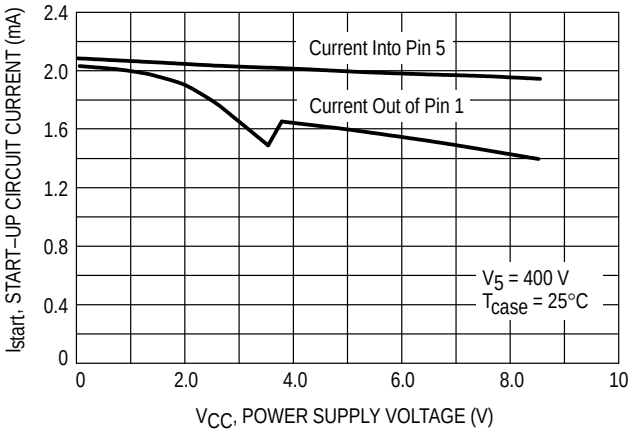


Figure 11. Power Switch Circuit Current Limit Threshold versus Temperature

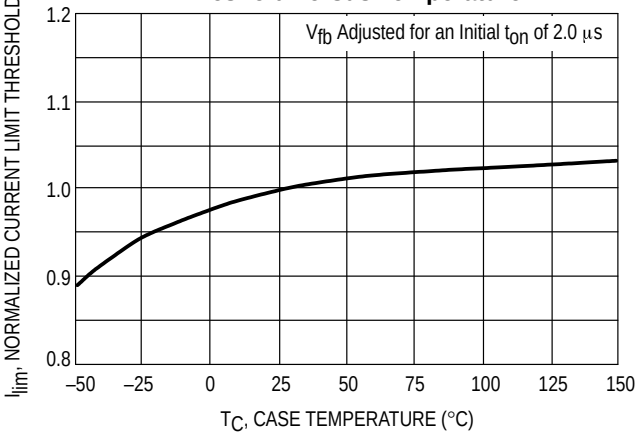


Figure 12. Power Switch Circuit Peak Current versus Current Rate of Change

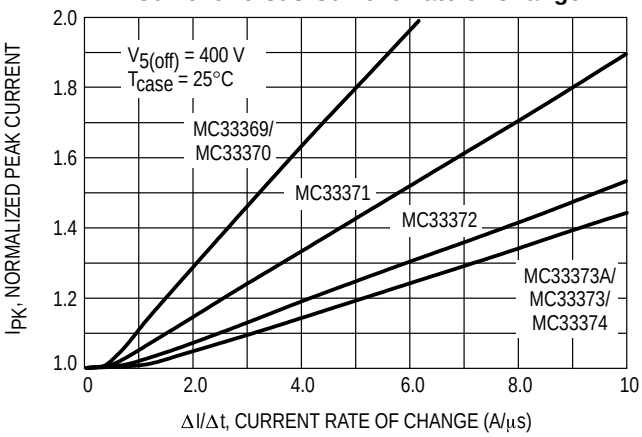


Figure 13. Power Switch Circuit Current versus Pin 5 Voltage

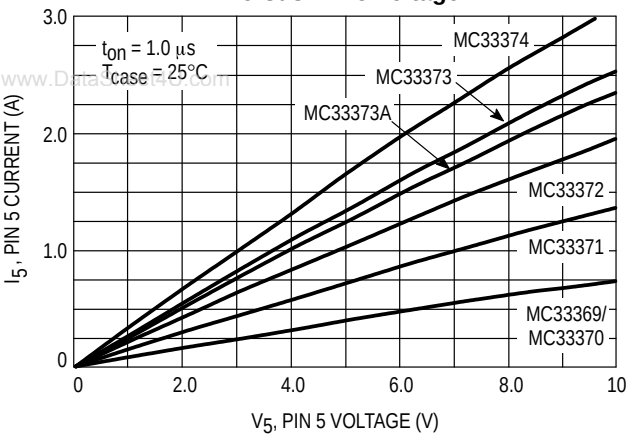


Figure 14. Normalized Power Switch Circuit On–Resistance Pin 5 to Pin 3 versus Temperature

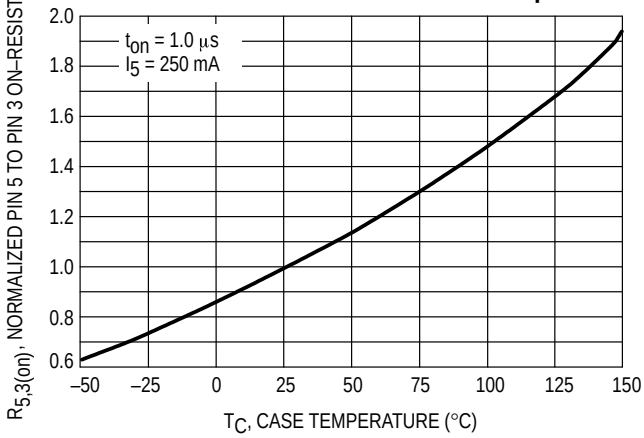


Figure 15. Power Switch Circuit Off–State Current versus Voltage

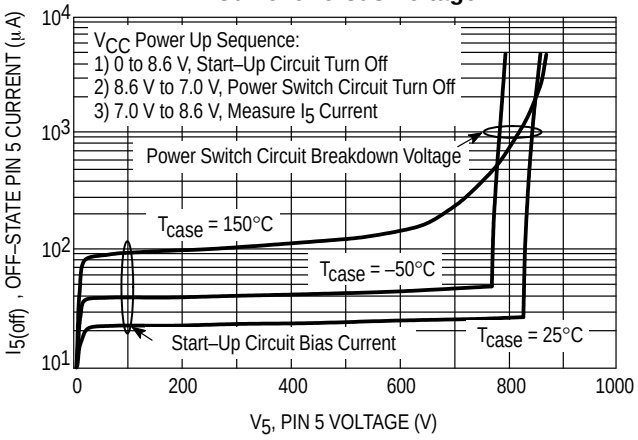


Figure 16. Power Switch Circuit Capacitance versus Pin 5 Voltage

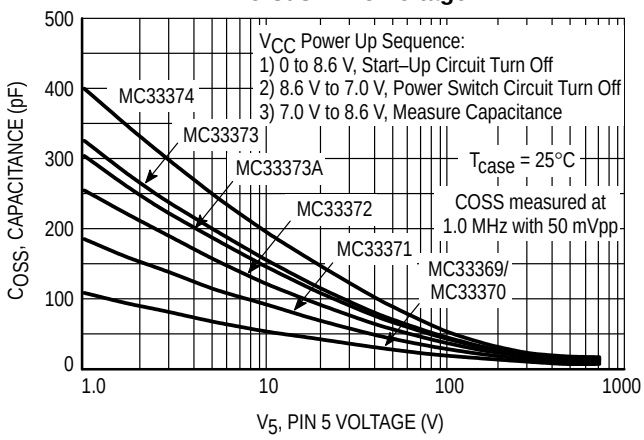


Figure 17. Pin Function Description

Pin	Function	Description
1	V_{CC}	This is the positive supply voltage input. During startup, power is supplied to this input from Pin 5. When V_{CC} reaches the UVLO upper threshold, the Start–Up circuit turns off and power is supplied from an auxiliary transformer winding.
2	Feedback Input	This is the Shunt Regulator/Amplifier input and is used to duty cycle control the Power Switch circuit. It has an 8.6 V threshold and normally connects to the converter output, or to a voltage that represents the converter output.
3	Ground	This pin is the control circuit and Power Switch circuit ground. It is part of the integrated circuit lead frame and is electrically common to the metal heatsink tab.
4	State Control Input	This is a multifunction input that is designed to interface with a small number of external components to implement various methods of converter on/off control.
5	Power Switch Pin	This pin is designed to directly drive the converter transformer primary, and internally connects to the Power Switch circuit and Start–Up circuit.

Figure 18. Representative Block Diagram

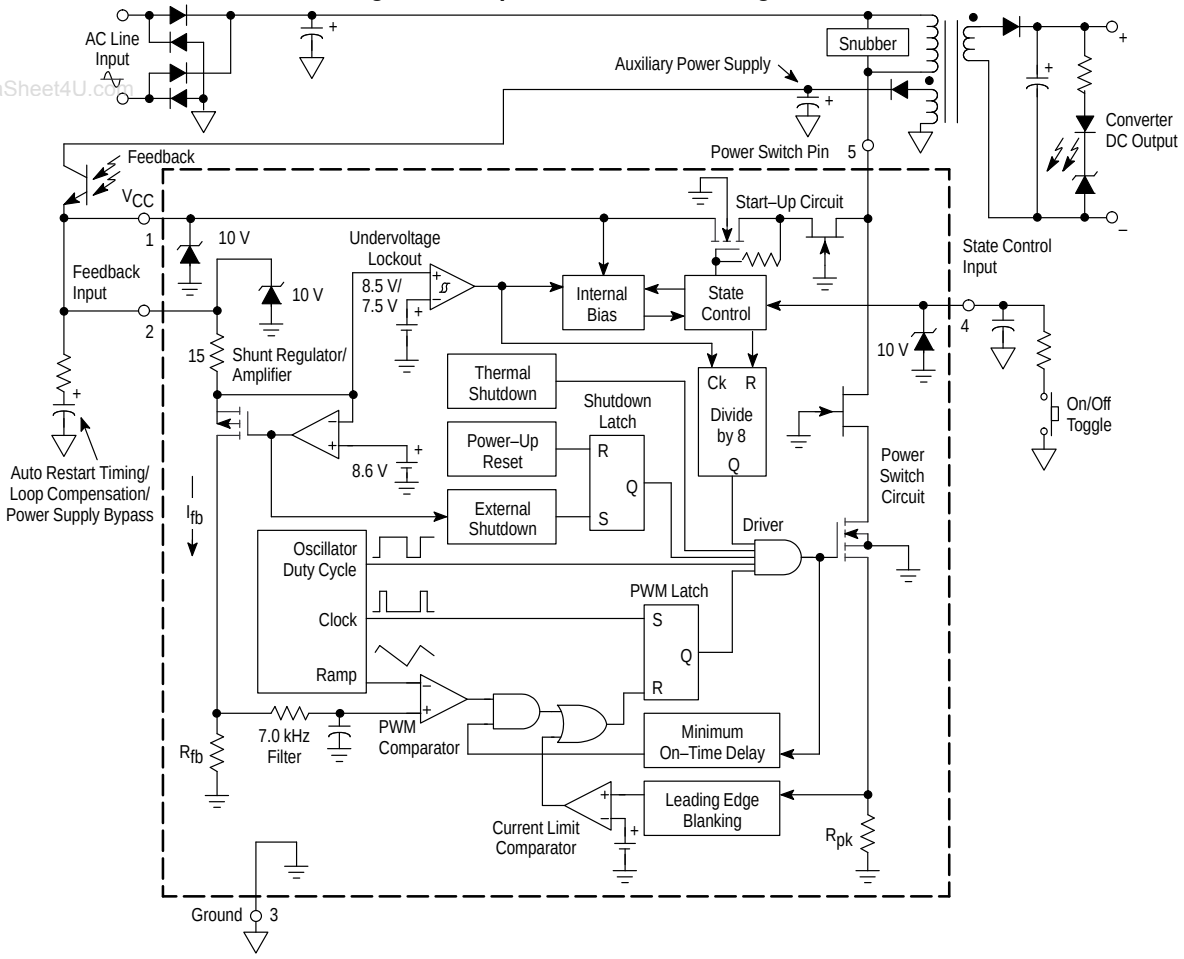
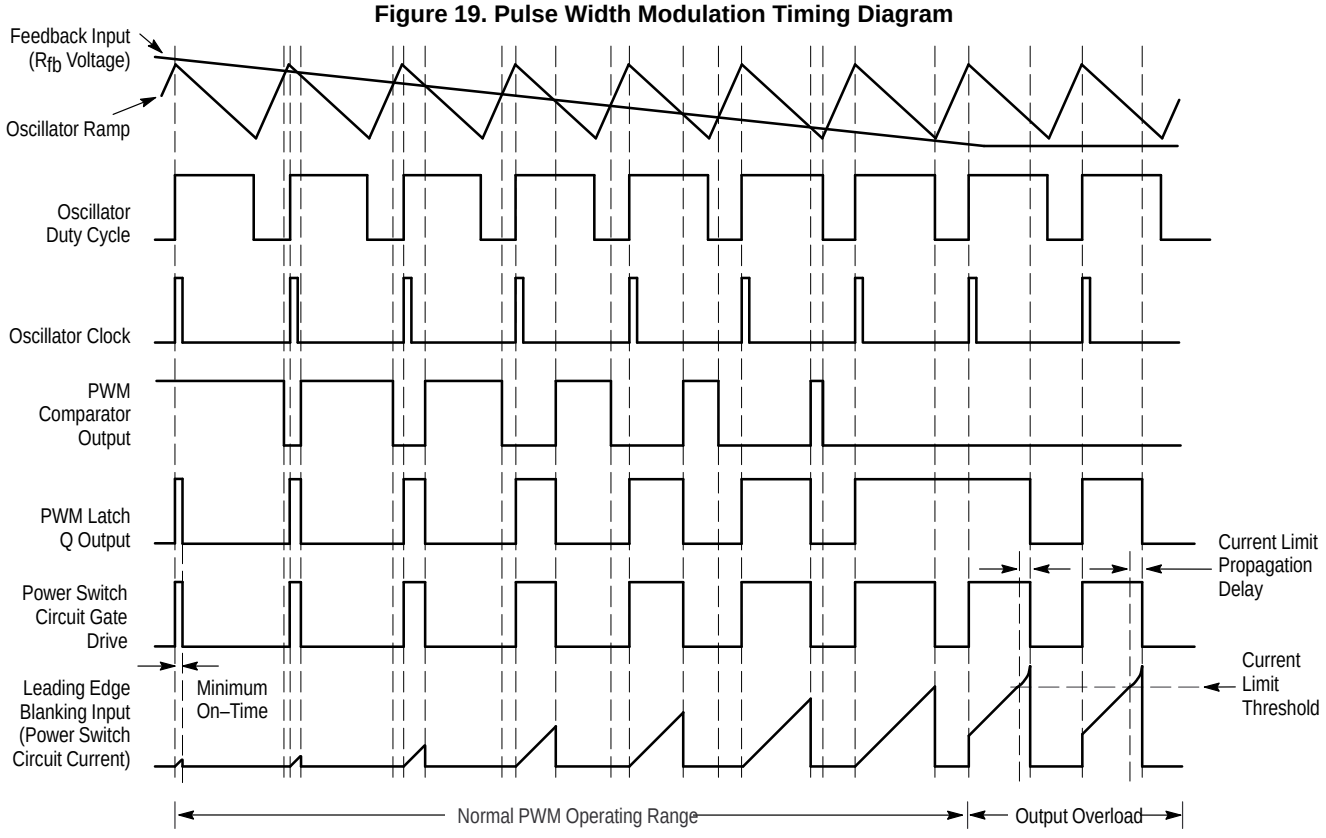


Figure 19. Pulse Width Modulation Timing Diagram



OPERATING DESCRIPTION

Introduction

The MC33369 thru MC33374 represent a new higher level of integration by providing on a single monolithic chip all of the active power, control, logic, and protection circuitry required to implement a high voltage flyback, forward, boost, or buck converter. This device series is designed for direct operation from a rectified 240 VAC line source and requires minimal external components for a complete cost sensitive converter solution. Potential markets include office automation, industrial, residential, personal computer, and consumer. A description of each of the functional blocks is given below, and the representative block diagram is shown in Figure 18.

Oscillator

The Oscillator block consists of two comparators that alternately gate on and off a trimmed current source and current sink which are used to respectively charge and discharge an on–chip timing capacitor between two voltage levels. This configuration generates a precise linear sawtooth ramp signal that is used to pulse width modulate the MOSFET of the Power Switch circuit. During the charge of the timing capacitor, the Oscillator duty cycle output holds one input of the Driver low. This action keeps the MOSFET of the Power Switch circuit off, thus limiting the maximum duty cycle. The Oscillator frequency is internally programmed for 100 kHz operation with a controlled charge to discharge current ratio that yields a maximum PWM duty cycle of 74%. The Oscillator temperature characteristics are shown in Figure 1.

PWM Comparator and Latch

The pulse width modulator (PWM) consists of a comparator with the Oscillator ramp output applied to the inverting input, while the Amplifier output is applied into the noninverting input. The Oscillator clock output applies a set pulse to the PWM Latch when the timing capacitor reaches its peak voltage, initiating Power Switch circuit conduction. As the timing capacitor discharges, the ramp voltage decreases to a level that is less than the Amplifier output, causing the PWM Comparator to reset the latch and terminate Power Switch circuit conduction for the duration of the ramp–down period. This method of having the Oscillator set and the PWM Comparator reset the Latch prevents the possibility of multiple output pulses during a given Oscillator clock cycle. This circuit configuration is commonly referred to as double pulse suppression logic. A timing diagram is shown in Figure 19 that illustrates the behavior of the pulse width modulator.

Shunt Regulator/Amplifier

Feedback Input, Pin 2, connects to the internal Shunt Regulator/Amplifier. This input is used as a means to close the feedback loop for converter output regulation. The internal circuitry consists of an Amplifier with a precise threshold that drives a MOSFET in a manner that forms an active Shunt Regulator. The initial current that flows into Pin 1 is used to bias the internal circuitry. Any additional current is in excess flows into Pin 2, and is shunted through resistor R_{fb} to ground. The voltage developed across R_{fb} is used to adjust the PWM Comparator threshold, which in turn controls the PWM duty cycle. The duty cycle is inversely proportional to the input current level that in excess of about 2 mA, and is reduced at a rate of about –14% per mA, refer to Figure 5. A 7.0 kHz low pass filter is placed between R_{fb} and the PWM input. This filter attenuates any switching noise that may be present and reduces the possibility of output pulse width jitter.

The Amplifier gain is set by the dynamic impedance of the feedback input and is nominally centered at 18 Ω. The dynamic impedance of this pin combined with the external resistive and capacitive components determines the control loop characteristics of the converter. The feedback input has a temperature compensated threshold of 8.6 V and is used as a voltage reference in non–isolated output applications. The input dynamic resistance is shown in Figure 6.

External Shutdown and Latch

A latching shutdown feature has been incorporated into this device series to eliminate the possibility of converter runaway output voltage during a sudden load removal. The External Shutdown block sets the Shutdown Latch when the feedback input current exceeds 60 mA. When set, the Latch holds the MOSFET of the Power Switch circuit off, and the Start–Up circuit hysteretically regulates the V_{CC} Pin 1 voltage between 8.5 V to 7.5 V. In order to resume the switching operation, the Shutdown Latch must be reset by the Power–Up Reset block. This can be accomplished directly by momentarily pulling the V_{CC} Pin 1 below the 3.7 V Power–Up Reset threshold, or indirectly by removing, waiting, and then restoring power to the converter input. The Power–Up Reset block automatically resets the Shutdown Latch each time power is applied to the device.

Current Limit Comparator and Power Switch Circuit

This device series uses cycle–by–cycle current limiting as a means of protecting the output switch circuit from overstress. Each on–cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch circuit current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch circuit for the duration of the oscillator ramp–down period.

The Power Switch circuit is constructed as a SENSEFET circuit with a high voltage JFET in series with a low voltage MOSFET. The drain of the high voltage JFET is connected to Pin 5. The gate of the JFET is grounded. The source of the JFET is connected to the drain of the low voltage MOSFET. The MOSFET has two sources of different size with a known ratio of about 1:100. One source of the MOSFET is connected to Pin 3 and provides the main current conduction path between Pin 5 and Pin 3. The second source of the MOSFET is used for current sensing by conducting a small percentage of the current between Pin 5 and Pin 3 through a ground referenced sense resistor, R_{PK}. The voltage across sense resistor R_{PK} represents the current from Pin 5 to Pin 3 divided by the known ratio of the MOSFET sources. The SENSEFET circuit allows a virtually lossless method of monitoring the current from Pin 5 to Pin 3. The current limit comparator detects if the voltage across R_{pk} exceeds the reference level that is present at the noninverting input. If exceeded, the comparator quickly resets the PWM Latch, thus protecting the Power Switch circuit. Figure 11 shows that this detection method yields a relatively constant current limit threshold over temperature. The high voltage Power Switch circuit is integrated with the control logic circuitry and is designed to directly drive the converter transformer. The Power Switch circuit is capable of switching 700 V with an associated current from Pin 5 to Pin 3 that ranges from 0.9 A to 3.3 A. Proper voltage snubbing on Pin 5 during converter startup and overload is mandatory for reliable device operation.

A Leading Edge Blanking circuit was placed in the current sensing signal path to prevent a premature reset of the PWM Latch. A potential premature reset signal is generated each time

the Power Switch circuit is driven into conduction and appears as a narrow voltage spike across the current sense resistor R_{pk}. The spike is due to the low voltage MOSFET gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. The Leading Edge Blanking circuit has a dynamic behavior that masks the current signal until the Power Switch circuit turn–on transition is completed. The current limit propagation delay time is typically 280 ns. This time is measured from when an overcurrent appears in the Power Switch circuit, to the beginning of turn–off. Care must be taken during transformer saturation so that the maximum device current limit rating is not exceeded.

Figure 20. Startup and Normal Operation Timing Diagram

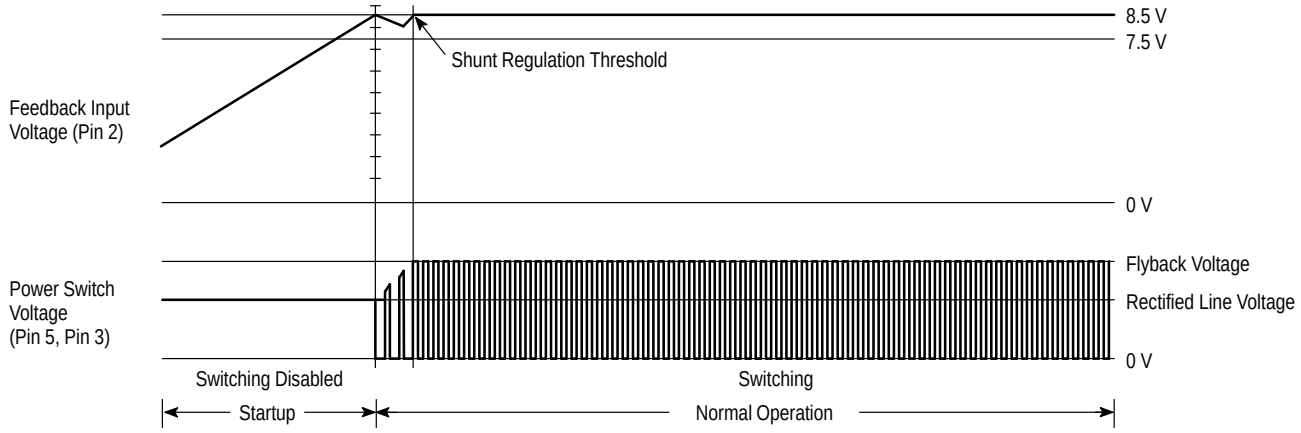
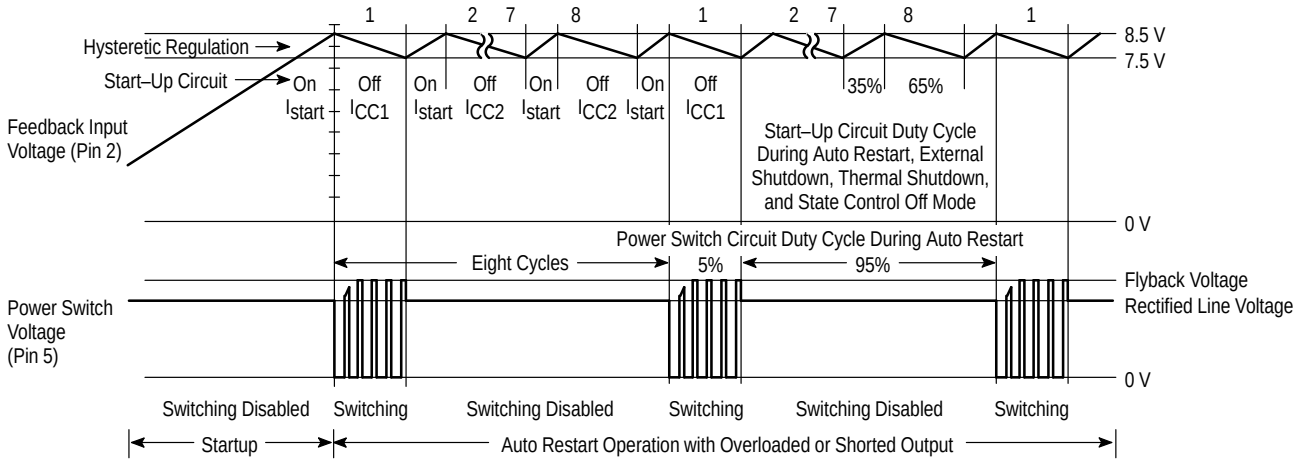


Figure 21. Auto Restart Operation Timing Diagram



Start–Up Circuit

Contained within the MC33369 thru MC33374 is a Start–Up circuit that is governed by the State Control block. The Start–Up circuit includes a high voltage JFET and a low voltage MOSFET. The drain of the high voltage JFET is connected to Pin 5. The gate of the JFET is grounded. The source of the high voltage JFET is connected to the drain of the low voltage MOSFET. The JFET pinches off and clamps the voltage on the drain of the MOSFET to a low voltage between 18–24 volts. A resistance of 550K ohms is connected between the drain and gate of the low voltage MOSFET. The low voltage on the drain and gate of the MOSFET simplifies construction of the Start–Up circuit. This circuitry yields an increase in converter efficiency by the elimination of an external startup resistor and its associated power dissipation that is common in most of the off–line converters that utilize a UC3842 type of controller.

Rectified AC line voltage is applied to the Start–Up circuit from Pin 5. This enables the Start–Up circuit to provide charge current to the V_{CC} bypass capacitor that connects from Pin 1 to ground. When V_{CC} reaches the UVLO upper threshold of 8.5 V, the Start–Up circuit is turned off to complete the startup phase. The IC then commences normal operation. As the converter output approaches regulation, the auxiliary transformer winding begins to provide operating bias. All of the required device power is now efficiently converted down directly from the rectified AC line. The Start–Up circuit will provide an initial charging current of 2.0 mA when powered from 400 V. This current will decrease as the V_{CC} pin voltage rises or if the device is powered from a lower input voltage, refer to Figures 9 and 10. The Start–Up circuit is rated at a maximum of 700 V with the V_{CC} pin shorted to ground.

Undervoltage Lockout

An Undervoltage Lockout comparator is included to guarantee that the integrated circuit has sufficient voltage to be fully functional before the output stage is enabled. The UVLO comparator monitors the feedback input voltage at Pin 2 and when it exceeds the startup threshold of 8.5 V, the Start–Up circuit turns off, the Internal Bias block is switched on, and the Power Switch circuit is enabled. To prevent erratic switching as the threshold is crossed, 1.0 V of hysteresis is provided. This level of hysteresis ensures that there is sufficient energy stored in the V_{CC} bypass capacitor to power the bias circuitry until auxiliary power supply takes over. If the converter output is nominally loaded, regulation will be established and the opto–isolator will provide sufficient current into the feedback input to keep the V_{CC} bypass capacitor charged. Figure 20 shows the timing waveforms during startup and normal operation.

If the converter output is overloaded or shorted, the device will enter into the auto restart mode. This happens when the opto–isolator is not able to provide sufficient current into the feedback input to keep the V_{CC} bypass capacitor charged. When the capacitor voltage falls below the minimum operating threshold of 7.5 V, the UVLO comparator switches the Internal Bias block off, and disables the Power Switch circuit. The Start–Up circuit is turned on and the V_{CC} bypass capacitor begins charging. When the UVLO startup threshold is reached, the Start–Up circuit again turns off, the Internal Bias block is switched on, and the Divide by 8 counter is clocked. Since the Power Switch circuit is now disabled by the Divide by 8 counter, the opto–isolator will not provide current to the V_{CC} bypass capacitor, the capacitor will discharge. The UVLO comparator and Start–Up circuit will regulate the capacitor voltage in a hysteretic mode, varying between 7.5 V to 8.5 V, with an effective ramp–up duty cycle of approximately 35%. The Divide by 8 counter will enable the Power Switch circuit to burst at the 100 kHz Oscillator frequency on every eighth ramp–down cycle. The device will remain in the auto restart mode until the output overload or short is removed and the threshold of regulation can again be reached. The purpose of the Divide by 8 counter is to reduce the Power Switch circuit and output rectifier power dissipation when the converter is subjected to an output overload or short. The counter effectively limits the average switching duty cycle to approximately 5%. Figure 21 shows the timing waveforms when in auto restart mode.

Thermal Shutdown and Package

The internal Thermal Shutdown block protects the device in the event that the maximum junction temperature is exceeded. When activated, typically at 157°C, one input of the Driver is held low to disable the Power Switch circuit. When disabled, the UVLO comparator and Start–Up circuit regulate the V_{CC} pin voltage in the hysteretic mode. Thermal shutdown activation is non–latching and the Power Switch circuit is allowed to resume operation when the junction temperature falls below 140°C. The thermal shutdown feature is provided to prevent catastrophic device failures from accidental overheating. It is not intended to be used as a substitute for proper heatsinking.

The die in the 8–pin dual–in–line package is mounted on a special heat tab copper alloy lead frame. The tab consists of pins 3, 6, 7, 8 is specifically designed to improve the thermal conduction from the die to the printed circuit board. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance.

The die in the 5 pin TO–220 style package is mounted directly on a copper alloy heat tab. This metal tab is exposed on the back side of the package for heatsink attachment and is electrically common to the device ground, Pin 3. A wide variety of TO–220 style heatsinks are commercially available for enhancing the thermal performance and converter output power capability.

State Control

The State Control block is designed to interface with a small number of external components to implement various methods of converter on/off control. By utilizing the distinctive features of the State Control Input, this device series can be programmed to enter into either the standby* or operating mode in response to an appropriate input stimulus. This stimulus can come from a user interface pushbutton switch, an optically coupled microcontroller output signal, a combination of both, or other circuit configurations. The State Control Logic can be disabled and made to appear transparent when converter on/off control is not required. Figures 22 and 23 respectively show the State Control operating table, and the Control Block along with seven input examples.

The State Control block consists of a resistor bias network, Toggle and Set Comparators for threshold detection, an Input Clamp to provide drive for an opto light emitting diode, control logic elements for storing the operating state, and a Reset MOSFET for discharging an

external capacitor. The State Control Input is internally biased at 3.55 V when the V_{CC} input is regulated at 8.6 V. This internal bias can be overridden and driven either low or high by an external signal in order to trip one of the comparators. The Toggle and Set Comparator thresholds are respectively at 1.8 V and 4.4 V. The comparator outputs are processed and stored by the State Control Logic block which in turn controls the Start–Up circuit, Internal Bias block, and the Divide by 8 reset.

Circuit A shows an input configuration for manual toggle operation. A toggle request is made each time the pushbutton switch is pressed and released. When the Toggle Comparator detects a request, its output clocks the State Control Logic, resulting in a converter mode change. Successive toggle requests causes the converter to alternate between the standby* and operating modes. When in standby* mode, the UVLO comparator and Start–Up circuit regulate the V_{CC} pin voltage in the hysteretic mode, and there is not any voltage present at the converter output.

Circuit B configures the input to interface with a microcontroller for graceful shutdown operation. Graceful shutdown is an advanced form of power management where the microcontroller has the overriding responsibility for determining if and when the converter enters into the standby* mode. This is usually programmed to occur after the microcontroller completes a set of housekeeping routines.

A toggle request is made each time the pushbutton switch is pressed and released. When the Set Comparator detects a request, its output sets the State Control Logic, causing the converter to enter the operating mode. If the converter was initially operating, no mode change takes place. Note that each toggle request is conveyed to the microcontroller via Opto A. A current path for biasing the light emitting diode is provided by the series resistor and the internal 5.5 V Input Clamp. The microcontroller receives and processes the toggle request and upon completion of a maintenance routine, it sends a toggle confirm signal back to the State Control input via Opto B. This signal is detected by the Toggle Comparator and the converter enters into the standby* mode. With this circuit configuration, the user only has control of the standby* to operating mode transition. The user can request the operating to standby* mode transition, but the microcontroller has total control on executing the request.

Circuit C configures the input for brownout protection. The cathode of the zener diode connects to the rectified and filtered AC line voltage that appears at the positive terminal of bulk capacitor C1. With appropriate zener diode and resistor values, the State Control Input voltage can be set to fall below 1.8 V during a brownout condition. This results in a toggle request that causes the converter to incisively change from operating to standby* mode without any converter output voltage bounce. When the AC line voltage returns back to nominal, the voltage at the State Control Input rises, causing the Set Comparator to change the converter mode from standby* to operating. Note that when the converter is in standby*, the Set Comparator threshold will be lower than specified, and is approximately 3.84 V. This is because V_{CC} is regulated in the hysteretic mode between 7.5 V to 8.5 V.

Circuit D shows a method of accomplishing digital on/off control of the converter. Pull–up resistor R serves to bias the Set Comparator for turn–on, while the NPN transistor biases the Toggle Comparator for turn–off. An economical optocoupler can be used if galvanic isolation of the signal source is required.

Capacitor C_{st} shown in each of the examples provides an important programming function. A small value capacitor ($\leq$0.05 μF) serves to filter noise that may be coupled into the state control pin, thereby preventing false triggering of the comparators. A relatively large value capacitor ($\geq$2.0 μF) will delay the initial rise of the state control voltage during startup. This action results in the converter powering up in standby* rather than the operating mode.

Circuit E configures the State Control Input to provide a power–up time delay of the converter. Upon the initial application of AC power, the large value of capacitor C_{st} causes the Toggle Comparator to place the converter in standby*. When pull–up resistor R charges C_{st} to the Set Comparator threshold, the converter changes to the operating mode. A graph of power–up time delay versus resistance for three values of C_{st} is shown.

The circuits shown in the example in Circuit F on page 13 exemplifies two possible methods of disabling the State Control block on/off capability, thus rendering it transparent. This feature is useful in applications where converter on/off control is not desired. When nominal AC line voltage is applied to the converter input, the resistor circuit will cause the Set Comparator to place the converter in the operating mode. The resistor value is not critical, but it should be at least 5.0 k to insure proper device start–up. The converter will also assume the operating mode if the State Control Input is left open or unconnected. Due to the relatively high input impedance, this input may be susceptible to noise pickup. A small bypass capacitor in the range of 1.0 nF to 50 nF is recommended for C_{st}. The converter will assume the operation mode with either of these circuits.

Applications

The TO220 devices have a single Ground, Pin 3, that serves as both a sense point for the Shunt Regulator/Amplifier and the high current return path for the power switch circuit. **Do not attempt to construct a converter circuit on a wire–wrap or plug–in prototype board**. In order to ensure proper device operation and stability, it is important to minimize the lead length and the associated inductance of the ground pin. This pin must connect as directly as possible to the printed circuit ground plane and should not be bent or offset by the board layout. The Power Switch Pin 5 can be offset using a TV suffix product if additional layout creepage distance is required. Due to the potentially high rate of change in switch circuit current, components R3 and C5 must be connected to IC1 through separate and short copper traces. This will significantly reduce the level of switching noise that can be imposed upon the feedback control signal.

Figures 24 through 27 show a universal input 52 watt 90 watt converter with the associated test data. The converters were constructed and tested using the printed circuit board layout shown in Figure 28. The board consists of a fiber glass epoxy material (FR4) with a single side of two ounce per square foot copper foil. It is designed as a general purpose single output laboratory test vehicle and therefore does not contain an input electromagnetic interference (EMI) filter.

The board layout is capable of encompassing the wide range of output power available from the TO220TV package devices by providing a means to accept several component

sizes and styles. Note that there are multiple positions for output filter capacitors C8 and C11, allowing up to four capacitors in parallel. The various positions for transformer T1 will accomodate four core/bobbin sizes, consisting of E19/8/5 (E187), E22, E25/10/6 (E250), and E28. Unused pins must be removed from the bobbin. A choice of four TO220 style heatsinks can be used for integrated circuit IC1 and output rectfier D7. They are available from several manufacturers including Aavid Engineering. The table shown below lists the Aavid part numbers along with the associated thermal characteristics. The extruded heatsink must be drilled and tapped to allow attachment of the device and the printed circuit board.

Aavid Part Number	Heatsink	
	Style	Thermal Resistance (°C/W)
592502B03400	Stamped	24 at 2.0 W
593002B03400	Stamped	14 at 4.0 W
593202B03500	Stamped	10.4 at 5.0 W
590302B03600	Stamped	9.2 at 5.0 W
604953B02500	Extruded	6.0 at 15 W

The maximum output power that can be obtained from a given converter design is limited by the maximum operating junction temperature and current limit threshold of the device selected. The table below provides a general guide for device selection assuming the following conditions:

Discontinuous mode flyback operation
Wide range input operation from 92 VAC to 276 VAC
Bulk capacitor C1 ripple voltage ≤ 25 Vpp at 92 VAC input
Converter efficiency of 75%
Ambient temperature of 25°C
Adequate heatsinking for a junction temperature ≤ 150°C

Device	Converter Output Power (W)
MC33369P	12
MC33370P	20
MC33371P	30
MC33372P	35
MC33373AP	40
MC33369T/TV	12
MC33370T/TV	25
MC33371T/TV	45
MC33372T/TV	60
MC33373T/TV	75
MC33374T/TV	90

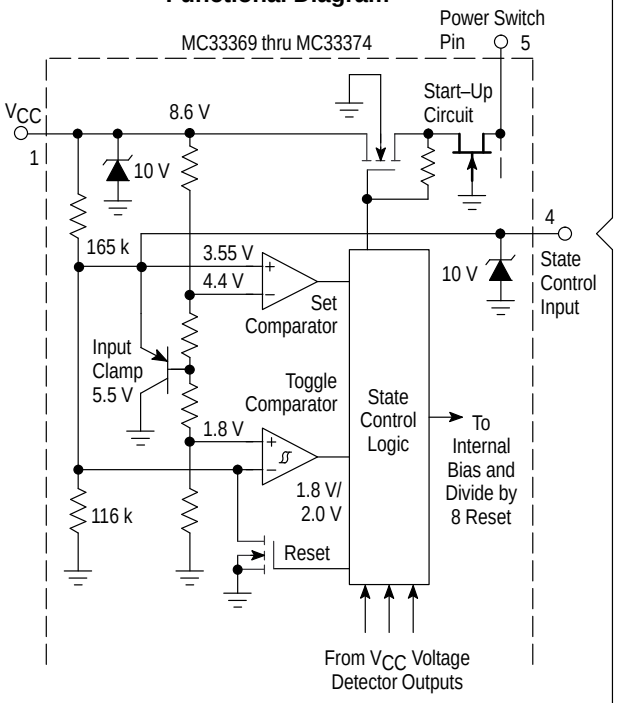
Figure 22. State Control Operating Table
(Circuits A through D of Figure 23)

Initial State				Subsequent State	
AC Line Voltage	Converter Mode	Input (Pin 4)		Converter Mode	Description
		Capacitor	Stimuli		
TOGGLE OPERATION (Circuit A)					
Nominal	Standby	Don't Care	Pulsed Low ≤ 1.8 V	Operating	The converter changes from standby to operating mode by the Toggle Comparator.
Nominal	Operating	Don't Care	Pulsed Low ≤ 1.8 V	Standby	The converter changes from operating to standby* mode by the Toggle Comparator.
MICROCONTROLLER GRACEFUL SHUTDOWN (Circuit B)					
Nominal	Standby	Don't Care	Pulsed High ≥ 4.4 V	Operating	Converter mode toggle requested. The Set Comparator changes the converter mode from standby to operating.
Nominal	Operating	Don't Care	Pulsed High ≥ 4.4 V	Operating	Converter mode toggle requested. No mode change takes place since the converter was initially operating. The change request is communicated to the MCU via Opto A.
Nominal	Operating	Don't Care	Pulsed Low ≤ 1.8 V	Standby	Converter mode toggle is confirmed by the MCU via Opto B. The converter mode changes from operating to standby.
BROWNOUT PROTECTION (Circuit C)					
Nominal to Brownout	Operating	Don't Care	Biased Low ≤ 1.8 V	Standby	The AC line voltage level changes from nominal to brownout and zener diode breakdown ceases. The lower divider resistor biases the Toggle Comparator input low, changing the converter mode from operating to standby.
Brownout to Nominal	Standby	Cst ≤ 0.05 μF	Biased High ≥ 3.85 V	Operating	The AC line voltage level changes from brownout to nominal and zener diode commences breakdown. This biases the Set Comparator input high, changing the converter mode from standby to operating.
DIGITAL ON/OFF CONTROL (Circuit D)					
Nominal	Standby	Don't Care	Biased High ≥ 4.4 V	Operating	The transistor is off and the collector resistor biases the Set Comparator input high, placing the converter in the operating mode.
Nominal	Operating	Don't Care	Biased Low ≤ 1.8 V	Standby	The transistor is on and the collector biases the Toggle Comparator input low, placing the converter in the standby mode.
DELAYED POWER–UP (Circuit E)					
Zero to Nominal	Off	Cst ≥ 2.0 μF	Pulsed Low by Cst ≤ 1.8 V Set High ≥ 4.4 V	Off Delay Operating	Discharged capacitor Cst causes the Toggle Comparator to change the control logic state. The converter is placed in the standby mode with the power switch circuit disabled. When Cst charges above 4.4 V, the Set Comparator changes the converter mode from standby to operating.
POWER–UP (Circuits A, and B)					
Zero to Nominal	Off	Cst ≤ 0.05 μF	None	Operating	Application of AC line power causes converter operation. The State Control Input is presently configured to be transparent and the control logic has no effect during power–up.
Zero to Nominal	Off	Cst ≥ 2.0 μF	Pulsed Low by Cst ≤ 1.8 V	Standby	Discharged capacitor Cst causes the Toggle Comparator to change the control logic state. The converter is placed in the standby mode with the power switch circuit disabled.

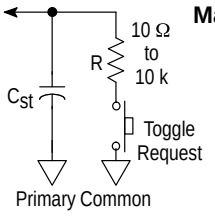
NOTE: When the converter is in the standby mode, there is not any voltage present at the output.

Figure 23. State Control Block with Input Control Examples

Internal State Control Block Functional Diagram

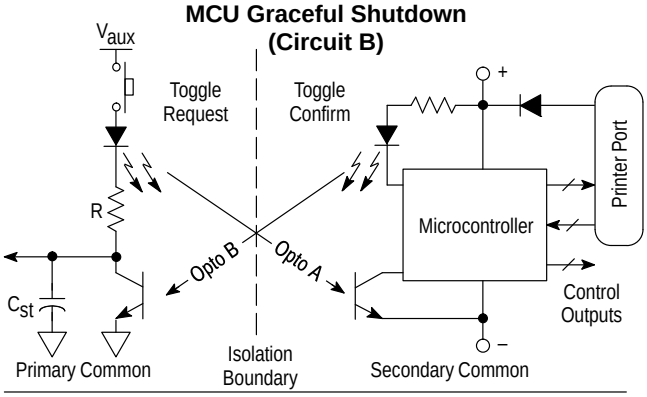


Manual Toggle Operation (Circuit A)

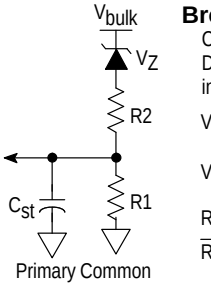


Resistor R is required for proper toggle functionality when operating the device at an elevated temperature with long leads to the pushbutton switch.

MCU Graceful Shutdown (Circuit B)



Brownout Protection (Circuit C)



Choose $VAC_{(on\ to\ off)}$ and $VAC_{(off\ to\ on)}$ thresholds. Determine converter output power P_O, efficiency η, and input bulk capacitance C_{blk}.

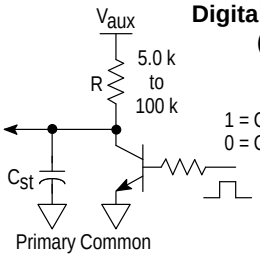
$$V_{blk(max)} \approx VAC_{(off\ to\ on)} \sqrt{2} - 1.4$$

$$V_Z = 1.88\ V_{blk(min)} - 0.88\ V_{blk(max)}$$

$$\frac{R_2}{R_1} = \frac{V_{blk(max)} - V_Z}{3.84} \text{ or } \frac{V_{blk(min)} - V_Z}{1.8}$$

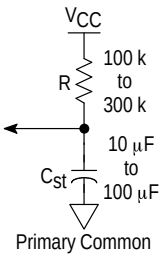
$$V_{blk(min)} \approx VAC_{(on\ to\ off)} \sqrt{2} - \left(\frac{P_O}{VAC_{(on\ to\ off)}\ 2f_{AC}\ C_{blk}\ \eta} \right) - 1.4$$

Digital On/Off Control (Circuit D)



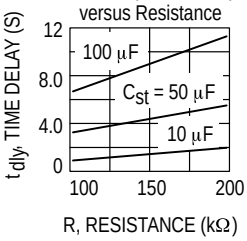
Digital on/off control of the converter is accomplished with a small signal NPN transistor. An optocoupler can be used if galvanic isolation is required.

Power–Up Time Delay (Circuit E)

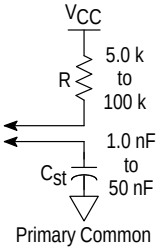


A programmed power–up time delay can be implemented with the addition of a simple RC circuit.

Power–Up Time Delay versus Resistance



State Control Disabled (Circuit F)



The State Control block on/off capability can be disabled and made to appear transparent by either connecting a pull–up resistor from the input to V_{CC} or a small value capacitor from the input to primary common. This input should not be left unconnected since it has a relatively high impedance and may be susceptible to noise pick–up.

Figure 24. Universal Input 52 W Off–Line Converter

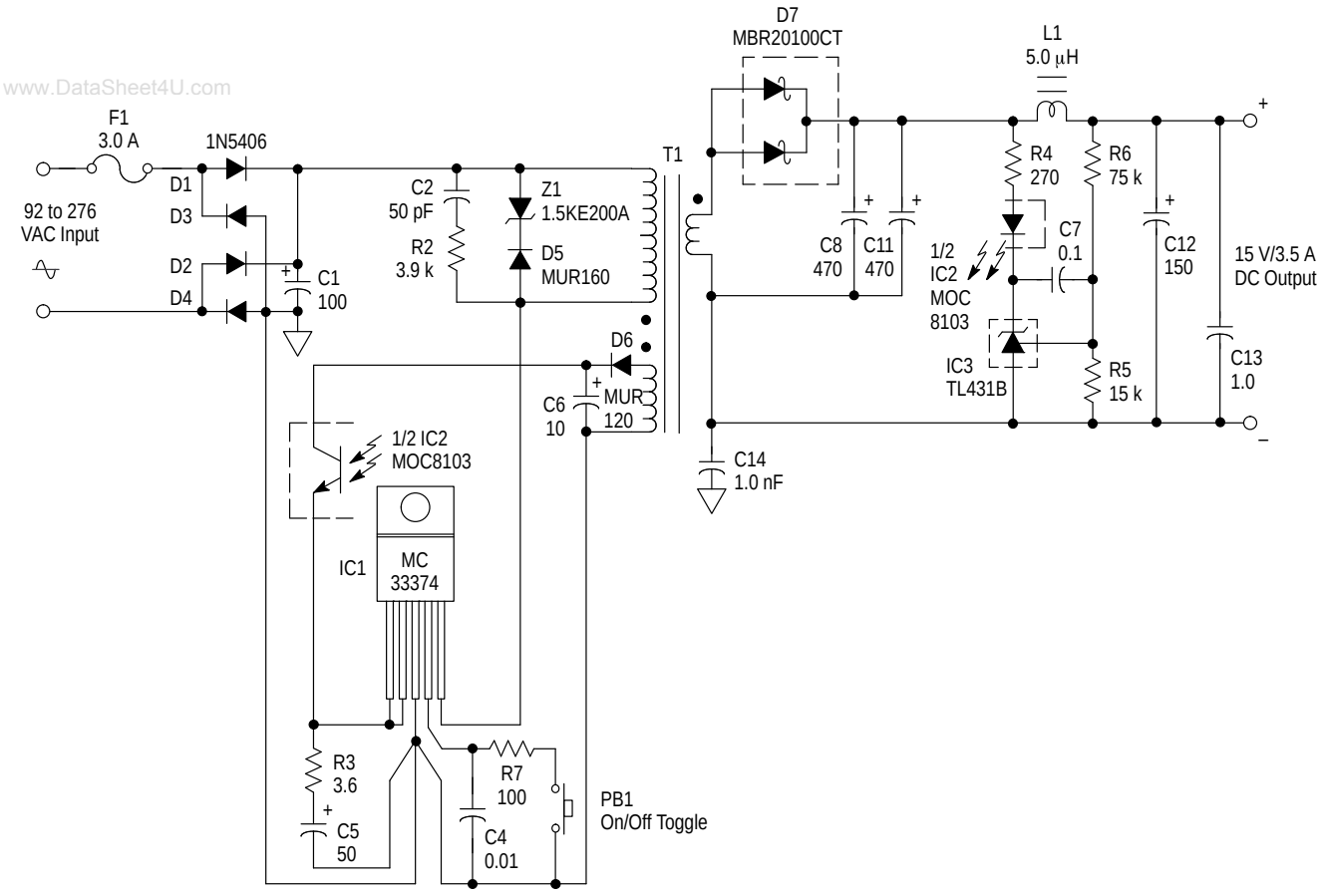


Figure 25. Converter Test Data

Test	Conditions	Results
Line Regulation	V_{in} = 92 Vac to 276 Vac, I_O = 3.5 A	Δ = 2.0 mV
Load Regulation	V_{in} = 115 Vac, I_O = 0.35 A to 3.5 A	Δ = 9.0 mV
	V_{in} = 230 Vac, I_O = 0.35 A to 3.5 A	Δ = 13 mV
Output Ripple	V_{in} = 92 Vac to 276 Vac, I_O = 3.5 A	Total = 170 $mV_{p–p}$
Efficiency	V_{in} = 115 Vac, I_O = 3.5 A	84.4%
	V_{in} = 230 Vac, I_O = 3.5 A	86.2%
AC Input Power	V_{in} = 115 Vac, Converter Toggle Off	0.06 W
	V_{in} = 230 Vac, Converter Toggle Off	0.19 W

This data was taken with the components listed below mounted on the printed circuit board shown if Figure 28.

C8, C11 = Sanyo Os–Con #16SA470M, 470 µF/16V.

C12 = Sanyo Os–Con #10SA150M, 150 µF/16V.

IC1, D7 = MC33374, MBR20100 mounted on Aavid #590302B03600 heatsink.

L1 = Coilcraft S5088–A, 5.0 µH, 0.011 Ω.

T1 = Coilcraft W7422–A
Primary: 49 turns of # 24 AWG, Pin 6 = start, Pin 5 = finish.
Two layers 0.002" Mylar tape.
Secondary: 9 turns of # 21 AWG, 2 strands bifilar wound, Pins 1 and 2 = start, Pins 9 and 10 = finish.
Auxiliary: 7 turns of #24 AWG wound in center of bobbin, Pin 7 = start, Pin 4 = finish.
Two layers 0.002" Mylar tape.
Gap: 0.017" total for a primary inductance (L_P) of 345 µH, with a primary to secondary leakage inductance of 14 µH.
Core: Ferrite International E24/25 (E25/10/6) TSF–7070 material.
Bobbin: Philips E24–25PCB1–10, Pins 3 and 8 removed.

Figure 26. Universal Input 90 W Off–Line Converter

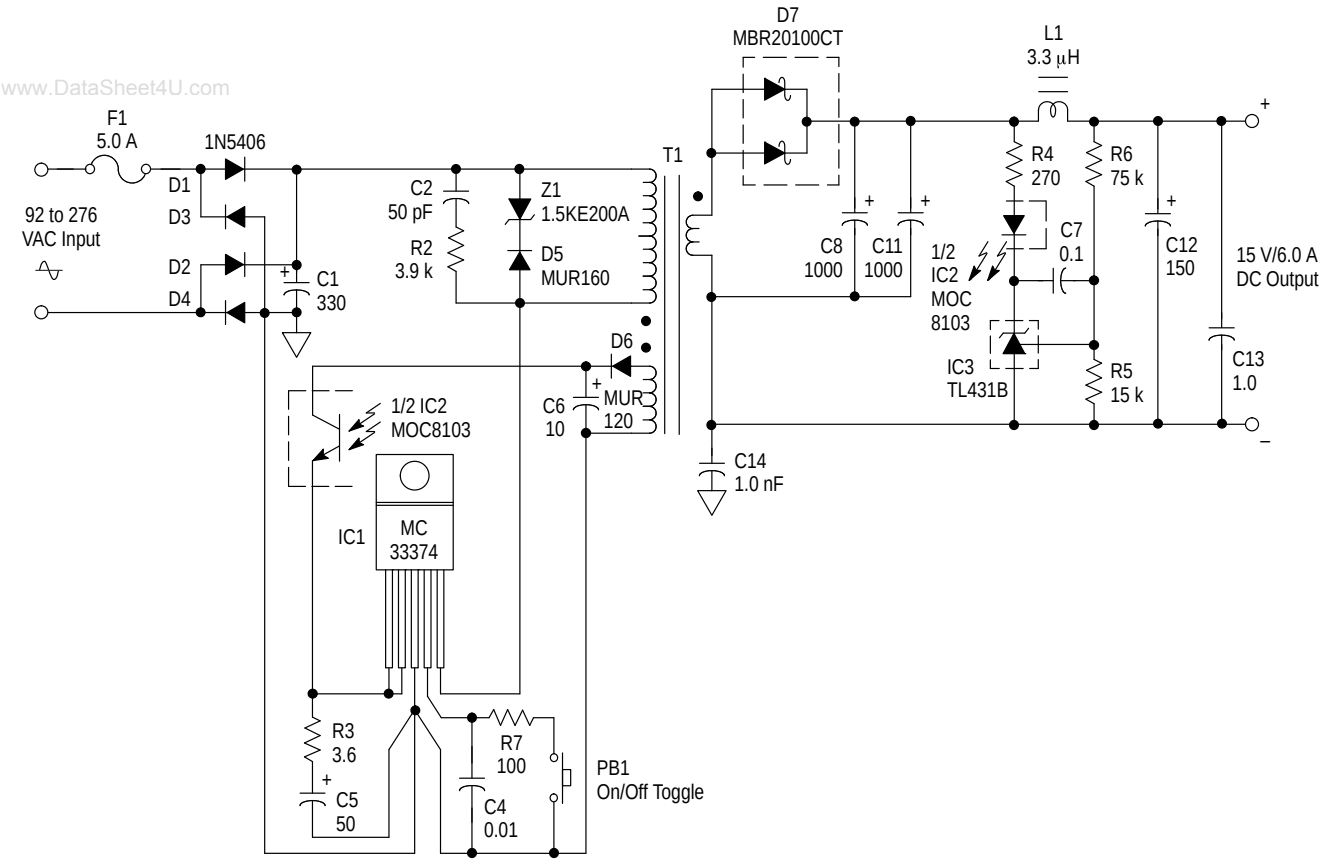


Figure 27. Converter Test Data

Test	Conditions	Results
Line Regulation	V_{in} = 92 Vac to 276 Vac, I_O = 6.0 A	Δ = 24 mV
Load Regulation	V_{in} = 115 Vac, I_O = 0.6 A to 6.0 A	Δ = 26 mV
	V_{in} = 230 Vac, I_O = 0.6 A to 6.0 A	Δ = 10 mV
Output Ripple	V_{in} = 92 Vac to 276 Vac, I_O = 6.0 A	Total = 105 $mV_{p–p}$
Efficiency	V_{in} = 115 Vac, I_O = 6.0 A	83.2%
	V_{in} = 230 Vac, I_O = 6.0 A	85.4%
AC Input Power	V_{in} = 115 Vac, Converter Toggle Off	0.07 W
	V_{in} = 230 Vac, Converter Toggle Off	0.17 W

This data was taken with the components listed below mounted on the printed circuit board shown if Figure 28.

C8, C11 = Sanyo Os–Con #16SA1000M, 1000 µF/16V.

C12 = Sanyo Os–Con #10SA150M, 100 µF/16V.

IC1 = MC33374 mounted on Aavid #604953B02500 extruded heatsink. The heatsink must be drilled and tapped to allow device & PCB attachment.

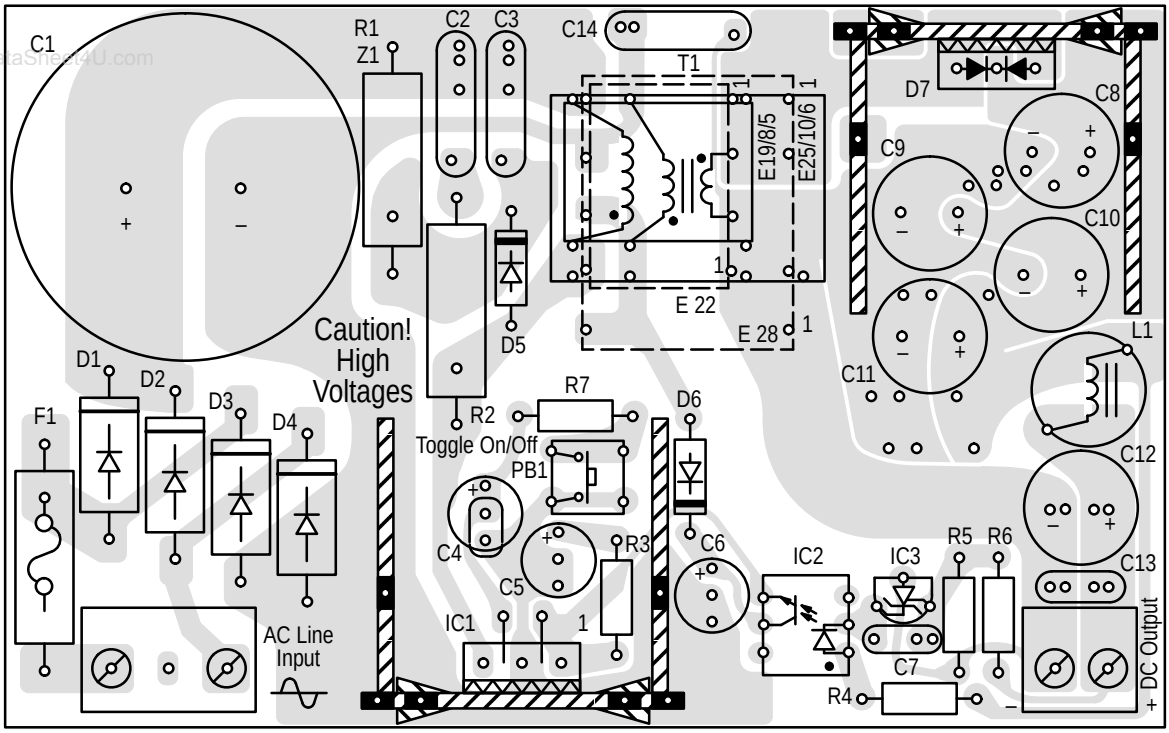
Z1 = 1.5KE200A with cathode lead soldered in the center of a 5/8" x 3/4" x 0.025" thick U–shaped copper heatsink.

D7 = MBR20100 mounted on Aavid #590302B03600 heatsink.

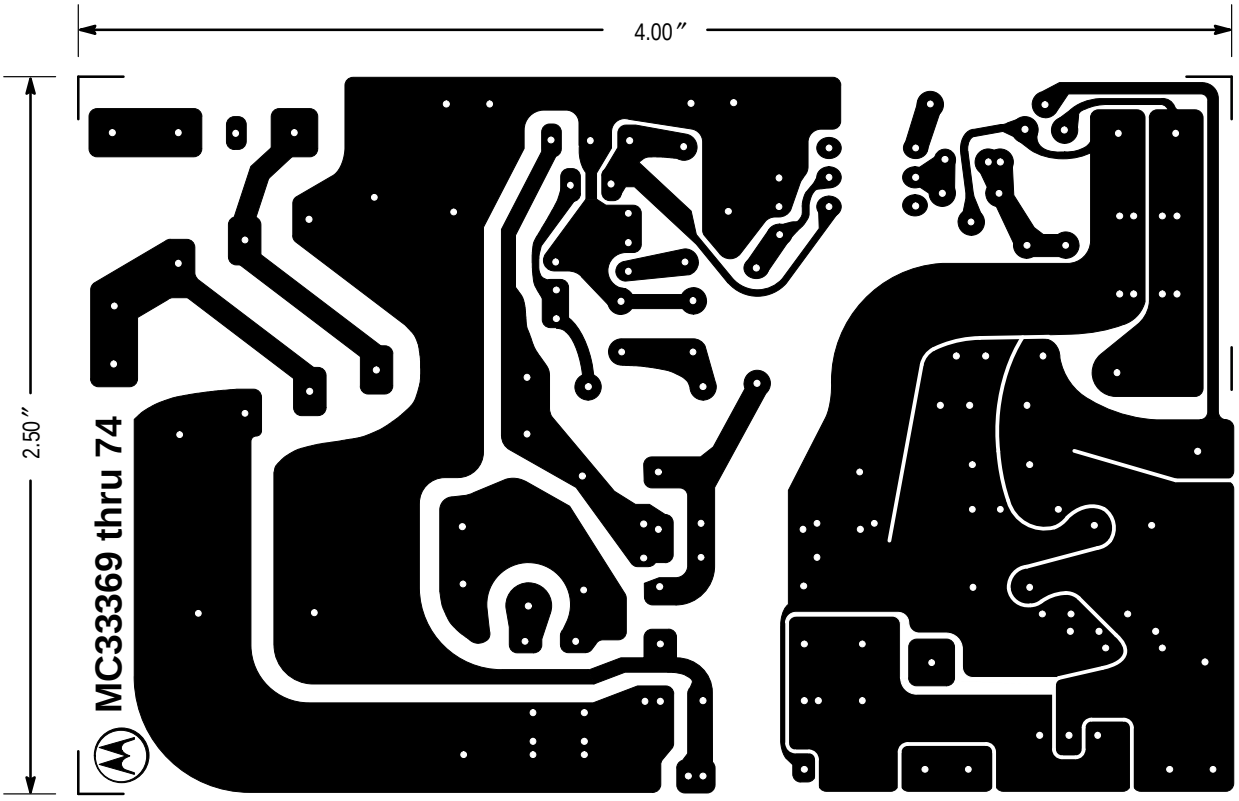
L1 = Coilcraft PCV–0–332–10, 3.3 µH, 0.005 Ω.

T1 = Coilcraft W7518–A
Primary: 34 turns of # 24 AWG, Pin 9 = start, Pin 6 = finish.
Two layers 0.002" Mylar tape.
Secondary: 5 turns of # 20 AWG, 2 strands bifilar wound, Pins 4 and 5 = start, Pins 1 and 2 = finish.
Two layers 0.002" Mylar tape.
Auxiliary: 4 turns of #24 AWG wound in center of bobbin, Pin 10 = start, Pin 7 = finish.
Two layers 0.002" Mylar tape.
Gap: 0.022" total for a primary inductance (L_P) of 290 µH, with a primary to secondary leakage inductance of 7.2 µH.
Core: TDK PC40 EI28Z, PC40 material.
Bobbin: TDK BE–28–1110CPL, Pins 3 and 8 removed.

Figure 28. Printed Circuit Board and Component Layout
(Circuit of Figures of 23 and 25)

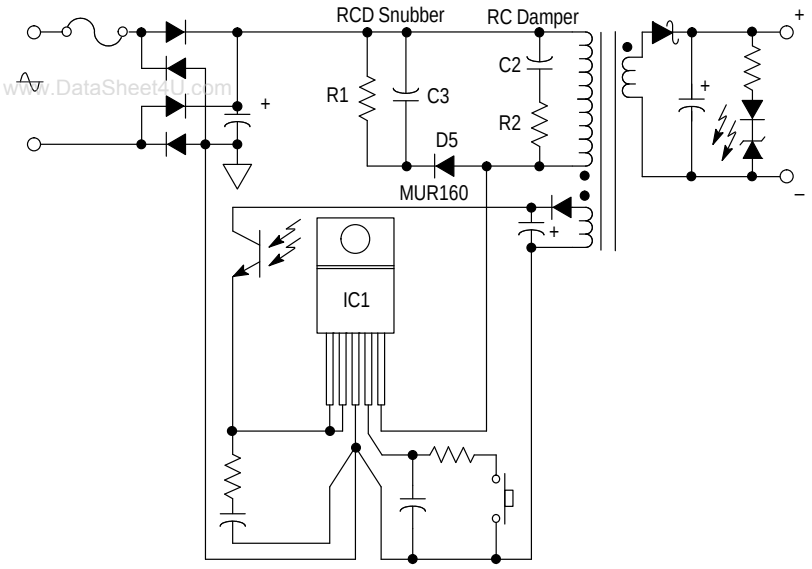


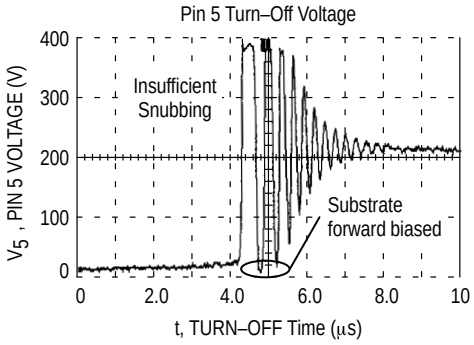
(Top View)

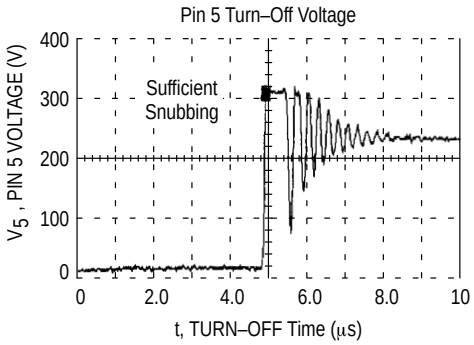


(Bottom View)

Figure 29. Snubber and Damper Circuits



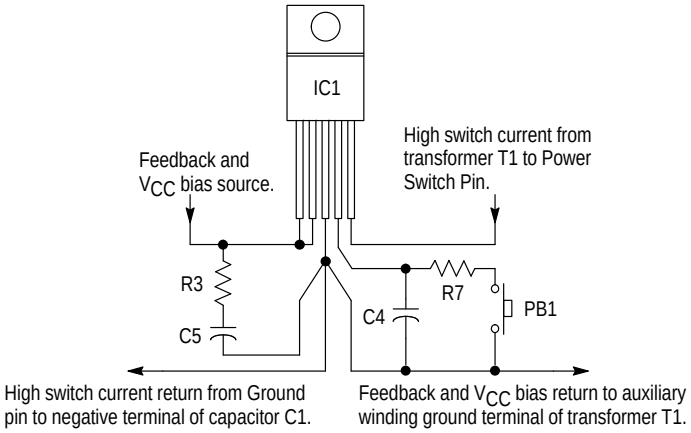




Converter Figure	Output Power	T1 Primary Leakage Inductance	Component Values			
			Snubber		Damper	
			R1	C3	R2	R2
24	50 W	14 μH	20 k 2.0 W	0.1 μF 400 V	6.2 k 1.0 W	47 pF 500 V
26	90 W	7.2 μH	10 k 3.0 W	0.1 μF 400 V	6.2 k 1.0 W	47 pF 500 V

Figures 24 and 26 use zener diode Z1 to limit the voltage on Pin 5 and a damper circuit consisting of resistor R2 and capacitor C2. The zener can be replaced with the snubber circuit shown above consisting of resistor R1 and capacitor C3. The component values selected must insure that the turn–off voltage on Pin 5 never exceeds 700 V under all line voltage and load current conditions when using a transformer with the highest anticipated leakage inductance. There must also be sufficient snubbing and damping to prevent the turn–off voltage on Pin 5 from ringing below ground. This will cause forward biasing of the substrate and can result in additional device power dissipation and converter instability. Suggested snubber and damper component values for Figures 24 and 26 are listed in the table above. The snubber and damper circuits will greatly reduce the radiated switching noise but there will be a slight penalty in converter efficiency.

Figure 30. Recommended Printed Circuit Board Layout



In order to ensure proper device operation, the integrated circuit Ground, Pin 3, must connect as directly as possible to the printed circuit board ground foil. The ground pin should not be bent or offset by the board layout. The Power Switch circuit, Pin 5, can be offset if additional creepage distance is required using a TV suffix product. Components R3 and C5 connect through seperate and short copper traces to IC1. This will reduce the level of undesirable switching noise that appears on the Feedback Input and V_{CC} pins.

Figure 31. Transformer Auxiliary Winding Elimination
Zener Shunt Regulator Method

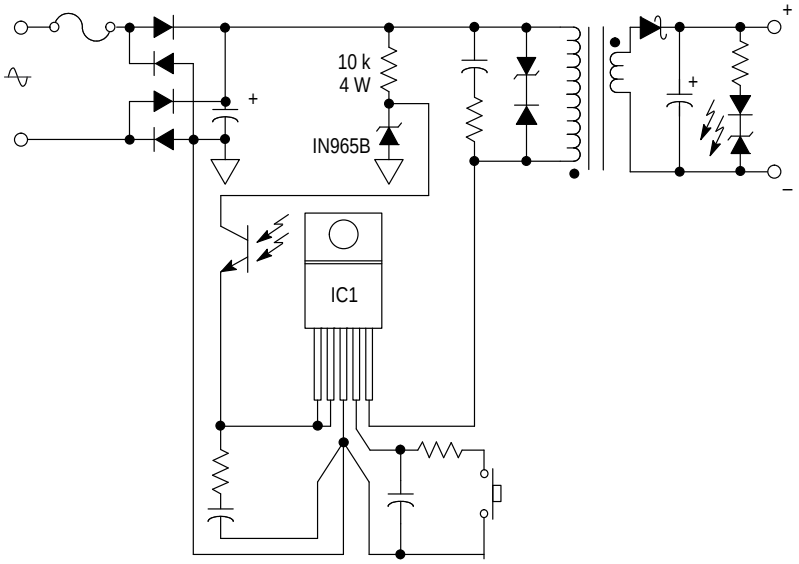


Figure 32. Transformer Auxiliary Winding Elimination
Bipolar Transistor Series Regulator Method

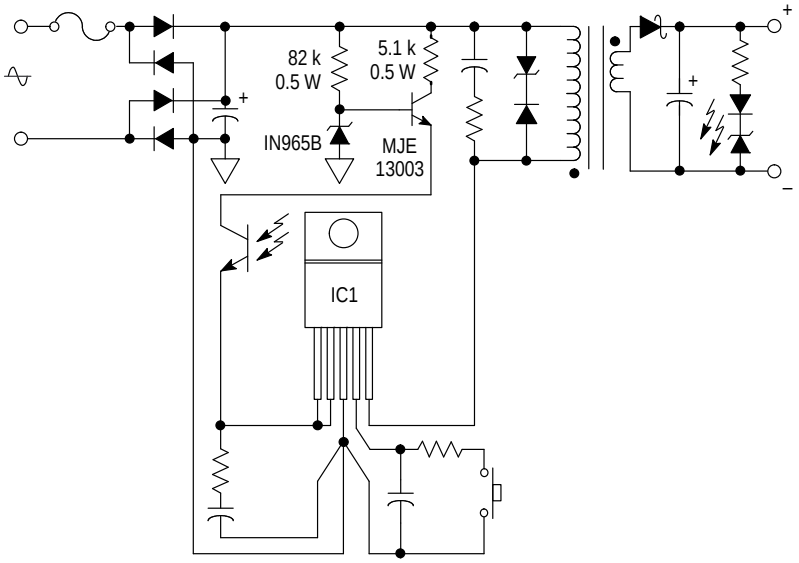
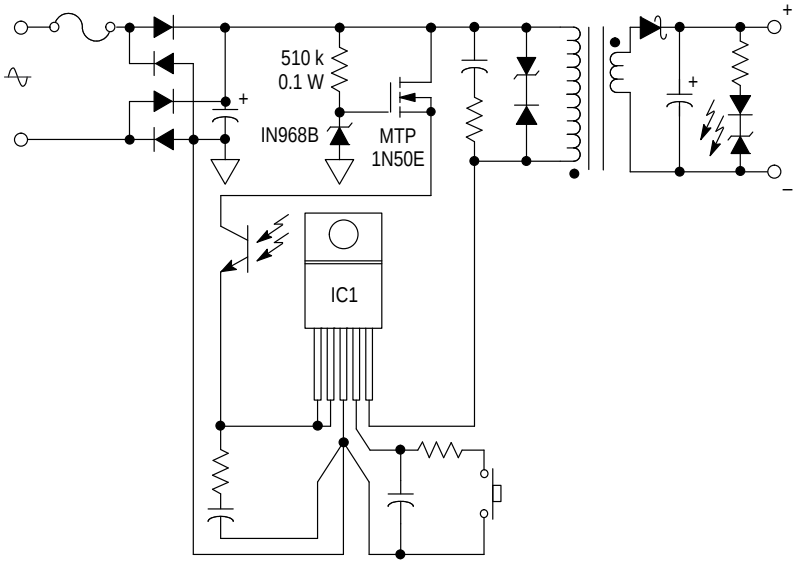
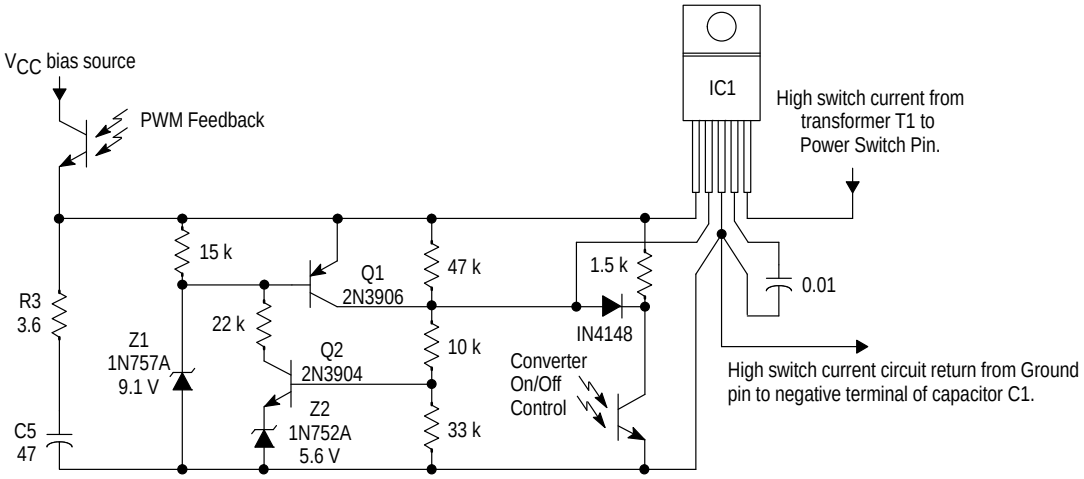


Figure 33. Transformer Auxiliary Winding Elimination
MOSFET Transistor Series Regulator Method



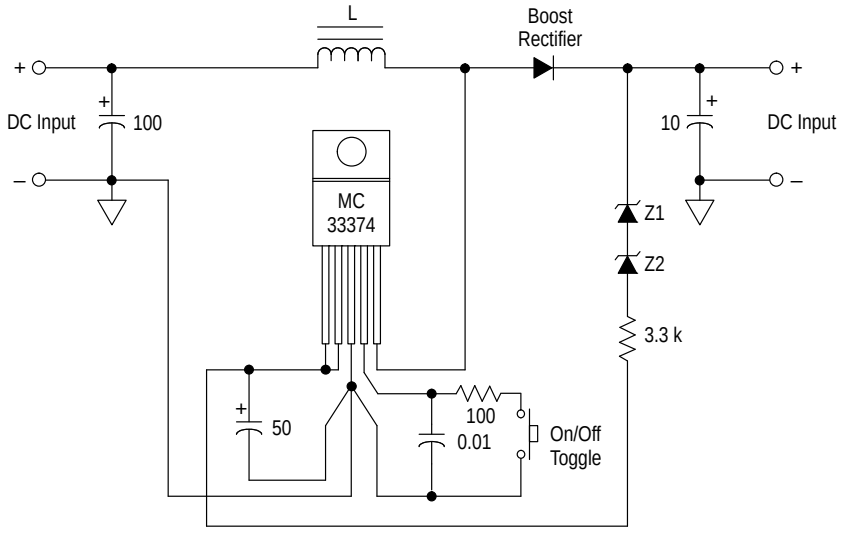
Figures 31 through 33 show three possible methods of eliminating the transformer auxiliary winding and the associated fast recovery diode and capacitor. These methods are most practical for fixed or narrow range AC line voltage applications. Care must be taken when used in wide range AC line voltage applications, as the power dissipation in the voltage dropping elements may become excessive. The shunt regulator method is the most economical but the series pass methods dissipate less power when used in wide range line voltage applications. The MOSFET method is the most efficient since the gate requires essentially zero current. The component values shown in the above figures are for a nominal AC line voltage of 115 volts ±20%.

Figure 34. Converter Soft–Start



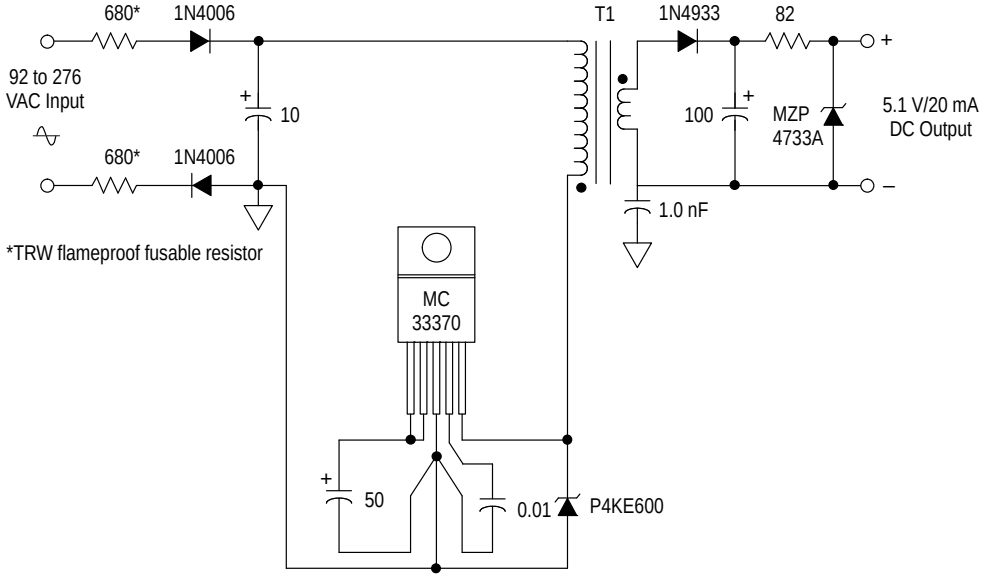
Converter soft–start can be implemented by separating the connection between Pins 1 and 2 with a resistor. Initially with the converter in the off state, the internal Start–Up circuit charges capacitor C5 to a voltage that exceeds the Vbe of Q1 plus the breakdown of Z1. This causes transistors Q1 and Q2 to latch on. Since the voltage at pin 2 is now greater than the internal shunt regulator threshold, minimum duty cycle pulses appear at the Power Switch circuit Pin 5. As the voltage across C5 approaches the regulation threshold, the PWM duty cycle will gradually increase until regulation is established at the converter output. Upon converter power down, the transistor latch will turn off at approximately 8.0 V which is slightly greater than the devices highest minimum operating voltage specification. This guarantees that soft–start will be active upon the next power–up cycle.

Figure 35. High Voltage Step–Up Converter



A simple transformerless high voltage step–up converter can be constructed with any of the devices in this series. The maximum output voltage of this topology is limited by the Power Switch circuit breakdown of 700 V minus the forward voltage drop of the boost rectifier. The converter requires a minimum input of 15 V to guarantee start–up. The regulated output voltage is equal to the sum of the zener voltage drops, plus the shunt regulator threshold, plus the voltage drop across the 3.3 k resistor. The boost rectifier must be a schottky or fast recovery type with sufficient current and voltage capability to meet the converter's output requirements.

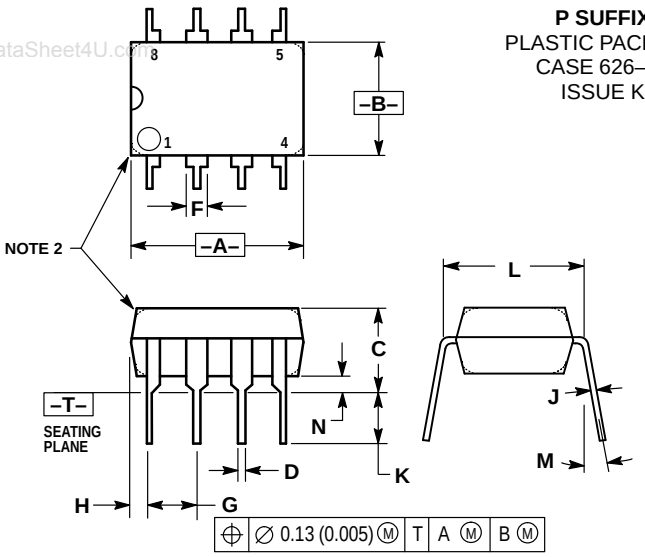
Figure 36. Low Power Off–Line Converter



The converter shown above was designed for cost sensitive low power applications that require a line isolated power source. Typical applications include consumer and industrial equipment. Note that the transformer auxiliary winding has been eliminated and the MC33370 operates continuously in the auto restart mode. This method of converter operation is capable of providing an output power of up to 200 mW.

OUTLINE DIMENSIONS

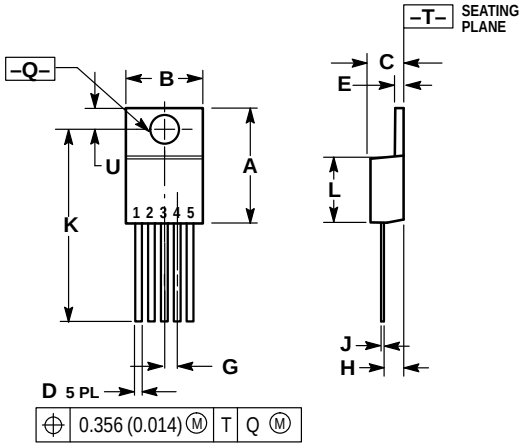
P SUFFIX
PLASTIC PACKAGE
CASE 626–05
ISSUE K



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

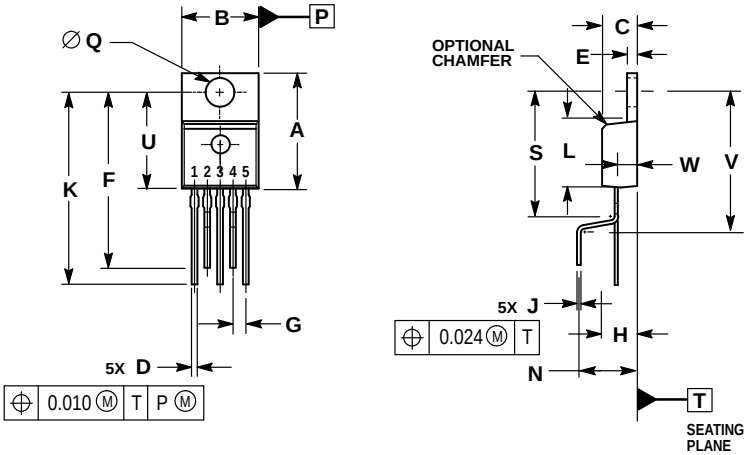
T SUFFIX
PLASTIC PACKAGE
CASE 314D–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
G	0.067 BSC		1.702 BSC	
H	0.087	0.112	2.210	2.845
J	0.015	0.025	0.381	0.635
K	0.990	1.045	25.146	26.543
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
U	0.105	0.117	2.667	2.972

TV SUFFIX
PLASTIC PACKAGE
CASE 314E–01
ISSUE O



NOTES:
1. DIMENSIONS ARE IN INCHES.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.005 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	INCHES	
DIM	MIN	MAX
A	0.572	0.613
B	0.390	0.415
C	0.170	0.180
D	0.025	0.038
E	0.048	0.055
F	0.890	0.930
G	0.067 BSC	
H	0.105 BSC	
J	0.015	0.025
K	0.900	1.000
L	0.320	0.365
N	0.259 BSC	
Q	0.140	0.153
S	—	0.620
U	0.468	0.505
V	—	0.718
W	0.090	0.100

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