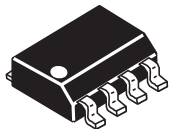
Document Number: MC33662
Rev. 7.0, 1/2014

LIN 2.1 / SAEJ2602-2, LIN Physical Layer

33662

LINCELL



EF SUFFIX (PB-FREE)
98ASB42564B
8-PIN SOICN

The Local Interconnect Network (LIN) is a serial communication protocol, designed to support automotive networks in conjunction with a Controller Area Network (CAN). As the lowest level of a hierarchical network, LIN enables cost-effective communication with sensors and actuators when all the features of CAN are not required.

The three 33662 versions are designed to operate at different maximum baud rates. The 33662LEF and 33662BLEF, and the 33662SEF and 33662BSEF, offer a normal baud rate (20 kbps), and the 33662JEF and 33662BJEF, a slow baud rate (10 kbps). They integrate a fast baud rate (above 100 kbps), as reported by the RXD pin for test and programming modes. They provide excellent EMC (Electromagnetic Compatibility) and Radiated Emission performance, ESD (Electrostatic Discharge) robustness, and safe behavior, in the event of a LIN bus short-to-ground, or a LIN bus leakage during low-power mode. This device is powered by SMARTMOS technology.

Features

- Operational from a V_{SUP} of 7.0 to 18 V DC, functional up to 27 V DC, and handles 40 V during Load Dump
- Compatible with LIN Protocol Specification 1.3, 2.0, 2.1, and SAEJ2602-2
- Active bus wave shaping, offering excellent radiated emission performance
- Sustains up to 15.0 kV minimum ESD IEC61000-4-2 on the LIN Bus, 20 kV on the WAKE pin, and 25 kV on the VSUP pin
- Very high immunity against electromagnetic interference
- Low standby current in Sleep mode
- Overtemperature protection
- Local and remote Wake-up capability reported by the RXD pin
- Fast baud rate selection reported by RXD pin
- 5.0 V and 3.3 V compatible digital inputs without any required external components

Applications

- Automotive Market:
  - Body electronics (BCM, gateway, roof, door, lighting, HVAC)
  - Powertrain (EMS, start & stop), BMS
  - Safety & Chassis (TPMS, seat belt)

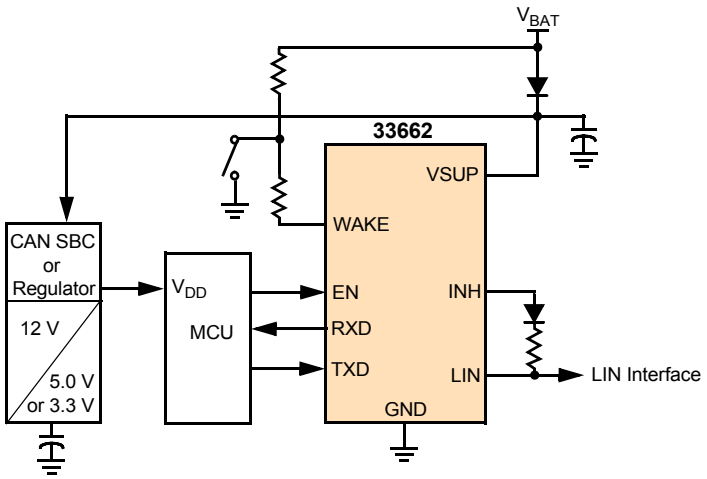


Figure 1. 33662 Master LIN Bus Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

DEVICE VARIATIONS

Table 1. Device Variations

Freescale Part No. (Add an R2 suffix for Tape and Reel orders)	Maximum Baud Rate	Temperature Range (T_A)	Package
MC33662LEF [1] MC33662BLEF	20 kbps	-40 to 125 °C	8 SOICN
MC33662SEF [1] MC33662BSEF	20 kbps with restricted limits for transmitter and receiver symmetry		
MC33662JEF [1] MC33662BJEF	10 kbps		

Notes

1. In Sleep mode, the total module current consumption may be higher than expected if the external pull-up resistor on the RxD pin is implemented. There may be an unexpected glitch on RxD as INH goes low.

INTERNAL BLOCK DIAGRAM

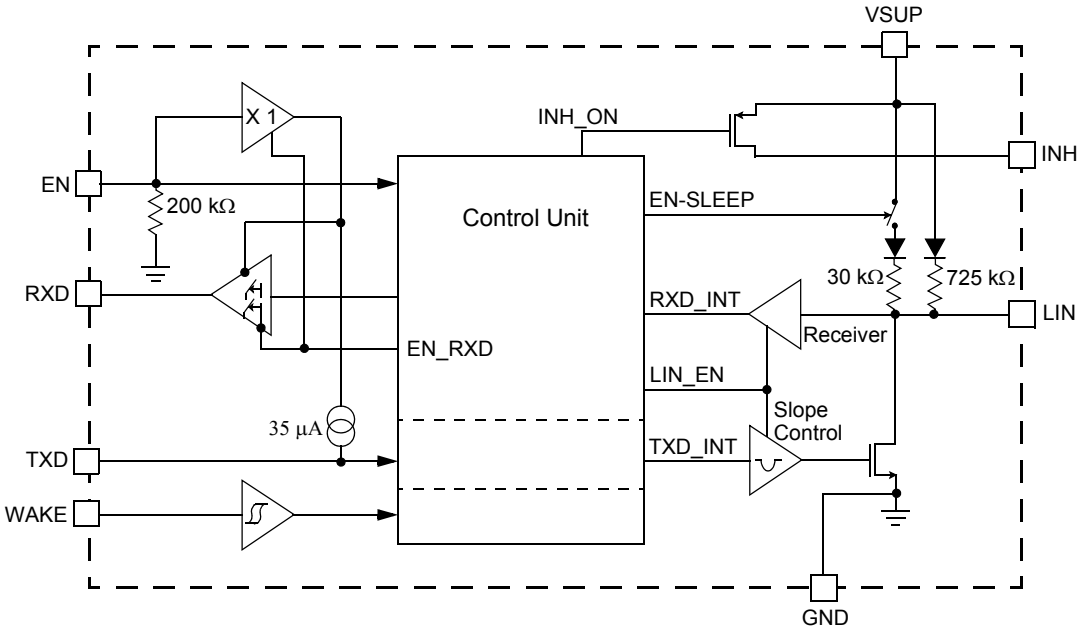


Figure 2. 33662 Simplified Internal Block Diagram

PIN CONNECTIONS

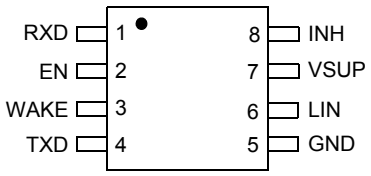


Figure 3. 33662 8-SOICN Pin Connections

Table 2. 33662 8-SOICN Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 21.

Pin	PIN NAME	Pin Function	Formal Name	Definition
1	RXD	Output	Data Output	This pin is the receiver output of the LIN interface which reports the state of the bus voltage to the MCU interface.
2	EN	Input	Enable Control	This pin controls the operation mode of the interface.
3	WAKE	Input	Wake Input	This pin is a high-voltage input used to wake-up the device from Sleep mode.
4	TXD	Input	Data Input	This pin is the transmitter input of the LIN interface which controls the state of the bus output.
5	GND	Ground	Ground	This pin is the device ground pin.
6	LIN	Input/Output	LIN Bus	This bidirectional pin represents the single-wire bus transmitter and receiver.
7	VSUP	Power	Power Supply	This pin is the device battery level power supply.
8	INH	Output	Inhibit Output	This pin can have two main functions: controlling an external switchable voltage regulator having an inhibit input, or driving an external bus resistor in the master node application.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Power Supply Voltage			V
Normal Operation (DC)	$V_{SUP(SS)}$	-0.3 to 27	
Transient input voltage with external component (according to ISO7637-2 & ISO7637-3 & "Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications" specification Rev1.1 / December 2nd, 2009) (See Table 4 and Figure 4)			
- Pulse 1 (test up to the limit for Damage - Class A[2])	$V_{SUP(S1)}$	-100	
- Pulse 2a (test up to the limit for Damage - Class A[2])	$V_{SUP(S2A)}$	+75	
- Pulse 3a (test up to the limit for Damage - Class A[2])	$V_{SUP(S3A)}$	-150	
- Pulse 3b (test up to the limit for Damage - Class A[2])	$V_{SUP(S3B)}$	+100	
- Pulse 5b (Class A)[2]	$V_{SUP(S5B)}$	-0.3 to 40	
WAKE			V
Normal Operation within series 2*18 kΩ resistor (DC)	$V_{WAKE(SS)}$	-27 to 40	
Transient input voltage with external component (according to ISO7637-2 & ISO7637-3 & "Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications" specification Rev1.1 / December 2nd, 2009) (See Table 4 and Figure 5)			
- Pulse 1 (test up to the limit for Damage - Class D[3])	$V_{WAKE(S1)}$	-100	
- Pulse 2a (test up to the limit for Damage - Class D[3])	$V_{WAKE(S2A)}$	+75	
- Pulse 3a (test up to the limit for Damage - Class D[3])	$V_{WAKE(S3A)}$	-150	
- Pulse 3b (test up to the limit for Damage - Class D[3])	$V_{WAKE(S3B)}$	+100	
Logic Voltage (RXD, TXD, EN Pins)	V_{LOG}	-0.3 to 5.5	V
LIN Bus Voltage			V
Normal Operation (DC)	$V_{BUS(SS)}$	-27 to 40	
Transient (Coupled Through 1.0 nF Capacitor, according to ISO7637-2 & ISO7637-3 & "Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications" specification Rev1.1 / December 2nd, 2009) (See Table 4 and Figure 6)			
- Pulse 1 (test up to the limit for Damage - Class D[3])	$V_{BUS(S1)}$	-100	
- Pulse 2a (test up to the limit for Damage - Class D[3])	$V_{BUS(S2A)}$	+75	
- Pulse 3a (test up to the limit for Damage - Class D[3])	$V_{BUS(S3A)}$	-150	
- Pulse 3b (test up to the limit for Damage - Class D[3])	$V_{BUS(S3B)}$	+100	
INH Voltage/Current			V
DC Voltage	V_{INH}	-0.3 to V_{SUP} +0.3	
Transient (Coupled Through 1.0 nF Capacitor, according to ISO7637-2 & ISO7637-3 & "Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications" specification Rev1.1 / December 2nd, 2009) (See Table 4 and Figure 7)			
- Pulse 1 (test up to the limit for Damage - Class D[3])	$V_{INH(S1)}$	-100	
- Pulse 2a (test up to the limit for Damage - Class D[3])	$V_{INH(S2A)}$	+75	
- Pulse 3a (test up to the limit for Damage - Class D[3])	$V_{INH(S3A)}$	-150	
- Pulse 3b (test up to the limit for Damage - Class D[3])	$V_{INH(S3B)}$	+100	

Notes

2. Class A: All functions of a device/system perform as designed during and after exposure to disturbance.
3. Class D: At least one function of the transceiver stops working properly during the test, and will return to proper operation automatically when the exposure to the disturbance has ended. No physical damage of the IC occurs.

Table 3. Maximum Ratings (continued)

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

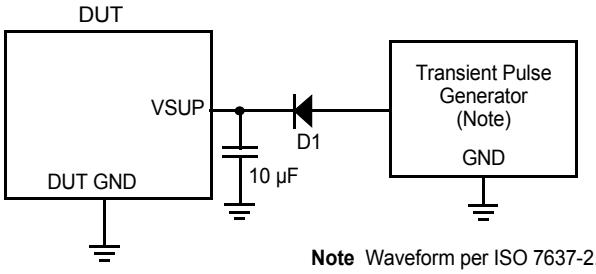
Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS (CONTINUED)			
ESD Capability - AECQ100			V
Human Body Model - JESD22/A114 (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω)			
LIN pin versus GND	V_{ESD1-1}	±10.0 k	
Wake pin versus GND	V_{ESD1-2}	±8.0 k	
All other pins	V_{ESD1-4}	±4.0 k	
Charge Device Model - JESD22/C101 (C_{ZAP} = 4.0 pF)			
Corner pins (Pins 1, 4, 5 and 8)	V_{ESD2-1}	±750	
All other pins (Pins 2, 3, 6 and 7)	V_{ESD2-2}	±500	
Machine Model - JESD22/A115 (C_{ZAP} = 220 pF, R_{ZAP} = 0 Ω)			
All pins	V_{ESD3-1}	±200	
According to “Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications” specification Rev1.1 / December 2nd, 2009 (C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω)			
Contact Discharge, Unpowered			
LIN pin without capacitor	V_{ESD4-1}	±15 k	
LIN pin with 220 pF capacitor	V_{ESD4-2}	±15 k	
VSUP (10 µF to ground)	V_{ESD4-3}	±25 k	
WAKE (2*18 kΩ serial resistor)	V_{ESD4-4}	±20 k	
INH pin	V_{ESD4-5}	±2.0 k	
LIN pin with 220 pF capacitor and indirect ESD coupling (according to ISO10605 - Annex F)	V_{ESD4-6}	>±15 k	
According to ISO10605 - Rev 2008 test specification			
(2.0 kΩ / 150 pF) - Unpowered - Contact discharge			
LIN pin without capacitor	V_{ESD5-1}	±20 k	
LIN pin with 220 pF capacitor	V_{ESD5-2}	±25 k	
VSUP (10 µF to ground)	V_{ESD5-3}	±25 k	
WAKE (2*18 kΩ serial resistor)	V_{ESD5-4}	±25 k	
(2.0 kΩ / 330 pF) - Powered - Contact discharge			
LIN pin without capacitor	V_{ESD6-1}	±8 k	
LIN pin with 220 pF capacitor	V_{ESD6-2}	±10 k	
VSUP (10 µF to ground)	V_{ESD6-3}	±12 k	
WAKE (2*18 kΩ serial resistor)	V_{ESD6-4}	±15 k	
THERMAL RATINGS			
Operating Temperature			°C
Ambient	T_A	-40 to 125	
Junction	T_J	-40 to 150	
Storage Temperature	T_{STG}	-40 to 150	°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	150	°C/W
Peak Package Reflow Temperature During Solder Mounting (4)	T_{SOLDER}	240	°C
Thermal Shutdown Temperature	T_{SHUT}	150 to 200	°C
Thermal Shutdown Hysteresis Temperature	T_{HYST}	20	°C

Notes

4. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

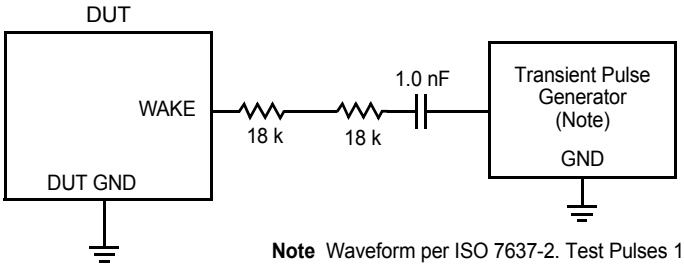
Table 4. Limits / Maximum Test Voltage for Transient Immunity Tests

Test Pulse	V_S [V]	Pulse repetition frequency [Hz] ($1/T_1$)	Test Duration [min]	R_i [Ω]	Remarks
1	-100	2	1 for function test 10 for damage test	10	t_2 = 0 s
2a	+75	2		2	
3a	-150	10000		50	
3b	+100	10000		50	



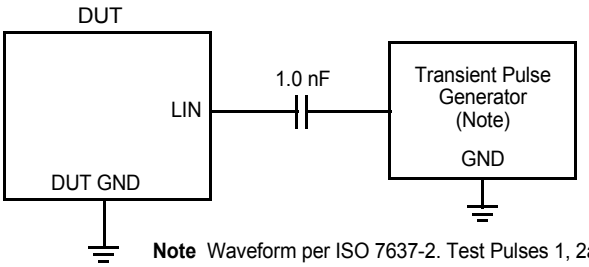
Note Waveform per ISO 7637-2. Test Pulses 1, 2a, 3a, 3b.

Figure 4. Test Circuit for Transient Test Pulses (VSUP)



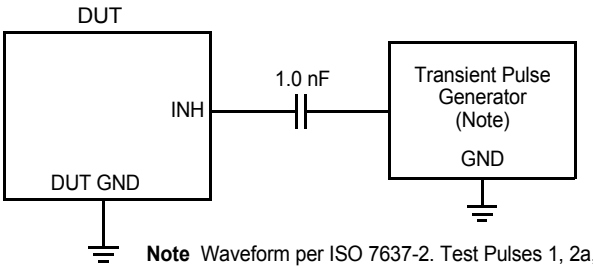
Note Waveform per ISO 7637-2. Test Pulses 1, 2a, 3a, 3b.

Figure 5. Test Circuit for Transient Test Pulses (WAKE)



Note Waveform per ISO 7637-2. Test Pulses 1, 2a, 3a, 3b.

Figure 6. Test Circuit for Transient Test Pulses (LIN)



Note Waveform per ISO 7637-2. Test Pulses 1, 2a, 3a, 3b.

Figure 7. Test Circuit for Transient Test Pulses (INH)

STATIC ELECTRICAL CHARACTERISTICS

Table 5. Static Electrical Characteristics

Characteristics under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VSUP PIN (DEVICE POWER SUPPLY)					
Nominal Operating Voltage	V_{SUP}	7.0	13.5	18.0	V
Functional Operating Voltage[5]	V_{SUPOP}	6.7	–	27	V
Load Dump	V_{SUPLD}	–	–	40	V
Power-On Reset (POR) Threshold V_{SUP} Ramp Down and INH goes High to Low	V_{POR}	3.5	–	5.3	V
Power-On Reset (POR) Hysteresis	$V_{PORHYST}$	–	270	–	mV
V_{SUP} Undervoltage Threshold (positive and negative) Transmission disabled and LIN bus goes in recessive state	V_{UVL}, V_{UVH}	5.8	–	6.7	V
V_{SUP} Undervoltage Hysteresis (V_{UVL} - V_{UVH})	V_{UVHYST}	–	130	–	mV
Supply Current in Sleep Mode V_{SUP} ≤ 13.5 V, Recessive State 13.5 V < V_{SUP} < 27 V V_{SUP} ≤ 13.5 V, Shorted to GND	 I_{S1} I_{S2} I_{S3}	 — — —	 6.0 — 24	 11 20 70	µA
Supply Current in Normal or Slow or Fast Mode Bus Recessive, Excluding INH Output Current Bus Dominant, Excluding INH Output Current	 $I_{S(REC)}$ $I_{S(DOM)}$	 — —	 4.0 6.0	 6.0 8.0	mA
RXD OUTPUT PIN (LOGIC)					
Low Level Output Voltage I_{IN} ≤ 1.5 mA	V_{OL}	0	—	0.9	V
High Level Output Voltage V_{EN} = 5.0 V, I_{OUT} ≤ 250 µA V_{EN} = 3.3 V, I_{OUT} ≤ 250 µA	V_{OH}	 4.25 3.0	 — —	 5.25 3.5	V
TXD INPUT PIN (LOGIC)					
Low Level Input Voltage	V_{IL}	—	—	0.8	V
High Level Input Voltage	V_{IH}	2.0	—	—	V
Input Threshold Voltage Hysteresis	V_{INHYST}	100	300	600	mV
Pull-up Current Source V_{EN} = 5.0 V, 1.0 V < V_{TXD} < 3.5 V	I_{PU}	-60	-35	-20	µA
EN INPUT PIN (LOGIC)					
Low Level Input Voltage	V_{IL}	—	—	0.8	V
High Level Input Voltage	V_{IH}	2.0	—	—	V
Input Voltage Threshold Hysteresis	V_{INHYST}	100	400	600	mV
Pull-down Resistor	R_{PD}	100	230	350	kohm

5. For the functional operating voltage, the device is functional and all features are operating. The electrical parameters are noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125° C, GND = 0 V.

Table 5. Static Electrical Characteristics (continued)

Characteristics under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER - TRANSCEIVER LIN[6]					
Operating Voltage Range[7]	V_{BAT}	8.0	–	18	V
Supply Voltage Range	V_{SUP}	7.0	–	18	V
Voltage Range (within which the device is not destroyed)	$V_{SUP\_NON\_OP}$	-0.3	–	40	V
Current Limitation for Driver Dominant State Driver ON, V_{BUS} = 18 V	I_{BUS_LIM}	40	90	200	mA
Input Leakage Current at the Receiver Driver off; V_{BUS} = 0 V; V_{BAT} = 12 V	$I_{BUS\_PAS\_DOM}$	-1.0	–	–	mA
Leakage Output Current to GND Driver Off; 8.0 V < V_{BAT} < 18 V; 8.0 V < V_{BUS} < 18 V; $V_{BUS} \geq V_{BAT}$; $V_{BUS} \geq V_{SUP}$	$I_{BUS\_PAS\_REC}$	–	–	20	µA
Control Unit Disconnected from Ground[8] GND_{DEVICE} = V_{SUP}; V_{BAT} = 12 V; 0 < V_{BUS} < 18 V	$I_{BUS\_NO\_GND}$	-1.0	–	1.0	mA
V_{BAT} Disconnected; V_{SUP_DEVICE} = GND; 0 V < V_{BUS} < 18 V[9]	I_{BUSNO_BAT}	–	–	10	µA
Receiver Dominant State[10]	V_{BUSDOM}	–	–	0.4	V_{SUP}
Receiver Recessive State[11]	V_{BUSREC}	0.6	–	–	V_{SUP}
Receiver Threshold Center (V_{TH_DOM} + V_{TH_REC})/2	V_{BUS_CNT}	0.475	0.5	0.525	V_{SUP}
Receiver Threshold Hysteresis (V_{TH_REC} - V_{TH_DOM})	V_{HYS}	–	–	0.175	V_{SUP}
LIN dominant level with 500 Ω, 680 Ω and 1.0 kΩ load on the LIN bus	V_{LINDOM_LEVEL}	–	–	0.25	V_{SUP}
V_{BAT}_SHIFT	V_{SHIFT_BAT}	0	–	11.5%	V_{BAT}
GND_SHIFT	V_{SHIFT_GND}	0	–	11.5%	V_{BAT}
LIN Wake-up Threshold from Sleep Mode	V_{BUSWU}	–	4.3	5.3	V
LIN Pull-up Resistor to V_{SUP}	R_{SLAVE}	20	30	60	kΩ
LIN Internal Capacitor[12]	C_{LIN}			30	pF
Overtemperature Shutdown[13]	T_{LINSD}	150	160	200	°C
Overtemperature Shutdown Hysteresis	T_{LINSD_HYS}	–	20	–	°C

Notes

6. Parameters guaranteed for 7.0 V ≤ V_{SUP} ≤ 18 V.
7. Voltage range at the battery level, including the reverse battery diode.
8. Loss of local ground must not affect communication in the residual network.
9. Node has to sustain the current that can flow under this condition. The bus must remain operational under this condition.
10. LIN threshold for a dominant state.
11. LIN threshold for a recessive state.
12. This parameter is guaranteed by process monitoring but not production tested.
13. When an overtemperature shutdown occurs, the LIN transmitter and receiver are in recessive state and INH switched off. This parameter is tested with a test mode on ATE and characterized at laboratory.

Table 5. Static Electrical Characteristics (continued)

Characteristics under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INH OUTPUT PIN					
Driver ON Resistance (Normal Mode) I_{INH} = 50 mA	INH_{ON}	—	—	50	Ω
Current load capability From 7.0 V < V_{SUP} < 18 V	I_{INH_LOAD}	—	—	30	mA
Leakage Current (Sleep Mode) 0 < V_{INH} < V_{SUP}	I_{LEAK}	-5.0	—	5.0	µA
Overtemperature Shutdown[14]	T_{INHSD}	150	160	200	°C
Overtemperature Shutdown Hysteresis	T_{INHSD_HYS}	—	20	—	°C
WAKE INPUT PIN					
High to Low Detection Threshold (5.5 V < V_{SUP} < 7 V)	V_{WUHL1}	2.0	—	3.9	V
Low to High Detection Threshold (5.5 V < V_{SUP} < 7 V)	V_{WULH1}	2.4	—	4.3	V
Hysteresis (5.5 V < V_{SUP} < 7 V)	V_{WUHYS1}	0.2	—	0.8	V
High to Low Detection Threshold (7 V ≤ V_{SUP} < 27 V)	V_{WUHL2}	2.4	—	3.9	V
Low to High Detection Threshold (7 V ≤ V_{SUP} < 27 V)	V_{WULH2}	2.9	—	4.3	V
Hysteresis (7 V ≤ V_{SUP} < 27 V)	V_{WUHYS2}	0.2	—	0.8	V
Wake-up Input Current (V_{WAKE} < 27 V)	I_{WU}	—	—	5.0	µA

Notes

14. When an overtemperature shutdown occurs, the INH high side is switched off and the LIN transmitter and receiver are in recessive state. This parameter is tested with a test mode on ATE and characterized at laboratory.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 6. Dynamic Electrical Characteristics

Characteristics under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER **DRIVER CHARACTERISTICS FOR NORMAL SLEW RATE - 20.0 KBIT/SEC ACCORDING TO LIN PHYSICAL LAYER SPECIFICATION**(15), (16) **33662L AND 33662S DEVICES**					
Duty Cycle 1: $TH_{REC(MAX)}$ = 0.744 * V_{SUP} $TH_{DOM(MAX)}$ = 0.581 * V_{SUP} D1 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 50 µs, 7.0 V ≤ V_{SUP} ≤ 18 V	D1	0.396	—	—	%
Duty Cycle 2: $TH_{REC(MIN)}$ = 0.422 * V_{SUP} $TH_{DOM(MIN)}$ = 0.284 * V_{SUP} D2 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 50 µs, 7.6 V ≤ V_{SUP} ≤ 18 V	D2	—	—	0.581	
LIN PHYSICAL LAYER **DRIVER CHARACTERISTICS FOR SLOW SLEW RATE - 10.4 KBIT/SEC ACCORDING TO LIN PHYSICAL LAYER SPECIFICATION**(15), (16) **33662J DEVICE**					
Duty Cycle 3: $TH_{REC(MAX)}$ = 0.778 * V_{SUP} $TH_{DOM(MAX)}$ = 0.616 * V_{SUP} D3 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 96 µs, 7.0 V ≤ V_{SUP} ≤ 18 V	D3	0.417	—	—	%
Duty Cycle 4: $TH_{REC(MIN)}$ = 0.389 * V_{SUP} $TH_{DOM(MIN)}$ = 0.251 * V_{SUP} D4 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 96 µs, 7.6 V ≤ V_{SUP} ≤ 18 V	D4	—	—	0.590	
LIN PHYSICAL LAYER **DRIVER CHARACTERISTICS FOR FAST SLEW RATE**					
Fast Bit Rate (Programming Mode)	BR_{FAST}	—	—	100	kBit/s
LIN PHYSICAL LAYER **TRANSMITTER CHARACTERISTICS FOR NORMAL SLEW RATE - 20.0 KBIT/SEC**(19) **33662S DEVICE**					
Symmetry of Transmitter delay(18) t_{TRAN_SYM} = MAX ($t_{TRAN\_SYM60\%}$, $t_{TRAN\_SYM40\%}$) $t_{TRAN\_SYM60\%}$ = | $t_{TRAN\_PDF60\%}$ - $t_{TRAN\_PDR60\%}$ | $t_{TRAN\_SYM40\%}$ = | $t_{TRAN\_PDF40\%}$ - $t_{TRAN\_PDR40\%}$ |	t_{TRAN_SYM}	-7.25	—	7.25	µs

Notes

15. Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 8.
16. See Figure 9.
17. See Figure 10.
18. See Figure 11
19. V_{SUP} from 7.0 to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 8.

Table 6. Dynamic Electrical Characteristics (continued)

Characteristics under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER **RECEIVER CHARACTERISTICS ACCORDING LIN2.1**[20] **33662L AND 33662J AND 33662S DEVICES**					
Propagation Delay and Symmetry[21]					µs
Propagation Delay of Receiver, t_{REC_PD} = MAX (t_{REC_PDR}, t_{REC_PDF})	t_{REC_PD}	—	—	6.0	
Symmetry of Receiver Propagation Delay, t_{REC_PDF} - t_{REC_PDR}	t_{REC_SYM}	-2.0	—	2.0	
LIN PHYSICAL LAYER **RECEIVER CHARACTERISTICS WITH TIGHTEN LIMITS**[22] **33662S DEVICE**					
Propagation Delay and Symmetry[23]					µs
Propagation Delay of Receiver, t_{REC_PD} = MAX (t_{REC_PDR}, t_{REC_PDF})	$t_{REC\_PD\_S}$	—	—	5.0	
Symmetry of Receiver Propagation Delay, t_{REC_PDF} - t_{REC_PDR}	$t_{REC\_SYM\_S}$	-1.3	—	1.3	
LIN PHYSICAL LAYER **RECEIVER CHARACTERISTICS - LIN SLOPE 1.0 V/ns**[22] **33662S DEVICE**					
Propagation Delay and Symmetry[24]					µs
Propagation Delay of Receiver, $t_{REC\_PD\_FAST}$= MAX ($t_{REC\_PDR\_FAST}$, $t_{REC\_PDF\_FAST}$)	$t_{REC\_PD\_FAST}$	—	—	6.0	
Symmetry of Receiver Propagation Delay, $t_{REC\_PDF\_FAST}$ - $t_{REC\_PDR\_FAST}$	$t_{REC\_SYM\_FAST}$	-1.3	—	1.3	
SLEEP MODE AND WAKE-UP TIMINGS					
Sleep Mode Delay Time [25]					µs
after EN High to Low to INH High to Low with 100 µA load on INH	t_{SD}	50	—	91	
WAKE-UP TIMINGS					
Bus Wake-up Deglitcher (Sleep Mode) [26]	t_{WUF}	40	70	100	µs
EN Wake-up Deglitcher [27]					µs
EN High to INH Low to High	t_{LWUE}	—	—	15	
Wake-up Deglitcher [28]					µs
Wake state change to INH Low to High	t_{WF}	10	48	70	
TXD TIMING					
TXD Permanent Dominant State Delay[29]	t_{TXDDOM}	3.75	5.0	6.25	ms
FIRST DOMINANT BIT VALIDATION					
First dominate bit validation delay when device in Normal Mode[30]	t_{FIRST_DOM}	—	50	80	µs

Notes

20. V_{SUP} from 7.0 to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 8.
21. See Figure 12.
22. V_{SUP} from 7.0 to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 8.
23. See Figure 12
24. See Figure 13
25. See Figure 25 and 26
26. See Figure 16, 19, and Figure 20
27. See Figure 14, 17, Figure 21, Figure 25 and Figure 26
28. See Figure 15, 18, Figure 25 and Figure 26
29. The LIN is in recessive state and the receiver is still active.
30. See Figure 14, 17, 15, 18, 16, 19 and Figure 24

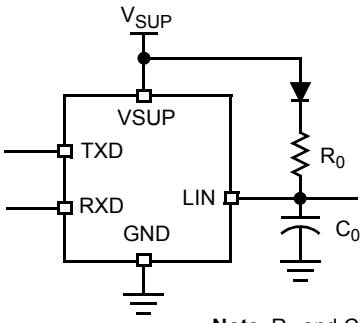
Table 6. Dynamic Electrical Characteristics (continued)

Characteristics under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
FAST BAUD RATE TIMING					
EN Low Pulse Duration to Enter in Fast Baud Rate using Toggle Function (31) EN High to Low and Low to High	t_1	—	—	45	µs
TXD Low Pulse Duration to Enter in Fast Baud Rate using Toggle Function (31)	t_2	12.5	—	—	µs
Delay Between EN Falling Edge and TXD Falling Edge to Enter in Fast Baud Rate Using Toggle Function (31)	t_3	12.5	—	—	µs
Delay Between TXD Rising Edge and EN Rising Edge to Enter in Fast Baud Rate Using Toggle Function (31)	t_4	12.5	—	—	µs
RXD Low Level duration after EN rising edge to validate the Fast Baud Rate entrance(31)	t_5	1.875		6.25	µs

Notes
31. See Figure 22 and 23

TIMING DIAGRAMS



Note R_0 and C_0: 1.0 kΩ/1.0 nF, 660 Ω/6.8 nF, and 500 Ω/10 nF.

Figure 8. Test Circuit for Timing Measurements

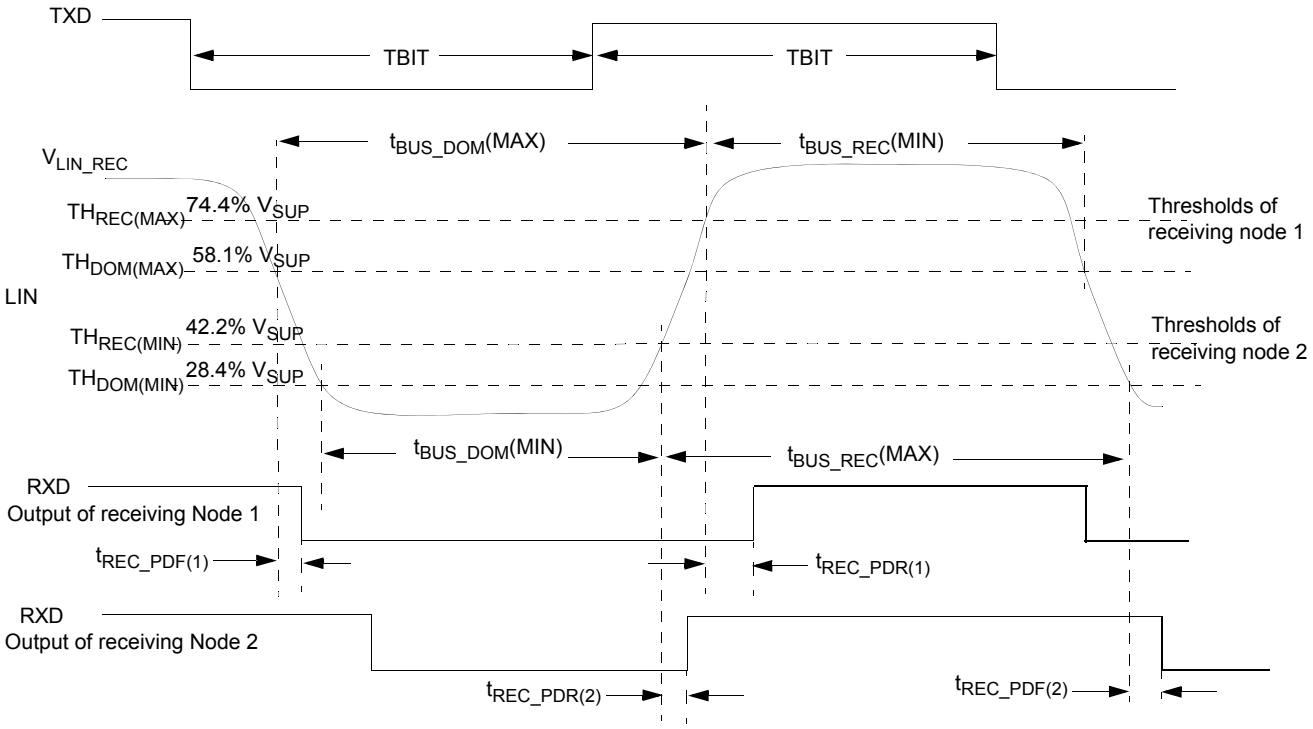


Figure 9. LIN Timing Measurements for Normal Baud Rate (33662L and 33662S)

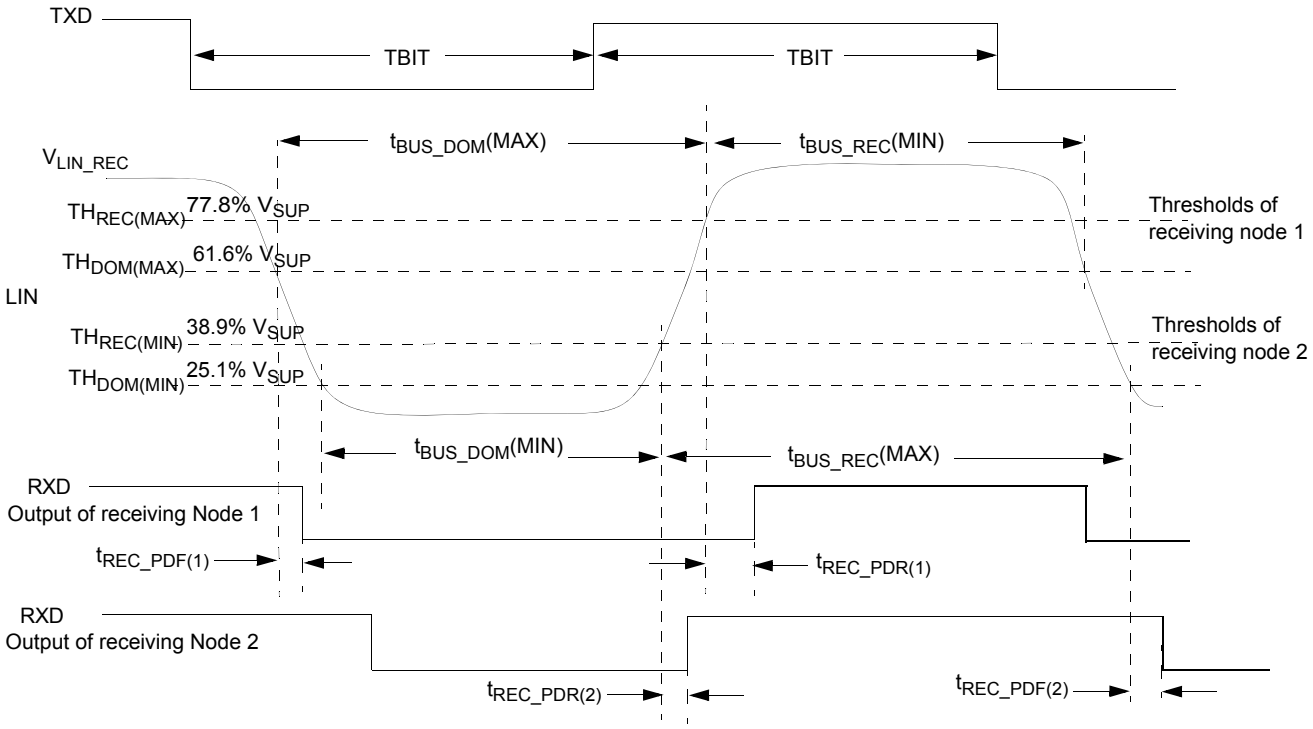


Figure 10. LIN Timing Measurements for Slow Baud Rate (33662J)

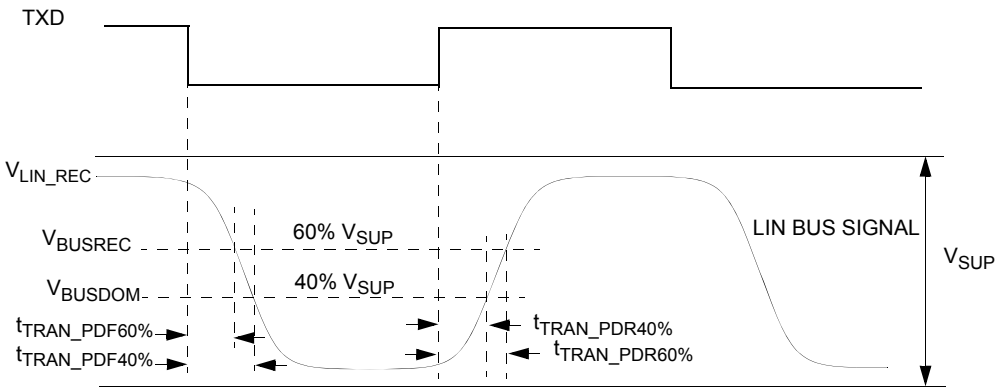


Figure 11. LIN Transmitter Timing for 33662S

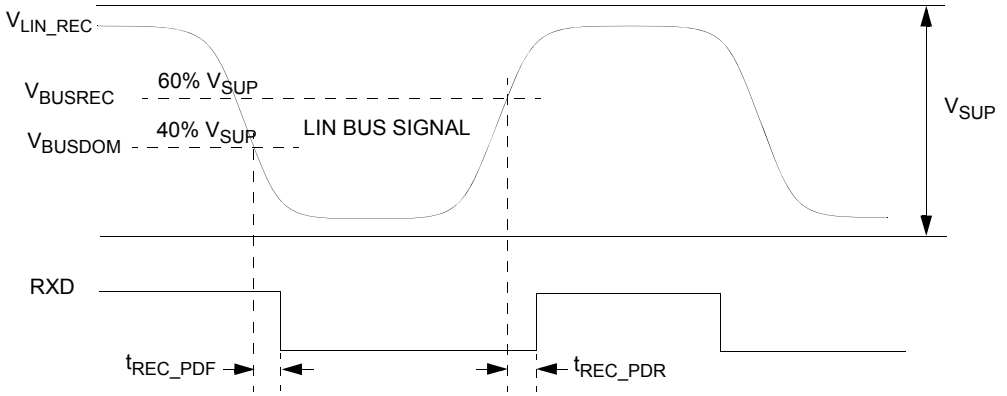


Figure 12. LIN Receiver Timing

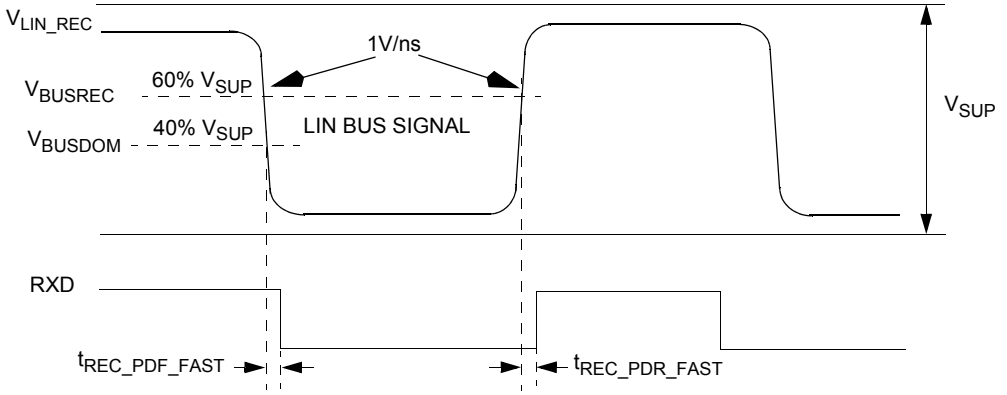


Figure 13. LIN Receiver Timing LIN slope 1V/ns

FUNCTIONAL DIAGRAMS

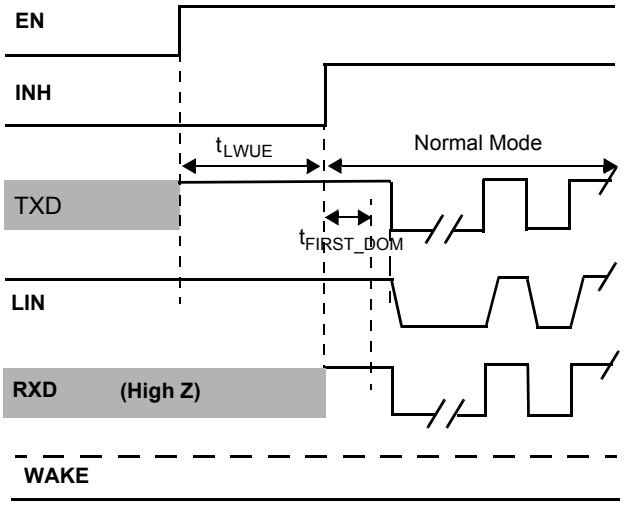


Figure 14. EN Pin Wake-up with TXD High

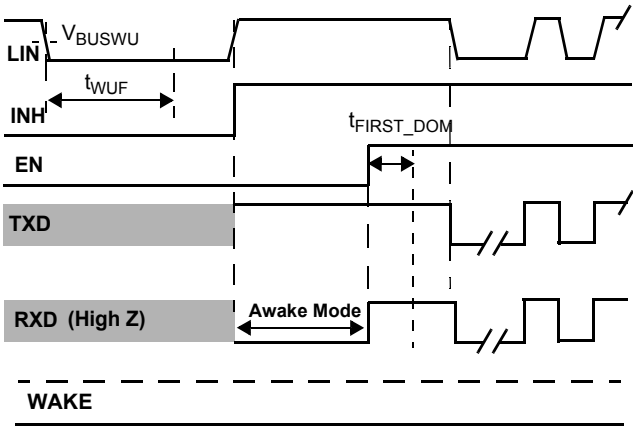


Figure 16. LIN Bus Wake-up with TXD High

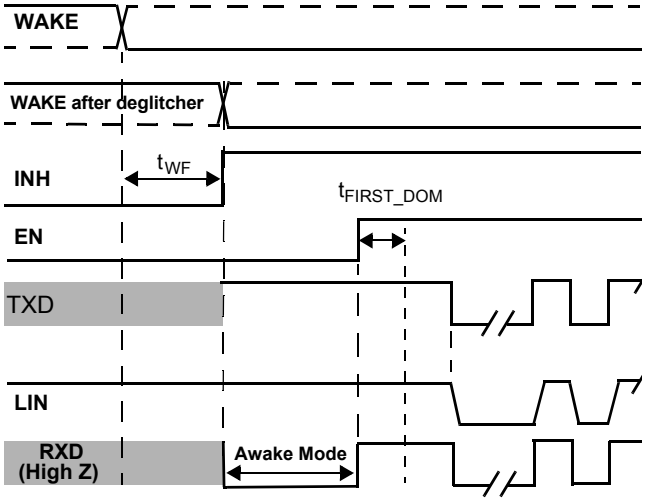


Figure 15. WAKE Pin Wake-up with TXD High

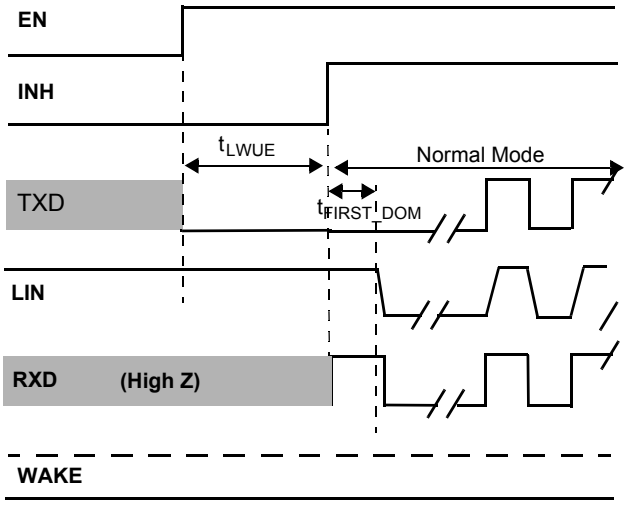


Figure 17. EN Pin Wake-up with TXD Low

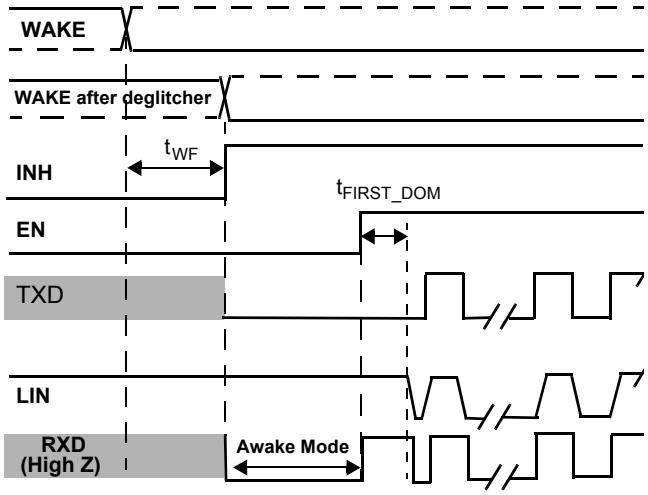


Figure 18. WAKE Pin Wake-up with TXD Low

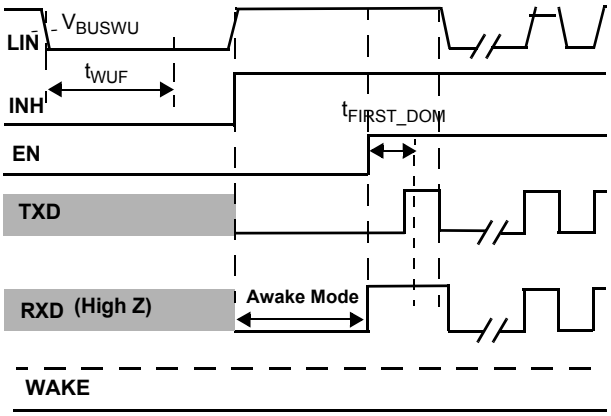


Figure 19. LIN Bus Wake-up with TXD Low

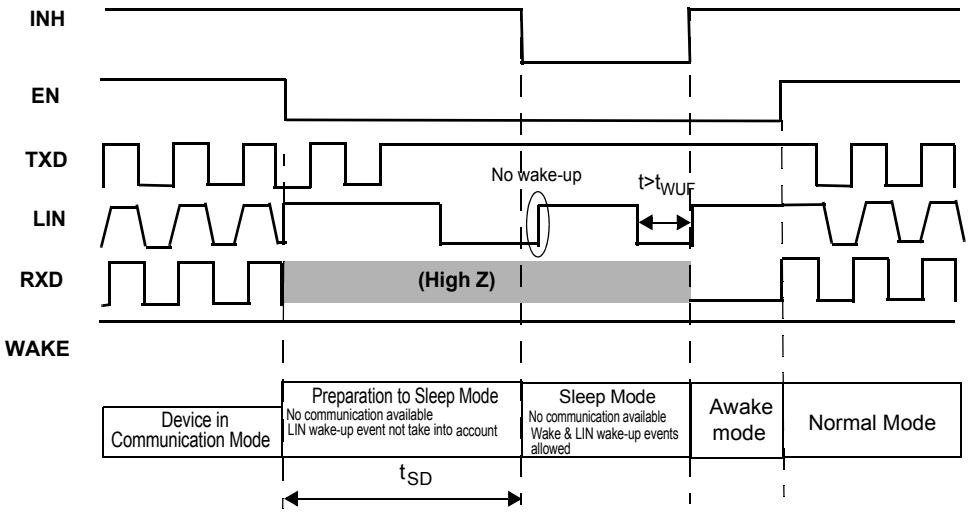


Figure 20. LIN Bus Wake-up with LIN bus in Dominant During the Preparation to Sleep Mode

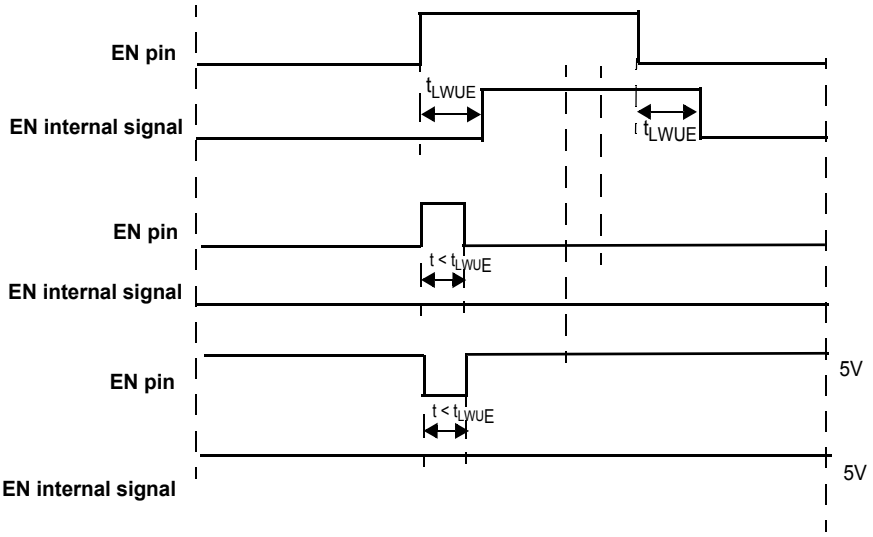


Figure 21. EN Pin Deglitcher

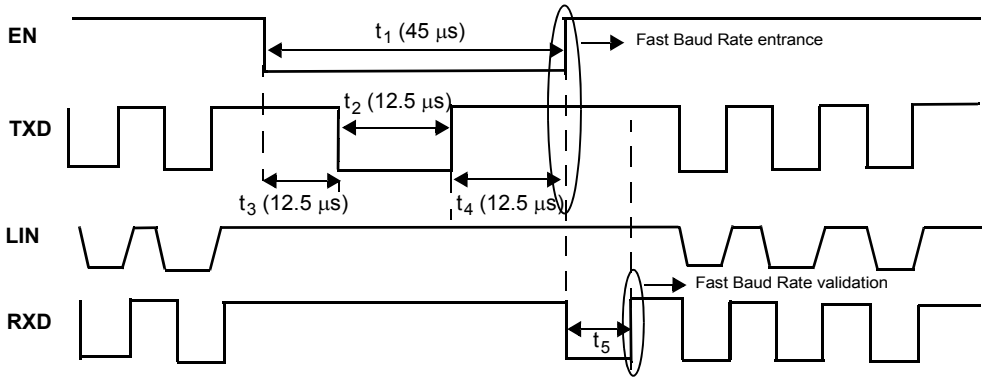


Figure 22. Fast Baud Rate Selection (Toggle Function)

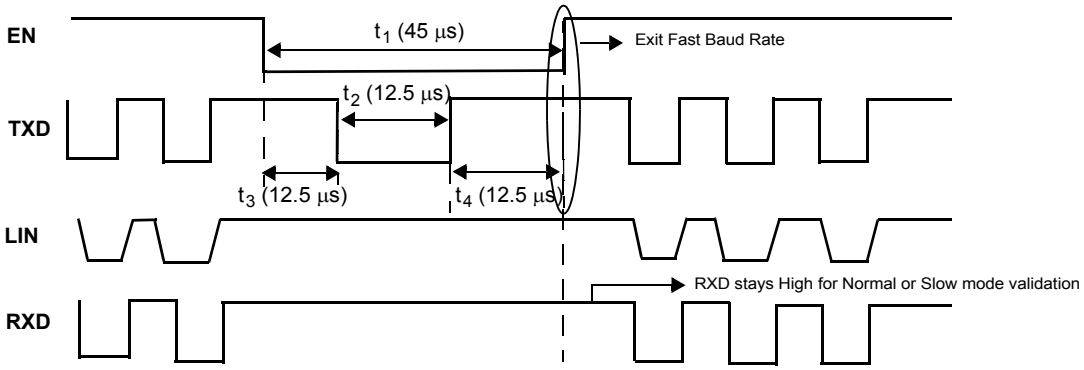


Figure 23. Fast Baud Rate Mode Exit (back to Normal or Slow slew rate)

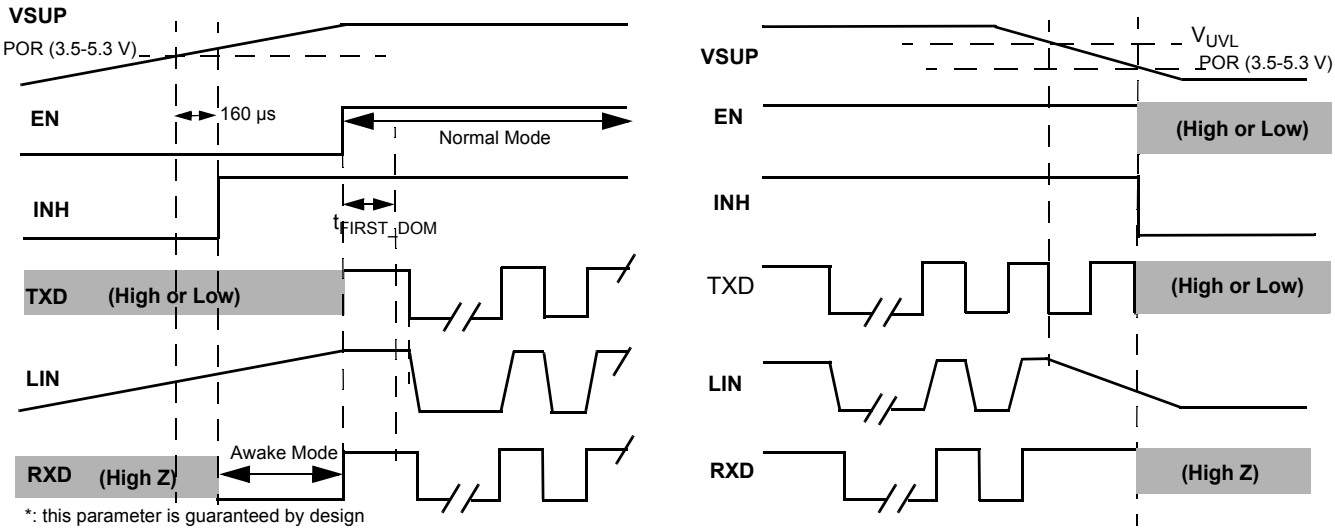


Figure 24. Power Up and Down Sequences

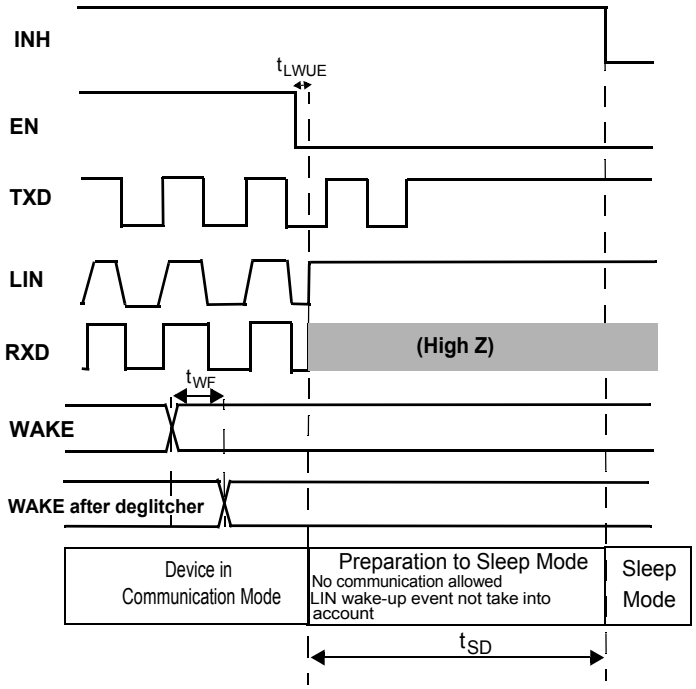


Figure 25. Sleep Mode Sequence

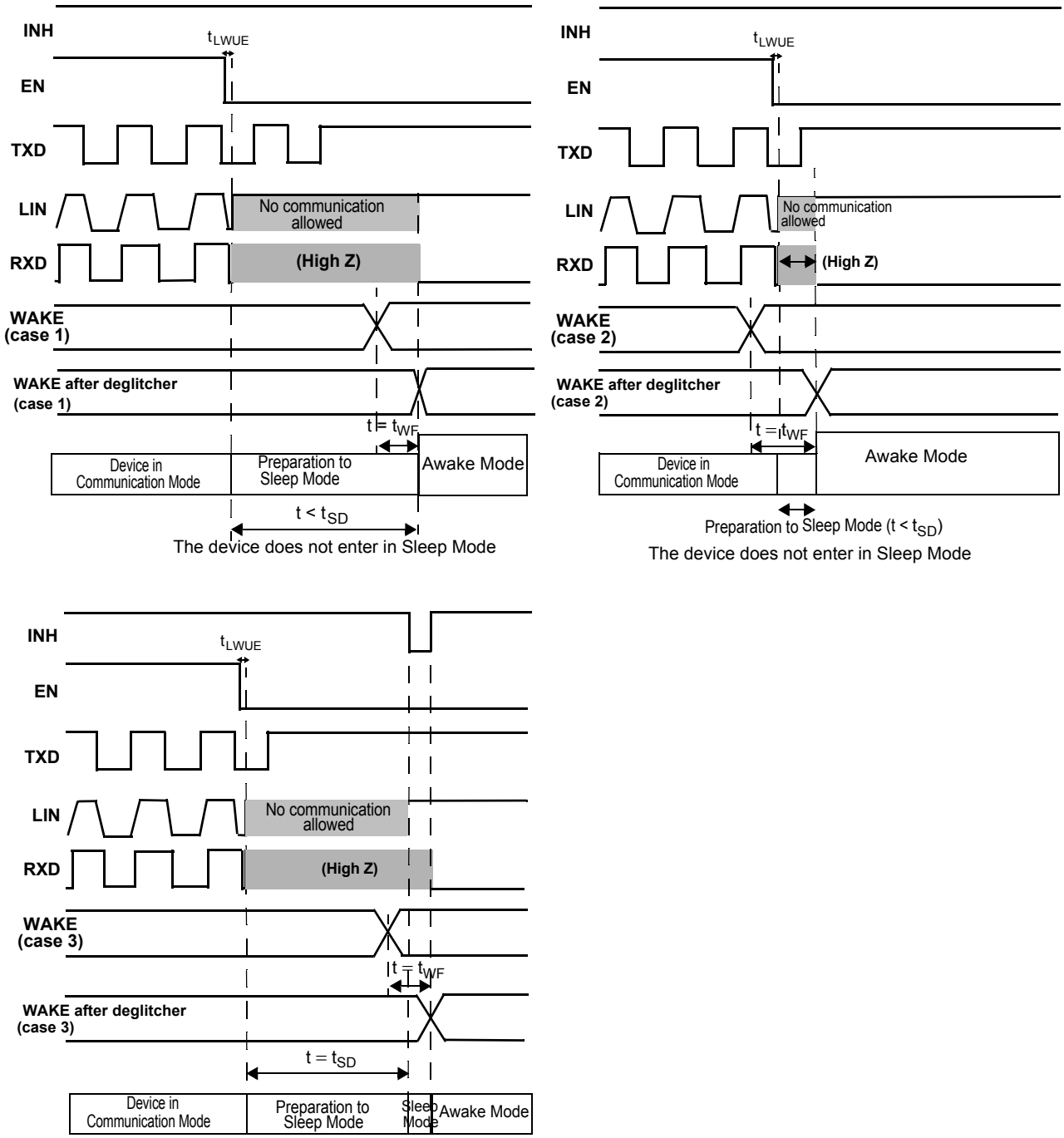


Figure 26. Examples of Sleep Mode Sequences

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33662L, 33662J, and 33662S are a physical layer component dedicated to automotive LIN sub-bus applications.

The 33662L and 33662S features include a 20 kbps baud rate and the 33662J a 10 kbps baud rate. They integrate fast baud rate for test and programming modes, excellent ESD robustness, immunity against disturbance, and radiated emission performance. They have safe behavior in case of a LIN bus short-to-ground, or a LIN bus leakage during low power mode.

Digital inputs are 5.0 and 3.3 V compatible without any external required components.

The INH output can be used to control an external voltage regulator, or to drive a LIN bus pull-up resistor.

FUNCTIONAL PIN DESCRIPTION

POWER SUPPLY PIN (VSUP)

The VSUP supply pin is the power supply pin for the 33662L, or 33662J, or 33662S. In an application, the pin is connected to a battery through a serial diode, for reverse battery protection. The DC operating voltage is from 7.0 to 18 V. This pin can sustain a standard automotive load dump condition up to 40 V. To avoid a false bus message, an undervoltage on VSUP disables the transmission path (from TXD to LIN) when V_{SUP} falls below 6.7 V. Supply current in Sleep mode is typically 6.0 μA.

GROUND PIN (GND)

In case of a ground disconnection at the module level, the 33662L, 33662J, and 33662S do not have significant current consumption on the LIN bus pin when in the recessive state.

LIN BUS PIN (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems, and is compliant to the LIN bus specification 1.3, 2.0, 2.1, and SAEJ2602-2.

The LIN interface is only active during Normal mode (See Figure 27).

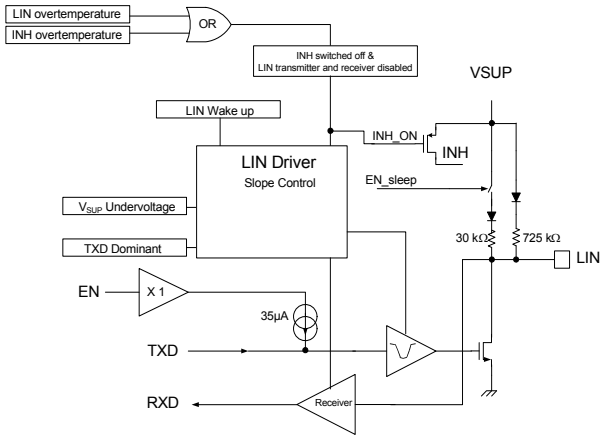


Figure 27. LIN Interface

Transmitter Characteristics

The LIN driver is a low side MOSFET with internal overcurrent thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated so no external pull-up components are required for the application in a slave node. An additional pull-up resistor of 1.0 kΩ must be added when the device is used in the master node.

The LIN pin exhibits no reverse current from the LIN bus line to V_{SUP}, even in the event of a GND shift or V_{SUP} disconnection. The 33662 is tested according to the application conditions (i.e. in normal mode and recessive state during communication).

The transmitter has a 20 kbps baud rate (Normal baud rate) for the 33662L and 33662S devices, or 10 kbps baud rate (Slow baud rate) for the 33662J device. As soon as the device enters in Normal mode, the LIN transmitter will be able to send the first dominant bit only after the t_{FIRST_DOM} delay. t_{FIRST_DOM} delay has no impact on the receiver. The receiver will be enabled as soon as the device enters in Normal mode.

Receiver Characteristics

The receiver thresholds are ratiometric with the device supply pin.

If the V_{SUP} voltage goes below the V_{SUP} undervoltage threshold (V_{UVL}, V_{UVH}), the bus enters into a recessive state even if communication is sent to TXD.

In case of LIN thermal shutdown, the transceiver and receiver are in recessive and INH turned off. When the temperature is below the T_{LINSD}, INH and LIN will be automatically enabled.

The Fast Baud Rate selection is reported by the RXD pin. Fast Baud Rate is activated by the toggle function (See Figure 22). At the end of the toggle function, just after EN rising edge, RXD pin is kept low for t_5 to flag the Fast Baud Rate entry (See Figure 22).

To exit the Fast Baud Rate and return in Normal or Slow baud rate, a toggle function is needed. At the end of the toggle function, the RXD pin stays high to signal Fast Baud Rate exit (See Figure 23). The device enters into Fast Baud Rate at room and hot temperature.

DATA INPUT PIN (TXD)

The TXD input pin is the MCU interface to control the state of the LIN output. When TXD is LOW (dominant), LIN output is LOW; when TXD is HIGH (recessive), the LIN output transistor is turned OFF. TXD pin thresholds are 3.3 V and 5.0 V compatible.

This pin has an internal pull-up current source to force the recessive state if the input pin is left floating.

If the pin stays low (dominant sate) more than 5.0 ms (typical value), the LIN transmitter goes automatically into recessive state.

DATA OUTPUT PIN (RXD)

RXD output pin is the MCU interface, which reports the state of the LIN bus voltage.

In Normal or Slow baud rate, LIN HIGH (recessive) is reported by a high voltage on RXD; LIN LOW (dominant) is reported by a low voltage on RXD.

The RXD output structure is a tristate output buffer (See Figure 28).

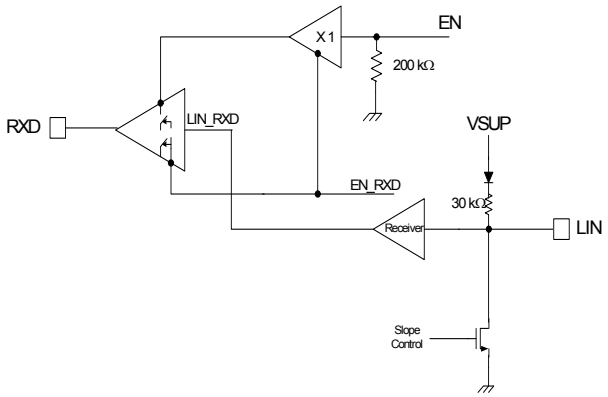


Figure 28. RXD Interface

The RXD output pin is the receiver output of the LIN interface. The low level is fixed. The high level is dependent on EN voltage. If EN is set at 3.3 V, RXD V_{OH} is 3.3 V. If EN is set at 5.0 V, RXD V_{OH} is 5.0 V.

In Sleep mode, RXD is high-impedance. When a wake-up event is recognized from the WAKE pin or from the LIN bus pin, RXD is pulled LOW to report the wake-up event. An external pull-up resistor may be needed.

ENABLE INPUT PIN (EN)

EN input pin controls the operation mode of the interface. If EN = 1, the interface is in Normal mode, TXD to LIN after t_{FIRST_DOM} delay and LIN to RXD paths are both active. EN pin thresholds are 3.3 V and 5.0 V compatible. RXD V_{OH} level follows EN pin high level. The device enters the Sleep mode by setting EN LOW for a delay higher than t_{SD} (70 µs typ. value) and if the WAKE pin state doesn't change during this delay (see Figure 25).

A combination of the logic levels on the EN and TXD pins allows the device to enter into the Fast Baud Rate mode of operation (see Figure 22).

INHIBIT OUTPUT PIN (INH)

The INH output pin is connected to an internal high side power MOSFET. The pin has two possible main functions. It can be used to control an external switchable voltage regulator having an inhibit input. It can also be used to drive the LIN bus external resistor in the master node application, thanks to its high drive capability. This is illustrated in Figure 30 and 31.

In Sleep mode, INH is turned OFF. If a voltage regulator inhibit input is connected to INH, the regulator will be disabled. If the master node pull-up resistor is connected to INH, the pull-up resistor will be unpowered and left floating.

In case of a INH thermal shutdown, the high side is turned off and the LIN transmitter and receiver are in recessive state.

An external 10 to 100 pF capacitor on INH pin is advised in order to improve EMC performances.

WAKE INPUT PIN (WAKE)

The WAKE pin is a high voltage input used to wake-up the device from the Sleep mode. WAKE is usually connected to an external switch in the application.

The WAKE pin has a special design structure and allows wake-up from both HIGH to LOW or LOW to HIGH transitions. When entering into Sleep mode, the device monitors the state of the WAKE pin and stores it as a reference state. The opposite state of this reference state will be the wake-up event used by the device to enter again into Normal mode.

If the Wake pin state changes during the Sleep mode Delay Time (t_{SD}) or before EN goes low with a deglitcher lower than t_{WF}, the device will not enter the Sleep mode, but will go into Awake mode (See Figure 26).

An internal filter is implemented to avoid a false wake-up event due to parasitic pulses (See Figure 15 and 18). WAKE pin input structure exhibits a high-impedance, with extremely low input current when voltage at this pin is below 27 V. Two serial resistors should be inserted in order to limit the input current mainly during transient pulses and ESD. The total recommended resistor value is 33 kΩ. An external 10 to 100 nF capacitor is advised for better EMC and ESD performances.

Important The WAKE pin should *not* be left open. If the wake-up function is not used, WAKE should be connected to ground to avoid a false wake-up.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

As described below and depicted in Figure 29 and Table 7, the 33662L, 33662J, and 33662S have two operational modes, Normal and Sleep. In addition, there are two transitional modes: Awake mode and Preparation to Sleep mode. The Awake mode allows the device to go into Normal mode. The Preparation to Sleep mode allows the device to go into Sleep mode.

NORMAL OR SLOW BAUD RATE

In the Normal mode, the LIN bus can transmit and receive information.

The 33662L and 33662S (20 kbps) have a slew rate and timing compatible with Normal Baud Rate and LIN protocol specification 1.3, 2.0, and 2.1.

The 33662J (10 kbps) has a slew rate and timing compatible with Low Baud Rate.

From Normal mode, the three devices can enter into Fast Baud Rate (Toggle function).

FAST BAUD RATE

In Fast Baud Rate, the slew rate is around 10 times faster than the Normal Baud Rate. This allows very fast data transmission (>100 kbps) -- for instance, for electronic control unit (ECU) tests and microcontroller program download. The bus pull-up resistor might be adjusted to ensure a correct RC time constant in line with the high baud rate used.

Fast Baud Rate is entered via a special sequence (called toggle function) as follows:

1- EN pin set LOW while TXD is HIGH

2- TXD stays HIGH for 12.5 µs min

3- TXD set LOW for 12.5 µs min

4- TXD pulled HIGH for 12.5 µs min

5- EN pin set LOW to HIGH while TXD still HIGH

The device enters into the Fast Baud Rate if the delay between Step 1 to Step 5 is 45 µs maximum. The toggle function is described in Figures 22. Once in Fast Baud Rate, the same toggle function just described previously is used to bring the device back into Normal Baud Rate.

Fast Baud Rate selection is reported to the MCU by RXD pin. Once the device enters in this Fast Baud Rate, the RXD pin goes at low level for t_5. When the device returns in Normal Baud Rate with the same toggle function, the RXD pin stays high. Both sequences are illustrated in Figures 22 and 23.

PREPARATION TO SLEEP MODE

To enter the Preparation to Sleep mode, EN must be low for a delay higher than t_{LWUE}.

If the WAKE pin state doesn't change during t_{SD} and t_{LWUE} then the 33662 goes into Sleep mode.

If the WAKE pin state changes during t_{SD} and if t_{WF} is reached after end of t_{SD} then the device goes into Sleep mode after the end of t_{SD} timing.

If the WAKE pin state changes during t_{SD} and t_{WF} delay has been reached before the end of t_{SD} then the device goes into Awake mode.

If the WAKE pin state changes before t_{SD} and the delay t_{WF} ends during t_{SD} then the device goes into Awake mode.

If EN goes high for a delay higher than t_{LWUE}, the 33662 returns to Normal mode.

SLEEP MODE

To enter into Sleep mode, EN must be low for a delay longer than t_{SD} and the Wake pin must stay in the same state (High or Low) during this delay.

The device conditions to not enter in Sleep mode but enter in Awake mode are detailed in the Preparation into Sleep mode chapter. See Figure 26.

In Sleep mode, the transmission path is disabled and the device is in Low Power mode. Supply current from V_{SUP} is very low (6.0 µA typical value). Wake-up can occur from LIN bus activity, from the EN pin and from the WAKE input pin. If during the preparation to Sleep mode delay (t_{SD}), the LIN bus goes low due to LIN network communication, the device still enters into the Sleep mode. The device can be awakened by a recessive to dominant start, followed by a dominant to recessive state after $t > t_{WUF}$.

After a Wake-up event, the device enters into Awake mode.

In the Sleep mode, the internal 725 kOhm pull-up resistor is connected and the 30 kOhm is disconnected.

DEVICE POWER-UP (Awake Transitional Mode)

At power-up (V_{SUP} rises from zero), when V_{SUP} is above the Power On Reset voltage, the device automatically switches after a 160 µs delay time to the Awake transitional mode. It switches the INH pin to a HIGH state and RXD to a LOW state. See Figure 24.

DEVICE WAKE-UP EVENTS

The 33662L, 33662J, and 33662S can be awakened from Sleep mode by three wake-up events:

- Remote wake-up via LIN bus activity
- Via the EN pin
- Toggling the WAKE pin

Remote Wake from LIN Bus (Awake Transitional Mode)

The device is awakened by a LIN dominant pulse longer than t_{WUF}. Dominant pulse means: a recessive to dominant transition, wait for $t > t_{WUF}$, then a dominant to recessive

transition. This is illustrated in Figure 16 and 19. Once the wake-up is detected (during the dominant to recessive transition), the device enters into Awake mode, with INH HIGH and RXD pulled LOW.

Once in the Awake mode, the EN pin has to be set to 3.3 V or 5.0 V (depending on the system) to enter into Normal mode. Once in Normal mode, the device has to wait t_{first_dom} delay before transmitting the first dominant bit.

Wake-up from EN pin

The device can be waked-up by a LOW to HIGH transition of the EN pin. When EN is switched from LOW to HIGH and stays HIGH for a delay higher than t_{LWUE}, the device is awakened and enters into Normal mode. See Figure 14 and 17. Once in Normal mode, the device has to wait t_{FIRST_DOM} delay before transmitting the first dominant bit.

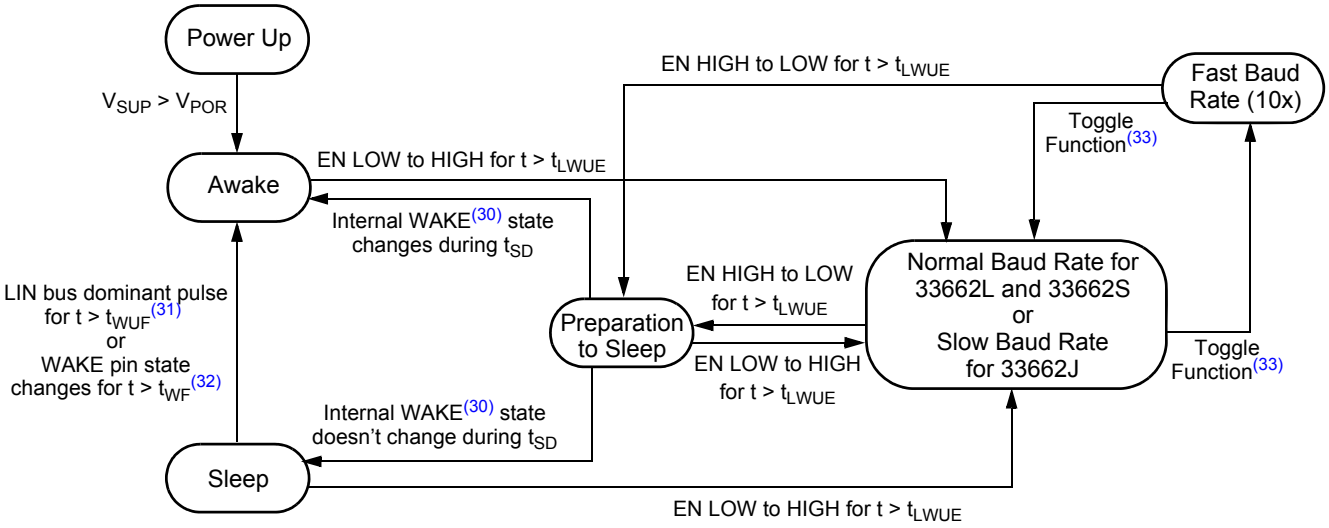
Wake-up from WAKE Pin (Awake Transitional Mode)

Just before entering the Sleep mode, the WAKE pin state is stored. A change in the level longer than the deglitcher time (70 µs maximum) will generate a wake-up, and the device enters into the Awake Transitional mode, with INH HIGH and RXD pulled LOW. See Figure 15 and 18. The device goes into Normal mode when EN is switched from LOW to HIGH and stays HIGH for a delay higher than t_{LWUE}. Once in Normal mode, the device has to wait t_{FIRST_DOM} delay before transmitting the first dominant bit.

FAIL-SAFE FEATURES

The table below describes the 33662 protections.

BLOCK	FAULT	FUNCTIONAL MODE	CONDITION	RESPONSE	RECOVERY CONDITION	RECOVERY FUNCTIONALITY MODE
Power Supply	Power on Reset (POR)	All modes	V_{SUP} < 3.5 V (min) then power up	No internal supplies	Condition gone	Device goes in Awake mode whatever the previous device mode
INH	INH Thermal Shutdown	Normal, Awake & Preparation to Sleep modes	Temperature > 160 °C (typ)	INH high side turned off. LIN transmitter and receiver in recessive state	Condition gone	Device returns in same functional mode
LIN	V_{SUP} undervoltage	Normal	V_{SUP} < V_{UVL}	LIN transmitter in recessive state	Condition gone	Device returns in same functional mode
	TXD Pin Permanent Dominant		TXD pin low for more than 5.0 ms (typ)	LIN transmitter in recessive state	Condition gone	Device returns in same functional mode
	LIN Thermal Shutdown	Normal mode	Temperature > 160 °C (typ)	LIN transmitter and receiver in recessive state INH high side turned off	Condition gone	Device returns in same functional mode



Notes

32. Internal WAKE is the WAKE signal filtered by t_{WF} (WAKE deglitcher)
33. See Figure 15 and Figure 18
34. See figures Figure 14 and Figure 17
35. The Toggle Function is guaranteed at ambient and hot temperature

Figure 29. Operational and Transitional Modes State Diagram

Table 7. Explanation of Operational and Transitional Modes State Diagram

Operational/ Transitional	LIN	INH	EN	TXD	RXD
Sleep	Recessive state, driver off with 725 kΩ pull-up	OFF (low)	LOW	X	High-impedance.(36) HIGH if external pull-up to V_{DD}
Awake	Recessive state, driver off. 725 kΩ pull-up active	ON (high)	LOW	X	LOW. If external pull-up, HIGH-to-LOW transition reports wake-up
Preparation to Sleep mode	Recessive state, driver off with 725 kΩ pull-up	ON (high)	LOW	X	High-impedance. HIGH if external pull-up to V_{DD}
Normal mode	Driver active. 30 kΩ pull-up active Normal Baud Rate for 33662L and 33662S Slow Baud Rate for 33662J Fast Baud Rate (> 100 kbps) for 33662L, 33662S, & 33662J	ON (high)	HIGH	LOW to drive LIN bus in dominant HIGH to drive LIN bus in recessive	Report LIN bus state: • Low LIN bus dominant • High LIN bus recessive

X = Don't care.

Notes

36. Only applies to 33662B. The 33662 will have a leakage current of typically 95 μA if a pull-up resistor is implemented.

COMPATIBILITY WITH LIN1.3

Following the Consortium LIN specification Package, Revision 2.1, November 24, 2006, Chapter 1.1.7.1 Compatibility with LIN1.3, page 15.

The LIN 2.1 physical layer and is backward compatible with the LIN 1.3 physical layer, but not the other way around. The LIN 2.1 physical layer sets harder requirements, i.e. a node using the LIN 2.1 physical layer can operate in a LIN 1.3 cluster.

TYPICAL APPLICATIONS

The 33662 can be configured for several applications. Figure 30 and 31 show master and slave node applications. An additional pull-up resistor of 1.0 kΩ in series with a diode between the INH and LIN pins must be added when the device is used in the master node.

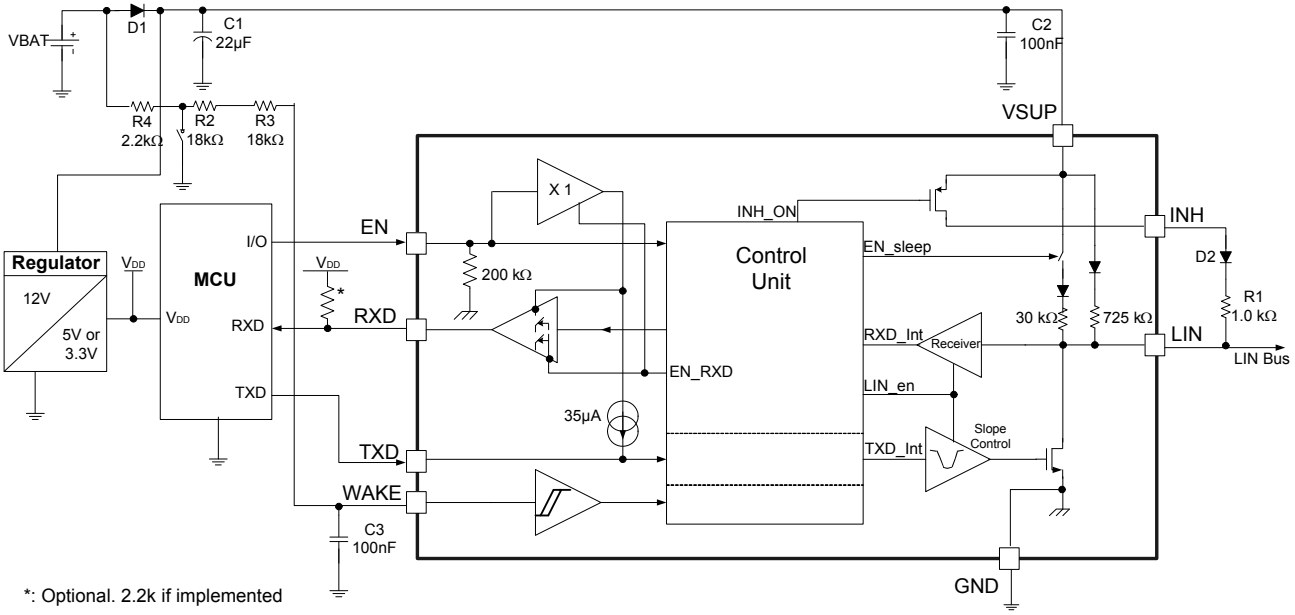


Figure 30. Master Node Typical Application

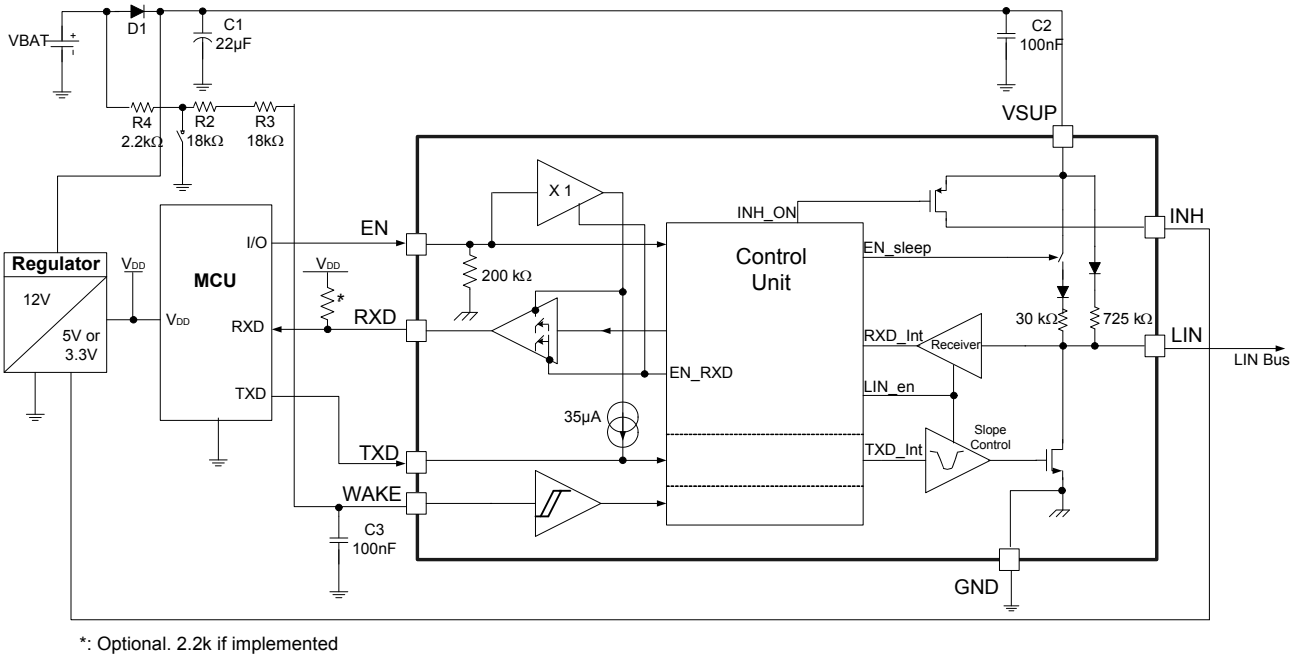
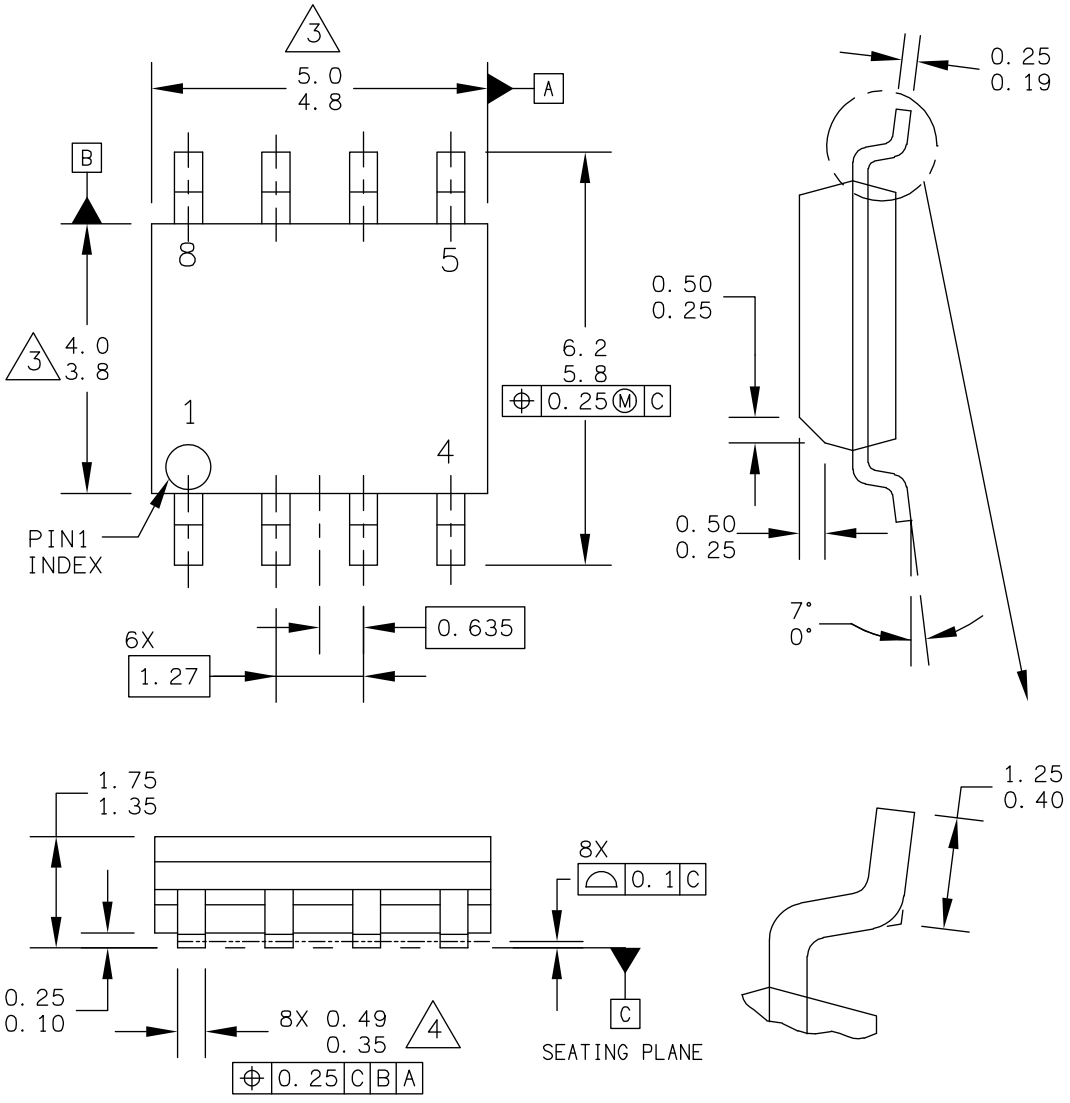


Figure 31. Slave Node Typical Application

PACKAGING

PACKAGE DIMENSIONS

Important For the most current revision of the package, visit www.Freescale.com and do a keyword search on the 98A drawing number below.



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TITLE: 8LD SOIC NARROW BODY	DOCUMENT NO: 98ASB42564B	REV: V
	CASE NUMBER: 751-07	20 NOV 2007
	STANDARD: JEDEC MS-012AA	

EF SUFFIX
8-PIN
98ASB42564B
REVISION V

33662

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 8LD SOIC NARROW BODY	DOCUMENT NO: 98ASB42564B	REV: V
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	STANDARD: JEDEC MS–012AA	

EF SUFFIX
8-PIN
98ASB42564B
REVISION V

33662

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
3.0	8/2011	Initial release
4.0	9/2011	Changed the PC part numbers in the Ordering Information Table to MC
5.0	1/2014	• Added MC33662BLEF, MC33662BJEF, and MC33662BSEF to the ordering information. • Updated Device Variations table • Changed LIN dominant level with 500 Ω, 680 Ω and 1.0 kΩ load on the LIN bus from 0.3 to 0.25 • Changed LIN Wake-up Threshold from Sleep Mode from 5.0 to 5.3 • MC33662LEF/MC33662SEF/MC33662JEF INH pin HBM level 8.0 KV removed to reflect performance
6.0	1/2014	• Corrected MC33662BLEF, MC33662BJEF, and MC33662BSEF to PC in the ordering information. • Minor corrections to format.
7.0	1/2014	• Changed MC33662BLEF, MC33662BJEF, and MC33662BSEF to MC in the ordering information. Now qualified.

RoHS

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