MC33664

Isolated network high-speed transceiver

Rev. 5.0 — 27 August 2024 **Product data sheet**

1 General description

The MC33664 is a SMARTMOS transceiver physical layer transformer driver designed to interface a microcontroller conveniently to a high speed isolated communication network. MCU serial peripheral interface (SPI) data bits are directly converted to pulse bit information and transferred to the bus network.

Slave response messages use the same structure to send pulse bit information to the MC33664, which is converted and sent back to the MCU as a SPI bit stream.

2 Features and benefits

- 2.0 Mbit/s isolated network communication rate
- Dual SPI architecture for message confirmation
- Robust conducted and radiated immunity with wake-up
- 3.3 V and 5.0 V compatible logic thresholds
- Low sleep mode current with automatic bus wake-up
- Ultra-low radiated emissions

3 Applications

- Automotive communication network
- Industrial communication network
- Utility vehicle battery systems
- Forklift/mining battery systems
- Battery backup systems

4 Ordering information

Table 1. Ordering information

Type number	Package			
	Name	Description	T_{amb} [°C]	Version
MC33664ATL1EG[1]	SO16	plastic small outline package; 16 leads; 1.27 mm pitch; body 9.9 mm × 3.9 mm × 1.75 mm	−40 to +125	SOT109-5

[1] To order parts in tape and reel, add R2 suffix to the part number.

5 Application circuit

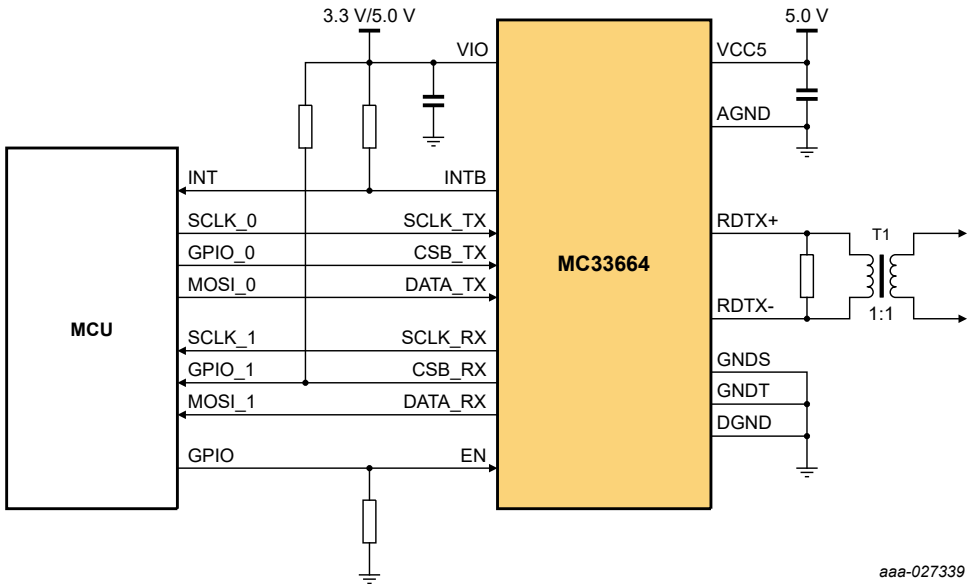


Figure 1. Typical application circuit

6 Internal block diagram

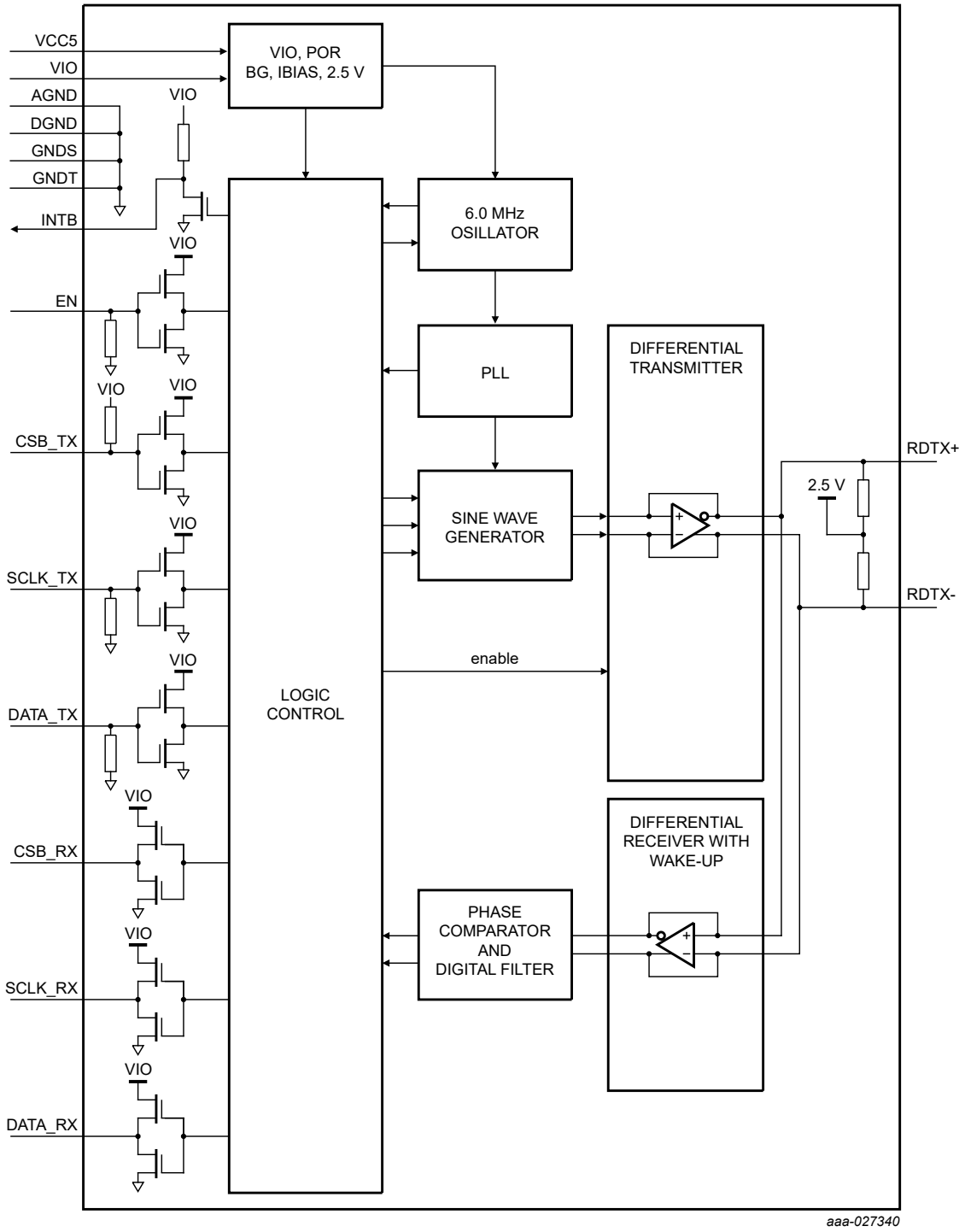


Figure 2. Simplified internal block diagram

7 Pinning information

7.1 Pinning

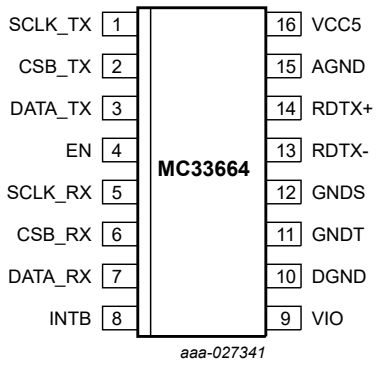


Figure 3. Pin configuration for SO16

7.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
SCLK_TX	1	input	SPI transmit clock from the microcontroller to the MC33664
CSB_TX	2	input	SPI transmit chip select from the microcontroller to the MC33664
DATA_TX	3	input	SPI transmit data from the microcontroller to the MC33664
EN	4	input	enable control pin for the MCU to control the MC33664 to Sleep mode or Normal mode
SCLK_RX	5	output	message receive SPI clock output to the microcontroller
CSB_RX	6	output	message receive SPI chip select output to the microcontroller
DATA_RX	7	output	message receive SPI data output to the microcontroller
INTB	8	output	digital interrupt pin used to trigger MCU wake-ups
VIO	9	power	digital 3.3 V/5.0 V power to the IC
DGND	10	ground	digital ground
GNDT	11	ground	terminate to ground
GNDS	12	ground	substrate ground; terminate to ground
RDTX-	13	I/O	transformer communication bi-directional bus
RDTX+	14	I/O	transformer communication bi-directional bus
AGND	15	ground	analog ground
VCC5	16	input	5.0 V input supply

8 Ratings and operating requirements relationship

The operating voltage range pertains to the VCC5 and VIO pins referenced to the AGND and DGND pins.

Table 3. Ratings versus operating requirements

Fatal range	Lower limited operating range	Normal operating range	Upper limited operating range	Fatal range
V_{PWR} < −0.3 V **Permanent failure may occur**	4.5 V ≤ V_{CC5} ≤ 4.75 V **no permanent failure, but IC functionality is not guaranteed**	4.75 V ≤ V_{CC5} ≤ 5.5 V 3.1 V ≤ V_{IO} ≤ 5.5 V **100 % functional**	5.5 V ≤ V_{CC5} ≤ 7.0 V 5.5 V ≤ V_{IO} ≤ 7.0 V	7.0 V ≤ V_{CC5} 7.0 V ≤ V_{IO} **permanent failure may occur**
	0 V ≤ V_{CC5} ≤ 4.5 V 0 V ≤ V_{IO} ≤ 3.1 V **reset**			
	handling range; no permanent failure			

9 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

All voltages are respect to reference ground (AGND and DGND) unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IO}	supply input voltage		−0.3	+7.0	V
V_{CC5}	supply input voltage		−0.3	+7.0	V
EN	digital enable pin for Sleep or Normal mode		−0.3	V_{IO} + 0.3	V
RDTX+, RDTX−	communication bus		−10	+10	V
INTB	interrupt pin		−0.3	V_{IO} + 0.3	V
SCLK_TX, SCLK_RX, CSB_TX, CSB_RX, DATA_TX, DATA_RX	serial peripheral interface communication ports		−0.3	V_{IO} + 0.3	V
V_{ESD}	electrostatic discharge voltage	human body model (HBM) [1]	±2000	-	V
		charge device model (CDM)	±500	-	V
		CDM corner pins	±750	-	V
		machine model (MM)	±200	-	V
		RDTX+, RDTX−; HBM [1]	±4000	-	V
		RDTX+, RDTX−; MM	±200	-	V

[1] Electrostatic discharge (ESD) testing is performed in accordance with the HBM (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).

10 Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
T_{amb}	ambient temperature		−40	+125	°C
T_j	junction temperature	[1]	−40	+150	°C
T_{stg}	storage temperature		−55	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	[2] [3]	-	260	°C
$R_{th(j-a)}$	thermal resistance from junction to ambient	single layer (1s) [4]	-	125	°C/W
$R_{th(j-pcb)}$	thermal resistance from junction to printed-circuit board	multi layer (2s2p) [5]	-	62	°C/W

[1] Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[2] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
[3] Package reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For peak package reflow temperature and moisture sensitivity levels (MSL), go to http://www.nxp.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx)], and review parametric.
[4] Per SEMI G38-87 and JEDEC standard JESD51-2 with the single-layer board horizontal.
[5] Indicates the maximum thermal resistance between the die and the exposed pad surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

11 Characteristics

Table 6. Characteristics

Characteristic noted under conditions 4.75 V ≤ V_{CC5} ≤ 5.5 V, 3.1 V ≤ V_{IO} ≤ 5.5 V, −40 °C ≤ T_{amb} ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at V_{CC5} = 5.0 V, V_{IO} = 3.3 V/5.0 V, T_{amb} = 25 °C and device operating under nominal conditions unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power supply VCC5						
V_{CC5}	supply voltage	fully operational	4.75	—	5.5	V
		limited operation	4.5	—	4.75	V
$I_{VCC5(NORMAL)}$	supply current	Normal mode; EN = 1; continuous transmit; 50 Ω load	15	40	70	mA
		Normal mode; EN = 1; continuous receive	2.5	3.0	3.8	mA
$I_{VCC5(SLEEP)}$	supply current	Sleep mode; EN = 0; INTB = 5.0 V	10	30	50	µA
$VCC5_{UV}$	VCC5 undervoltage POR threshold		4.0	—	4.5	V
$VCC5_{UV\_FLT}$	VCC5 undervoltage POR filter		1.0	2.5	5.7	µs
$VCC5_{UVHYS}$	VCC5 undervoltage POR hysteresis		50	100	175	mV
Power supply VIO						
V_{IO}	supply voltage		3.1	—	5.5	V
VIO_{UV}	VIO undervoltage POR threshold		2.2	—	3.1	V

Table 6. Characteristics...*continued*

Characteristic noted under conditions 4.75 V ≤ V_{CC5} ≤ 5.5 V, 3.1 V ≤ V_{IO} ≤ 5.5 V, −40 °C ≤ T_{amb} ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at V_{CC5} = 5.0 V, V_{IO} = 3.3 V/5.0 V, T_{amb} = 25 °C and device operating under nominal conditions unless otherwise noted.

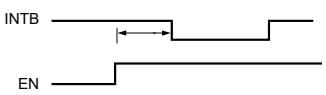
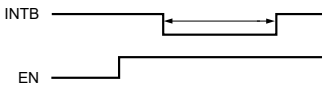
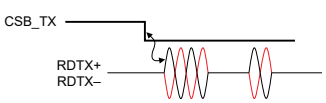
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIO_{UV_FLT}	VIO undervoltage POR filter		1.0	2.5	5.7	µs
VIO_{UVHYS}	VIO undervoltage POR hysteresis		50	100	150	mV
$I_{VIO(SLEEP)}$	VIO sleep current	EN = 0; INTB = 1	0.1	—	4.5	µA
$I_{VIO(NORMAL)}$	VIO Normal mode current	EN = 1; continuous communication; SPI_1 open	0.1	1.0	2.0	mA
Logic transmit EN, CSB_TX, SCLK_TX, DATA_TX						
V_{IH}	HIGH-level input voltage		1.7	—	V_{IO} + 0.3	V
V_{IL}	LOW-level input voltage		—	—	0.95	V
V_{hys}	hysteresis voltage		75	150	475	mV
R_{pd}	pull-down resistance	EN, SCLK_TX, DATA_TX	50	100	200	kΩ
R_{pu}	pull-up resistance	CSB_TX	50	100	200	kΩ
t_{READY}	Sleep mode to Normal mode	EN LOW to HIGH transition to device ready to transmit	—	—	100	µs
$t_{INTB\_PULSE\_DELAY}$	EN LOW to HIGH transition to INTB verification pulse 		—	—	100	µs
t_{INTB_PULSE}	INTB verification pulse duration 		—	100	—	µs
f_{SCLK_TX}	SPI_0 frequency	SCLK_TX	1.9	2.0	2.1	MHz
a	SCLK_TX HIGH	see Figure 4	240	250	260	ns
b	SCLK_TX LOW	see Figure 4	240	250	260	ns
e	SCLK_TX to CSB_TX	see Figure 4	—	250	—	ns
L	CSB_TX to start of message 		—	—	1.1	µs

Table 6. Characteristics...*continued*

Characteristic noted under conditions 4.75 V ≤ V_{CC5} ≤ 5.5 V, 3.1 V ≤ V_{IO} ≤ 5.5 V, −40 °C ≤ T_{amb} ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at V_{CC5} = 5.0 V, V_{IO} = 3.3 V/5.0 V, T_{amb} = 25 °C and device operating under nominal conditions unless otherwise noted.

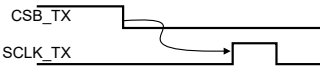
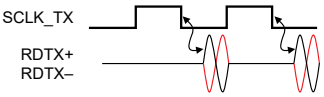
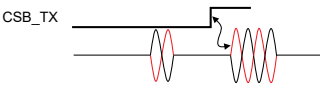
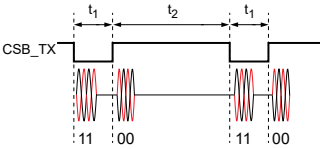
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f	falling edge of CSB_TX to rising edge SCLK_TX 	see Figure 4	1.75	—	—	µs
t_{RDTX_DLY}	propagation delay SCLK_TX LOW to sine out 	[1]	—	80	150	ns
g	SCLK_TX LOW to CSB_TX HIGH	see Figure 4	600	—	—	ns
c	DATA_TX to SCLK_TX setup	see Figure 4	40	—	—	ns
d	DATA_TX hold	see Figure 4	40	—	—	ns
$t_{CSB\_TX\_HIGH\_EOM}$	propagation delay CSB_TX LOW to HIGH to end of message 	[1]	—	—	150	ns
t_1	CSB_TX wake-up pulse sequence timing 	CSB_TX LOW period	20	21	24	µs
t_2		CSB_TX HIGH period	500	600	700	µs
h	time between consecutive transmit messages	see Figure 4	1.0	3.0	—	µs
Logic receive pins (CSB_RX, SCLK_RX, DATA_RX)						
V_{OH}	HIGH-level output voltage	I_{OH} = −2.0 mA; V_{IO} = 3.1 V	V_{IO} − 0.4	—	—	V
V_{OL}	LOW-level output voltage	I_{OL} = 2.0 mA; V_{IO} = 3.1 V	—	—	0.4	V
f_{SPI}	SPI_1 frequency	SCLK_RX	1.9	2.0	2.1	MHz
q	pulse frequency	see Figure 5	3.7	4.0	4.3	MHz

Table 6. Characteristics...*continued*

Characteristic noted under conditions 4.75 V ≤ V_{CC5} ≤ 5.5 V, 3.1 V ≤ V_{IO} ≤ 5.5 V, −40 °C ≤ T_{amb} ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at V_{CC5} = 5.0 V, V_{IO} = 3.3 V/5.0 V, T_{amb} = 25 °C and device operating under nominal conditions unless otherwise noted.

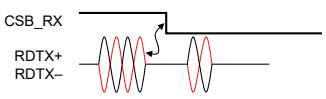
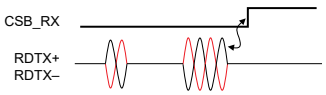
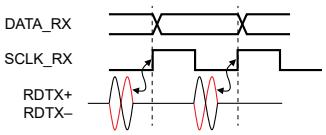
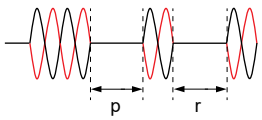
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
o	start of message	see Figure 5 [1]	460	500	540	ns
a	SCLK_RX HIGH	[1]	230	250	270	ns
b	SCLK_RX LOW	[1]	210	250	290	ns
$t_{SOM\_CSB\_RX}$	start of message to CSB_RX 	[1]	140	160	350	ns
$t_{EOM\_CSB\_RX}$	end of message to CSB_RX 	[1]	40	60	160	ns
$t_{PDB\_SCLK\_DATA\_RX}$	pulse data bit to DATA_RX and SCLK_RX 	[1]	220	280	365	ns
r	start of message to MSB (receive) 	see Figure 5 [1]	—	250	—	ns
p		see Figure 5 [1]	—	600	—	ns
m	time between consecutive messages received	see Figure 5	1.0	3.0	—	µs
Bus differential transmitter/receiver						
$V_{RDTX(PK\_DIFF)}$	RDTX± differential output voltage	R_L = 50 Ω; V_{CC5} = 4.75 V	2.2	2.5	3.0	V
I_{RDTX}	RDTX± current limit	sinking/sourcing to 2.5 V	65	—	300	mA
$V_{RDTX\_IN(TH)}$	RDTX± differential receiver threshold voltage	rising edge	0.68	0.74	0.80	V
		falling edge	0.515	0.61	0.70	V
$V_{RDTX\_IN\_HYST}$	RDTX± differential receiver threshold voltage hysteresis		100	130	165	mV
V_{RDTX_BIAS}	transformer bias voltage	transmitter in 3-state	2.2	2.5	2.85	V

Table 6. Characteristics...*continued*

Characteristic noted under conditions 4.75 V ≤ V_{CC5} ≤ 5.5 V, 3.1 V ≤ V_{IO} ≤ 5.5 V, −40 °C ≤ T_{amb} ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at V_{CC5} = 5.0 V, V_{IO} = 3.3 V/5.0 V, T_{amb} = 25 °C and device operating under nominal conditions unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RDTX}	transmit/receive pulse frequency		3.7	4.0	4.3	MHz
Wake-up receiver						
V_{RDTXWU_TH}	RDTX± wake-up differential receiver threshold voltage	rising edge	0.4	0.6	0.85	V
		falling edge	0.3	0.6	0.75	V
$V_{RDTXWU\_TH\_HYS}$	RDTX± wake-up differential receiver threshold hysteresis		50	100	150	mV
V_{RDTXWU_FLT}	RDTX± wake-up filter		20	50	80	ns

[1] All bus network signals to SPI timing are referenced to 0.8 V differential threshold.

11.1 Timing diagrams

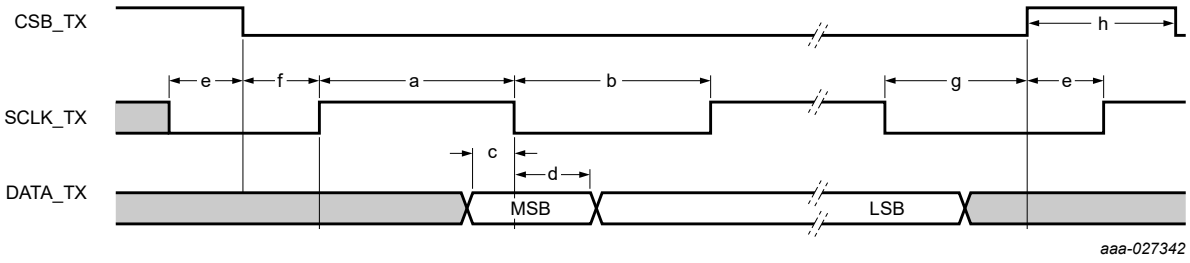


Figure 4. SPI transmit timing

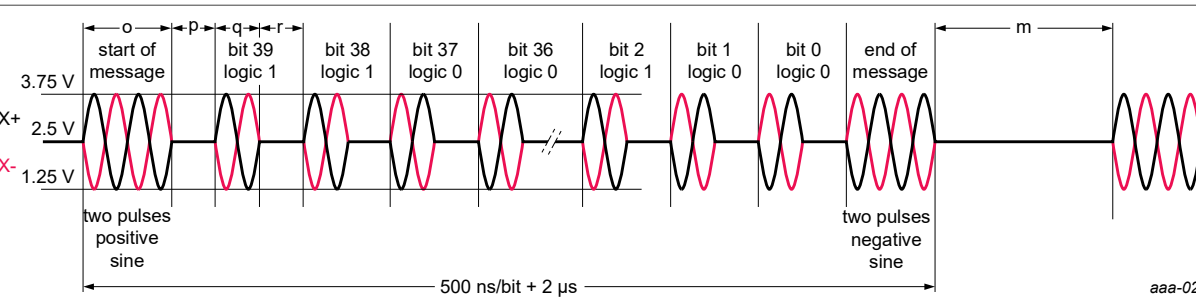


Figure 5. Transformer receive communication timing

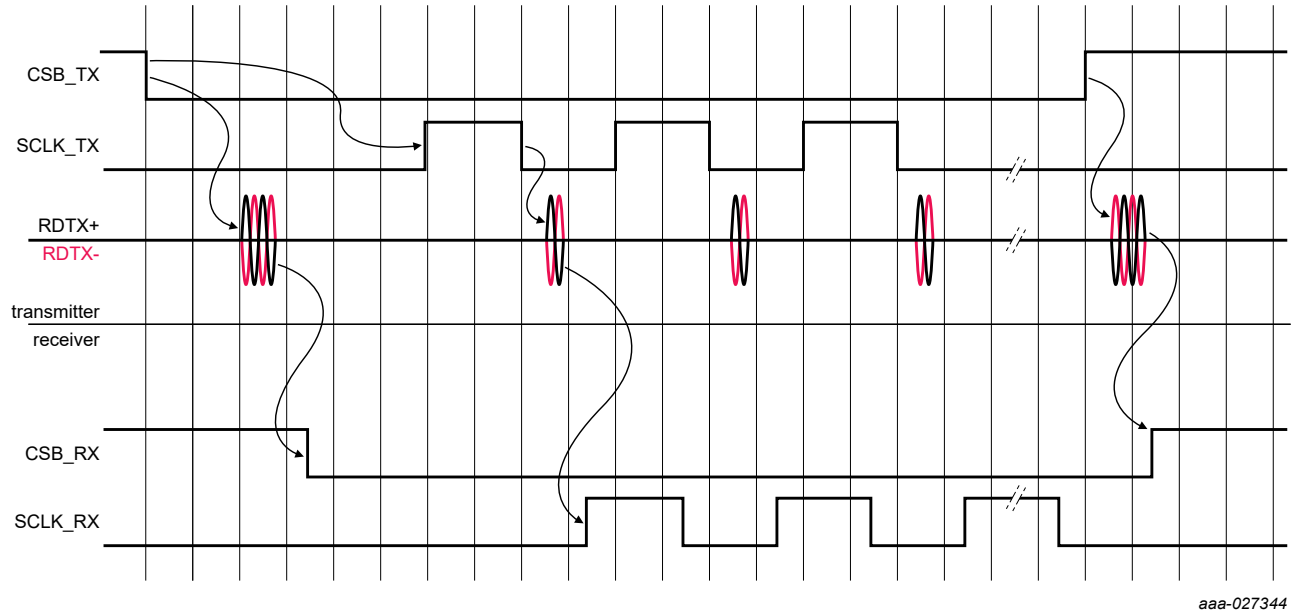


Figure 6. Transmit/receive signal propagation

12 Functional description

12.1 Introduction

The MC33664 provides the automotive industry a simple and convenient method for isolated high-speed differential communication. The device uses two MCU SPI ports for transmitting and receiving messages from the bus. The MC33664 is designed for half-duplex master-slave daisy chain architecture with a communication rate of up to 2.0 Mbit/s.

12.2 Functional description

The MC33664 receives SPI transmit signals from the MCU and creates bit by bit pulse phase encoded differential signals which are transmitted to the bus through an isolation transformer. SPI data to transmit is determined on the falling edge of SCLK_TX. Bus messages received by the MC33664 through the isolation transformer are converted bit by bit and transferred through the CSB_RX, SCLK_RX, and DATA_RX to the MCU.

To start a message transmission, the MCU transitions CSB_TX LOW. The falling edge of CSB_TX is a start of message (SOM) indication to the MC33664 to initiate a message transmission. Via the falling edge of CSB_TX, the MC33664 generates a positive phase encoded double pulse signal to the bus. With each SPI SCLK_TX from the MCU, the MC33664 then generates a single differential positive or negative pulse, depending on the level of the DATA_TX signal. On the rising edge of CSB_TX, the MC33664 generates a negative phase encoded double pulse indicating an end of message (EOM) transmission.

Receiving messages from the bus begins with the SOM pulse. On reception of the SOM, the MC33664 transitions the CSB_RX signal LOW. Each following single pulse generates a logic 1 or a logic 0 depending on the pulse phase. The bit information is clocked to the MCU through the SCLK_RX and DATA_RX pins. Receiving the EOM transmission ends the message and transitions the CSB_RX signal HIGH.

12.3 Modes of operation

The MC33664 has the following modes of operation defined by the level of the VIO and EN pins:

Table 7. Modes of operation

Mode	EN pin	VIO pin
Normal mode	1	1
Sleep mode	0	1
Reset	X	0

In Normal mode, the MC33664 operates as a full transceiver. MCU messages transmitted on the SPI_TX emerge on the SPI_RX for the MCU to read. In Normal mode, the MCU has complete control of the bus through the transceiver. Before placing the transceiver into Sleep mode, it is recommended the MCU place the slave nodes in Sleep mode through communication.

The MCU commands the MC33664 to Sleep mode by transitioning the EN pin to logic 0. In Sleep mode, the transceiver activates the INTB pin when a valid wake-up sequence is detected. The INTB pin remains LOW until the rising edge of the EN pin places the device in Normal mode. The MC33664 exits Sleep mode and enter Normal mode when the MCU enables the device through the EN pin.

Note: *The MC33664 provides a verification pulse for termination verification of the INTB pin to the MCU on every rising edge of the EN pin.*

12.3.1 Unpowered mode

When VIO is below VIO_{UV} or VCC5 is below $VCC5_{UV}$, the device is in Reset mode. The RDTX± outputs are in high-impedance and the device is not able to transmit, receive, or report bus wake-up events.

12.4 Wake-up pulse sequence

A wake-up pulse sequence can be generated by the master or any slave in the network system. The MCU commands a system wake-up by transitioning the EN pin from LOW to HIGH and generating two CSB_TX transitions. No SCLK_TX or DATA_TX signals are necessary during the MCU controlled wake-up sequence. See timing parameters t_1 and t_2 in Table 6.

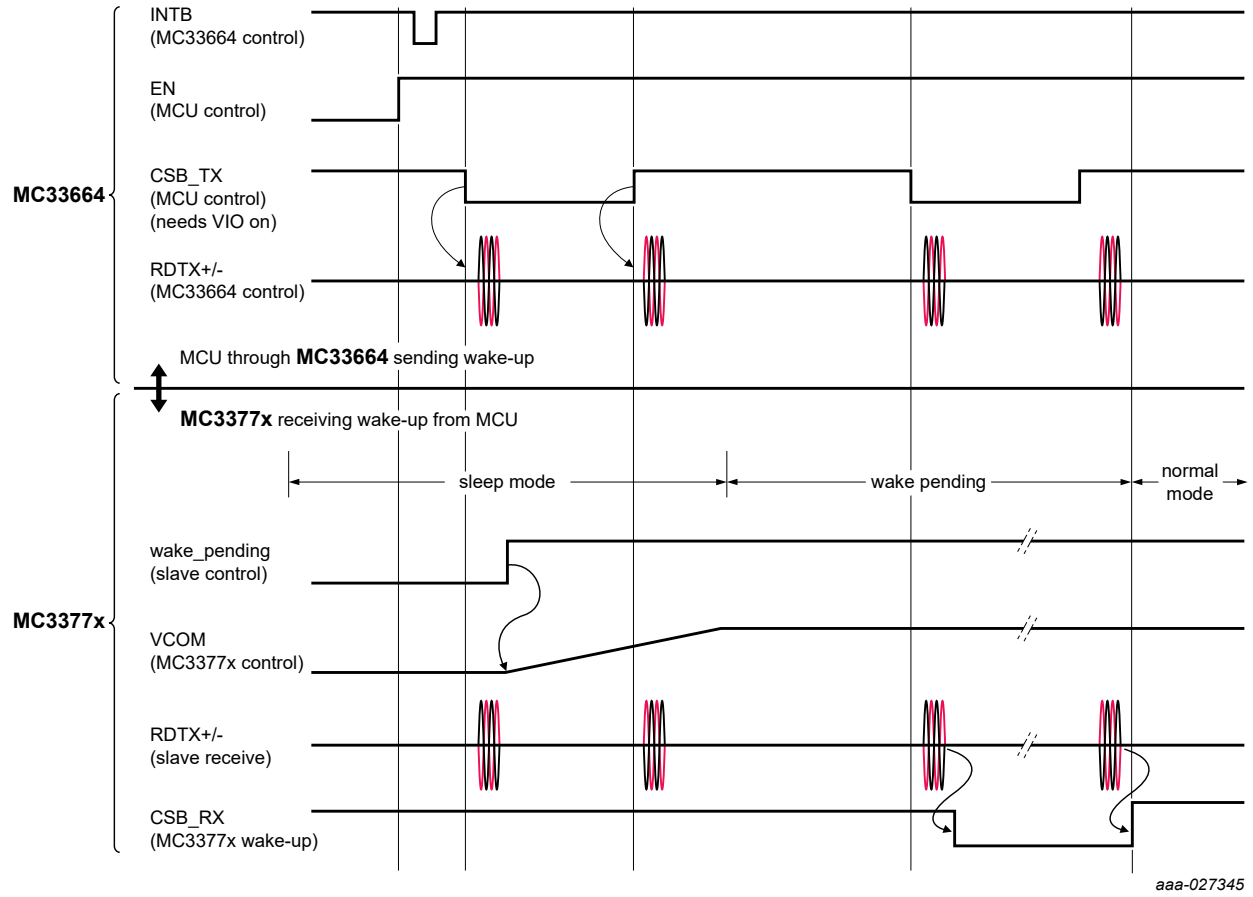


Figure 7. MCU system wake-up

A wake-up pulse sequence can be generated by any slave node on the network by using the same wake-up pulse sequence. Figure 8 illustrates a wake-up generated by a slave device on the network.

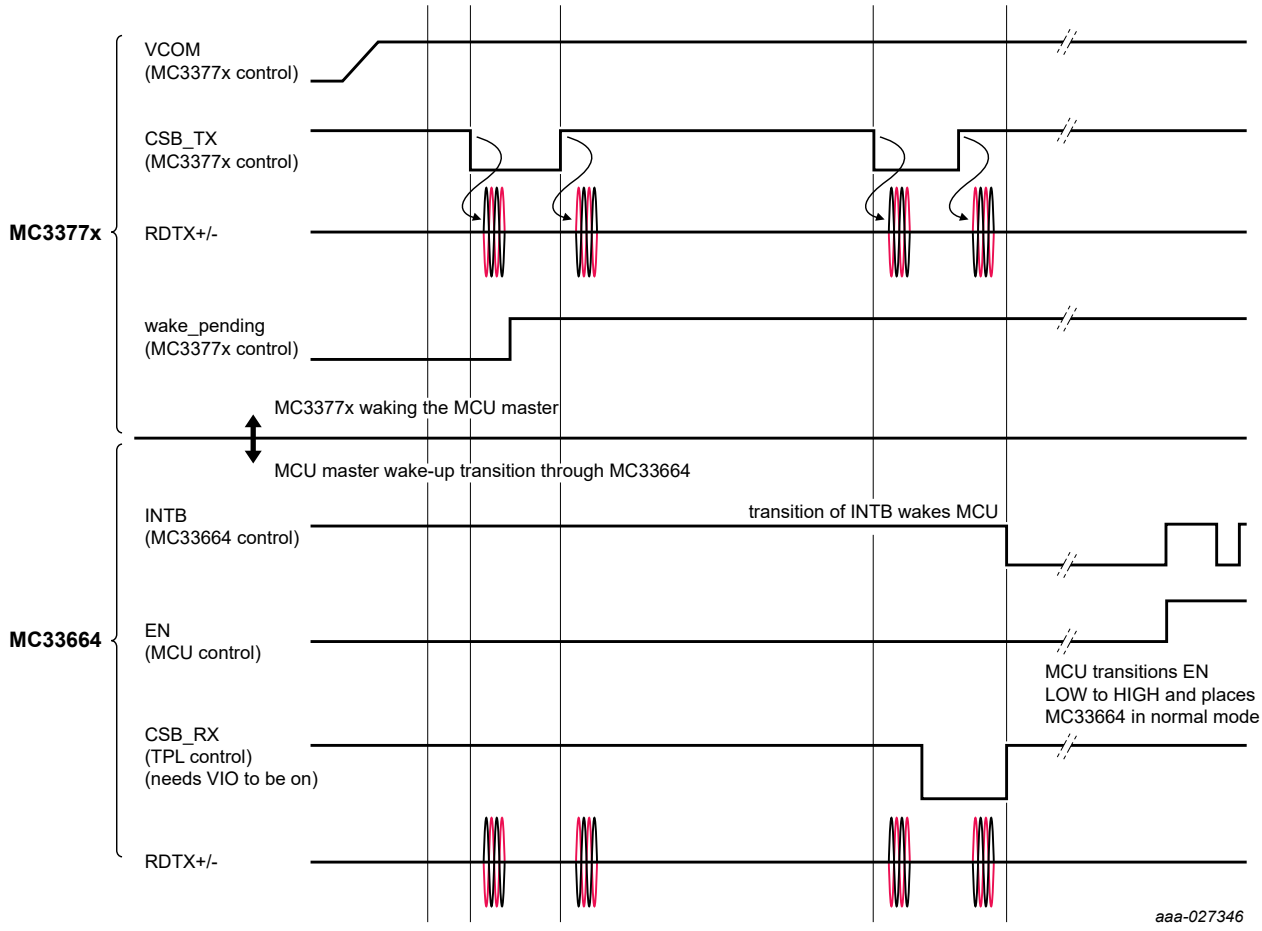


Figure 8. Slave system wake-up

13 Protection and diagnostics

The MC33664 physical layer is designed with a current limit protection feature to prevent failure of the output driver under shorted conditions. In the event the RDTX+ and RDTX- pins are shorted together, the current limit feature prevents failure of the drivers. The current limit feature also protects the output driver in the event the short occurs between the RDTX± outputs and ground. When the short conditions are removed, the device resumes normal operation.

All terminations between the MC33664 physical layer and the MCU can be confirmed. SPI transmit and receive messages are confirmed by performing a message transmit. The transmit message is received bit for bit with an additional phase delay. Performing this operation confirms the CSB_TX, SCLK_TX, DATA_TX, and CSB_RX, SCLK_RX, DATA_RX are terminated between the MCU and the MC33664. Additionally, the INTB and EN pin terminations are verified by transitioning the EN pin from LOW to HIGH. With each EN LOW to HIGH transition, a negative edge verification pulse is generated on the INTB pin. See $t_{INTB\_PULSE\_DELAY}$ and t_{INTB_PULSE} in Table 6 for timing parameters.

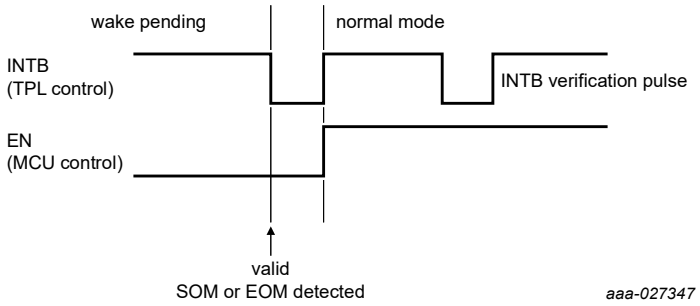


Figure 9. INTB termination verification

14 Application information

The MC33664 is designed primarily for automotive high-voltage electrical systems; however, the device can be used in any system requiring isolated communication. Figure 10 illustrates a typical application diagram for an automotive electric vehicle battery monitoring system.

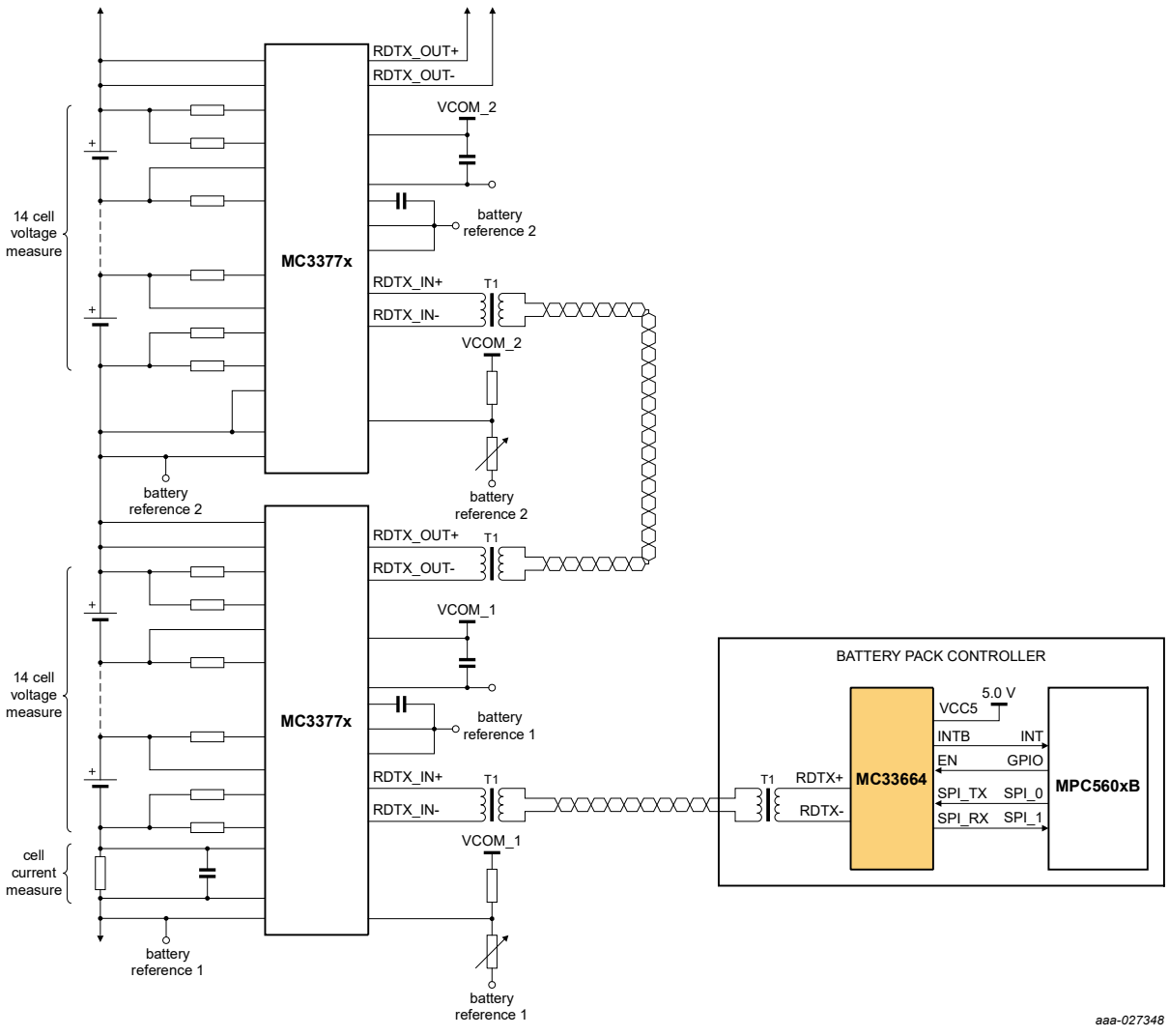


Figure 10. Typical distributed battery monitoring system

There are significant advantages to using transformers for isolation and communication. The most obvious benefit to the pulse transformers is the high degree of voltage isolation. Using pulse transformers allow the battery management system to achieve communication rates of 2.0 MHz with very low radiated emissions. Transformers by virtue of magnetic coupling, force the secondary signals to be true differential reducing radiated emissions and susceptibility. Recommended transformers are SUMIDA ESMIT-4180/C, PULSE HM2102NL, PULSE HM2103NL.

14.1 Electromagnetic compatibility (EMC) considerations

The MC33664 is designed to minimize radiated emissions by using sine pulse wave transmission as an alternative to pulse square waves. Automotive radiated emission tests have been conducted and the data is available upon request.

The MC33664 is designed to communicate under automotive bulk current injection (BCI) and direct power injection (DPI) conditions with minimal external components.

Minimal capacitance on a network system makes electrostatic discharge a constant concern for standard automotive physical layers. To protect the MC33664 from gun stress static discharge events, it is required to use a PESD5V0F1BL or equivalent ESD protection diode devices for protection on the primary side of the transformer.

14.2 PCB layout recommendations

Standard printed-circuit board (PCB) layout practices to be considered.

- SPI and digital interface traces routed over a continuous ground plane from the MC33664 to the MCU.
- Minimize the decoupling loop area for VCC5 to AGND, eliminating vias within the loop.
- Minimize the decoupling loop area for VIO to DGND, eliminating vias within the loop.
- Route RDTX+/RDTX- differentially from the MC33664 to the primary of the transformer over a continuous ground plane, eliminating all vias and stubs from the differential route.
- Locate the transformer as close as possible to the module connector.
- For maximum BCI performance, reduce the capacitance between the transformer and the PCB, by eliminating the ground plane under and around the transformer traces from the secondary to the connector and module connector itself. The ground must be removed from all PCB layers to be effective.
- Place the 150 Ω termination resistor close to the primary of the transformer without forming a stub.
- TVS devices should be placed close to the primary of the transformer. A minimum of two vias from the TVS device to the ground plane minimizes the inductance for greater performance to ESD events.

14.3 Application schematic

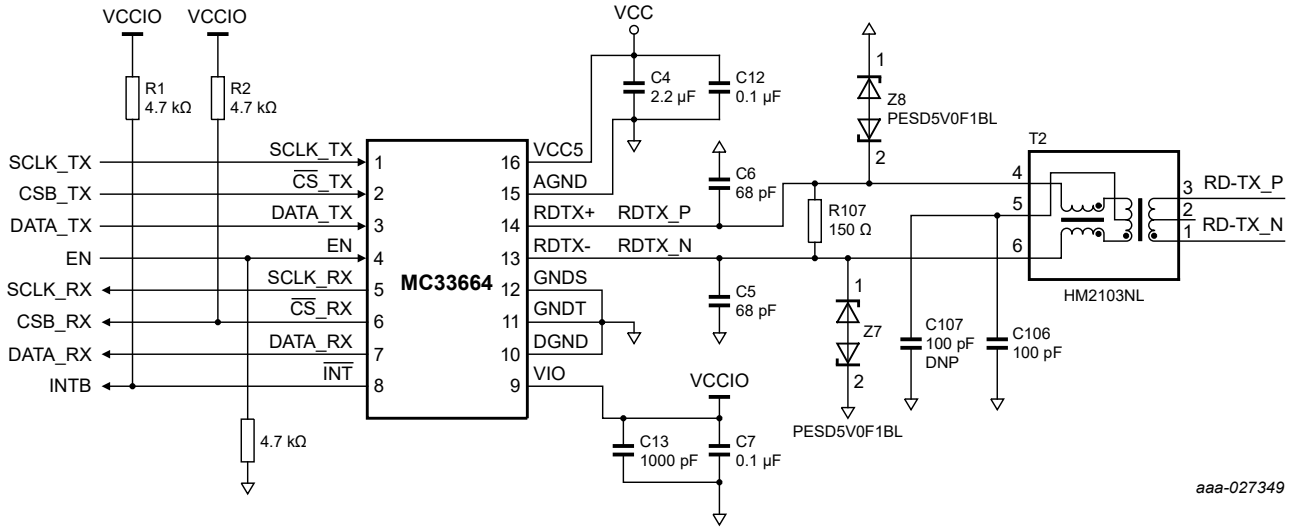


Figure 11. Application schematic

15 Package outline

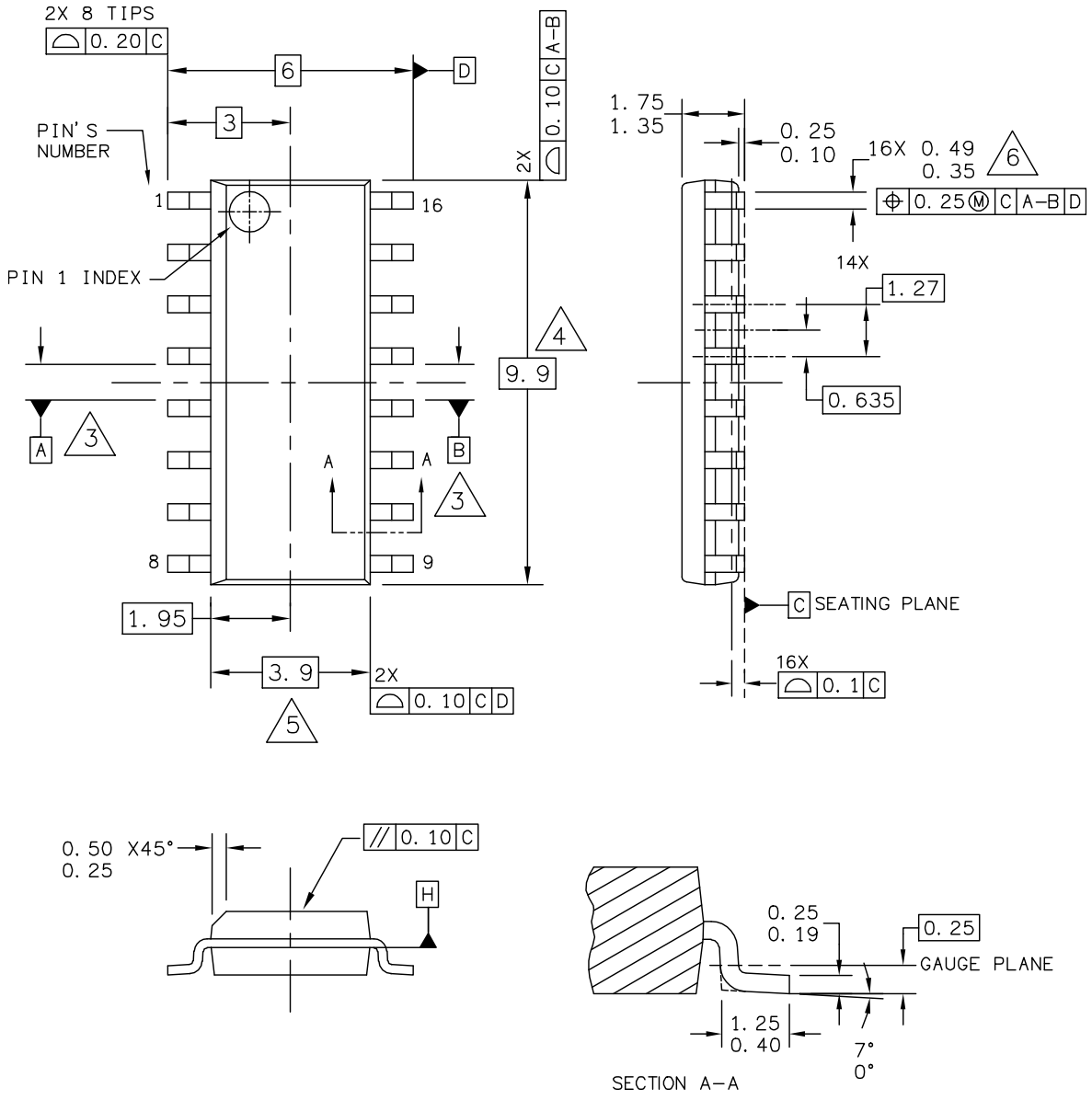


Figure 12. Package outline SOT109-5 (SO16)

16 Revision history

Table 8. Revision history

Revision	Release date	Modifications
MC33664 v.5.0	27 August 2024	changed security status to public
4.0	20170803	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Device number changed from 33664TL to MC33664 • Delete feature from list: Engineered for 5.0 meter, 15 node system • Table 6: MCU spec text has been deleted • Table 6: for symbol L, the reference to Figure 4 has been deleted • Table 6: for symbol t_1, the text 'MCU commanded bus wake-up' has been deleted • Table 6: for symbol t_2, the text 'Normal mode' has been deleted • Table 6: for symbols a and b the reference to Figure 4 has been added • Table 6: for symbol r, the text 'depends on communication frequency' has been deleted • Table 6: for symbol p, minimum value has been changed from 600 ns to nothing, typical value has been changed from nothing to 600 ns • Table 6: for symbols p and r, the text '250 ns blank time from SOM, 250 ns clock high, 100 ns for transmit logic to process falling of clock' has been deleted; reference to Figure 5 has been added • Section 14.2: deleted list item 6 and changed the list to unnumbered • Section 14.2: 300 Ω termination resistor replaced with 150 Ω termination resistor • Added Section 14.3 "Application schematic"
3.0	12/2015	• Corrected typo for transmit/receive pulse frequency
	11/2015	• Adjusted limits for $I_{VCC5(NORMAL)}$, $I_{VCC5(SLEEP)}$, $VCC5_{UVHYS}$, IIO_{SLEEP}, CSB_TX to start of message, start of message to CSB_RX, end of message to CSB_RX, pulse data bit to DATA_RX and SCLK_RX, $V_{RDTX\_IN(TH)}$, $V_{RDTX\_IN\_HYST}$, and V_{RDTX_BIAS} • Rewrote the steps in Section 14.2 • Updated Freescale form and style
2.0	4/2014	• Updated parameter table • Updated PCB layout recommendations
1.0	2/2014	• Initial release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

Suitability for use in automotive applications (functional safety) — This NXP product has been qualified for use in automotive applications. It has been developed in accordance with ISO 26262, and has been ASIL classified accordingly. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

Suitability for use in industrial applications (functional safety) — This NXP product has been qualified for use in industrial applications. It has been developed in accordance with IEC 61508, and has been SIL-classified accordingly. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures

Contents