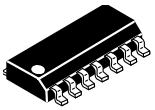
RoHS

High Speed CAN Interface with Embedded 5.0 V Supply

33902

HIGH SPEED CAN PHYSICAL INTERFACE



EF SUFFIX (PB-FREE)
98ASB42565B
14-PIN SOICN

The MC33902 is a high speed CAN physical interface. The device includes an internal 5.0 V supply for the CAN bus transceiver, and requires only a connection to a battery line.

The MC33902 provides 4 operation modes, including low power modes with remote and local wake-up.

The device has very low sleep and standby current consumption.

Features

- High speed CAN interface for baud rates of 40 kb/s to 1.0 Mb/s
- Compatible to ISO11898 standard
- Single supply from battery. No need for a 5.0 V supply for CAN interface
- I/O compatible from 2.75 V to 5.5 V via a dedicated input terminal (3.3 V or 5.0 V logic compatible)
- Low Power mode with remote CAN wake-up and local wake-up recognition and reporting
- CAN bus failure diagnostics and TXD/RXD pin monitoring, cold start detection, wake-up sources reported through the $\overline{\text{ERR}}$ pin
- Enhanced diagnostics for bus, TXD, RXD and supply pins available through Pseudo SPI via existing terminals EN, $\overline{\text{STBY}}$ and $\overline{\text{ERR}}$.
- Split terminal for bus recessive level stabilization
- INH output to control external voltage regulator
- Pb-free packaging designated by suffix code EF

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MCZ33902EF/R2	-40°C to 125°C	14 SOIC

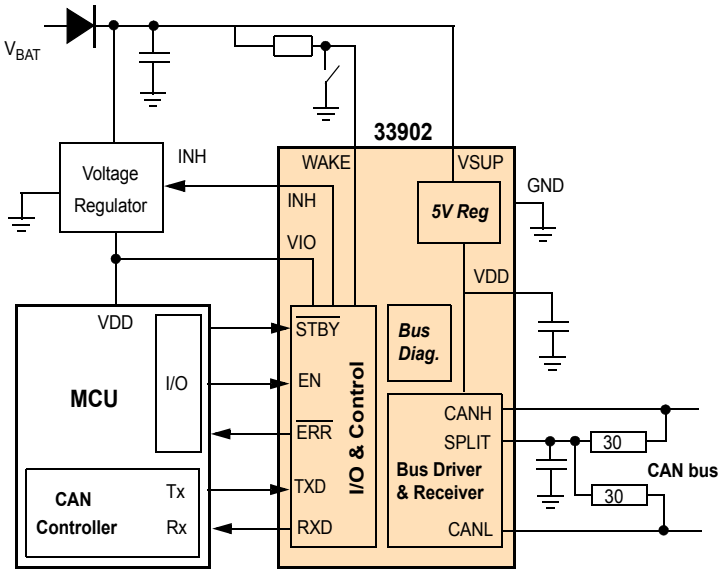


Figure 1. MC33902 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

freescale semiconductor

INTERNAL BLOCK DIAGRAM

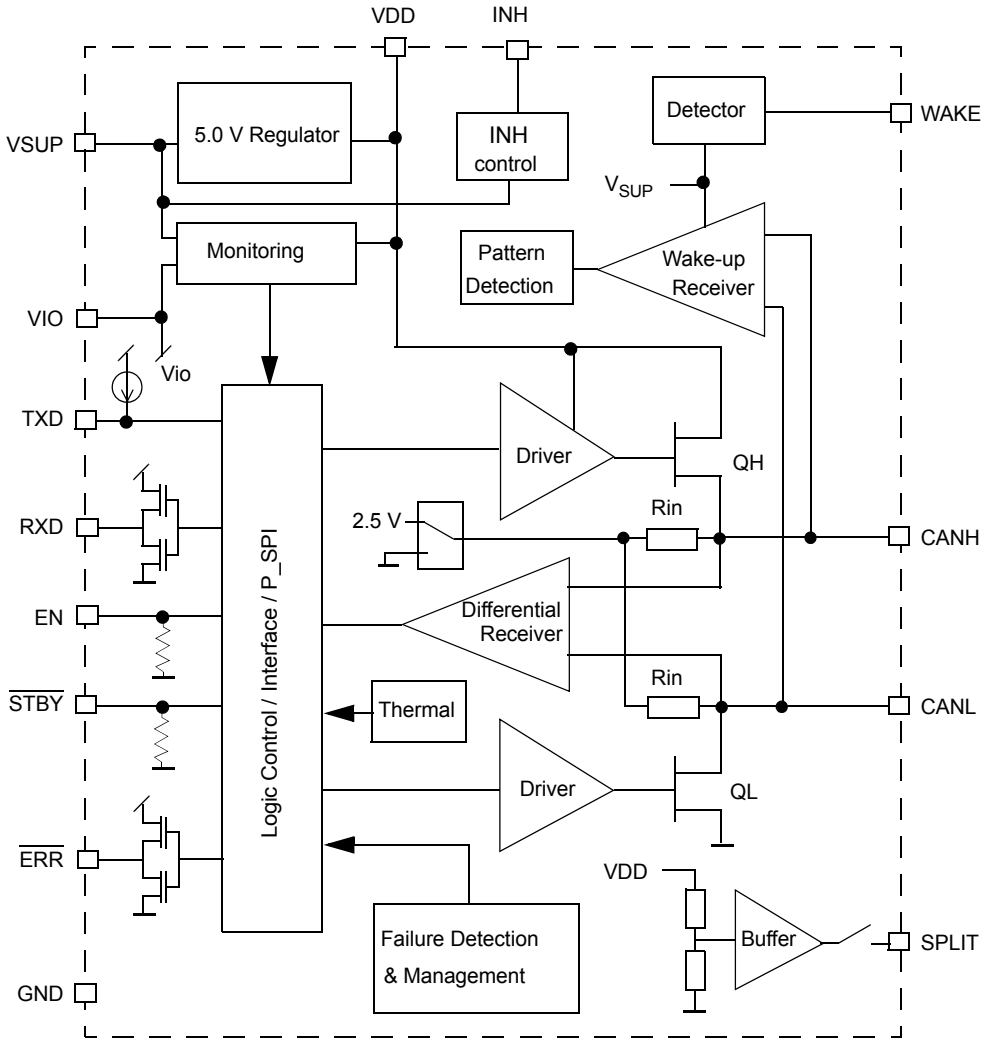


Figure 2. 33902 Simplified Internal Block Diagram

PIN CONNECTIONS

PIN CONFIGURATION

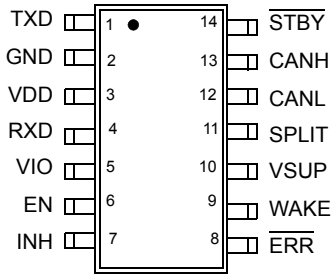


Figure 3. 33902 Pin Connections

Table 1. 33902 Pin Definitions

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	TXD	Input	Transmit data	CAN bus transmit data input pin
2	GND	Output	Ground	Ground termination
3	VDD	Output	Voltage Digital Drain	CAN dedicated internal voltage regulator, (decoupling capacitor required for voltage stabilization)
4	RXD	Output	Receive data	CAN bus receive data output pin, wake-up flag in Low Power mode
5	VIO	Input	Voltage supply for I/O	Input supply for the digital input output pins
6	EN	Input	Enable	Enable input for device static mode control. MOSI (Master Out, Slave In) during P_SPI operation.
7	INH	Output	Inhibit	Inhibit output for control of an external power supply regulator
8	$\overline{\text{ERR}}$	Output	Active low Error	Pin for static error and wake-up flag reporting MISO (Master In, Slave Out) during P_SPI operation.
9	WAKE	Input	Wake	Wake input
10	VSUP	Input	Voltage supply	Battery supply pin
11	SPLIT	Output	Split	Output for connection of the CAN bus termination middle point
12	CANL	Input/output	CAN LOW	CAN low pin
13	CANH	Input/output	CAN HIGH	CAN high pin
14	$\overline{\text{STBY}}$	Input	Standby	Standby input for device static mode control. CLK (Clock) during P_SPI operation.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
DC voltage on VSUP	V_{SUP}	-0.3 to +40	V
DC voltage on CANL, CANH, SPLIT Continuous (Steady State) Transient Voltage (Load Dump)	V_{BUS}	 -27 to +27 -27 to +40	V
DC voltage on VIO	V_{VIO}	-0.3 to 5.5	V
DC voltage on EN, $\overline{STBY}$, $\overline{ERR}$, TXD, RXD	V_{DIG}	-0.3 to VIO +0.3	V
DC voltage on Wake	V_{WAKE}	-0.3 to 29	V
Continuous current on CANH and CANL	ILH	200	mA
DC current on VDD	IVDD	240	mA
ESD on CANH, CANL and Split (HBM)	V_{ESDCH}	+-2000	V
ESD on CANH, CANL and Split (IEC61000-4, C_{ZAP} = 150 pF, Rzap = 330 Ω)	V_{ESDIEC}	+-8000	V
ESD on all pins except CANH, CANL, Split (HBM)	V_{ESCH}	+-2000	V
THERMAL RATINGS			
Junction temperature	T_J	150	°C
Ambient temperature	T_A	-40 to 125	°C
Storage temperature	T_{ST}	-55 to 165	°C
THERMAL RESISTANCE			
Thermal resistance junction to ambient (SO14)	$R_{\theta JA}$	140	°C/W

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 27 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT PIN (VSUP)					
Nominal voltage range	V_{SUPN}	5.5	-	27	V
Extended voltage range, fully functional, parametric value(s) not guaranteed	V_{SUPEX}	4.5	-	5.5	V
Supply current in Sleep mode, V_{SUP} ≤ 13.5 V, VIO = 0 V	$ISUP_{SLEEP}$	-	10		µA
Supply current in Standby mode (V_{SUP} ≤13.5 V, 5 V enabled at VDD terminal, default operation)	$ISUP_{STB}$	-	14	30	µA
Supply current in Normal mode, TXD high	$ISUP_{NORMAL}$	1.0	4.0	6.0	mA
Supply current in Listen Only mode, TXD high	$ISUP_{LISTEN}$	1.0	4.0	6.0	mA
BATFAIL Flag internal threshold	VBF_{THS}	1.5	3.3	5.5	V
BATFAIL Flag hysteresis	VBF_{HYS}	-	0.5	-	V
V_{SUP} under-voltage threshold (In Normal and Listen only)	VSUV	-	5.8	-	V
V_{SUP} under-voltage threshold hysteresis (In Normal and Listen only)	$VSUV_{HYS}$	-	0.2	-	V
OUTPUT PIN (VDD)					
Output Voltage	VDD_{OUT}	4.5	5.0	5.5	V
Drop voltage at I_{OUT} = 100 mA	V_{DROP}	-	-	500	mV
VDD low detection threshold	VDD_{TH}	4.0	4.25	4.5	V
Output Current Capability, for information only. Current for CAN tranceiver supply only.	I_{OUT}	150	-	-	mA
Current Source Capability, in standby and Go To Sleep mode.	I_{OUTLP}	5.0	-	100	µA
Thermal prewarning junction temperature (Available via P_SPI. $\overline{ERR}$ low if $\overline{ERR}$-EXT flag is set)	T_{PR}	130	150	170	°C
Thermal shutdown (junction)	T_{SD}	155	170	190	°C
Temperature threshold difference	T_{DIFF}	20	-	-	°C
External Capacitor	C_{EXT}	1.0	-	100	µF
INPUT SUPPLY PIN (VIO)					
Voltage range	V_{IO}	2.75	–	5.5	V
Input Current in Normal and Listen Only modes, RXD and $\overline{ERR}$ PIN current =0, TXD = high	$I_{VIOLIST}$	5.0	30	200	µA
Input Current in Normal mode, TXD = 0 V (Normal and Listen Only)	$I_{VIONORM}$	50	350	1000	µA
Input Current in Standby or Sleep mode, V_{IO} < 5.0 V	$I_{VIOSLP-STBY}$	–	2.0	5.0	µA

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 27 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUT PINS (EN, $\overline{STBY}$, TXD)					
High Level Input Voltage	V_{IH}	0.7 VIO	-	-	V
Low Level Input Voltage	V_{IL}	-	-	0.3 VIO	V
Pull-down Current, EN, $\overline{STBY}$, V_{IN} = V_{IO}	$I_{PD\ EN\text{-}\overline{STBY}}$	1.0	4.0	10	µA
Pull-up Current, TXD, V_{IN} = 0 V	$I_{PD\ TXD}$	-	-250	-	µA
DATA OUTPUT PINS (RXD) AND ($\overline{ERR}$)					
Low Level Output Voltage I = 5.0 mA	$VOUT_{LOW}$	0.0	-	0.3 VIO	V
High Level Output Voltage I = -3.0 mA	$VOUT_{HIGH}$	0.7 VIO	-	VIO	V
High Level Output Current V = VIO - 0.4 V	$IOUT_{HIGH}$	-12	-5.0	-2.0	mA
Low Level Output Current V = 0.4 V	$IOUT_{LOW}$	2.0	5.0	12	mA
OUTPUT PIN (INH)					
Output Drop Voltage ($I_{INH)}$, I_{OUT} = 100 uA)	INH_{DROP}	0.05	0.2	0.8	V
leakage Current (Sleep mode)	INH_{LEAK}	-	-	5.0	µA
INPUT PIN (WAKE)					
Low level threshold voltage	$WAKE_{LTH}$	2.0	2.5	3.0	V
High level threshold voltage	$WAKE_{HTH}$	2.0	2.7	3.5	V
Input Current V_{WAKE} = -0.2 to 18 V	$IWAKE_{IN}$	-10	0	10	µA
LOGIC INPUT/OUTPUT PINS (CANH, CANL)					
Bus pins common mode voltage for full functionality	V_{COM}	-12	-	12	V
Differential input voltage, recessive state at RXD	$V_{CANH\text{-}VCANL\text{-}R}$	-	-	500	mV
Differential input voltage, dominant state at RXD	$V_{CANH\text{-}VCANL\text{-}D}$	900	-		mV
Differential input hysteresis (RXD)	$V_{DIFF\text{-}HYST}$	-	100	-	mV
Input resistance	R_{IN}	5.0	-	50	kΩ
Differential input resistance	R_{IND}	10	-	100	kΩ
Common mode input resistance matching	R_{INM}	-3.0	0.0	3.0	%
CANH output voltage(45 Ω < R_{BUS} < 65 Ω) TX dominant state TX recessive state	V_{CANH}	 2.75 2.0	 3.5 2.5	 4.5 3.0	V
CANL output voltage(45 Ω < R_{BUS} < 65 Ω) TX dominant state TX recessive state	V_{CANL}	 0.5 2.0	 1.5 2.5	 2.25 3.0	V
Differential output voltage(45 Ω < R_{BUS} < 65 Ω) TX dominant state TX recessive state	V_{OH}-V_{OL}	 1.5 -500	 2.0 0.0	 3.0 50	 V mV

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 27 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUT/OUTPUT PINS (CANH, CANL) (CONTINUED)					
CANH output current capability - Dominant state	I_{CANH}	-	-	-25	mA
CANL output current capability - Dominant state	I_{CANL}	25	-	-	mA
CANL over-current detection - Error reported in register	$I_{CANL-OC}$	75	120	195	mA
CANH over-current detection - Error reported in register	$I_{CANH-OC}$	-195	-120	-75	mA
CANH, CANL input resistance device supplied and in Sleep mode, VCANH, VCANL from 0 V to 5.0 V	$R_{INSLEEP}$	5.0	-	50	kΩ
CANL, CANH output voltage in Sleep and Standby modes (45 Ω < R_{BUS} < 65 Ω)	V_{CANLP}	-0.1	0.0	0.1	V
CANH, CANL input current, device un supplied, V_{SUP} and V_{IO} connected to GND (ref. fig.) VCANH, VCANL = 5.0 V VCANH, VCANL = -2.0 to + 7.0 V	I_{CAN}	 - -	 - -	 250 400	µA
CANH AND CANL DIAGNOSTIC INFORMATION					
CANL to GND detection threshold	V_{LG}	-	1.75	-	V
CANH to GND detection threshold	V_{HG}	-	1.75	-	V
CANL to V_{BAT} detection threshold, valid if V_{SUP} > 7.0 V	V_{LVB}	-	V_{SUP}-2.0	-	V
CANH to V_{BAT} detection threshold, valid if V_{SUP} > 7.0 V	V_{HVB}	-	V_{SUP}-2.0	-	V
CANL to V_{DD} detection threshold	V_{L5}	-	V_{DD}-0.43	-	V
CANH to V_{DD} detection threshold	V_{H5}	-	V_{DD}-0.43	-	V
SPLIT					
Output voltage Loaded condition I_{split} =+- 500 µA Unloaded condition Rmeasure > 1.0 MΩ	V_{SPLIT}	 0.3 V_{DD} 0.45 V_{DD}	 0.5 V_{DD} 0.5 V_{DD}	 0.7 V_{DD} 0.55 V_{DD}	V
Leakage current -12 V < V_{SPLIT}< +12 V -22 V < V_{SPLIT}< +35 V	I_{LSPLIT}	 - -	 0.0 -	 5.0 70	µA

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 27 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

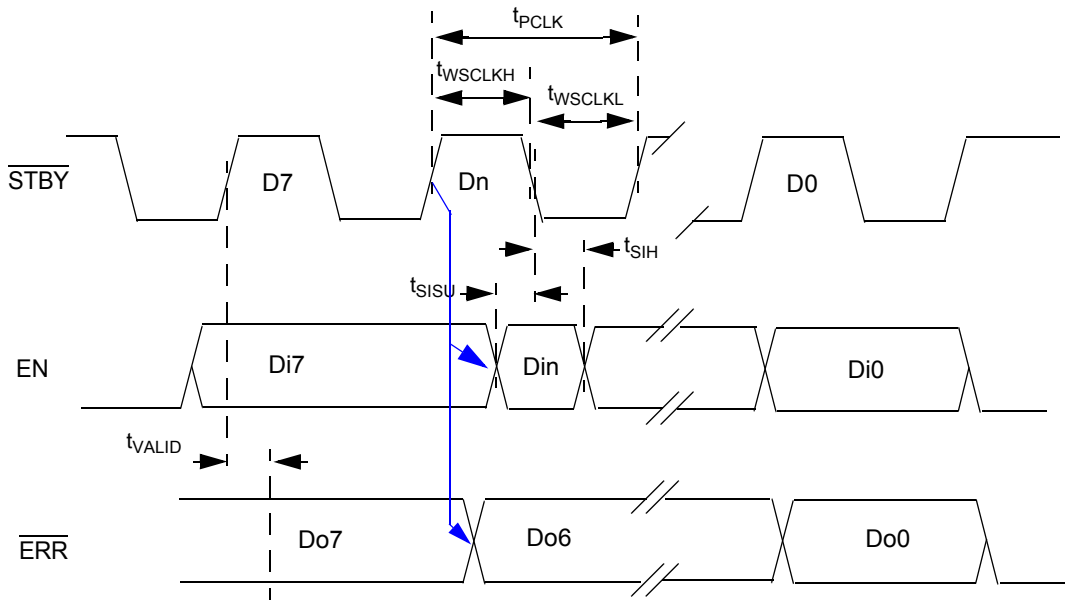
Characteristic	Symbol	Min	Typ	Max	Unit
TIMING (REF TO FIG 7)					
TXD Dominant State Timeout	t_{DOUT}	300	600	900	µs
Bus dominant clamping detection	t_{DOM}	300	700	1000	µs
Propagation loop delay TXD to RXD, recessive to dominant	t_{LRD}	60	140	210	ns
Propagation delay TXD to CAN, recessive to dominant	t_{TRD}	-	70	110	ns
Propagation delay CAN to RXD, recessive to dominant	t_{RRD}	-	45	140	ns
Propagation loop delay TXD to RXD, dominant to recessive	t_{LDR}	50	120	200	ns
Propagation delay TXD to CAN, dominant to recessive	t_{TDR}	-	75	150	ns
Propagation delay CAN to RXD, dominant to recessive	t_{RDR}	-	50	140	ns
Loop time TXD to RXD, Slew rate 1 (Selected by P_SPI) Rec to Dom Dom to Rec	$t_{LOOPSL1}$	50	-	310	ns
Loop time TXD to RXD, Slew rate 2 (Selected by P_SPI) Rec to Dom Dom to Rec	$t_{LOOPSL2}$	50	-	310	ns
STATE MACHINE TIMING					
External Wake-up Filter Time	t_{WAKE}	-	10	-	µs
3-Pulse pattern wake-up - Pulse width	t_{PWIDTH}				µs
V_{DIFF} = 1.15 V, Ta =-40°C		2.5	-	-	
V_{DIFF} = 2.0 V, Ta =-40°C		2.0	-	-	
V_{DIFF} = 1.15 V, 25°C ≤ Ta ≤ 125°C.		2.0	-	-	
Time to report local wake-up event	$t_{LOC\ WAKE-REP}$	-	35	-	µs
Time to report CAN wake-up event	$t_{CAN\ WAKE-REP}$	-	25	-	µs
Device state transition time (P_SPI versus static mode change distinction) except from Standby and Go To Sleep modes	t_{DEV-TR}	8.0	-	15	µs
Transition time from Standby mode to any mode	t_{LP-NP}	-	35	-	µs
Transition time from go to sleep to Sleep mode («Go To Sleep» command)	t_H	-	35	-	µs
V_{IO} low to Sleep mode timing	$t_{VIO-SLP}$	-	10	-	ms
V_{DD} low to CAN driver disable timing	$t_{VDD-CANOFF}$	-	10	-	ms
V_{DD} low to regulator disable timing	t_{VDDOFF}	-	50	-	ms
PSEUDO SPI (P_SPI)TIMING					
P_SPI Operation frequency	FREQ	0.0625	-	4.0	MHz
SCLK Clock High Time	t_{WSCLKH}	0.125	-	8.0	µs
SCLK Clock Low Time	t_{WSCLKL}	0.125	-	8.0	µs
EN to Falling Edge of $\overline{STBY}$	t_{SISU}	40	-	-	ns
Falling Edge of $\overline{STBY}$ to EN	t_{SIH}	40	-	-	ns
$\overline{ERR}$ rise Time CL = 15 pF	t_{RSO}	-	25	50	ns
$\overline{ERR}$ fall Time CL = 15 pF	t_{FSO}	-	25	50	ns

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 27 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Time from Rising Edge of $\overline{STBY}$ to $\overline{ERR}$ valid data	t_{VALID}	-	-	50	ns
Delay Between P_SPI Command and CAN in Normal Mode or CAN in Sleep mode. Device in Normal mode (measured after P_SPI 8th clock cycle rising edge).	$t_{CANON-OFF}$	-	-	20	µs

TIMING DIAGRAMS



EN and $\overline{ERR}$ state changed at $\overline{STBY}$ rising edge

Figure 4. P_SPI Timing

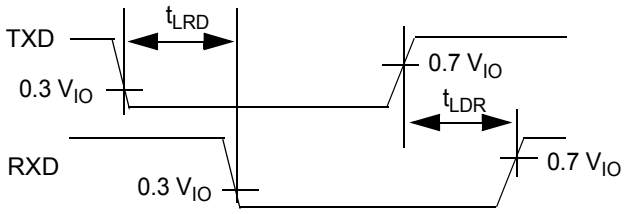


Figure 5. Propagation Loop Delay TXD to RXD

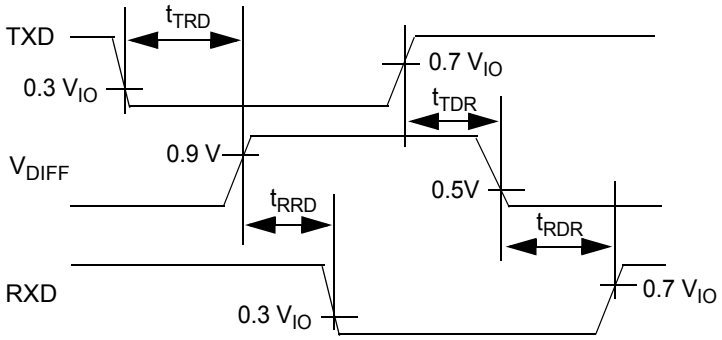


Figure 6. Propagation Delays TXD to CAN and CAN to RXD

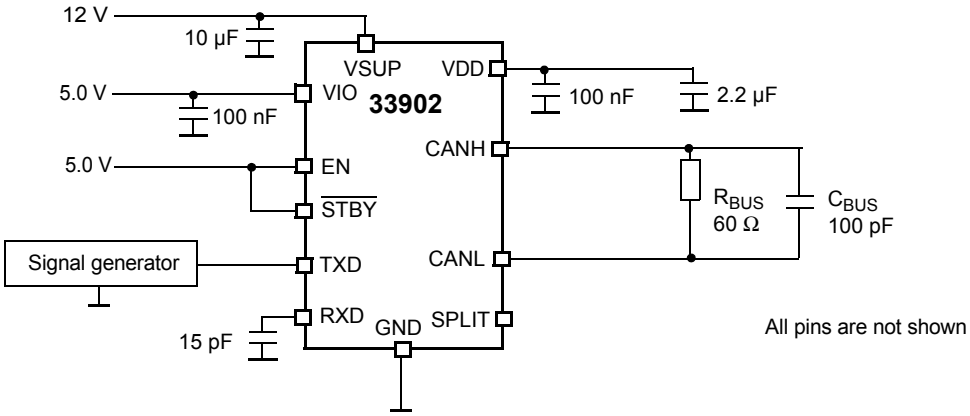


Figure 7. Test Circuit for Timing Characteristics

FUNCTIONAL DESCRIPTION

FUNCTIONAL PIN DESCRIPTION

TRANSMIT DATA (TXD)

This input is the CAN transmit data pin. It is the interface from the MCU to the output on the CAN bus. If TxD is low (dominant), then the signal on the CAN bus will be dominant (CANH is ~5.0 V and CANL is ~0 V). If TxD is high (recessive), then the signal on the CAN bus will be recessive (CANH and CANL will be ~2.5 V). The TxD thresholds are 3.3 V and 5.0 V compatible (depending on VIO voltage) to accommodate the implementation of various MCUs. There are three slew rates available, which are selected via the Pseudo SPI.

GROUND (GND)

Ground termination pin.

VOLTAGE DIGITAL DRAIN (VDD)

This is the dedicated embedded supply voltage for the CAN interface. A capacitor must be connected to this pin. CAN interface current is sourced from this pin if device is in transmit and receive mode. In low power modes, current for the CAN interface is sourced directly from the VSUP pin.

RECEIVE DATA (RXD)

This output pin is the CAN receive data. It is the interface to the MCU, which reports the state of the CAN bus. If the CAN bus is recessive (CANH and CANL ~2.5 V), then the signal on RxD will be high (recessive). If the CAN bus is dominant (CANH is ~5.0 V and CANL is ~0 V), then the signal on RxD will be low (dominant). This pin is also an active-low wake-up flag in low power, which reports a wake-up event to the MCU. RxD thresholds are 3.3 V and 5.0 V compatible (depending on the VIO voltage) to accommodate the implementation of various MCUs.

VOLTAGE SUPPLY FOR I/O (VIO)

This is the dedicated input supply pin to determine voltage thresholds for the digital input/output pins. The VIO thresholds range from 2.75 V to 5.5 V to accommodate the implementation of 3.3 V or 5.0 V MCUs.

ENABLE (EN)

This is the enable input pin for device static mode control. This pin is connected to the MCU to place transceiver in the desired mode. Functional voltage thresholds are determined by VIO voltage to accommodate the implementation of 3.3 V or 5.0 V MCUs. MOSI (Master Out, Slave In) during Pseudo SPI communication.

INHIBIT (INH)

The inhibit output pin controls an external power supply regulator. When the INH output is low, the external regulator is expected to shut down, which would then turn off the MCU and any other device that is powered up by the external regulator. This should considerably decrease the module's current consumption.

ACTIVE LOW ERROR ($\overline{\text{ERR}}$)

The dedicated active low flag reporting pin reports any static errors, flags and wake-ups to the MCU depending on devices operating state. MISO (Master In, Slave Out) during Pseudo SPI communication.

WAKE (WAKE)

The Wake input pin is used to wake-up the device from sleep mode after a Battery to Gnd, or Gnd to Battery transition. This pin is usually connected to an external switch in the application module, and SHOULD NOT be left open. If Wake pin functionality is not being used, it should be connected to GND to avoid false wake-ups. This pin exhibits a high-impedance for low input current when implemented below 18 V. If voltage exceeds 18V at the pin, a series resistor should be used to limit the amount of current that the device will start sinking.

VOLTAGE SUPPLY (VSUP)

This is the power supply input pin. The DC operating voltage for the device is 5.5 V to 27 V. A reverse battery protection diode should be implemented. This pin is able to sustain automotive transient conditions, such as 40 V load dumps and 27 V jump start conditions. The device's quiescent sleep current is typically around 10 μA.

SPLIT (SPLIT)

This is the output pin for middle point connection of CANH and CANL when implementing split termination. Pin voltage is typically around half of VDD (2.5 V) with or without loads. This pin must be left open if split CAN termination is not implemented.

CAN HIGH (CANH)

This is the CAN High input/output pin. CANH circuitry is design to work as a high side switch connected to VDD. In the recessive state, this switch is turned off and CANH is then biased to SPLIT voltage or GND, depending on device's operating state. In the dominant state, the switch is turned on and CANH is biased to VDD voltage. The CANH pin is protected and diagnostics reporting is available against short to Battery, Gnd, and 5.0 V (VDD).

CAN LOW (CANL)

This is the CAN Low input/output pin. CANL circuitry is design to work as a low side switch connected to GND. In the recessive state, this switch is turned off and CANL is then biased to SPLIT voltage or Gnd, depending on device's operating state. In the dominant state, the switch is turned on and CANL is biased to GND voltage. The CANL pin is protected and diagnostics reporting is available against short to Battery, Gnd, and 5.0 V (VDD).

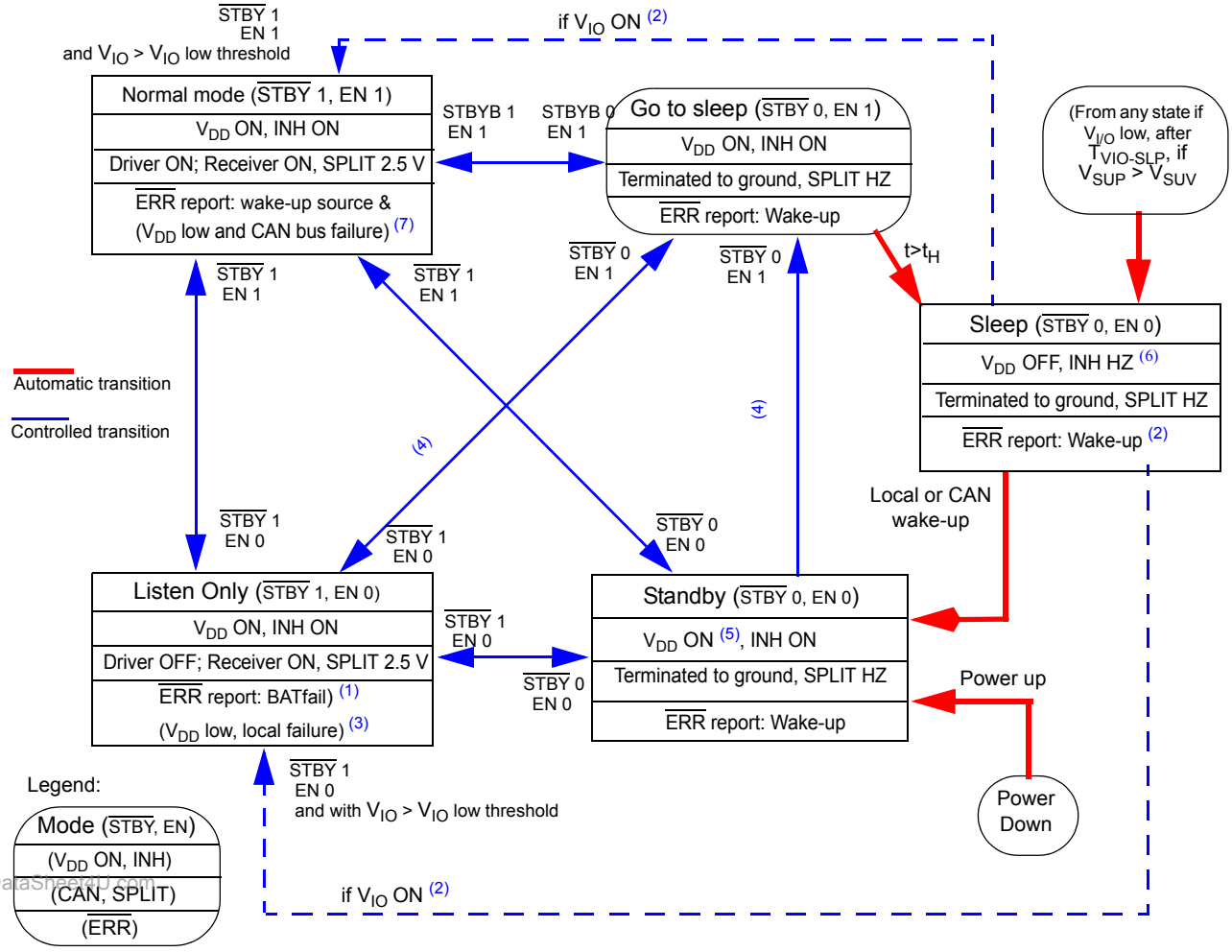
STANDBY ($\overline{\text{STBY}}$)

This is the standby input pin for device static mode control. This pin is connected to the MCU to place transceiver in the desired mode. Functional voltage thresholds are determined by VIO voltage to accommodate the implementation of 3.3 V or 5.0 V MCUs. CLK (Clock) during Pseudo SPI communication.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

STATE DIAGRAMS



Notes

1. Coming from Standby mode
2. If $V_{I/O}$ is still switched on
3. Coming from Normal mode
4. If batfail flag and wake-up flag are cleared. An attempt to enter Sleep mode without batfail and wake-up flag cleared has no effect
5. Limited current capability, to maintain the capacitor at V_{DD} charged.
6. A high level on INH will report a wake-up in Sleep mode
7. After 4 TXD pulses rising edge

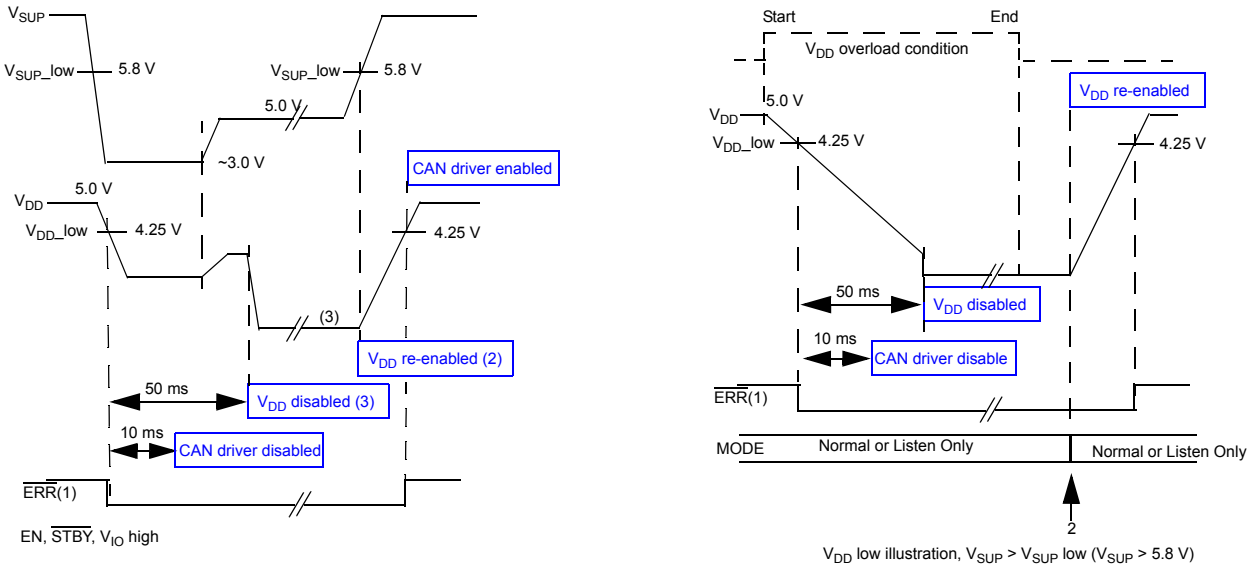
Figure 8. State Diagram

Table 5. Functional Table

$\overline{STBY}$	EN	Mode	V_{DD}	INH	RXD	CAN	$\overline{ERR}$ (active low)
0	0	Standby	ON [8]	High	Active LOW: report wake-up event [9]	Terminated to GND	Active LOW: report wake-up event [9]
0	0	Sleep	OFF	HZ			
0	1	Go to sleep	ON	High			
1	0	Listen Only	ON	High	High: recessive state Low: dominant state	Receiver: ON Driver: OFF	•Report local failure, V_{DD} low, Bat fail
1	1	Normal	ON	High		Driver and Receiver: ON	•wake-up source [10] •BUS failures, V_{DD} low

Notes

8. With limited current capability, in order to maintain the capacitor at V_{DD} pin charged
9. Provided if V_{IO} > 2.5 V.
10. Before 4th TX pulse rising edge



V_{DD} low illustration, cranking pulse V_{SUP} < V_{SUP} low (V_{SUP} < 5.8 V) and CRANK bit low in P_SPI register.
1) See figure on $\overline{ERR}$ reporting
2) V_{DD} is re enabled when V_{SUP} recovers (V_{SUP} low flag goes from H to L) or by a mode change via EN and $\overline{STBY}$ input.
3) Capacitor charged maintained by internal device current source

Figure 9. V_{DD} Low Illustration

DEVICE STATE DESCRIPTION

STANDBY MODE

Standby mode is a reduced current consumption mode. CANH and CANL lines are terminated to GND, the SPLIT pin is high-impedance. In order to monitor bus activities, the CAN wake-up receiver is ON, INH output remains ON. The voltage on VIO should be maintained.

The VDD regulator is ON with limited current capability, in order to maintain the capacitor at VDD charged and allow a fast transition to Normal mode and fast CAN communication.

Wake-up events occurring on the CAN bus or on the WAKE pin are reported by a low level of the $\overline{ERR}$ and RXD pins. The Standby mode is also the first mode entered after a device power up. In this case, the VDD regulator is activated to charge the V_{DD} capacitor, and then the regulator enters the reduced current capability mode, in order to optimize and reduce system current consumption. Depending upon the V_{DD} capacitor 's Equivalent Series Resistance (ESR), a voltage drop can be observed. See Figure 10.

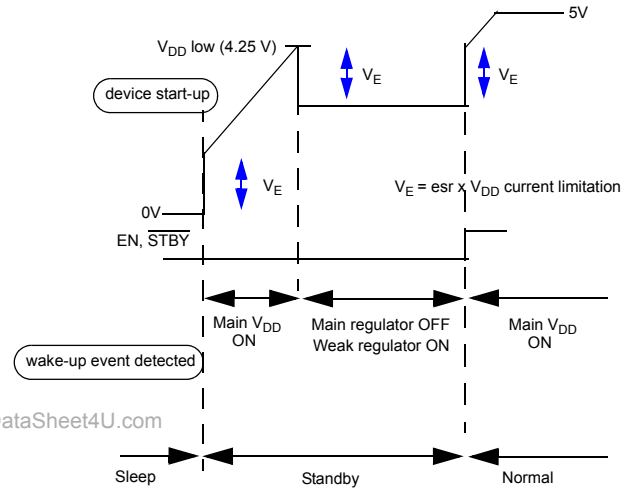


Figure 10. V_{DD} Regulator Start-up

NORMAL MODE

In Normal mode, both the CAN driver and receiver are ON. In this mode, the CAN bus is controlled by the TXD pin level, and the CAN bus state is reported on the RXD pin.

The VDD regulator is ON. It supplies the CAN driver and receiver.The SPLIT pin is active and a 2.5 V biasing is provided on the SPLIT output pin.

In Normal mode, the $\overline{ERR}$ pin reports the wake-up source and the bus failure, after 4 TXD pulses. Normal mode is entered by setting the EN and $\overline{STBY}$ pins high. Entering Normal mode will clear the BATFAIL flag.

LISTEN ONLY MODE

This mode is used to disable the CAN driver, but leave the CAN receiver active. In this mode, the device is only able to report the CAN state on the RXD pin. The TXD pin has no effect on CAN bus lines. This mode is entered by setting the EN and $\overline{STBY}$ pins to [0, 1].

In this mode, coming from Normal mode, the $\overline{ERR}$ pin reports local failures occurring on the TXD and RXD pins, and V_{DD} low. When this mode is entered from the Standby mode, the $\overline{ERR}$ pin reports the BATFAIL flag.

The VDD regulator is ON. The SPLIT pin is active and a 2.5 V biasing is provided on the SPLIT output pin.

GO TO SLEEP MODE

Go to sleep is an intermediate mode to ultimately set the device in Sleep mode. The go to sleep is entered by setting the EN and $\overline{STBY}$ pins to [1, 0]. If the EN and $\overline{STBY}$ pins are maintained to [1,0] for a time longer than t_H, the Sleep mode is automatically entered. In go to Sleep mode, the VDD regulator remains in its previous state and the SPLIT pin is deactivated. INH is active.

SLEEP MODE

The Sleep mode is a low power mode. It is entered from the Go To Sleep mode by setting the EN and $\overline{STBY}$ pins to [1 0], and automatically from Go To Sleep mode after t_H. In Sleep mode, the VDD regulator is turned off and the SPLIT pin is deactivated, INH is high-impedance.

In Sleep mode and Go To Sleep mode, the device is able to wake-up on CAN bus activity or transitions on the WAKE pin. A wake-up from Sleep mode will set the device in Standby mode. Sleep mode is also automatically reached if the voltage at VIO is below the VIO_{TH} for more time than $T_{VIO-SLP}$.

DEVICE MAIN FLAGS DESCRIPTION:

This section describes the flags available when the device is controlled via the EN and $\overline{STBY}$ pins in a static manner (no P_SPI control). Additional information and control are possible using the Pseudo SPI (refer to Extended device operation).

BATFAIL

This flag is set to signal that the voltage on the VSUP pin has dropped below VBF_{THS}, particularly after the device was disconnected from the battery. In Listen Only mode, the BATFAIL flag will be available on the $\overline{ERR}$ pin, coming from standby, Go To Sleep and Sleep modes. When V_{SUP} is below VBF threshold, all internal flags and registers are reset to their initial condition.

CAN Bus Wake-up (WU)

From Standby or Sleep mode, this flag is set if a correct pattern has been received on the CAN bus. This wake-up is reported on $\overline{ERR}$ and RXD pins by a low level in Standby mode, as well as in Sleep mode if VIO is present.

The flag is cleared by leaving the Normal mode or by a P_SPI reading.

WAKE Pin - Local Wake-up (WU)

From the Standby, Go To Sleep or Sleep mode, this flag is set if a transition on the WAKE pin is detected. This wake-up is reported on the $\overline{ERR}$ pin by a low level in Standby mode, as well as in Sleep mode if VIO is present.

The wake-up flag is cleared by leaving the Normal mode or by P_SPI reading.

Wake-up Source

Wake-up source is reported on the $\overline{ERR}$ pin by entering Normal mode, before 4 TX pulses. The $\overline{ERR}$ pin is low to indicate a local wake-up, and high to indicate CAN wake-up.

Local Failure

This flag is a logic «OR» of the following failures: TXD dominant clamping, RXD recessive clamping, TXD-to-RXD short-circuit and VDD low condition. This flag is reported in Listen Only on the $\overline{ERR}$ pin coming from Normal mode.

Using the P_SPI, it is possible to get detailed failure information.

BUS Failure

The BUS failure flag is set if the CAN transceiver detects a bus line short-circuit condition to VSUP, VDD, or GND, during five consecutive dominant-recessive cycles on the TXD pin. In addition, this flag reports a bus dominant clamping condition. In Normal mode, the bus failure flag is available on the $\overline{ERR}$ pin.

Using the P_SPI, it is possible to get detailed failure information.

VDD low

V_{DD} low flag is set in Normal and Listen Only mode when V_{DD} is below the V_{DD} low threshold. After a time longer than $t_{VDD-CANOFF}$, the CAN is disabled and after a time longer than t_{VDDOFF}, the V_{DD} regulator is disabled to avoid a battery discharge.

If the CRANK bit is set high, the V_{DD} regulator and CAN will not be disabled if V_{SUP} is below V_{SUV}. When V_{SUP} is above V_{SUV}, the CRANK bit has no effect.

V_{DD} low flag is reported in Normal and Listen Only mode, so the user can differentiate between local and bus failures by changing modes and observing $\overline{ERR}$ staying low.

In case of a double failure (local and bus failure) at the same time, the results will be the same: $\overline{ERR}$ low in Normal and in Listen Only mode. However, this is unlikely to occur.

This flag is cleared when entering low power, or when V_{DD} is above V_{DD} low threshold, plus the P_SPI reading.

The V_{DD} regulator is re enabled as soon as V_{SUP} rises above V_{SUP} low, or by a mode change (refer to the crank pulse illustration).

The CAN is re-enabled as soon as V_{DD} is above V_{DD} low threshold. (refer to crank pulse illustration).

$\overline{ERR}$ Pin

The $\overline{ERR}$ pin reports various information depending upon the device state, the device state transition, and event on the TXD pin.

Table 6 shows the diagnostic flag availability when the device is controlled in a static manner.

Table 6. "Static" Diagnostic Flags

Flag	Accessibility	Clearing Diagnostic
BATFAIL	Listen-Only mode (coming from Standby, Go-to-Sleep, Sleep)	Leaving Normal mode
CANWU or Local WU	Standby, Go-to-Sleep, Sleep (provided VIO is present)	Leaving Normal mode or by setting the BATFAIL
Wake-up source	Normal mode (Before the fourth dominant to recessive edge on the TXD pin)	Leaving Normal mode, or by setting BATFAIL flag.
BUS Failure	Normal mode (After the fourth dominant to recessive edge on the TXD pin)	Re-entering Normal mode
Local Failure	Listen Only mode (coming from Normal mode)	Entering Normal mode or TXD high while RXD low.
V_{DD} low	Normal mode (After the fourth dominant to recessive edge on the TXD pin) and Listen Only mode (coming from Normal mode)	$V_{DD} > V_{DD}$ low threshold
Evaluation mode	By RXD low, when coming from Sleep or Standby into Normal or Listen Only modes.	RXD goes from low to high, to signal the device is ready and has exited low power modes (TLP-NP parameter).

Figure 11 shows the meaning of the $\overline{ERR}$ pin versus the device state, the state transition and the events on TXD.

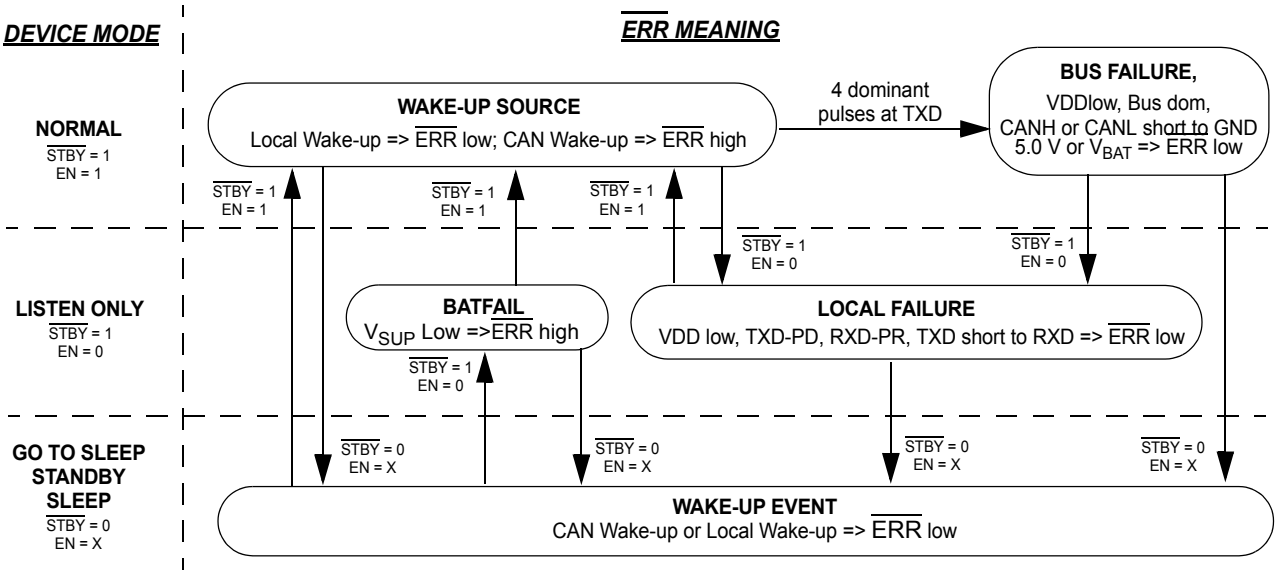


Figure 11. $\overline{ERR}$ versus device state

CAN INTERFACE DESCRIPTION:

CAN Interface Supply

The supply voltage for the CAN driver is the VDD pin. The CAN interface also has a supply path from the battery line, through the VSUP pin. This path is used in CAN Sleep mode to allow wake-up detection.

During CAN communication (transmission and reception), the CAN interface current is sourced from the VDD pin. During CAN low power mode, the current is sourced from the VSUP pin.

CAN Driver Operation in Normal Mode

The CAN driver will be enabled as soon as the device is in Normal mode and the TXD pin is recessive.

When the CAN interface is in Normal mode, the driver has two states: recessive or dominant. The driver state is controlled by the TXD pin. The bus state is reported through the RXD pin.

When TXD is high, the driver is set in the recessive state, and CANH and CANL lines are biased to the voltage set at VDD divided by 2, approx. 2.5 V.

When TXD is low, the bus is set into the dominant state, and the CANL and CANH drivers are active. CANL is pulled low and CANH is pulled high.

The RXD pin reports the bus state: CANH minus the CANL voltage is compared versus an internal threshold (a few hundred mV).

If “CANH minus CANL” is below the threshold, the bus is recessive and RXD is set high.

If “CANH minus CANL” is above the threshold, the bus is dominant and RXD is set low.

The SPLIT pin is active and provide a 2.5 V biasing to the SPLIT output.

Normal Mode and Slew Rate Selection

The CAN signal slew rate selection is done via the P_SPI. By default, and if no P_SPI is used, the device is in the fastest slew rate. Three slew rates are available. The slew rate controls the recessive to dominant and dominant to recessive transitions, which are also dependent on CANH and CANL capacitance. This also affects the delay time from the TXD pin to the bus, and from the bus to RXD. The loop time is thus affected by the slew rate selection.

Minimum Baud rate

The minimum baud rate is determined by the shortest TXD permanent dominant timing detection. The maximum number of consecutive dominant bits in a frame is 12 (6 bits of active error flag and its echo error flag).

The shortest TXD dominant detection time of 300 µs leads to a single bit time of: 300 µs / 12 = 25 µs.

So the minimum Baud rate is 1 / 25 µs = 40 kBaud.

Termination

The device supports the two main types of bus terminations:

- Differential termination resistors between CANH and CANL lines
- Split termination concept, with the mid point of the differential termination connected to GND through a capacitor, and to the SPLIT pin
- Refer to Typical Application and Bus Termination Options and WAKE Pin Configuration on page 27

Low Power Mode

In low power mode, the CAN is internally supplied from the VSUP pin.

In low power mode, the CANH and CANL drivers are disabled, and the receiver is also disabled. CANH and CANL have a typical 40 kΩ impedance to GND. The wake-up receiver can be activated if wake-up is enabled by the P_SPI command. The SPLIT pin is high-impedance.

When the device is set back into Normal mode, CANH and CANL are set back into the recessive level. This is illustrated in the following diagram.

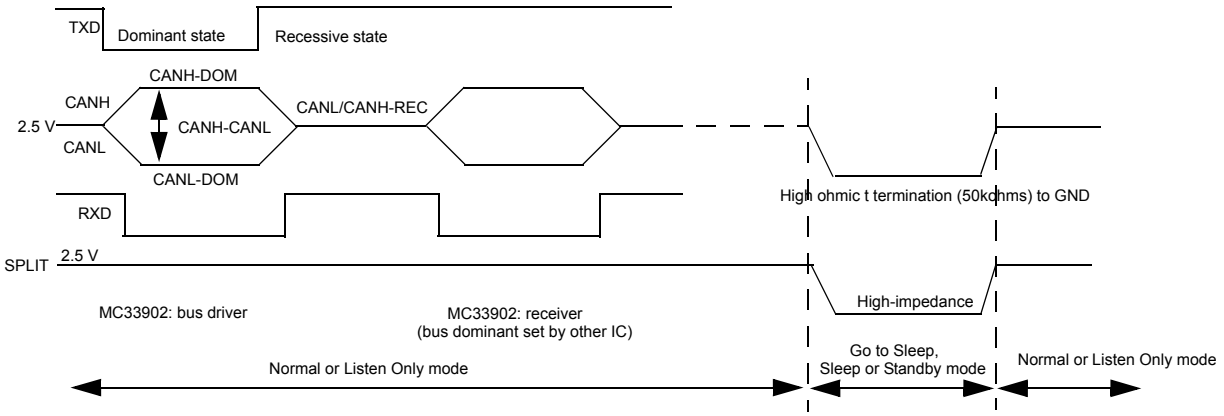


Figure 12. Bus Signal in Normal and Low Power Mode

Wake-up

When the CAN interface is in Sleep mode with wake-up enabled, the CAN bus traffic is detected. The CAN bus wake-up signal is a pattern wake-up. CAN wake-up cannot be disabled.

CAN Wake-up Report

The CAN wake reports depend upon the low power mode selected, Sleep or Standby. In Sleep mode, the INH pin is activated. In Standby mode, the VIO voltage is present and the wake-up is reported by the $\overline{\text{ERR}}$ and RXD pin low level. Ref to Table 5.

Pattern Wake-up

In order to wake-up the CAN interface, the wake-up receiver must receive a series of 3 consecutive valid dominant pulses. This is the default setting in which the CAN WU-pattern bit is set low. CAN WU-pattern bit can be set high by P_SPI, and the wake up will occur after a single pulse duration of a minimum of 4.0 µs.

A valid dominant pulse should be longer than t_{PWIDTH}. The 3 pulses should occur in a time frame of 120 µs to be considered valid. When 3 pulses pass these criteria the wake signal is detected. This is illustrated in Figure 13.

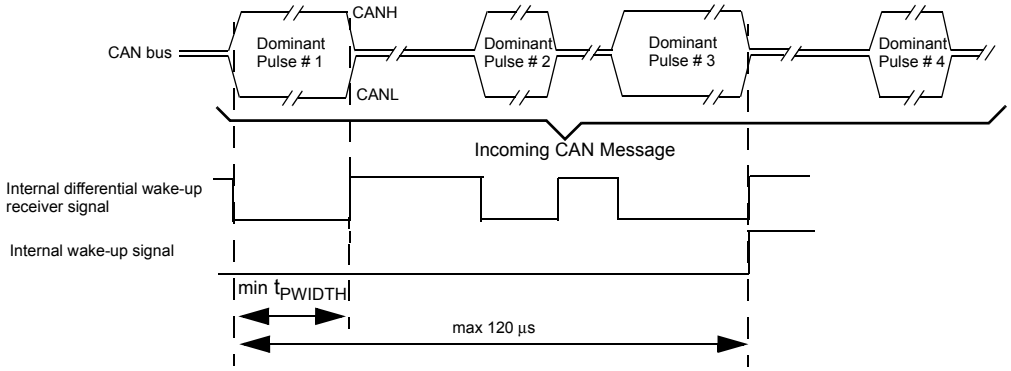


Figure 13. Pattern Wake-up

CAN BUS DIAGNOSTIC

The aim is to implement a diagnostic of bus short-circuit to GND, VBAT, and the internal application circuit board 5.0 V. Several comparators are implemented on the CANH and CANL lines. These comparators monitor the bus level in the recessive and dominant states. The information is then managed by the logic circuitry to properly determine the failure and report it.

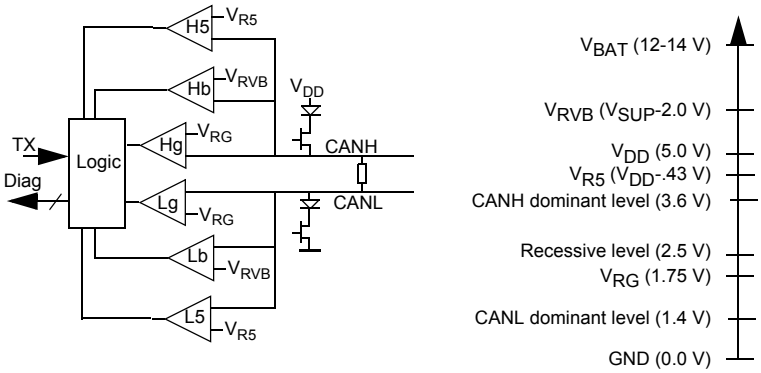


Figure 14. CAN Bus Simplified Structure Truth Table for Failure Detection

Table 7 indicates the state of the comparators in case of a bus failure, and depending upon the driver state.

Table 7. Failure Detection Truth Table

Failure description	Driver recessive state		Driver dominant state	
	Lg (threshold 1.75 V)	**Hg (threshold 1.75 V)**	**Lg (threshold 1.75 V)**	**Hg (threshold 1.75 V)**
No failure	1	1	0	1
CANL to GND	0	0	0	1
CANH to GND	0	0	0	0
	Lb (threshold V_{SUP}-2.0 V)	**Hb (threshold V_{SUP}-2.0 V)**	**Lb (threshold V_{SUP}-2.0 V)**	**Hb (threshold V_{SUP}-2.0 V)**
No failure	0	0	0	0
CANL to VBAT	1	1	1	1
CANH to VBAT	1	1	0	1
	L5 (threshold V_{DD}-0.43 V)	**H5 (threshold V_{DD}-0.43 V)**	**L5 (threshold V_{DD}-0.43 V)**	**H5 (threshold V_{DD}-0.43 V)**
No failure	0	0	0	0
CANL to 5.0 V	1	1	1	1
CANH to 5.0 V	1	1	0	1

Detection Principle

In the recessive state, if one of the two bus lines are shorted to GND, VDD, or VBAT, the voltage at the other line follows the shorted line, due to the bus termination resistance. For example: if CANL is shorted to GND, the CANL voltage is zero, the CANH voltage measured by the Hg comparator is also close to zero.

In the recessive state, the failure detection to GND or VBAT is possible. However, it is not possible with the above implementation to distinguish which of the CANL or CANH lines are shorted to GND or VBAT. A complete diagnostic is possible once the driver is turned on, and in the dominant state.

Number of Samples for Proper Failure Detection

The failure detector requires at least one cycle of the recessive and dominant states to properly recognize the bus failure. The error will be fully detected after 5 cycles of the recessive-dominant states. As long as the failure detection circuitry has not detected the same error for 5 recessive-dominant cycles, the error is not reported.

Bus clamping detection

If the bus is detected to be in dominant for a time longer than (t_{DOM}), the bus failure flag is set and the $\overline{ERR}$ is set low in Normal mode.

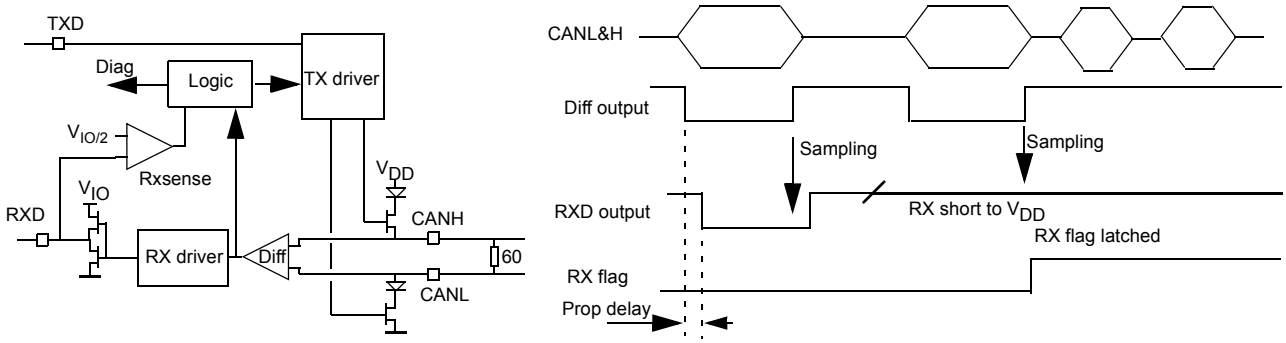
Such conditions could occur if the CANH line is shorted to a high voltage. In this case, current will flow from the high voltage short-circuit through the bus termination resistors (60 Ω) and then in the Split terminal (if used), and through the device CANH and CANL input resistors, which are terminated to an internal 2.5 V biasing or to GND (Sleep mode).

Depending upon the high voltage short-circuit, the number of nodes, usage of split terminal, R_{IN} actual resistor, and node state (sleep or active), the voltage developed across the bus termination can be sufficient to create a positive dominant voltage between CANH and CANL. The RXD pin will be low. This would prevent the start of any CAN

communication, and thus a proper failure identification (requires 5 pulses on TXD). The bus dominant clamp circuit will help to determine such failure situation.

RX Permanent Recessive Failure

The aim of this detection is to diagnose an external hardware failure at the RX output pin and ensure that a permanent failure at RX does not disturb the network communication. If RX is shorted to a logic high signal, the CAN protocol module within the MCU will not recognize any incoming message. In addition it will not be able to easily distinguish the bus idle state and can start communication at any time. In order to prevent this, an RX failure detection is necessary.



The RX flag is not the RXPR bit in the LPC register, and neither is the CANF in the INTR register.

Figure 15. RX Path Simplified Schematic, Rx Short to V_{DD} Detection

Implementation for Detection

The proposed implementation is to sense the RXD output voltage at each low to high transition of the differential receiver. Excluding the internal propagation delay, the RXD output should be low when the differential receiver is low. In case of an external short to VDD at the RXD output, RXD will be tied to a high level and can be detected at the next low to high transition of the differential receiver.

As soon as the RXD permanent recessive is detected, the RXD driver is deactivated.

Once the error is detected, the flag is latched and the driver is disabled. The error is reported at $\overline{\text{ERR}}$ pin and via P_SPI.

Recovery Condition

The internal recovery is done by sampling a correct low level at the Bus as shown in Figure 16.

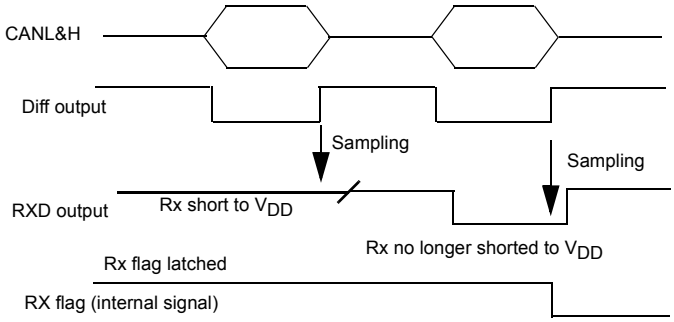


Figure 16. RX Path Simplified Schematic, Rx Short to V_{DD} Detection

Important Information for Bus Driver Reactivation RXD

The driver stays disabled until the failure is cleared (RX is no longer permanent recessive). One transition on the CAN bus (internal differential receiver transition), and the bus driver is activated by entering into Normal mode.

TXD PERMANENT DOMINANT

Principle

If the TXD is set to a permanent low level, the CAN bus is set into dominant level, and no communication is possible. The 33902 has a TXD permanent time out detector. After the timeout, the bus driver is disabled and the bus is released into a recessive state. The TXD permanent flag is set.

Recovery

The TXD permanent dominant is used and activated in case of a TXD short to RXD. The recovery condition for a TXD permanent dominant (recovery means the re-activation of the CAN drivers) is done by entering into a Normal mode controlled by the MCU, or when TXD is recessive, while RXD changes from recessive to dominant.

TXD TO RXD SHORT CIRCUIT:

Principle

If TXD is shorted to RXD during incoming dominant information, RXD is set low. Consequently, the TXD pin is low and drives CANH and CANL into a dominant state. Thus the bus is stuck in dominant state. No further communication is possible.

Detection and Recovery

The TXD permanent dominant time out will be activated and release the CANL and CANH drivers. However, at the next incoming dominant bit, the bus will then be stuck in dominant again. The recovery condition is same as the TXD dominant failure.

EXTENDED DEVICE OPERATION

The device has extended functionality which allows device control and diagnostic readings via the P_SPI (Pseudo Serial Peripheral Interface), and using the $\overline{\text{STBY}}$, EN and $\overline{\text{ERR}}$ pins.

P_SPI Operation

The P_SPI operation is similar to a standard SPI interface operation in slave mode. It uses the EN, $\overline{\text{STBY}}$ and $\overline{\text{ERR}}$ pins, which have the functions of MOSI, SCLK and MISO. There is no chip select (CS).

In write mode, the following functions and control are accessible:

- CAN driver slew rate selection
- $\overline{\text{ERR}}$ pin operation mode
- CAN wake-up mode
- CRANK mode operation

In read mode, the following flags are available:

- CAN bus detail diagnostic
- Local failure diagnostic
- Voltage monitoring
- Wake-up flags, wake pin level
- P_SPI errors
- Device identification

P_SPI Diagram

Figure 17 illustrates the P_SPI operation. A clock signal should be generated on the $\overline{\text{STBY}}$ pin, EN input operates as Data In (MOSI) and the $\overline{\text{ERR}}$ output pin operates as Data Out (MISO).

In order to start a P_SPI operation, the level at $\overline{\text{STBY}}$ should be low (1), as shown in Figure 17. Bit D7 starts at the rising edge of $\overline{\text{STBY}}$. Bit D7 level should be opposite to the level before. D7 is then internally sampled at the $\overline{\text{STBY}}$ falling edge.

The sampling of opposite level at (1) and (3) is the confirmation of a P_SPI message start.

Then the P_SPI bit D6 starts, and the device will drive the $\overline{\text{ERR}}$ pin to a level opposite to the one when P_SPI started (5): this is the confirmation that the device has correctly detected a P_SPI message start (acknowledgement).

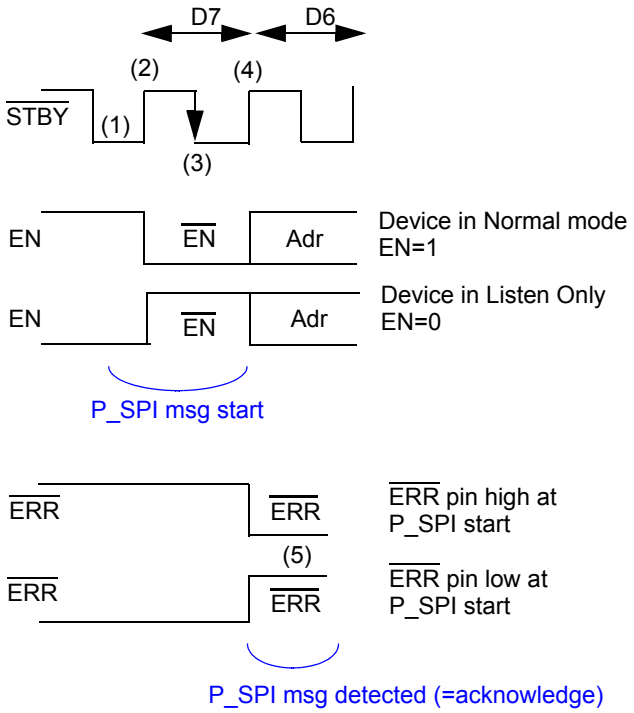


Figure 17. : P_SPI Message Start

Full P_SPI Message:

Figure 4 describes the complete P_SPI message and timing.

Distinction Between P_SPI and Traditional Operation.

The distinction between static device control and control via P_SPI is performed by the duration of the EN and $\overline{\text{STBY}}$ level. If the EN and $\overline{\text{STBY}}$ levels change before a time of "t_{DEV-TR}" then the device detects a P_SPI operation. If the EN and / or $\overline{\text{STBY}}$ levels are stable for a time longer than 15 µs, then the device state will be changed according to EN / $\overline{\text{STBY}}$ level and device state diagram.

This means that the device mode change is done after a delay of typ t_{DEV-TR} and consequently the P_SPI frequency operation should be faster than (1 / (2 * t_{DEV-TR}).
With t_{DEV-TR} = 8.0 µs, the SPI equivalent frequency should be greater than 62.5 kHz.

End of P_SPI Message:

At the P_SPI message, the state of EN and $\overline{\text{STBY}}$ pins should be in line with the device mode expectation:

example:

If the device is in Normal mode and should stay in Normal mode after the P_SPI command, the EN and $\overline{\text{STBY}}$ pins should be 1,1 at end of the P_SPI command.

If the device is in Listen Only mode, EN and $\overline{\text{STBY}}$ pins should be 0,1, in order to set or maintain the device in Listen Only mode.

Time between 2 P_SPI Message:

A min delay of 15 µs should be observed between two P_SPI messages.

The delay is measured between the last transition of the EN/$\overline{\text{STBY}}$ of the 1st message, and the 1st EN/$\overline{\text{STBY}}$ transition of the next message.

P_SPI Availability:

The P_SPI is operating only in Normal and Listen Only mode. It is not operating in Standby and Sleep modes.

Table 8 is the mapping of the P_SPI register.

Table 8. P_SPI Bit Mapping

	D7	D6	D5		D4		D3		D2		D1		D0	
MOSI	START	ADRR	Rb/W		MOSI 4		MOSI 3		MOSI 2		MOSI 1		MOSI 0	
MISO	ERR	ACK=ERRb	MISO 5		MISO 4		MISO 3		MISO 2		MISO 1		MISO 0	
MOSI	START	0	0 (read)		0	1	0	1	0	1	0	1	0	1
MISO	ERR	ACK=ERRb	0		BATFAIL	X	LxWU	WILS	CANWU	Test/def	VMONF	SPIerr	CANF	0
MOSI	START	0	1 (write)		$\overline{\text{ERR}}$_EXT		CAN SR1		CAN SR0		CAN WU - pattern		CRANK	
MISO	ERR	ACK=ERRb	0		0		PASS ID1		PASS ID0		MET ID1		MET ID0	
MOSI	START	1	0	1	0	1	0	1	0	1	0	1	0	1
MISO	ERR	ACK=ERRb	Bus dom	VDD temp	Rx-PR	CAN cur	Tx-PD	VSOV	CANF2	VSUV	CANF1	VIO low	CANF0	VDDlow

Low power mode definition: Standby, Go To Sleep and Sleep modes.

BATFAIL	Description	V_{SUP} voltage < V_{SUP} low threshold, also called Power On flag
	Set	V_{SUP} below V_{BFTH} (3.3 V)
	Reset	Entering Normal mode or P_SPI reading (Listen Only)
	Action	Avoid entering Go To Sleep. Set $\overline{\text{ERR}}$ low in Listen Only mode coming from low power modes

LxWU	Description	Wake-up event occurred on the WAKE pin
	Set	In low power mode, by a local wake pin transition
	Reset	Exit Normal mode or P_SPI reading (Listen Only and Normal mode)
	Action	Avoid entering Go To Sleep mode. Set $\overline{ERR}$ low in low power modes
CANWU	Description	Wake-up event occurred on CAN bus
	Set	In low power mode, by CAN wake-up
	Reset	Exit Normal mode or P_SPI reading (Listen Only and Normal mode)
	Action	Avoid entering Go To Sleep mode. Set $\overline{ERR}$ and RXD low in low power modes
VMONF	Description	Voltage monitoring flag: OR of V_{SOV}, V_{SUV}, V_{IO}, V_{DDLOW}, V_{DD} prewarning Temp
	Set	In normal and listen only modes: OR of V_{SOV}, V_{SUV}, V_{IO}, V_{DDLOW}, V_{DD} prewarning Temp
	Reset	Entering low power mode or (Failure removed + P_SPI reading (Listen Only and Normal mode))
	Action	If $\overline{ERR}$_EXT is set, $\overline{ERR}$ pin set low. $\overline{ERR}$ is low for the VDD low flag, despite the $\overline{ERR}$-EXT bit.
CANF	Description	Failure on the CAN bus. OR of CANF2, CANF1, CANF0 bits
	Set	In Normal and Listen Only modes: OR of TXDPD, RXDPR, CANcur, CAN bus failures
	Reset	Entering low power mode or (Failure removed + P_SPI reading (Listen Only and Normal mode))
	Action	Depending upon failure. ref to detail flag description
WILS	Description	Real time WAKE input level. Low is WAKE below threshold, high is WAKE above threshold.
	Set	WAKE pin higher than threshold
	Reset	WAKE pin lower than threshold
	Action	No action
SPIerr	Description	Pseudo SPI error: Incomplete transmission error during start of P_SPI
	Set	When P_SPI frame does not have 8 clock pulses
	Reset	Entering low power mode or P_SPI reading (Listen Only and Normal mode)
	Action	P_SPI wrong command is ignored
$\overline{ERR}$_EXT	Description	$\overline{ERR}$ pin operation report all flags
	Configure	By P_SPI
	Reset	Entering low power mode
	Action	When high, extend the $\overline{ERR}$ output pin to report all flags (when available) in any modes. When low (default) $\overline{ERR}$ reports default flags.

CANSR (1,0)	Description	00: CAN slew rate 0 11: CAN slew rate 0 01: CAN slew rate 1 10: CAN slew rate 2
	Configure	By P_SPI in Listen Only and Normal mode
	Reset	Entering low power mode
	Action	Change CAN slew rate (ref to parametric). Default is 00.
CAN WU - pattern	Description	Select between 2 wake-up mechanisms
	Configure	By P_SPI in Listen Only and Normal mode
	Reset	Leaving low power mode
	Action	When high wake-up occurs after 1 pulse of a minimum of 4.0 µs (parameter). When low, (default) wake-up occurs after 3 pulses of a minimum of 600ns (parameters).
CRANK	Description	When this flag is set, the V_{DD} low condition does not disable CAN and V_{DD} regulator, if V_{SUV} flag is set.
	Configure	By P_SPI in Normal and Listen Only modes
	Reset	Entering low power mode or P_SPI write (Listen Only and Normal mode)
	Action	No disable of CAN and V_{DD} regulator in case of a V_{DD} low condition, and the V_{SUV} flag is set. $\overline{ERR}$ reports a V_{DD} low condition. The P_SPI VDD low flag is set.
PASS ID(1,0), METID(1,0)	Set	Report device internal identification
	Reset	
	Action	
BUS dom	Description	Detect a bus voltage dominant for a time longer than t_{DOM}.
	Set	This flag is set if the bus is detected to be in dominant for more than t_{DOM}
	Reset	Entering low power mode, bus recessive P_SPI reading (Listen Only and Normal mode)
	Action	No action, set $\overline{ERR}$ low in Normal mode
CAN cur	Description	Over-current occurred on the CANH or CANL driver
	Set	In Normal mode, if the CANH or CANL current exceed the threshold (parameter)
	Reset	Entering low power mode, the CAN current below threshold + P_SPI reading (Listen Only and Normal mode)
	Action	By default no action. If the $\overline{ERR}$-EXT bit is set, the $\overline{ERR}$ is set low.

RX-PR	Description	RXD short to high (recessive level)
	Set	In Normal and Listen Only modes, if the RXD permanent recessive condition is detected
	Reset	Entering low power mode, the RXD recovery condition reached + P_SPI reading (Listen Only and Normal mode)
	Action	Set the local failure flag, disable the CAN driver, set $\overline{ERR}$ low in Listen Only mode coming from Normal mode
TX-PD	Description	TXD permanent dominant
	Set	In NORMAL modes, if TXD permanent dominant condition detected
	Reset	Entering low power mode, TXD recovery condition reached + P_SPI reading (Listen Only and Normal mode)
	Action	Set the local failure flag, disable the CAN driver, set $\overline{ERR}$ low in Listen Only mode coming from Normal mode
CANF (2,1,0)	Description	0 0 0: No CAN bus failure 0 0 1:CANL short to GND 0 1 0: CANL short to VDD 0 1 1: CANL short to VBAT 1 0 1: CANH short to GND 1 1 0: CANH short to VDD 1 1 1: CANH short to V_{SUP}
	Set	In Normal modes, if CAN failure condition detected
	Reset	Entering low power mode, CAN failure recovery condition reached + P_SPI reading (Listen Only and Normal mode)
	Action	Set the bus failure flag, set the $\overline{ERR}$ low in Normal mode after 4 Tx pulses
VDD temp	Description	V_{DD} regulator reaches temperature prewarning
	Set	In Normal mode or Listen Only mode, if the V_{DD} temperature reaches the prewarning threshold
	Reset	Real time report, reset if the temperature falls below the prewarning threshold
	Action	By default no action. If the $\overline{ERR}$-EXT bit is set, $\overline{ERR}$ is set low.
V_{SOV}	Description	V_{SUP} over-voltage detected
	Set	In Normal and Listen Only modes, if the V_{SUP} over-voltage threshold condition detected
	Reset	Entering low power mode, V_{SUP} over-voltage threshold condition recovered + P_SPI reading (Listen Only and Normal mode)
	Action	By default no action. If the $\overline{ERR}$-EXT bit is set, the $\overline{ERR}$ is set low.

V_{SUV}	Description	V_{SUP} under-voltage detected
	Set	In Normal and Listen Only modes, if the V_{SUP} under-voltage threshold condition detected
	Reset	Entering low power mode, V_{SUP} under-voltage threshold condition recovered + P_SPI reading (Listen Only and Normal mode)
	Action	When V_{SUP} voltage rises above the V_{SUS} threshold, the V_{DD} regulator is re-enabled if disabled previously by a V_{DD} low condition
V_{IO} low	Description	V_{IO} low detected
	Set	In all modes, if V_{IO} under-voltage threshold condition detected
	Reset	Entering low power mode, V_{IO} under-voltage threshold condition recovered + P_SPI reading (listen only and normal mode)
	Action	After 10ms, set the device in Sleep mode, if V_{SUV} low (don't enter Sleep mode during crank and power up phase).
V_{DD} low	Description	V_{DD} voltage < V_{DDLOW} flag threshold
	Set	In all modes, if V_{DD} under-voltage threshold condition detected
	Reset	Entering low power mode, V_{DD} under-voltage threshold condition recovered + P_SPI reading (Listen Only and Normal mode), mode change between Normal and Listen Only if V_{DD} regulator was turned off previously by a V_{DD} low condition for more than 50ms.
	Action	After 10 ms, disable the CAN, after 50 ms disable the regulator, if CRANK bit is set low (default).

TYPICAL APPLICATIONS

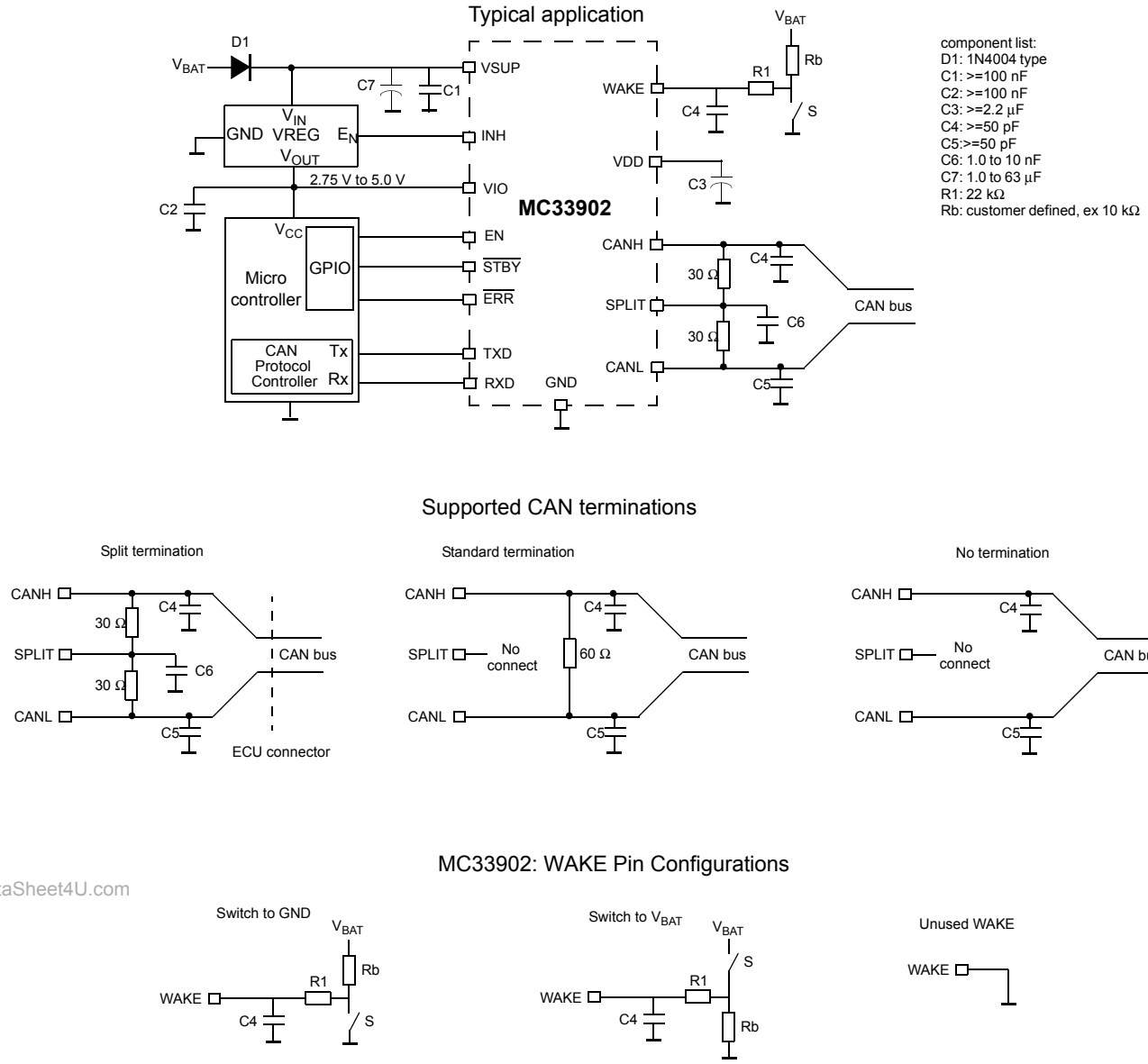


Figure 18. Typical Application and Bus Termination Options and WAKE Pin Configuration

COMPARISON WITH COMPETITION 14 PIN HIGH SPEED CAN TRANSCEIVER

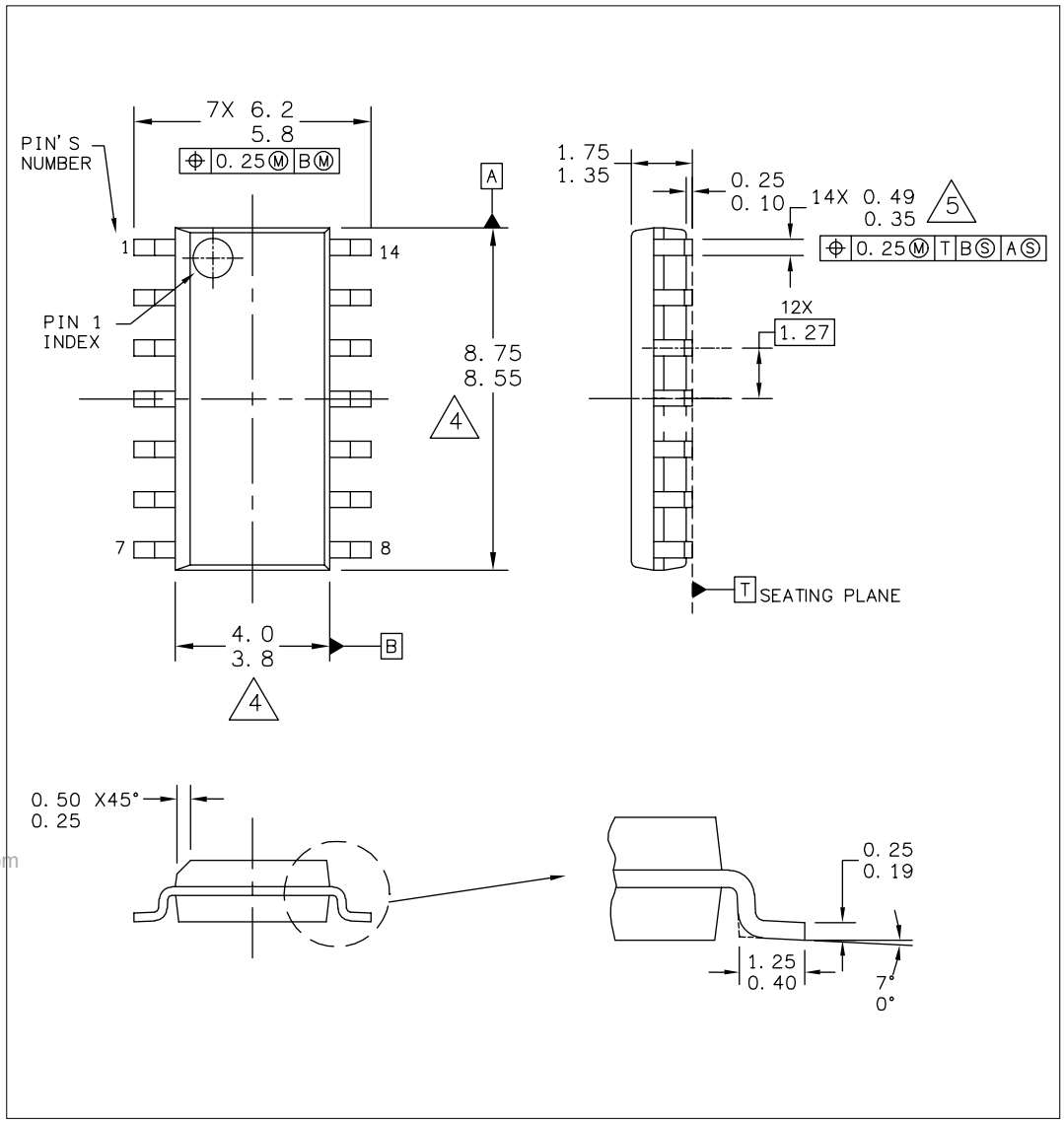
The table below is a comparison between the MC33902 and the competition 14 pin high speed CAN transceiver having no embedded power supply.

Item	MC33902	Competition w/o Embedded Regulator
V_{DD} pin	Output. Requires local decoupling capacitor(s). No extra load should be connected.	Input. Requires connection to a 5.0 V supply.
Wake pin	Fixed threshold typ 3.0 V with hysteresis. No pull-up or pull-down. High-impedance input. Connect to GND when not used.	Threshold V_{BAT} -3.0 V. Active pull-up when input is above threshold. Active pull-down when input is below threshold.
$\overline{ERR}$ pin	Active low, reports flags, or used as MISO during P_SPI communication. Strong driver (capability typ. 3.0 mA).	Active low, reports flags, weak driver, requiring 8.0 µs stabilization time
EN and $\overline{STBY}$ pins	Input used for static mode control. Used as CLOCK and MOSI during P_SPI communication.	Input used for mode control.
Bus dom failure flag	Failure reported on $\overline{ERR}$ pin in Normal mode (considered as a bus failure => reported in Normal mode)	Failure reported on the $\overline{ERR}$ pin in Listen Only mode (considered as a local failure)
V_{DD} low flag	No effect on device mode. Failure on CAN transceiver supply should not affect the complete ECU. V_{DD} is disabled “locally” to reduce current consumption. The $\overline{ERR}$ pin is set low in Normal and Listen Only mode. V_{DD} low threshold set at 4.25 V	Set the device into Sleep mode. INH is turned OFF. If the ECU regulator is controlled by INH, ECU is turned OFF.
V_{IO} low flag	Same	Same
Wake-up time	From Sleep or Standby mode, device needs 35 µs typ. to be ready.	No need for a delay for device ready.
Transition time	At least 8.0 µs, to differentiate between a static transition and P_SPI communication	Immediate transition. However, the $\overline{ERR}$ pin has weak driver and an 8.0 µs stabilization time is required. When the device is switched between Normal and Listen Only mode to check the fail flag, a delay of 8.0 µs is needed.

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the **98ASB42565B** listed below.



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	CASE NUMBER: 751A-03	19 JUL 2005
	STANDARD: JECDEC MS-012AB	

EF-PIN (PB-FREE)
98ASB42565B
ISSUE H

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
3.0	8/2009	• Initial Release

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MC33902
Rev. 3.0
8/2009