

# FS6500-FS4500-ASILB

Safety power system basis chip with CAN FD and LIN transceivers

Rev. 4 — 5 August 2024

Product data sheet



## 1 General description

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The FS6500/FS4500 SMARTMOS devices are a multi-output, power supply, integrated circuit, including CAN Flexible Data (FD) and/or LIN transceivers, dedicated to the automotive market.

Multiple switching and linear voltage regulators, including low-power mode (32  $\mu$ A) are available with various wake-up capabilities. An advanced power management scheme is implemented to maintain high efficiency over a wide range of input voltages (down to 2.7 V) and output current ranges (up to 2.2 A).

The FS6500/FS4500 includes configurable fail-safe/fail silent safety behavior and features, with two fail-safe outputs, becoming a full part of a safety oriented system partitioning, to reach a high integrity safety level (up to ASIL B).

The built-in CAN FD interface fulfills the ISO 11898-2<sup>(12)</sup> and -5<sup>(13)</sup> standards. The LIN interface fulfills LIN protocol specifications 2.0, 2.1<sup>(22)</sup>, 2.2<sup>(23)</sup>, and SAE J2602-2<sup>(24)</sup>.

High temperature capability up to  $T_A = 125\text{ }^\circ\text{C}$  and  $T_J = 150\text{ }^\circ\text{C}$ , compliant with AEC-Q100 Grade 1 automotive qualification.

## 2 Features and benefits

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- Battery voltage sensing and MUX output pin
- Highly flexible SMPS pre-regulator, allowing two topologies: non-inverting buck-boost and standard buck
- Family of devices to supply MCU core from 1.0 V to 5.0 V, with SMPS (0.8 A, 1.5 A or 2.2 A) or LDO (0.5 A)
- Linear voltage regulator dedicated to auxiliary functions, or to sensor supply ( $V_{CCA}$  tracker or independent), 5.0 V, or 3.3 V
- Linear voltage regulator dedicated to MCU Analog/Digital (A/D) reference voltage or I/Os supply ( $V_{CCA}$ ), 5.0 V, or 3.3 V
- 3.3 V keep alive memory supply available in low-power mode
- Long duration timer, counting up to 6 months with 1.0 s resolution
- Multiple wake-up sources in low-power mode: CAN, LIN, IOs, LDT
- Five configurable I/Os



### 3 Applications

- Drive Train Electrification (BMS, Hybrid EV and HEV, Inverter, DC-DC, Alternator Starter)
- Drive Train - Chassis and Safety (Active Suspension, Steering, Safety Domain Gateway)
- Power Train (EMS, TCU, Gear Box)
- ADAS (LDW, Radar, Sensor Fusion Safety area)
- On board charger
- Motor control

### 4 Simplified application diagrams

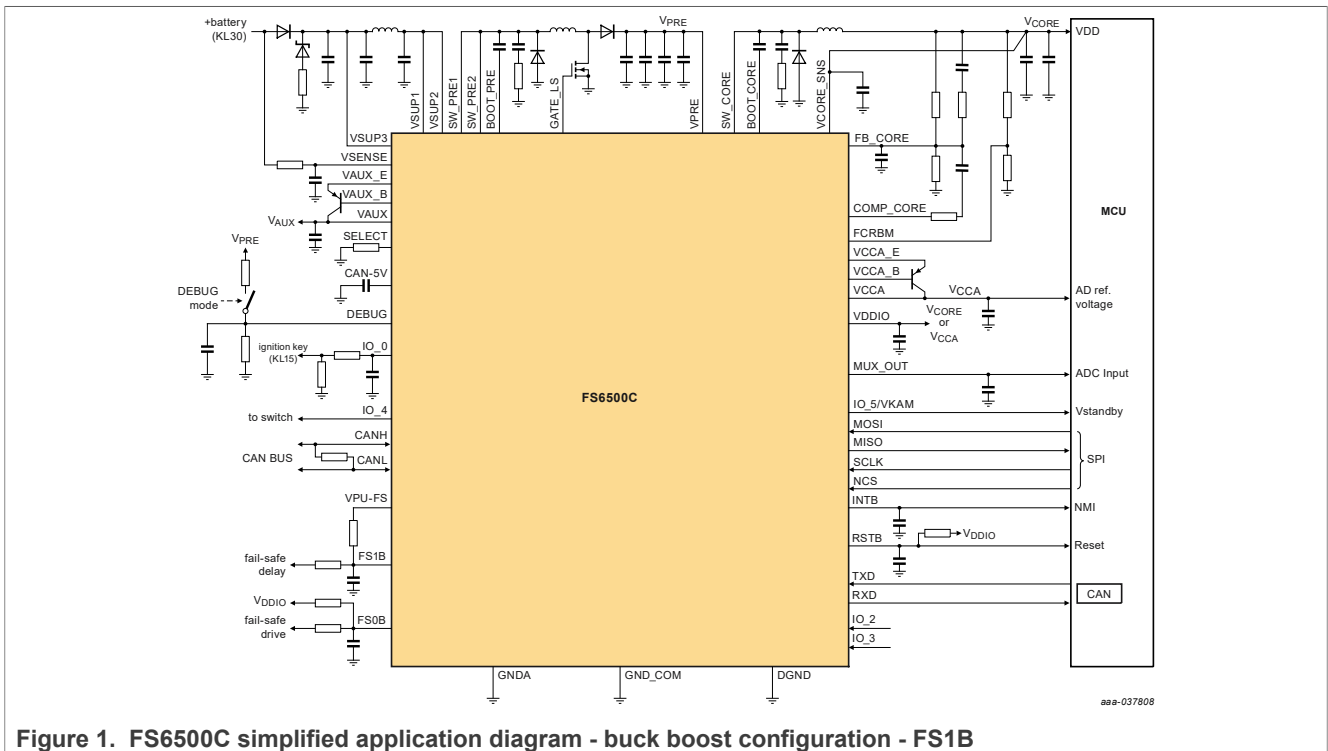
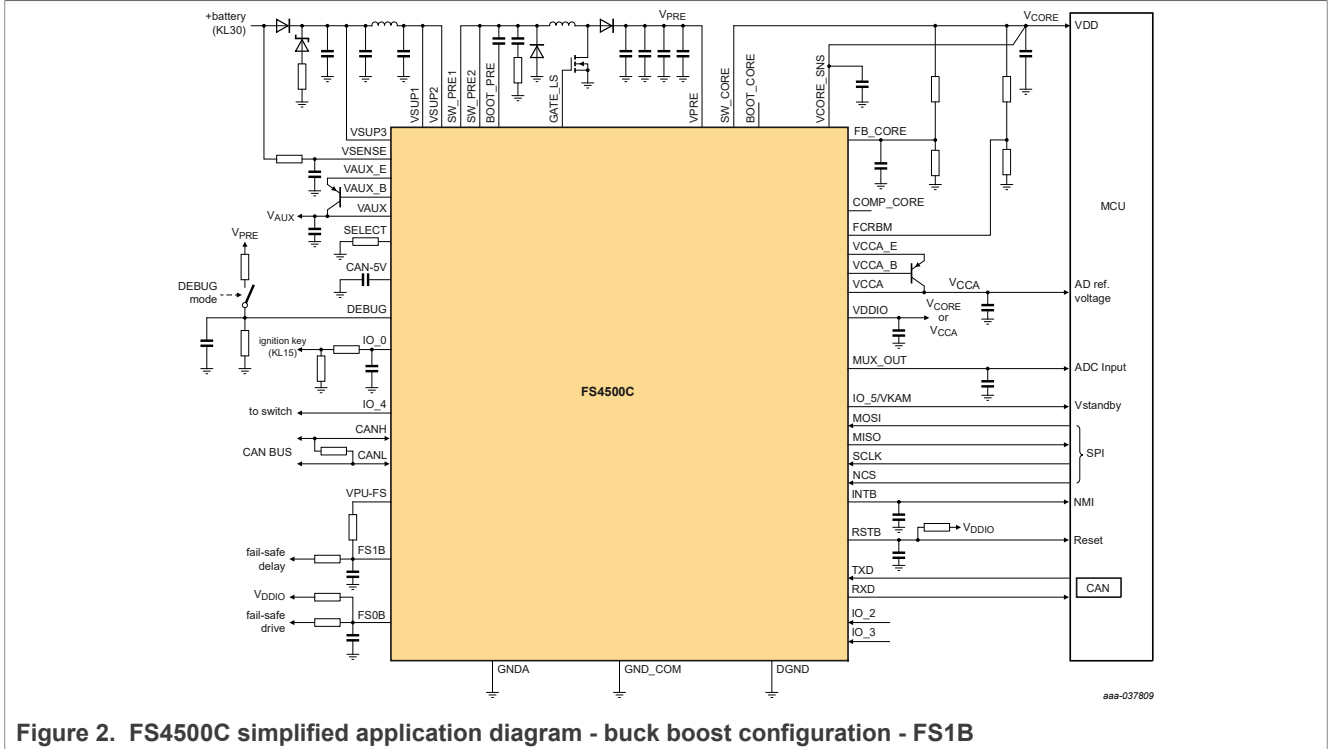


Figure 1. FS6500C simplified application diagram - buck boost configuration - FS1B



## 5 Ordering information

### 5.1 Part number definition

MC33FS c 5 x y z AE/R2

Table 1. Part number breakdown

Code	Option	Variable	Description
c	4 series	V <sub>CORE</sub> type	Linear
	6 series		DC-DC
x	0	V <sub>CORE</sub> current	0.5 A or 0.8 A
	1		1.5 A
	2		2.2 A
y	5	Functions	None
	6		FS1B
	7		LDT
	8		FS1B and LDT
z	N	Physical interface	None
	C		CAN FD
	K		LIN only
	L		CAN FD and LIN

**5.2 Part numbers list**

**Table 2. Orderable part variations**

Part Number	Temperature (T <sub>A</sub> )	Package	FS1B	LDT	VCORE	VCORE type	VKAM On	CAN FD	LIN	ASIL	Notes
MC33FS4505NAE	-40 °C to 125 °C	48-pin LQFP exposed pad	0	0	0.5 A	Linear	by SPI	0	0	B	[1]
MC33FS4505CAE			0	0	0.5 A	Linear	by SPI	1	0	B	
MC33FS4505KAE			0	0	0.5 A	Linear	By SPI	0	1	B	
MC33FS4505LAE			0	0	0.5 A	Linear	By SPI	1	1	B	
MC33FS4506NAE			1	0	0.5 A	Linear	by SPI	0	0	B	
MC33FS4506CAE			1	0	0.5 A	Linear	by SPI	1	0	B	
MC33FS4507NAE			0	1	0.5 A	Linear	by SPI	0	0	B	
MC33FS4507CAE			0	1	0.5 A	Linear	by SPI	1	0	B	
MC33FS4507KAE			0	1	0.5 A	Linear	by SPI	0	1	B	
MC33FS4507LAE			0	1	0.5 A	Linear	by SPI	1	1	B	
MC33FS4508NAE			1	1	0.5 A	Linear	by SPI	0	0	B	
MC33FS4508CAE			1	1	0.5 A	Linear	by SPI	1	0	B	
MC33FS6505NAE			0	0	0.8 A	DC-DC	by SPI	0	0	B	
MC33FS6505CAE			0	0	0.8 A	DC-DC	by SPI	1	0	B	
MC33FS6505KAE			0	0	0.8 A	DC-DC	by SPI	0	1	B	
MC33FS6505LAE			0	0	0.8 A	DC-DC	by SPI	1	1	B	
MC33FS6506NAE			1	0	0.8 A	DC-DC	by SPI	0	0	B	
MC33FS6506CAE			1	0	0.8 A	DC-DC	by SPI	1	0	B	
MC33FS6507NAE			0	1	0.8 A	DC-DC	by SPI	0	0	B	
MC33FS6507CAE			0	1	0.8 A	DC-DC	by SPI	1	0	B	
MC33FS6507KAE			0	1	0.8 A	DC-DC	by SPI	0	1	B	
MC33FS6507LAE			0	1	0.8 A	DC-DC	by SPI	1	1	B	
MC33FS6508NAE			1	1	0.8 A	DC-DC	by SPI	0	0	B	
MC33FS6508CAE			1	1	0.8 A	DC-DC	by SPI	1	0	B	
MC33FS6515NAE			0	0	1.5 A	DC-DC	by SPI	0	0	B	
MC33FS6515CAE			0	0	1.5 A	DC-DC	by SPI	1	0	B	
MC33FS6515KAE			0	0	1.5 A	DC-DC	by SPI	0	1	B	
MC33FS6515LAE			0	0	1.5 A	DC-DC	by SPI	1	1	B	
MC33FS6516NAE			1	0	1.5 A	DC-DC	by SPI	0	0	B	
MC33FS6516CAE			1	0	1.5 A	DC-DC	by SPI	1	0	B	
MC33FS6517NAE			0	1	1.5 A	DC-DC	by SPI	0	0	B	
MC33FS6517CAE			0	1	1.5 A	DC-DC	by SPI	1	0	B	
MC33FS6517KAE			0	1	1.5 A	DC-DC	by SPI	0	1	B	
MC33FS6517LAE			0	1	1.5 A	DC-DC	by SPI	1	1	B	
MC33FS6518NAE			1	1	1.5 A	DC-DC	by SPI	0	0	B	
MC33FS6518CAE			1	1	1.5 A	DC-DC	by SPI	1	0	B	
MC33FS6525NAE	0	0	2.2 A	DC-DC	by SPI	0	0	B			
MC33FS6525CAE	0	0	2.2 A	DC-DC	by SPI	1	0	B			

**Table 2. Orderable part variations...continued**

Part Number	Temperature (T <sub>A</sub> )	Package	FS1B	LDT	VCORE	VCORE type	VKAM On	CAN FD	LIN	ASIL	Notes
MC33FS6525KAE			0	0	2.2 A	DC-DC	by SPI	0	1	B	
MC33FS6525LAE			0	0	2.2 A	DC-DC	by SPI	1	1	B	
MC33FS6526NAE			1	0	2.2 A	DC-DC	by SPI	0	0	B	
MC33FS6526CAE			1	0	2.2 A	DC-DC	by SPI	1	0	B	
MC33FS6527NAE			0	1	2.2 A	DC-DC	by SPI	0	0	B	
MC33FS6527CAE			0	1	2.2 A	DC-DC	by SPI	1	0	B	
MC33FS6527KAE			0	1	2.2 A	DC-DC	by SPI	0	1	B	
MC33FS6527LAE			0	1	2.2 A	DC-DC	by SPI	1	1	B	
MC33FS6528NAE			1	1	2.2 A	DC-DC	by SPI	0	0	B	
MC33FS6528CAE			1	1	2.2 A	DC-DC	by SPI	1	0	B	

[1] To order parts in tape and reel, add the R2 suffix to the part number.

6 Block diagram

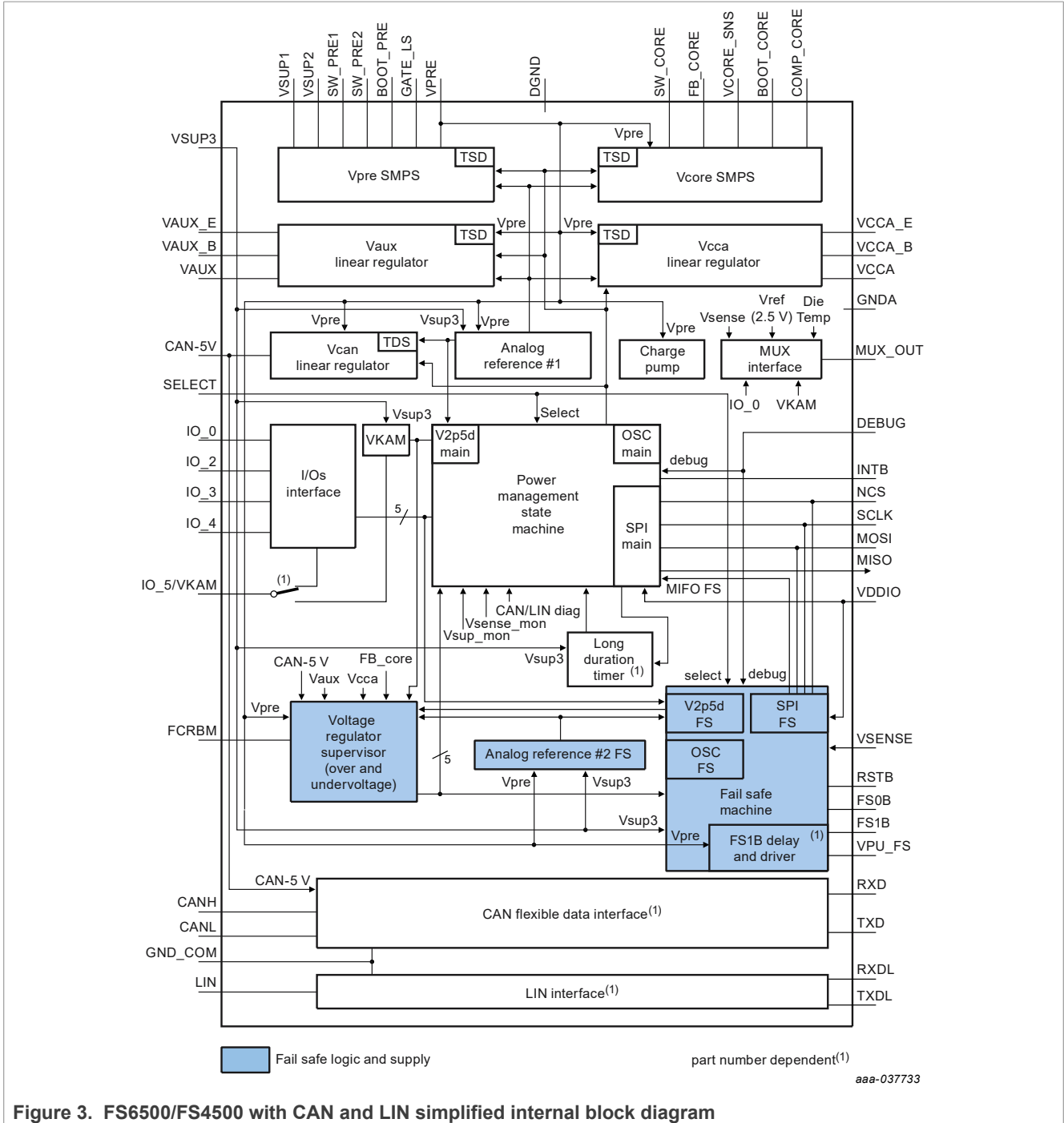
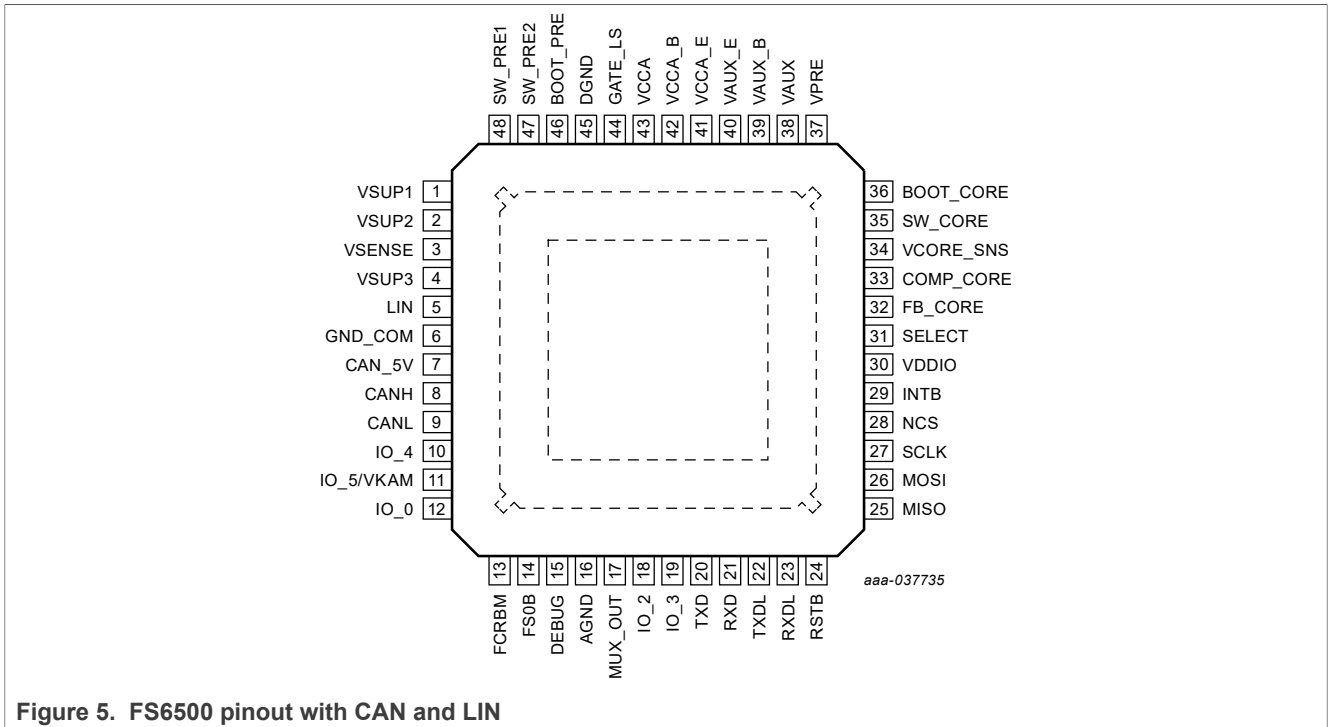
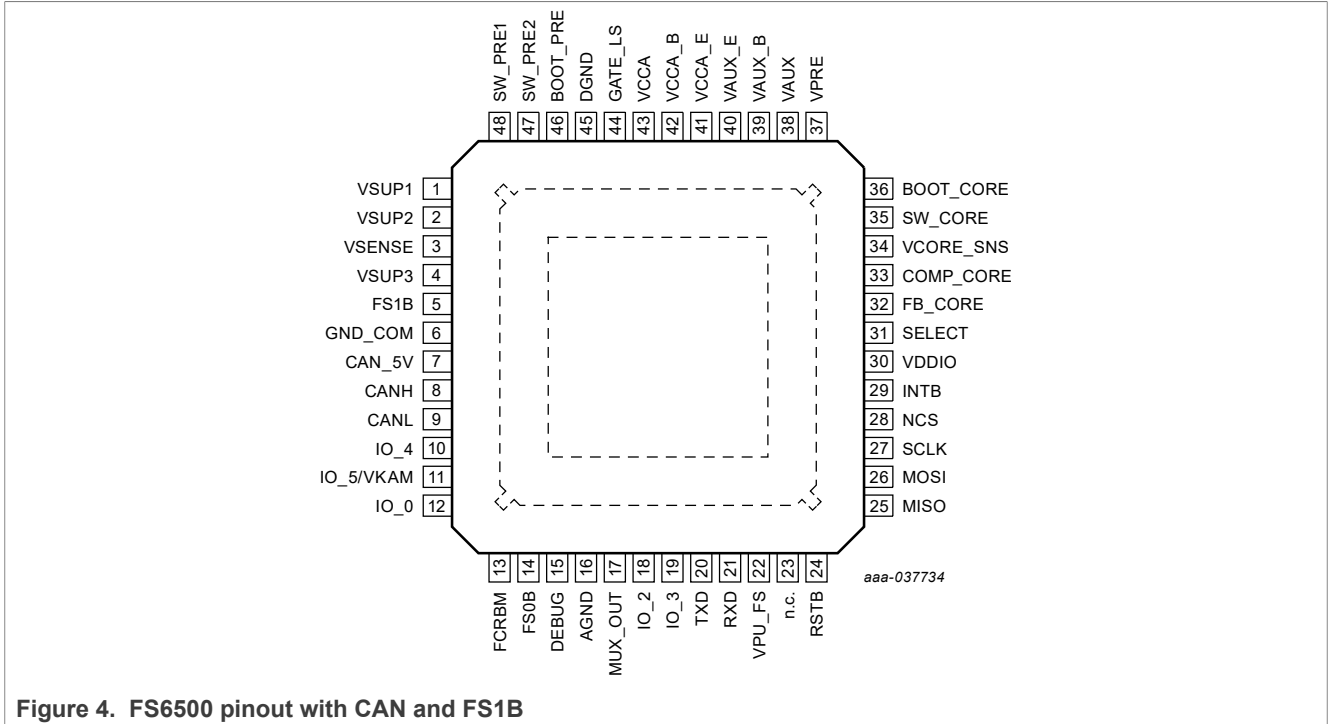


Figure 3. FS6500/FS4500 with CAN and LIN simplified internal block diagram

## 7 Pinning information

### 7.1 Pinning information



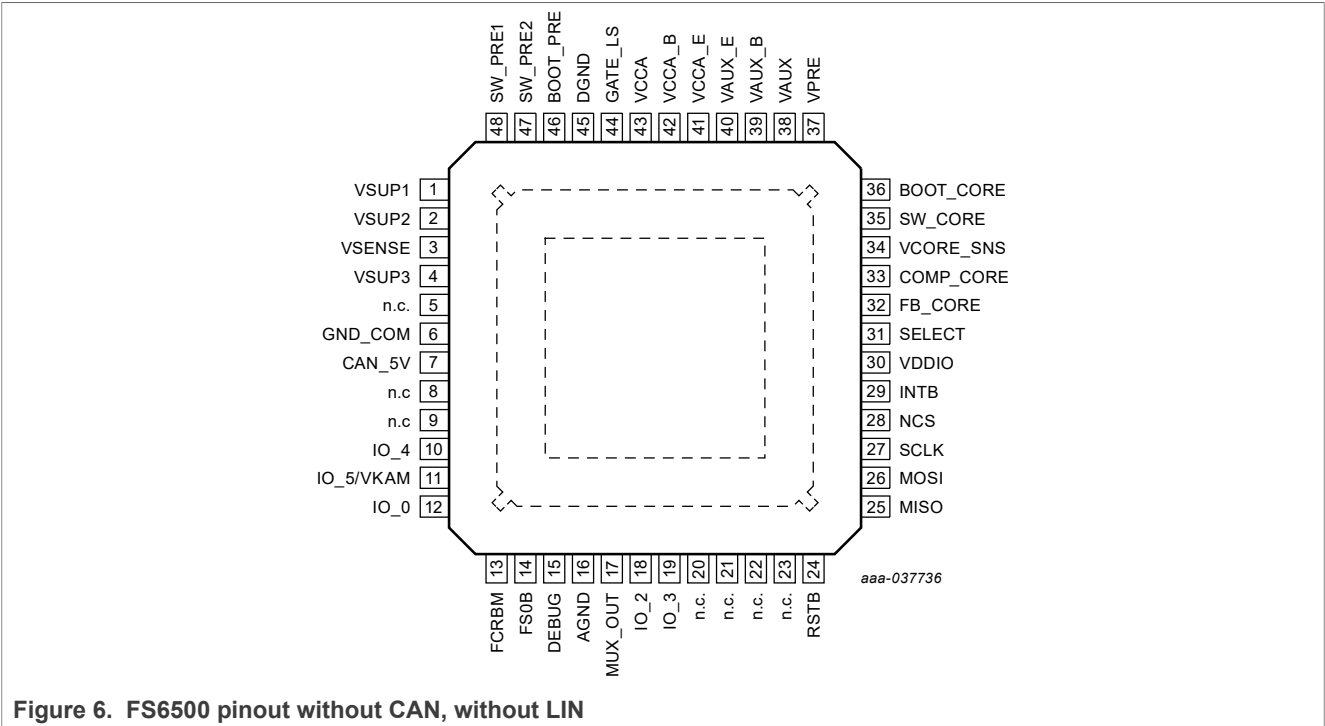


Figure 6. FS6500 pinout without CAN, without LIN

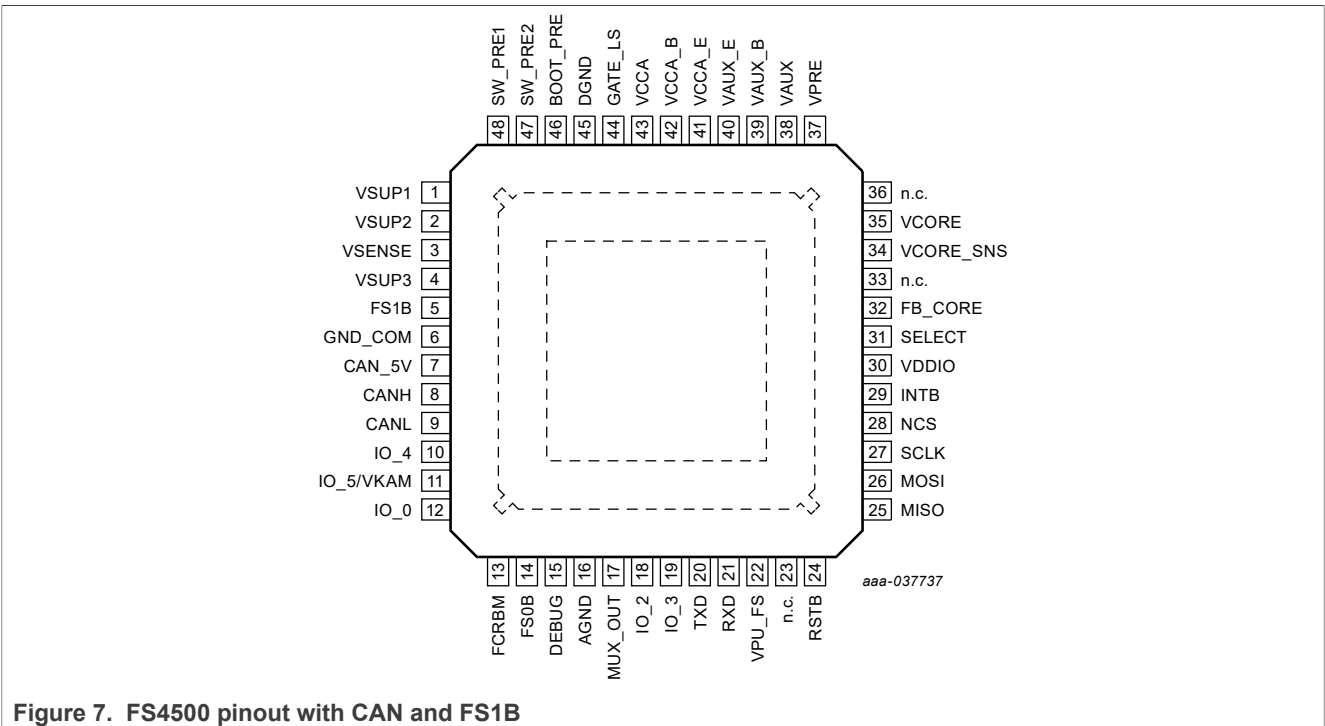


Figure 7. FS4500 pinout with CAN and FS1B



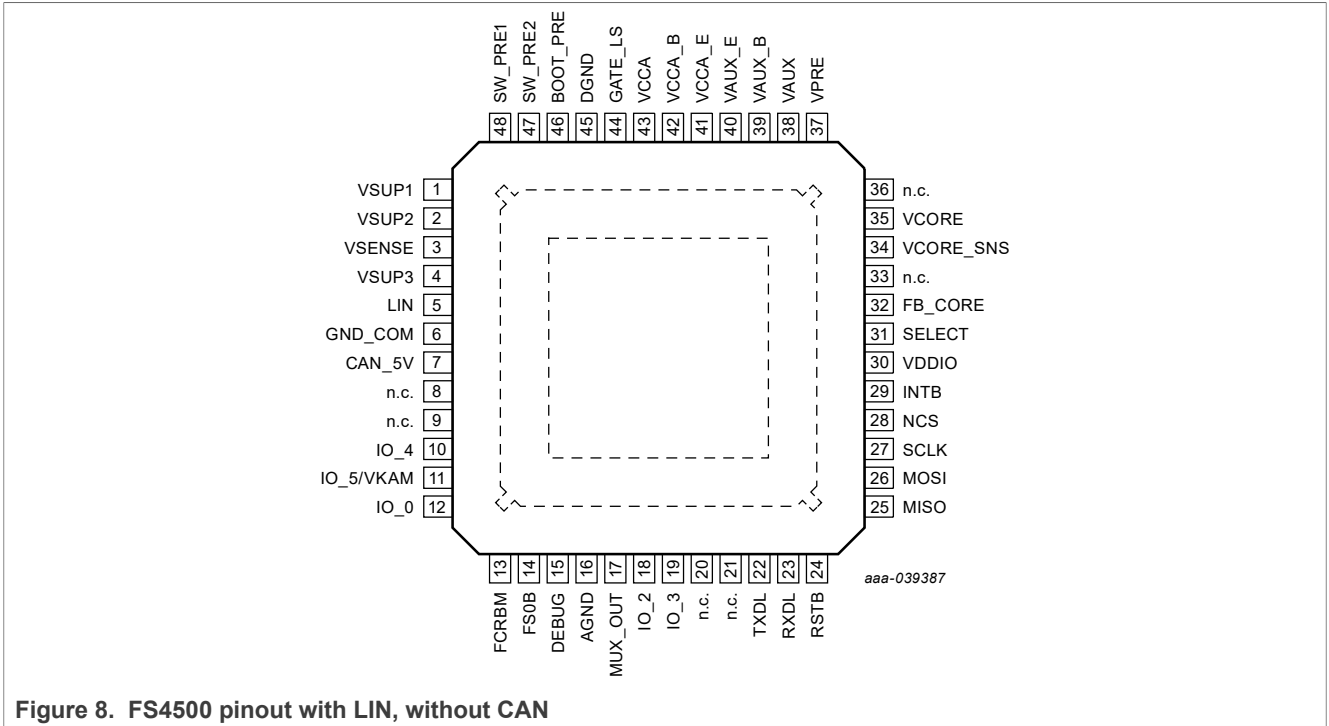


Figure 8. FS4500 pinout with LIN, without CAN

## 7.2 Pin description

A functional description of each pin can be found in [Section 11](#).

Table 3. FS6500/FS4500 pin definition

Pin number	Pin name	Type	Definition
1	VSUP1	A_IN	Power supply of the device. An external reverse battery protection diode in series is mandatory
2	VSUP2	A_IN	Second power supply. Protected by the external reverse battery protection diode used for VSUP1. VSUP1 and VSUP2 must be connected together externally.
3	VSENSE	A_IN	Sensing of the battery voltage. Must be connected prior to the reverse battery protection diode.
4	VSUP3	A_IN	Third power supply dedicated to the device supply. Protected by the external reverse battery protection diode used for VSUP1. Must be connected between the reverse protection diode and the input PI filter.
5	LIN	A_IN/OUT	LIN single-wire bus transmitter and receiver.
	or FS1B	D_OUT	Second output of the safety block (active low). The pin is asserted low at start-up and when a fault condition is detected, with a configurable delay or duration versus FS0B output terminal. Open drain structure.
	LIN and FS1B functions are exclusive. The differentiation is made by part numbers. When LIN is available, FS1B is not, and vice versa. If neither LIN, nor FS1B functions are used, this pin must be left open.		
6	GND_COM	GROUND	Dedicated ground for physical layers
7	CAN_5V	A_OUT	Output voltage for the embedded CAN FD interface
8	CANH	A_IN/OUT	CAN output high. If CAN function is not used, this pin must be left open.
9	CANL	A_IN/OUT	CAN output low. If CAN function is not used, this pin must be left open.
10	IO_4	D_IN A_OUT	Can be used as digital input (load dump proof) with wake-up capability or as an output gate driver <b>Digital input:</b> Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes (when used with IO_5). <b>Wake-up capability:</b> Can be selectable to wake-up on edges or levels. <b>Output gate driver:</b> Can drive a logic level low-side NMOS transistor. Controlled by the SPI.
11	IO_5/VKAM	A_IN D_IN A_OUT	Can be used as digital input with wake-up capability or as an analog output providing keep alive memory supply in low-power mode. <b>Analog input:</b> Pin status can be read through the MUX output terminal <b>Digital input:</b> Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes (when used with IO_4). <b>Wake-up capability:</b> Can be selectable to wake-up on edges or levels. <b>Supply output:</b> Provide keep alive memory supply in low-power mode
12	IO_0	A_IN D_IN	Can be used as analog or digital input (load dump proof) with wake-up capability (selectable) <b>Analog input:</b> Pin status can be read through the MUX output terminal <b>Digital input:</b> Pin status can be read through the SPI. <b>Wake-up capability:</b> Can be selectable to wake-up on edges or levels.
13	FCRBM	A_IN	Feedback core resistor bridge monitoring: For safety purposes, this pin is used to monitor the middle point of a redundant resistor bridge connected on V <sub>CORE</sub> (in

Table 3. FS6500/FS4500 pin definition...continued

Pin number	Pin name	Type	Definition
			parallel to the one used to set the $V_{CORE}$ voltage). If not used, this pin must be connected directly to FB_CORE.
14	FS0B	D_OUT	First output of the safety block (active low). The pin is asserted low at start-up and when a fault condition is detected. Open drain structure.
15	DEBUG	D_IN	Debug mode entry input
16	AGND	GROUND	Analog ground connection
17	MUX_OUT	A_OUT	Multiplexed output to be connected to a MCU ADC. Selection of the analog parameter is available at MUX-OUT through the SPI.
18 19	IO_2:3	D_IN	Digital input pin with wake-up capability (logic level compatible) <b>Digital input:</b> Pin status can be read through the SPI. <b>Wake-up capability:</b> Can be selectable to wake-up on edges or levels.
20	TXD	D_IN	Transceiver input from the MCU which controls the state of the CAN-bus. Internal pull-up to VDDIO. If CAN function is not used, this pin must be left open.
21	RXD	D_OUT	Receiver output which reports the state of the CAN-bus to the MCU If CAN function is not used, this pin must be left open.
22	TXDL	D_IN	Transceiver input from the MCU controlling the state of the LIN bus. Internal pull-up to VDDIO.
	or VPU_FS	A_OUT	Pull-up output for FS1B function.
LIN and FS1B functions are exclusive. The differentiation is made by part numbers. When LIN is available, FS1B is not, and vice versa. If neither LIN, nor FS1B functions are used, this pin must be left open.			
23	RXDL	D_OUT	Receiver output reporting the state of the LIN bus to the MCU. If LIN function is not used, this pin must be left open.
24	RSTB	D_OUT	This output is asserted low when the safety block reports a failure. The main function is to reset the MCU. Reset input voltage is also monitored in order to detect external reset and fault condition. Open drain structure.
25	MISO	D_OUT	SPI bus. primary input secondary output
26	MOSI	D_IN	SPI bus. primary output secondary input
27	SCLK	D_IN	SPI Bus. Serial clock
28	NCS	D_IN	Not chip select (active low)
29	INTB	D_OUT	This output pin generates a low pulse when an Interrupt condition occurs. Pulse duration is configurable. Internal pull-up to VDDIO.
30	VDDIO	A_IN	Input voltage for MISO output buffer. Allows voltage compatibility with MCU I/Os.
31	SELECT	D_IN	Hardware selection pin for VAUX and VCCA output voltages
32	FB_CORE	A_IN	VCORE voltage feedback. Input of the error amplifier.
33	COMP_CORE	A_OUT	Compensation network. Output of the error amplifier. For FS4500 series, this pin must be left open (NC).
34	VCORE_SNS	A_IN	VCORE input voltage sense
35	SW_CORE	A_OUT	VCORE output switching point for FS6500 series

Table 3. FS6500/FS4500 pin definition...continued

Pin number	Pin name	Type	Definition
	or VCORE	A_OUT	VCORE output voltage for FS4500 series
36	BOOT_CORE	A_IN/OUT	Bootstrap capacitor for VCORE internal NMOS gate drive For FS4500 series, this pin must be left open (NC).
37	VPRE	A_IN	VPRE input voltage sense
38	VAUX	A_OUT	VAUX output voltage. External PNP ballast transistor. Collector connection
39	VAUX_B	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Base connection
40	VAUX_E	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Emitter connection
41	VCCA_E	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Emitter connection
42	VCCA_B	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Base connection
43	VCCA	A_OUT	VCCA output voltage. External PNP ballast transistor. Collector connection
44	GATE_LS	A_OUT	Low-side MOSFET gate drive for non-inverting buck-boost configuration
45	DGND	GROUND	Digital ground connection
46	BOOT_PRE	A_IN/OUT	Bootstrap capacitor for the VPRE internal NMOS gate drive
47	SW_PRE2	A_OUT	Second pre-regulator output switching point
48	SW_PRE1	A_OUT	First pre-regulator output switching point

## 8 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
<b>Electrical ratings</b>				
V <sub>SUP1/2/3</sub>	DC voltage at power supply pins	-1.0 to 40	V	[1]
V <sub>SENSE</sub>	DC voltage at battery sense pin (with ext R in series mandatory)	-14 to 40	V	
V <sub>SW1,2</sub>	DC voltage at SW_PRE1 and SW_PRE2 Pins	-1.0 to 40	V	
V <sub>PRE</sub>	DC voltage at VPRE Pin	-0.3 to 8	V	
V <sub>GATE_LS</sub>	DC voltage at Gate_LS pin	-0.3 to 8	V	
V <sub>BOOT_PRE</sub>	DC voltage at BOOT_PRE pin	-1.0 to 50	V	
V <sub>SW_CORE</sub>	DC voltage at SW_CORE pin	-1.0 to 8	V	
V <sub>CORE_SNS</sub>	DC voltage at VCORE_SNS pin	0.0 to 8	V	
V <sub>BOOT_CORE</sub>	DC voltage at BOOT_CORE pin	0.0 to 15	V	
V <sub>FB_CORE</sub>	DC voltage at FB_CORE pin	-0.3 to 2.5	V	
V <sub>COMP_CORE</sub>	DC voltage at COMP_CORE pin	-0.3 to 2.5	V	
V <sub>FCRBM</sub>	DC voltage at FCRBM pin	-0.3 to 8	V	
V <sub>AUX_B,E</sub>	DC voltage at VAUX_B, VAUX_E pins	-0.3 to 40	V	
V <sub>AUX</sub>	DC voltage at VAUX pin	-2.0 to 40	V	
V <sub>CCA_B,E</sub>	DC voltage at VCCA_B, VCCA_E pins	-0.3 to 8	V	
V <sub>CCA</sub>	DC voltage at VCCA pin	-0.3 to 8	V	

**Table 4. Maximum ratings ...continued**

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
V <sub>DDIO</sub>	DC voltage at VDDIO pin	-0.3 to 8	V	
V <sub>CAN_5V</sub>	DC voltage on CAN_5V pin	-0.3 to 8	V	
V <sub>PU_FS</sub>	DC voltage at VPU_FS pin	-0.3 to 8	V	
V <sub>FSxB</sub>	DC voltage at FS0B, FS1B pins (with ext R in series mandatory)	-0.3 to 40	V	
V <sub>DEBUG</sub>	DC voltage at DEBUG pin	-0.3 to 40	V	
V <sub>IO_0,4</sub>	DC voltage at IO_0, IO_4 pins (with ext R in series mandatory)	-0.3 to 40	V	
V <sub>IO_5</sub>	DC voltage at IO_5 pin	-0.3 to 20	V	
V <sub>KAM</sub>	DC voltage at VKAM pin	-0.3 to 8	V	
V <sub>DIG</sub>	DC voltage at INTB, RSTB, MISO, MOSI, NCS, SCLK, MUX_OUT, RXD, TXD, RXDL, TXDL, IO_2, IO_3 pins	-0.3 to 8	V	
V <sub>SELECT</sub>	DC voltage at SELECT pin	-0.3 to 8	V	
V <sub>BUS_CAN</sub>	DC voltage on CANL, CANH pins	-27 to 40	V	
I <sub>Isense</sub>	V <sub>SENSE</sub> maximum current capability	-5.0 to 5.0	mA	
I <sub>IO_0, 4, 5</sub>	IOs maximum current capability (IO_0, IO_4, IO_5)	-5.0 to 5.0	mA	
<b>ESD voltage</b>				
<b>Human body model (JESD22/A114)<sup>(19)</sup> – 100 pF, 1.5 kΩ</b>				
V <sub>ESD-HBM1</sub>	• All pins	±2.0	kV	[2]
V <sub>ESD-HBM2</sub>	• VSUP1, 2, 3, VSENSE, VAUX, IO_0,4, FS0B, FS1B, DEBUG	±4.0	kV	
V <sub>ESD-HBM3</sub>	• CANH, CANL	±6.0	kV	
V <sub>ESD-HBM4</sub>	• LIN	±8.0	kV	
<b>Charge device model (JESD22/C101)<sup>(20)</sup>:</b>				
V <sub>ESD-CDM1</sub>	• All pins	±500	V	
V <sub>ESD-CDM2</sub>	• Corner pins	±750	V	
<b>System level ESD (gun test)</b>				
	• VSUP1, 2, 3, VSENSE, VAUX, IO_0, 4, 5, FS0B, FS1B			
V <sub>ESD-GUN1</sub>	330 Ω/150 pF unpowered according to IEC 61000-4-2: <sup>(16)</sup>	±8.0	kV	
V <sub>ESD-GUN2</sub>	330 Ω/150 pF unpowered according to OEM LIN, CAN, FlexRay Conformance	±8.0	kV	
V <sub>ESD-GUN3</sub>	2.0 kΩ/150 pF unpowered according to ISO 10605 <sup>(15)</sup>	±8.0	kV	
V <sub>ESD-GUN4</sub>	2.0 kΩ/330 pF powered according to ISO 10605 <sup>(15)</sup>	±8.0	kV	
	• CANH, CANL			
V <sub>ESD-GUN5</sub>	330 Ω/150 pF unpowered according to IEC 61000-4-2: <sup>(16)</sup>	±15.0	kV	
V <sub>ESD-GUN6</sub>	330 Ω/150 pF unpowered according to OEM LIN, CAN, FlexRay Conformance	±12.0	kV	
V <sub>ESD-GUN7</sub>	2.0 kΩ/150 pF unpowered according to ISO 10605 <sup>(15)</sup>	±15.0	kV	
V <sub>ESD-GUN8</sub>	2.0 kΩ/330 pF powered according to ISO 10605 <sup>(15)</sup>	±12.0	kV	
	• LIN			
V <sub>ESD-GUN9</sub>	330 Ω/150 pF unpowered according to IEC 61000-4-2: <sup>(16)</sup>	±12.0	kV	
V <sub>ESD-GUN10</sub>	330 Ω/150 pF unpowered according to OEM LIN, CAN, FlexRay conformance	±12.0	kV	

**Table 4. Maximum ratings ...continued**

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
V <sub>ESD-GUN11</sub>	2.0 kΩ/150 pF unpowered according to ISO 10605 <sup>[15]</sup>	±12.0	kV	
V <sub>ESD-GUN12</sub>	2.0 kΩ/330 pF powered according to ISO 10605 <sup>[15]</sup>	±12.0	kV	
<b>Thermal ratings</b>				
T <sub>A</sub>	Ambient temperature	-40 to 125	°C	
T <sub>J</sub>	Junction temperature	-40 to 150	°C	
T <sub>STG</sub>	Storage temperature	-55 to 150	°C	
<b>Thermal resistance</b>				
R <sub>θJA</sub>	Thermal resistance junction to ambient	30	°C/W	[3]
R <sub>θJCTOP</sub>	Thermal resistance junction to case top	23.8	°C/W	[4]
R <sub>θJCBOTTOM</sub>	Thermal resistance junction to case bottom	0.9	°C/W	[5]

[1] All V<sub>SUPS</sub> (V<sub>SUP1/2/3</sub>) must be connected to the same supply (Figure 70).

[2] Compared to AGND.

[3] Per JEDEC JESD51-6<sup>[17]</sup> with the board (JESD51-7)<sup>[18]</sup> horizontal.

[4] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC - 883 Method 1012.1)<sup>[21]</sup>.

[5] Thermal resistance between the die and the solder pad on the bottom of the packaged based on simulation without any interface resistance.

## 9 Static electrical characteristics

**Table 5. Static electrical characteristics**

T<sub>A</sub> = -40 °C to 125 °C, unless otherwise specified. V<sub>SUP</sub> = V<sub>SUP\_UV\_L</sub> to 36 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V<sub>SUP</sub> < 36 V, thermal dissipation must be considered (see Figure 29).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
<b>Power supply</b>						
I <sub>SUP123</sub>	Power supply current in normal mode	—	—	15.0	mA	
I <sub>SUP3</sub>	Power supply current for VSUP3 in normal mode	—	3.5	5.0	mA	
I <sub>SUP_LPOFF1</sub>	Power supply current in LPOFF (V <sub>SUP</sub> = 14 V at T <sub>A</sub> = 25 °C)	—	32	—	μA	[1]
I <sub>SUP_LPOFF2</sub>	Power supply current in LPOFF (V <sub>SUP</sub> = 18 V at T <sub>A</sub> = 80 °C)	—	42	60	μA	
V <sub>SNS_UV</sub>	Power supply undervoltage warning	7.0	8.0	9.0	V	
V <sub>SNS_UV_HYST</sub>	Power supply undervoltage warning hysteresis	0.1	—	0.5	V	
V <sub>SUP_IPFF</sub>	I <sub>PF</sub> input voltage detection	21	—	27	V	
V <sub>SUP_IPFF_HYST</sub>	I <sub>PF</sub> input voltage hysteresis	0.2	—	—	V	
V <sub>SUP_UV_7</sub>	Power supply undervoltage lockout (power up)	7.0	—	8.0	V	
V <sub>SUP_UV_5</sub>	Power supply undervoltage lockout (power up)	—	—	5.6	V	
V <sub>SUP_UV_L</sub>	Power supply undervoltage lockout (falling — boost configuration)	—	—	2.7	V	
V <sub>SUP_UV_L_B</sub>	Power supply undervoltage lockout (falling — buck configuration)	—	—	4.5	V	[2]
V <sub>SUP_UV_LPOFF</sub>	Power supply undervoltage lockout in LPOFF	—	—	4.5	V	[3]
V <sub>SUP_UV_HYST</sub>	Power supply undervoltage lockout hysteresis	—	0.1	—	V	[4]

**Table 5. Static electrical characteristics ...continued**

$T_A = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 36 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 36\text{ V}$ , thermal dissipation must be considered (see [Figure 29](#)).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
<b>V<sub>PRE</sub> voltage pre-regulator</b>						
V <sub>PRE</sub>	V <sub>PRE</sub> output voltage				V	
	• Buck mode ( $V_{SUP} > V_{SUP\_UV\_7}$ )	6.25	—	6.75		
	• Buck mode ( $V_{SUP\_UV\_7} \geq V_{SUP} \geq 4.5\text{ V}$ )	$V_{PRE\_UV\_4P3}$	$V_{SUP} - R_{DS(on)\_PRE} * I_{PRE}$	—		
	• Boost mode ( $V_{SUP} \geq 2.7\text{ V}$ )	6.0	—	7.0		
I <sub>PRE</sub>	V <sub>PRE</sub> maximum output current capability				A	[4]
	• Buck or boost with $V_{SUP} > V_{SUP\_UV\_7}$	2.0	—	—		
	• Buck with $V_{SUP\_UV\_7} \geq V_{SUP} \geq 4.5\text{ V}$	0.5	2.0	—		
	• Boost with $V_{SUP\_UV\_7} \geq V_{SUP} \geq 6.0\text{ V}$	2.0	—	—		
	• Boost with $6.0\text{ V} \geq V_{SUP} \geq 4.0\text{ V}$	1.0	—	—		
	• Boost with $4.0\text{ V} \geq V_{SUP} \geq 2.7\text{ V}$	0.3	—	—		
I <sub>PRE\_LIM1</sub>	SW <sub>PRE</sub> output current limitation in buck-boost mode ( $V_{SUP} \leq 28\text{ V}$ )	3.5	—	—	A	
I <sub>PRE\_LIM2</sub>	SW <sub>PRE</sub> output current limitation in buck mode ( $V_{SUP} \leq 28\text{ V}$ )	2.5	—	—	A	
I <sub>PRE\_OC</sub>	SW <sub>PRE</sub> overcurrent detection threshold in buck mode ( $V_{SUP} \leq 28\text{ V}$ )	4.5	—	—	A	
V <sub>PRE\_UV</sub>	V <sub>PRE</sub> undervoltage detection threshold (falling)	5.5	—	6.0	V	
V <sub>PRE\_UV\_HYST</sub>	V <sub>PRE</sub> undervoltage hysteresis	0.05	—	0.15	V	[5]
V <sub>PRE\_UV\_4P3</sub>	V <sub>PRE</sub> shut-off threshold (falling – buck and buck/boost)	4.1	—	4.5	V	
V <sub>PRE\_UV\_4P3\_HYST</sub>	V <sub>PRE</sub> shut-off hysteresis	0.05	—	0.15	V	[5]
R <sub>DSON\_PRE</sub>	V <sub>PRE</sub> pass transistor on resistance with $V_{SUP} \leq 28\text{ V}$	—	—	200	mΩ	
L <sub>IR\_VPRE</sub>	V <sub>PRE</sub> line regulation	—	20	—	mV	[5]
LOR <sub>VPRE\_BUCK</sub>	V <sub>PRE</sub> load regulation for C <sub>OUT\_VPRE</sub> = 57 μF • I <sub>PRE</sub> from 50 mA to 2.0 A - buck mode	—	100	—	mV	[5]
LOR <sub>VPRE\_BOOST</sub>	V <sub>PRE</sub> load regulation for C <sub>OUT\_VPRE</sub> = 57 μF • I <sub>PRE</sub> from 50 mA to 2.0 A - boost mode	—	500	—	mV	[5]
V <sub>PRE\_LL\_H</sub> V <sub>PRE\_LL\_L</sub>	V <sub>PRE</sub> pulse skipping thresholds	—	200 180	—	mV	
T <sub>WARN\_PRE</sub>	V <sub>PRE</sub> thermal warning threshold	—	125	—	°C	
T <sub>SD\_PRE</sub>	V <sub>PRE</sub> thermal shutdown threshold	160	—	—	°C	
T <sub>SD\_PRE\_HYST</sub>	V <sub>PRE</sub> thermal shutdown hysteresis	—	10	—	°C	[5]
V <sub>G\_LS\_OH</sub>	LS gate driver high output voltage (I <sub>OUT</sub> = 50 mA)	$V_{PRE} - 1$	—	$V_{PRE}$	V	
V <sub>G\_LS\_OL</sub>	LS gate driver low level (I <sub>OUT</sub> = 50 mA)	—	—	0.5	V	
I <sub>G\_LS</sub>	LS gate driver current capability	—	300	—	mA	
R <sub>G\_SHORT</sub>	GATE <sub>LS</sub> pin short to GND resistance to detect buck mode only	—	—	10	Ω	

**Table 5. Static electrical characteristics ...continued**

$T_A = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 36 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 36\text{ V}$ , thermal dissipation must be considered (see [Figure 29](#)).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
<b>V<sub>core</sub> voltage regulator</b>						
V <sub>CORE_FB</sub>	V <sub>CORE</sub> feedback input voltage	0.784	0.8	0.816	V	
I <sub>PD_CORE</sub>	V <sub>CORE</sub> internal pull-down current (active when V <sub>CORE</sub> is enabled)	5.0	12	25	mA	
I <sub>CORE</sub>	V <sub>CORE</sub> output current capability in normal mode • FS450x • FS650x • FS651x • FS652x	—	—	0.5 0.8 1.5 2.2	A	
I <sub>CORE_LIM</sub>	V <sub>CORE</sub> output current limitation • FS450x • FS650x • FS651x • FS652x	0.55 1 1.8 2.5	— — — —	1.7 2 2.8 3.5	A	
R <sub>DSON_CORE</sub>	V <sub>CORE</sub> pass transistor on resistance	—	—	200	mΩ	
FS65_ LOR <sub>V<sub>CORE</sub>_1.2</sub>	V <sub>CORE</sub> transient load regulation – 1.2 V range C <sub>OUT_V<sub>CORE</sub></sub> = 40 μF, I <sub>CORE</sub> = 10 mA to 2.2 A, dI <sub>CORE</sub> /dt ≤ 2.0 A/μs	-60	—	60	mV	[4]
FS65_ LOR <sub>V<sub>CORE</sub>_3.3</sub>	V <sub>CORE</sub> transient load regulation – 3.3 V range C <sub>OUT_V<sub>CORE</sub></sub> = 40 μF, I <sub>CORE</sub> = 10 mA to 1.5 A, dI <sub>CORE</sub> /dt ≤ 2.0 A/μs	-100	—	100	mV	[4]
FS65_ LOR <sub>V<sub>CORE</sub>_5</sub>	V <sub>CORE</sub> transient load regulation – 5.0 V range C <sub>OUT_V<sub>CORE</sub></sub> = 20 μF, I <sub>CORE</sub> = 10 mA to 0.8 A, dI <sub>CORE</sub> /dt ≤ 2.0 A/μs	-150	—	150	mV	[4]
FS45_ LOR <sub>V<sub>CORE</sub>_1.2</sub>	V <sub>CORE</sub> transient load regulation – 1.2 V range C <sub>OUT_V<sub>CORE</sub></sub> = 20 μF, I <sub>CORE</sub> = 10 mA to 0.2 A, dI <sub>CORE</sub> /dt ≤ 0.5 A/μs	-60	—	60	mV	[4]
FS45_ LOR <sub>V<sub>CORE</sub>_3.3</sub>	V <sub>CORE</sub> transient load regulation – 3.3 V range C <sub>OUT_V<sub>CORE</sub></sub> = 20 μF, I <sub>CORE</sub> = 10 mA to 0.35 A, dI <sub>CORE</sub> /dt ≤ 0.5 A/μs	-100	—	100	mV	[4]
FS45_ LOR <sub>V<sub>CORE</sub>_5</sub>	V <sub>CORE</sub> transient load regulation – 5 V range C <sub>OUT_V<sub>CORE</sub></sub> = 20 μF, I <sub>CORE</sub> = 10 mA to 0.5 A, dI <sub>CORE</sub> /dt ≤ 0.5 A/μs	-150	—	150	mV	[4]
V <sub>CORE_LL_H</sub> V <sub>CORE_LL_L</sub>	V <sub>CORE</sub> pulse skipping thresholds	— —	180 160	— —	mV	
T <sub>WARN_CORE</sub>	V <sub>CORE</sub> thermal warning threshold	—	125	—	°C	
T <sub>SD_CORE</sub>	V <sub>CORE</sub> thermal shutdown threshold	160	—	—	°C	
T <sub>SD_CORE_HYST</sub>	V <sub>CORE</sub> thermal shutdown hysteresis	—	10	—	°C	[4]
<b>V<sub>CCA</sub> voltage regulator</b>						
V <sub>CCA</sub>	V <sub>CCA</sub> output voltage • 5.0 V configuration with Internal ballast at 100 mA • 5.0 V configuration with external ballast at 200 mA • 5.0 V configuration with external ballast at 300 mA • 3.3 V configuration with Internal ballast at 100 mA • 3.3 V configuration with external ballast at 200 mA • 3.3 V configuration with external ballast at 300 mA	4.95 4.9 4.85 3.267 3.234 3.201	5.0 5.0 5.0 3.3 3.3 3.3	5.05 5.1 5.15 3.333 3.366 3.399	V	[6]
I <sub>CCA_IN</sub>	V <sub>CCA</sub> output current (int. MOSFET)	—	—	100	mA	



**Table 5. Static electrical characteristics ...continued**

$T_A = -40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 36 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 36\text{ V}$ , thermal dissipation must be considered (see [Figure 29](#)).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
I <sub>CCA_OUT</sub>	V <sub>CCA</sub> output current (external PNP)	—	—	300	mA	
I <sub>CCA_LIM_INT</sub>	V <sub>CCA</sub> output current limitation (int. MOSFET)	100	—	675	mA	
I <sub>CCA_LIM_OUT</sub>	V <sub>CCA</sub> output current limitation (external PNP)	300	—	675	mA	
I <sub>CCA_LIM_FB</sub>	V <sub>CCA</sub> output current limitation foldback	60	—	240	mA	
V <sub>CCA_LIM_FB</sub>	V <sub>CCA</sub> output voltage foldback threshold	0.6	—	1.2	V	
V <sub>CCA_LIM_HYST</sub>	V <sub>CCA</sub> output voltage foldback hysteresis	0.03	—	0.3	V	
I <sub>CCA_BASE_SC</sub> I <sub>CCA_BASE_SK</sub>	V <sub>CCA</sub> base current capability	— 20	-20 65	-30 —	mA	
T <sub>WARN_CCA</sub>	V <sub>CCA</sub> thermal warning threshold (int. MOSFET only)	—	125	—	°C	
TSD <sub>CCA</sub>	V <sub>CCA</sub> thermal shutdown threshold (int. MOSFET only)	160	—	—	°C	
TSD <sub>CCA_HYST</sub>	V <sub>CCA</sub> thermal shutdown hysteresis	—	10	—	°C	[5]
LOR <sub>VCCA</sub>	V <sub>CCA</sub> static load regulation • I <sub>CCA</sub> = 10 mA to 100 mA (internal MOSFET) • I <sub>CCA</sub> = 10 mA to 300 mA (external ballast)	—	15	—	mV	[5]
LORT <sub>VCCA</sub>	V <sub>CCA</sub> transient load regulation • I <sub>CCA</sub> = 10 mA to 100 mA (internal MOSFET) • I <sub>CCA</sub> = 10 mA to 300 mA (external ballast)	—	—	1.0	%	[5]
R <sub>PD_CCA</sub>	V <sub>CCA</sub> internal pull-down resistor (active when V <sub>CCA</sub> is disabled)	50	—	170	Ω	
<b>V<sub>AUX</sub> voltage regulator</b>						
V <sub>AUX_5</sub>	V <sub>AUX</sub> output voltage (5.0 V configuration)	4.85	5.0	5.15	V	
V <sub>AUX_33</sub>	V <sub>AUX</sub> output voltage (3.3 V configuration)	3.2	3.3	3.4	V	
V <sub>AUX_TRK</sub>	V <sub>AUX</sub> tracking error (V <sub>AUX_5</sub> and V <sub>AUX_33</sub> )	-15	—	+15	mV	
I <sub>AUX_OUT</sub>	V <sub>AUX</sub> output current	—	—	400	mA	
I <sub>AUX_LIM</sub>	V <sub>AUX</sub> output current limitation	400	—	800	mA	
I <sub>AUX_LIM_FB</sub>	V <sub>AUX</sub> output current limitation foldback	60	—	240	mA	
V <sub>AUX_LIM_FB</sub>	V <sub>AUX</sub> output voltage foldback threshold	0.6	—	1.2	V	
V <sub>AUX_LIM_HYST</sub>	V <sub>AUX</sub> output voltage foldback hysteresis	0.03	—	0.3	V	
I <sub>AUX_BASE_SC</sub> I <sub>AUX_BASE_SK</sub>	V <sub>AUX</sub> base current capability	— 7.0	-15 30	-7.0 —	mA	
TSD <sub>AUX</sub>	V <sub>AUX</sub> thermal shutdown threshold	160	—	—	°C	
TSD <sub>AUX_HYST</sub>	V <sub>AUX</sub> thermal shutdown hysteresis	—	10	—	°C	[5]
LOR <sub>VAUX</sub>	V <sub>AUX</sub> static load regulation (I <sub>AUX_OUT</sub> = 10 mA to 400 mA)	—	15	—	mV	[5]
LORT <sub>VAUX</sub>	V <sub>AUX</sub> transient load regulation • I <sub>AUX_OUT</sub> = 10 mA to 400 mA	—	—	1.0	%	[5]
R <sub>PD_AUX</sub>	V <sub>AUX</sub> internal pull-down resistor (active when V <sub>AUX</sub> is disabled)	50	—	170	Ω	
<b>CAN_5V voltage regulator</b>						
V <sub>CAN</sub>	V <sub>CAN</sub> output voltage V <sub>SUP</sub> > 6.0 V in buck mode V <sub>SUP</sub> > V <sub>SUP\_UV\_L</sub> in boost mode	4.8	5.0	5.2	V	
I <sub>CAN_OUT</sub>	V <sub>CAN</sub> output current	—	—	100	mA	
I <sub>CAN_LIM</sub>	V <sub>CAN</sub> output current limitation	100	—	250	mA	

**Table 5. Static electrical characteristics ...continued**

$T_A = -40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 36 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 36\text{ V}$ , thermal dissipation must be considered (see [Figure 29](#)).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
TSD <sub>CAN</sub>	V <sub>CAN</sub> thermal shutdown threshold	160	—	—	°C	
TSD <sub>CAN_HYST</sub>	V <sub>CAN</sub> thermal shutdown hysteresis	—	10	—	°C	[5]
V <sub>CAN_UV</sub>	V <sub>CAN</sub> undervoltage detection threshold	4.25	—	4.8	V	
V <sub>CAN_UV_HYST</sub>	V <sub>CAN</sub> undervoltage hysteresis	0.07	—	0.22	V	
V <sub>CAN_OV</sub>	V <sub>CAN</sub> overvoltage detection threshold (rising)	5.2	—	5.85	V	
V <sub>CAN_OV_HYST</sub>	V <sub>CAN</sub> overvoltage hysteresis	0.07	—	0.22	V	
LOR <sub>V<sub>CAN</sub></sub>	V <sub>CAN</sub> transient load regulation • I <sub>CAN_OUT</sub> = 0 mA to 50 mA	—	100	—	mV	[5]
<b>VKAM voltage regulator</b>						
V <sub>KAM</sub>	V <sub>KAM</sub> output voltage	3.0	3.5	4.0	V	
I <sub>KAM_OUT</sub>	V <sub>KAM</sub> output current	—	—	3.0	mA	
I <sub>KAM_LIM</sub>	V <sub>KAM</sub> output current limitation	4.0	—	10.0	mA	
I <sub>SUP_KAM</sub>	V <sub>KAM</sub> current consumption from V <sub>SUP3</sub> • I <sub>KAM_OUT</sub> = 0 mA • I <sub>KAM_OUT</sub> < 1.0 mA • 1.0 mA < I <sub>KAM_OUT</sub> < 3.0 mA	—	—	25	µA	
		—	—	150	µA	
		—	—	2.15	mA	
<b>Long duration timer</b>						
I <sub>LDT</sub>	Timer current consumption (from V <sub>SUP3</sub> )	—	5.0	10	µA	
<b>Fail-safe machine voltage supervisor</b>						
V <sub>PRE_OV</sub>	V <sub>PRE</sub> overvoltage detection threshold	7.2	—	8.0	V	
V <sub>PRE_OV_HYST</sub>	V <sub>PRE</sub> overvoltage hysteresis	—	0.1	—	V	[5]
V <sub>CORE_FB_UV</sub>	V <sub>CORE</sub> FB undervoltage detection threshold	0.67	—	0.773	V	
V <sub>CORE_FB_UV_D</sub>	V <sub>CORE</sub> FB undervoltage detection threshold - degraded mode	0.45	—	0.58	V	
V <sub>CORE_FB_UV_HYST</sub>	V <sub>CORE</sub> FB undervoltage hysteresis	10	—	27	mV	[5]
V <sub>CORE_FB_OV</sub>	V <sub>CORE</sub> FB overvoltage detection threshold	0.84	—	0.905	V	
V <sub>CORE_FB_OV_HYST</sub>	V <sub>CORE</sub> FB overvoltage hysteresis	10	—	30	mV	[5]
V <sub>CORE_FB_DRIFT</sub>	V <sub>CORE_FB</sub> drift versus FCRBM	50	100	150	mV	
V <sub>CCA_UV_5</sub>	V <sub>CCA</sub> undervoltage detection threshold (5.0 V configuration)	4.5	—	4.75	V	
V <sub>CCA_UV_5D</sub>	V <sub>CCA</sub> undervoltage detection threshold (degraded 5.0 V)	3.0	—	3.2	V	
V <sub>CCA_UV_33</sub>	V <sub>CCA</sub> undervoltage detection threshold (3.3 V configuration)	3.0	—	3.2	V	
V <sub>CCA_OV_5</sub>	V <sub>CCA</sub> overvoltage detection threshold (5.0 V configuration)	5.25	—	5.5	V	
V <sub>CCA_OV_33</sub>	V <sub>CCA</sub> overvoltage detection threshold (3.3 V configuration)	3.4	—	3.6	V	
V <sub>CCA_5_HYST</sub>	V <sub>CCA</sub> undervoltage and overvoltage hysteresis (5.0 V configuration)	—	0.105	—	V	[5]
V <sub>CCA_33_HYST</sub>	V <sub>CCA</sub> undervoltage and overvoltage hysteresis (3.3 V configuration)	—	0.07	—	V	[5]
V <sub>AUX_UV_5</sub>	V <sub>AUX</sub> undervoltage detection threshold (5.0 V configuration)	4.5	—	4.75	V	
V <sub>AUX_UV_5D</sub>	V <sub>AUX</sub> undervoltage detection threshold (degraded 5.0 V)	3.0	—	3.2	V	
V <sub>AUX_UV_33</sub>	V <sub>AUX</sub> undervoltage detection threshold (3.3 V configuration)	3.0	—	3.2	V	

**Table 5. Static electrical characteristics ...continued**

$T_A = -40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 36 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 36\text{ V}$ , thermal dissipation must be considered (see [Figure 29](#)).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
$V_{AUX\_OV\_5}$	$V_{AUX}$ overvoltage detection threshold (5.0 V configuration)	5.25	—	5.5	V	
$V_{AUX\_OV\_33}$	$V_{AUX}$ overvoltage detection threshold (3.3 V configuration)	3.4	—	3.6	V	
$V_{AUX\_5\_HYST}$	$V_{AUX}$ undervoltage and overvoltage hysteresis (5.0 V configuration)	—	0.105	—	V	[5]
$V_{AUX\_33\_HYST}$	$V_{AUX}$ undervoltage and overvoltage hysteresis (3.3 V configuration)	—	0.07	—	V	[5]
<b>Fail-safe outputs</b>						
$V_{RSTB\_OL}$	Reset low output level ( $I_{RSTB} = 2.0\text{ mA}$ )	—	—	0.5	V	
$I_{RSTB\_LIM}$	Reset output current limitation	12	—	25	mA	
$V_{RSTB\_IL}$	Reset low level detection threshold (falling)	1.0	—	—	V	
$V_{RSTB\_IH}$	Reset high level detection threshold (rising)	—	—	2.0	V	
$V_{RSTB\_HYST}$	Reset hysteresis	200	—	—	mV	
$RSTB_{PULL-DOWN}$	RSTB pull-down resistor	—	1.0	—	M $\Omega$	
$V_{FS0B\_OL}$	FS0B low output level ( $I_{FS0B} = 2.0\text{ mA}$ )	—	—	0.5	V	
$I_{FS0B\_LIM}$	FS0B output current limitation	4.0	—	16	mA	
$V_{FS0B\_IL}$	FS0B low level detection threshold (falling)	1.0	—	—	V	
$V_{FS0B\_IH}$	FS0B high level detection threshold (rising)	—	—	2.0	V	
$V_{FS0B\_HYST}$	FS0B hysteresis	100	—	—	mV	
$FS0B_{PULL-DOWN}$	FS0B pull-down resistor	—	4.0	—	M $\Omega$	
$V_{FS1B\_OL}$	FS1B low output level ( $I_{FS1B} = 2.0\text{ mA}$ )	—	—	0.5	V	
$I_{FS1B\_LIM}$	FS1B output current limitation	4.0	—	16	mA	
$V_{FS1B\_IL}$	FS1B low level detection threshold (falling)	1.0	—	—	V	
$V_{FS1B\_IH}$	FS1B high level detection threshold (rising)	—	—	2.0	V	
$V_{FS1B\_HYST}$	FS1B hysteresis	100	—	—	mV	
$FS1B_{PULL-DOWN}$	FS1B pull-down resistor	—	4.0	—	M $\Omega$	
<b>Fail-safe pull-up</b>						
$I_{VPU\_FS}$	VPU_FS circuitry consumption	—	5.0	10	$\mu\text{A}$	
$V_{VPU\_FS\_TH}$	VPU_FS falling threshold to assert FS1B (FS1B_trig)	2.9	3.2	3.5	V	
$R_{VPU\_FS}$	Resistor between VPRE and VPU_FS	—	1.0	1.5	k $\Omega$	[5]
<b>Digital input</b>						
$V_{IO\_IH}$	Digital high input voltage level (IO_0, IO_4, IO_5)	2.6	—	—	V	
$V_{IO23\_IH}$	Digital high input voltage level (IO_2, IO_3)	2.0	—	—	V	
$V_{IO\_IL}$	Digital low input voltage level (IO_0, IO_4, IO_5)	—	—	2.1	V	
$V_{IO\_HYST}$	Input voltage hysteresis (IO_0, IO_4, IO_5)	50	120	500	mV	[5]
$V_{IO23\_IL}$	Digital low input voltage level (IO_2, IO_3)	—	—	0.9	V	
$V_{IO23\_HYST}$	Input voltage hysteresis (IO_2, IO_3)	200	450	700	mV	[5]
$I_{IO\_IN\_2:4}$	Input current for IO_2, IO_3 and IO_4	-5.0	—	5.0	$\mu\text{A}$	
$I_{IO\_IN\_LPOFF}$	Input current for IO_0:5 in LPOFF	-1.0	—	1.0	$\mu\text{A}$	

**Table 5. Static electrical characteristics ...continued**

$T_A = -40\text{ °C}$  to  $125\text{ °C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to  $36\text{ V}$ , unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 36\text{ V}$ , thermal dissipation must be considered (see [Figure 29](#)).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
<b>Analog input - multi-purpose IOs</b>						
$V_{IO\_ANA\_WD}$	Measurable input voltage (wide range)	3.0	—	19	V	
$V_{IO\_ANA\_TG}$	Measurable input voltage (tight range)	3.0	—	9.0	V	
$I_{IO\_IN\_ANA}$	Input current for IO_0 and IO_5	-5.0	—	100	µA	[7]
<b>Output gate driver (IO_4)</b>						
$V_{IO4\_OH}$	High output level at $I_{IO4\_OUT} = -2.0\text{ mA}$	$V_{PRE} - 1.5$	—	$V_{PRE}$	V	
$V_{IO4\_OL}$	Low output level at $I_{IO4\_OUT} = +2.0\text{ mA}$	0.0	—	1.0	V	
$V_{IO4\_OUT\_SK}$ $V_{IO4\_OUT\_SC}$	Output current capability	2.0 —	— —	— -2.0	mA	
<b>Analog multiplexer</b>						
$V_{AMUX\_ACC}$	Voltage sense accuracy ( $V_{SNS}$ , IO_0, IO_5) using 5.1 kΩ resistor	-5.0	—	5.0	%	[8]
$V_{AMUX\_WD\_5}$	Divider ratio (wide input voltage range) at $V_{DDIO} = 5.0\text{ V}$	—	5.0	—		[9]
$V_{AMUX\_WD\_3P3}$	Divider ratio (wide input voltage range) at $V_{DDIO} = 3.3\text{ V}$	—	7.0	—		20 <sup>[9]</sup>
$V_{AMUX\_TG\_5}$	Divider ratio (tight input voltage range) at $V_{DDIO} = 5.0\text{ V}$	—	2.0	—		
$V_{AMUX\_TG\_3P3}$	Divider ratio (tight input voltage range) at $V_{DDIO} = 3.3\text{ V}$	—	3.0	—		
$V_{AMUX\_REF1}$	Internal voltage Reference with $6.0\text{ V} < V_{SUP} < 19\text{ V}$	2.475	2.5	2.525	V	
$V_{AMUX\_REF2}$	Internal voltage reference with $V_{SUP} \leq 6.0\text{ V}$ , or $V_{SUP} \geq 19\text{ V}$	2.468	2.5	2.532	V	
$V_{AMUX\_TP\_CO}$	Internal temperature sensor coefficient	—	9.9	—	mV/°C	[5]
$V_{AMUX\_TP}$	Temperature sensor MUX_OUT output voltage (at $T_J = 165\text{ °C}$ )	2.08	2.15	2.22	V	
<b>Interrupt</b>						
$V_{INTB\_OL}$	Low output level ( $I_{INT} = 2.5\text{ mA}$ )	—	—	0.5	V	
$R_{PU\_INT}$	Internal pull-up resistor (connected to VDDIO)	—	10	—	KΩ	
$I_{INT\_LK}$	Input leakage current	—	—	1.0	µA	
<b>Digital interface</b>						
$MISO_H$	High output level on MISO ( $I_{MISO} = 1.5\text{ mA}$ )	$V_{DDIO} - 0.4$	—	—	V	
$MISO_L$	Low output level on MISO ( $I_{MISO} = 2.0\text{ mA}$ )	—	—	0.4	V	
$I_{MISO}$	Tri-state leakage current ( $V_{DDIO} = 5.0\text{ V}$ )	-5.0	—	5.0	µA	
$V_{DDIO}$	Supply voltage for MISO output buffer	3.0	—	5.5	V	
$I_{V_{DDIO}}$	Current consumption on VDDIO	—	1.0	3.0	mA	
$SPI_{LK}$	SCLK, NCS, MOSI input current	-1.0	—	1.0	µA	
$V_{SPI\_IH}$	SCLK, NCS, MOSI high input threshold	2.0	—	—	V	
$V_{SPI\_IL}$	SCLK, NCS, MOSI low input threshold	—	—	0.8	V	
$R_{SPI}$	NCS, MOSI internal pull-up (pull-up to VDDIO)	200	400	800	KΩ	
<b>Debug</b>						
$V_{DEBUG\_IL}$	Low input voltage threshold	2.1	2.35	2.8	V	
$V_{DEBUG\_IH}$	High input voltage threshold	4.35	4.6	4.97	V	
$I_{DEBUG\_LK}$	Input leakage current	-10	—	10	µA	

**Table 5. Static electrical characteristics ...continued**

$T_A = -40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 36 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 36\text{ V}$ , thermal dissipation must be considered (see [Figure 29](#)).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
<b>CAN transceiver (FD 2.0 Mbit/s)</b>						
<b>CAN logic input pin (TXD)</b>						
$V_{TXD\_IH}$	TXD high input threshold	$0.7 \times V_{DDIO}$	—	—	V	
$V_{TXD\_IL}$	TXD low input threshold	—	—	$0.3 \times V_{DDIO}$	V	
$TXD_{PULL-UP}$	TXD main device pull-up	20	33	50	k $\Omega$	
$TXD_{LK}$	TXD input leakage current, $V_{TXD} = V_{DDIO}$	-1.0	—	1.0	$\mu\text{A}$	
<b>CAN logic output pin (RXD)</b>						
$V_{RXD\_OL1}$	Low level output voltage ( $I_{RXD} = 250\text{ }\mu\text{A}$ )	—	—	0.4	V	
$V_{RXD\_OL2}$	Low level output voltage ( $I_{RXD} = 1.5\text{ mA}$ )	—	—	0.9	V	
$V_{OUT\_HIGH}$	High level output voltage ( $I_{RXD} = -250\text{ }\mu\text{A}$ , $V_{DDIO} = 3.0\text{ V}$ to $5.5\text{ V}$ )	$V_{DDIO} - 0.4$	—	—	V	
<b>CAN output pins (CANH, CANL)</b>						
$V_{DIFF\_COM\_MODE}$	Differential input comparator common mode range in normal mode	-20	—	20	V	
$V_{IN\_DIFF}$	Differential input voltage threshold in normal mode	0.5	—	0.9	V	
$V_{DIFF\_COM\_SLEEP}$	Differential input comparator common mode range in sleep mode	-12	—	12	V	
$V_{IN\_DIFF\_SLEEP}$	Differential input voltage threshold in sleep mode	0.4	—	1.1	V	
$V_{IN\_HYST}$	Differential input hysteresis (in TX, RX mode)	50	—	—	mV	
$R_{IN\_CHCL}$	CANH, CANL input resistance	5.0	—	50	k $\Omega$	
$R_{IN\_DIFF}$	CAN differential input resistance	10	—	100	k $\Omega$	
$R_{INSLEEP}$	CANH, CANL input resistance device supplied and in CAN sleep mode	5.0	—	50	k $\Omega$	
$R_{IN\_MATCH}$	Input resistance matching	-3.0	—	3.0	%	
$C_{IN\_CM}$	Common mode input capacitance	—	20	—	pF	[5]
$C_{IN\_DIFF}$	Differential input capacitance	—	10	—	pF	
$V_{CANH}$	CANH output voltage ( $45\text{ }\Omega < R_{BUS} < 65\text{ }\Omega$ ) • TX dominant state • TX recessive state	2.75 2.0	— 2.5	4.5 3.0	V	
$V_{CANL}$	CANL output voltage ( $45\text{ }\Omega < R_{BUS} < 65\text{ }\Omega$ ) • TX dominant state • TX recessive state	0.5 2.0	— 2.5	2.25 3.0	V	
$V_{CAN\_SYM}$	CAN dominant voltage symmetry ( $V_{CANL} + V_{CANH}$ )	4.5	5.0	5.5	V	
$V_{OH-VOL}$	Differential output voltage • TX dominant state ( $45\text{ }\Omega < R_{BUS} < 65\text{ }\Omega$ ) • TX recessive state	1.5 -50	2.0 0.0	3.0 50	V mV	
$I_{CANL-SK}$	CANL sink current under short-circuit condition ( $V_{CANL} \leq 12\text{ V}$ , CANL driver ON, TXD low)	40	—	100	mA	
$I_{CANH-SC}$	CANH source current under short-circuit condition ( $V_{CANH} = -2.0\text{ V}$ , CANH driver ON, TXD low)	-100	—	-40	mA	

**Table 5. Static electrical characteristics ...continued**

$T_A = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 36 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 36\text{ V}$ , thermal dissipation must be considered (see [Figure 29](#)).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
$V_{CANLP}$	CANL, CANH output voltage in sleep modes. No termination load.	-0.1	0.0	0.1	V	
$I_{CAN}$	CANH, CANL input current, device unsupplied, ( $V_{CANH}, V_{CANL} = 5.0\text{ V}$ ) <ul style="list-style-type: none"> <li><math>V_{SUP}</math> and <math>V_{CAN}</math> connected to GND</li> <li><math>V_{SUP}</math> and <math>V_{CAN}</math> connected to GND via 47 kΩ resistor</li> </ul>	-10 -10	— —	10 10	μA μA	[10]
$T_{OT}$	Overtemperature detection	160	—	—	°C	
$T_{HYST}$	Overtemperature hysteresis	—	—	20	°C	
<b>LIN transceiver (when <math>7.0\text{ V} &lt; V_{SUP1,2,3} &lt; 18\text{ V}</math>, unless otherwise specified)</b>						
<b>LIN logic input pin (TXDL)</b>						
$V_{TXDL\_IH}$	TXDL high input threshold	2.0	—	—	V	
$V_{TXDL\_IL}$	TXDL low input threshold	—	—	0.8	V	
$TXDL\_PULL\_UP$	TXDL internal pull-up (to VDDIO)	20	33	50	kΩ	
$TXDL\_LK$	TXD input leakage current, $V_{TXDL} = V_{DDIO}$	-1.0	—	1.0	μA	
<b>LIN logic input pin (RXDL)</b>						
$V_{RXDL\_OL1}$	Low level output voltage ( $I_{RXDL} = 250\text{ }μ\text{A}$ )	—	—	0.4	V	
$V_{RXDL\_OL2}$	Low level output voltage ( $I_{RXDL} = 1.5\text{ mA}$ )	—	—	0.9	V	
$V_{RXDL\_OUT\_HIGH}$	High level output voltage ( $I_{RXDL} = -250\text{ }μ\text{A}$ , $V_{DDIO} = 3.0\text{ V}$ to $5.5\text{ V}$ )	$V_{DDIO}$ -0.4	—	—	V	
<b>LIN output pin</b>						
$I_{BUS\_PAS\_DOM}$	Input leakage current at the receiver. dominant state (Driver OFF, $V_{BAT} = 12\text{ V}$ , $V_{BUS} = 0\text{ V}$ )	-1.0	—	—	mA	[11]
$I_{BUS\_PAS\_REC}$	Input leakage current at the receiver. recessive state (Driver OFF, $8.0\text{ V} < V_{BAT} < 18\text{ V}$ , $8.0\text{ V} < V_{BUS} < 18\text{ V}$ , $V_{BUS} \geq V_{BAT}$ )	—	—	20	μA	
$V_{DRIVER\_DOM}$	Driver dominant voltage	—	—	$0.251 \times V_{SUP}$	V	
$V_{BUS\_DOM}$	Receiver dominant state	—	—	$0.4 \times V_{SUP}$	V	
$V_{BUS\_REC}$	Receiver recessive state	$0.6 \times V_{SUP}$	—	—	V	
$V_{BUS\_WU}$	LIN wake-up detection threshold ( $7.0\text{ V} < V_{SUP} < 18\text{ V}$ )	$0.4 \times V_{SUP}$	—	$0.6 \times V_{SUP}$	V	
$V_{LIN\_UV}$	$V_{SUP}$ undervoltage threshold	—	—	7.0	V	
$V_{SER\_DIODE}$	Series diode voltage drop ( $D_{SER\_COMMANDER}$ and $D_{SER\_INT}$ in pull-up path)	0.4	0.7	1.0	V	
$I_{BUS\_LIM}$	Current limitation for driver dominant state ( $V_{BUS} = 18\text{ V}$ )	40	—	200	mA	[12]
$R_{RESPONDER}$	LIN pull-up resistor	20	—	60	kΩ	
$V_{SHIFT\_GND}$	Ground shift ( $V_{SHIFT\_GND} = V_{GND\_ECU} - V_{GND\_BATTERY}$ )	0.0	—	$11.5\% V_{BAT}$	V	
$V_{SHIFT\_BAT}$	Battery voltage shift ( $V_{SHIFT\_BAT} = V_{BATTERY} - V_{SHIFT\_GND} - V_{BAT}$ )	0.0	—	$11.5\% V_{BAT}$	V	[13]
$V_{SHIFT\_DIF}$	Difference between battery shift and ground shift ( $V_{SHIFT\_DIF} = V_{SHIFT\_BAT} - V_{SHIFT\_GND}$ )	0.0	—	$8.0\% V_{BAT}$	V	[14]
$V_{BUS\_CNT}$	$V_{BUS\_CNT} = (V_{TH\_REC} + V_{TH\_DOM})/2$	$0.475 \times V_{SUP}$	—	$0.525 \times V_{SUP}$	V	[15]

**Table 5. Static electrical characteristics ...continued**

$T_A = -40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 36 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 36\text{ V}$ , thermal dissipation must be considered (see [Figure 29](#)).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
$V_{HYST}$	$V_{HYST} = V_{TH\_REC} - V_{TH\_DOM}$	—	—	$0.175 \times V_{SUP}$	V	
$I_{BUS\_NO\_GND}$	Ground disconnection. $GND = V_{SUP}$ , $0\text{ V} < V_{BUS} < 18\text{ V}$ , $V_{BAT} = 12\text{ V}$ . Loss of local GND does not affect communication in the remaining network	-1.0	—	1.0	mA	[16]
$I_{BUS\_NO\_BAT}$	V <sub>BAT</sub> disconnection. $V_{SUP} = GND$ , $0\text{ V} < V_{BUS} < 18\text{ V}$ . Node sustains the current which can flow under this condition. BUS remains operational.	—	—	30	μA	
$LIN_{TSD}$	LIN thermal shutdown	150	175	—	°C	[5]
$LIN_{TSD\_HYST}$	LIN thermal shutdown hysteresis	—	20	—	°C	
$C_{LIN}$	LIN internal capacitor	—	—	10	pF	[5]

- [1] Long duration timer and VKAM disable.
- [2]  $V_{SUP\_UV\_L\_B} = V_{PRE\_UV\_4P3} + R_{DSON\_PRE} \times I_{PRE}$ .
- [3]  $V_{SUP}$  min to guarantee  $V_{KAM}$  and main logic supply in LPOFF.
- [4] Guaranteed by characterization.
- [5] Guaranteed by design.
- [6] External PNP gain within 150 to 450.
- [7] Valid for  $V_{SUP3} \geq IO\_5$ .
- [8] If a higher resistor value than recommended is used, the accuracy degrades.
- [9] Wide range accuracy for input voltage from 9.0 V to 19 V.
- [10] Guaranteed by design and characterization.
- [11]  $V_{BAT}$  is the voltage at the input of the control unit.
- [12] Current flowing inside the pin. A transceiver must be capable to sink at least 40 mA.
- [13]  $V_{BAT}$ : voltage across the battery connectors of the vehicle.  $V_{GND\_ECU}$ : voltage on the local ECU ground connector with respect to battery ground of the vehicle ( $V_{GND\_BATTERY}$ ).
- [14] This constraint refers to duty cycle D1 and D2 only.
- [15]  $V_{TH\_DOM}$ : receiver threshold of the recessive to dominant LIN bus edge.  $V_{TH\_REC}$  receiver threshold of the dominant to recessive LIN bus edge.
- [16]  $V_{SUP}$  is the voltage at the input of the device (different from  $V_{BAT}$  when a reverse current protection diode is implemented).

## 10 Dynamic electrical characteristics

**Table 6. Dynamic electrical characteristics**

$T_A = -40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 36 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 36\text{ V}$ , thermal dissipation must be considered (see [Figure 29](#)).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
<b>Digital interface timing</b>						
$f_{SPI}$	SPI operation frequency (50 % DC)	0.5	—	8.0	MHz	
$t_{MISO\_TRANS}$	MISO transition speed, 20 – 80 % • $V_{DDIO} = 5.0\text{ V}$ , $C_{LOAD} = 50\text{ pF}$ • $V_{DDIO} = 5.0\text{ V}$ , $C_{LOAD} = 150\text{ pF}$	5.0	—	30	ns	
		5.0	—	50		
$t_{CLH}$	Minimum time SCLK = HIGH	62	—	—	ns	
$t_{CLL}$	Minimum time SCLK = LOW	62	—	—	ns	
$t_{PCLD}$	Propagation delay (SCLK to data at 10 % of MISO rising edge)	—	—	30	ns	
$t_{CSDV}$	NCS = low to data at MISO active	—	—	75	ns	
$t_{SCLCH}$	SCLK low before NCS low (setup time SCLK to NCS change H/L)	75	—	—	ns	
$t_{HCLCL}$	SCLK change L/H after NCS = low	75	—	—	ns	
$t_{SCLD}$	SDI input setup time (SCLK change H/L after MOSI data valid)	40	—	—	ns	
$t_{HCLD}$	SDI input hold time (MOSI data hold after SCLK change H/L)	40	—	—	ns	



**Table 6. Dynamic electrical characteristics ...continued**

$T_A = -40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 36 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 36\text{ V}$ , thermal dissipation must be considered (see [Figure 29](#)).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
$t_{SCLCL}$	SCLK low before NCS high	100	—	—	ns	
$t_{HCLCH}$	SCLK high after NCS high	100	—	—	ns	
$t_{PCHD}$	NCS L/H to MISO at high-impedance	—	—	75	ns	
$t_{ONNCS}$	NCS min. high time	500	—	—	ns	
$t_{NCS\_MIN}$	NCS filter time	10	—	40	ns	
<b>Functional state machine</b>						
$t_{WU\_GEN}$	General wake-up signal deglitch time (for any wake-up signal on IOs)	60	70	80	$\mu\text{s}$	
<b>Fail-safe state machine</b>						
$CLK_{FS}$	Fail-safe oscillator	406	—	495	kHz	
$CLK_{FS\_MON}$	Fail-safe oscillator monitoring	200	—	950	kHz	
$t_{IC\_ERR}$	IO_4:5 Ext. IC filter time	4.0	—	20	$\mu\text{s}$	
$t_{ACK\_FS}$	Acknowledgment counter (used for IC error handling IO_5)	7.0	—	9.7	ms	
$t_{DFS\_RECOVERY}$	IO_0 filter time to recover from deep reset and fail state	0.8	—	1.3	ms	
$t_{CORE\_DRIFT\_MON}$	FCRBM filter time	1.0	—	2.0	ms	
<b>Fail-safe output</b>						
$t_{RSTB\_FB}$	RSTB feedback filter time	8.0	—	15	$\mu\text{s}$	
$t_{FS0B\_FB}$	FS0B feedback filter time	8.0	—	15	$\mu\text{s}$	
$t_{FS1B\_FB}$	FS1B feedback filter time	8.0	—	15	$\mu\text{s}$	
$t_{RSTB\_BLK}$	RSTB feedback blanking time	180	—	320	$\mu\text{s}$	
$t_{FS0B\_BLK}$	FS0B feedback blanking time	180	—	320	$\mu\text{s}$	
$t_{FS1B\_BLK}$	FS1B feedback blanking time	180	—	320	$\mu\text{s}$	
$t_{RSTB\_POR}$	Reset delay time (after a power-on reset or from LPOFF)	12.5	16.5	24.3	ms	[1]
$t_{RSTB\_LG}$	Reset duration (long pulse)	8.0	—	10	ms	
$t_{RSTB\_ST}$	Reset duration (short pulse)	1.0	—	1.3	ms	
$t_{RSTB\_IN}$	External reset delay time	8.0	—	15	$\mu\text{s}$	
$t_{DIAG\_SC}$	Fail-safe output diagnostic counter (RSTB, FS0B, FS1B)	500	—	800	$\mu\text{s}$	
<b>V<sub>SENSE</sub> voltage supply</b>						
$t_{VSNS\_UV}$	V <sub>SNS</sub> undervoltage filtering time	1.0	—	3.0	$\mu\text{s}$	
<b>V<sub>SUP</sub> voltage supply</b>						
$t_{VSUP\_IPFF}$	I <sub>PFF</sub> input voltage filtering time	1.0	—	5.0	$\mu\text{s}$	
$C_{SUP}$	Minimum capacitor on V <sub>SUP</sub>	47	—	—	$\mu\text{F}$	
<b>V<sub>PRE</sub> voltage pre-regulator</b>						
$f_{SW\_PRE}$	V <sub>PRE</sub> switching frequency	412	437.5	463	kHz	
$t_{SW\_PRE}$	V <sub>SW\_PRE</sub> on and off switching time	—	—	30	ns	[2]
$t_{PRE\_SOFT}$	V <sub>PRE</sub> soft start duration ( $C_{OUT\_VPRE} \leq 100\text{ }\mu\text{F}$ )	500	—	700	$\mu\text{s}$	
$t_{PRE\_BLK\_LIM}$	V <sub>PRE</sub> current limitation blanking time	200	—	600	ns	
$t_{PRE\_OC}$	V <sub>PRE</sub> overcurrent filtering time	30	—	120	ns	[2]
$t_{PRE\_UV}$	V <sub>PRE</sub> undervoltage filtering time	20	—	40	$\mu\text{s}$	



**Table 6. Dynamic electrical characteristics ...continued**

$T_A = -40\text{ °C}$  to  $125\text{ °C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 36 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 36\text{ V}$ , thermal dissipation must be considered (see [Figure 29](#)).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
$t_{PRE\_UV\_4p3}$	$V_{PRE}$ shutoff filtering time	3.0	—	7.0	$\mu\text{s}$	
$d_{IPRE/DT}$	$V_{PRE}$ load regulation variation	—	—	25	A/ms	[2]
$t_{PRE\_WARN}$	$V_{PRE}$ thermal warning filtering time	30	—	40	$\mu\text{s}$	
$t_{PRE\_TSD}$	$V_{PRE}$ thermal detection filtering time	1.0	—	3.0	$\mu\text{s}$	
$t_{LS\_RISE/FALL}$	LS gate voltage switching time ( $I_{OUT} = 300\text{ mA}$ )	—	—	50	ns	
$t_{BBTO}$	GATE_LS boost transistor timeout detection	—	120	—	$\mu\text{s}$	
<b><math>V_{CORE}</math> voltage regulator</b>						
$t_{CORE\_BLK\_LIM}$	$V_{CORE}$ current limitation blanking time	20	—	40	ns	
$f_{SW\_CORE}$	$V_{CORE}$ switching frequency	2.2	2.34	2.48	MHz	
$t_{SW\_CORE}$	$V_{SW\_CORE}$ on and off switching time	—	—	12	ns	
$V_{CORE\_SOFT}$	$V_{CORE}$ soft start ( $C_{OUT\_V_{CORE}} = 100\text{ }\mu\text{F}$ max)	—	—	10	V/ms	
$t_{CORE\_WARN}$	$V_{CORE}$ thermal warning filtering time	30	—	40	$\mu\text{s}$	
$t_{CORE\_TSD}$	$V_{CORE}$ thermal detection filtering time	1.0	—	3.0	$\mu\text{s}$	
<b><math>V_{CCA}</math> voltage regulator</b>						
$t_{CCA\_LIM}$	$V_{CCA}$ output current limitation filter time	1.0	—	3.0	$\mu\text{s}$	
$t_{CCA\_LIM\_OFF1}$ $t_{CCA\_LIM\_OFF2}$	$V_{CCA}$ output current limitation duration	10 50	— —	15 60	ms	
$t_{CCA\_WARN}$	$V_{CCA}$ thermal warning filtering time (int. MOSFET)	30	—	40	$\mu\text{s}$	
$t_{CCA\_TSD}$	$V_{CCA}$ thermal detection filter time (int. MOSFET)	1.0	—	3.0	$\mu\text{s}$	
$dI_{LOAD}/dt$	$V_{CCA}$ load transient	—	2.0	—	A/ms	[2]
$V_{CCA\_SOFT}$	$V_{CCA}$ soft start (5.0 V and 3.3 V)	—	—	50	V/ms	
<b><math>V_{AUX}</math> voltage regulator</b>						
$t_{AUX\_LIM}$	$V_{AUX}$ output current limitation filter time	1.0	—	3.0	$\mu\text{s}$	
$t_{AUX\_LIM\_OFF1}$ $t_{AUX\_LIM\_OFF2}$	$V_{AUX}$ output current limitation duration	10 50	— —	15 60	ms	
$t_{AUX\_TSD}$	$V_{AUX}$ thermal detection filter time	1.0	—	3.0	$\mu\text{s}$	
$dI_{AUX}/dt$	$V_{AUX}$ load transient	—	2.0	—	A/ms	[2]
$V_{AUX\_SOFT}$	$V_{AUX}$ soft start (5.0 V and 3.3 V)	—	—	50	V/ms	
<b>CAN_5V voltage regulator</b>						
$t_{CAN\_LIM}$	Output current limitation filter time	2.0	—	4.0	$\mu\text{s}$	
$t_{CAN\_TSD}$	$V_{CAN}$ thermal detection filter time	1.0	—	3.0	$\mu\text{s}$	
$t_{CAN\_UV}$	$V_{CAN}$ undervoltage filtering time	4.0	—	7.0	$\mu\text{s}$	
$t_{CAN\_OV}$	$V_{CAN}$ overvoltage filtering time	100	—	200	$\mu\text{s}$	
$dI_{CAN}/dt$	$V_{CAN}$ load transient	—	100	—	A/ms	[2]
<b>Fail-safe machine voltage supervisor</b>						
$t_{PRE\_OV}$	$V_{PRE}$ overvoltage filtering time	128	—	234	$\mu\text{s}$	
$t_{PRE\_OV\_R}$	$V_{PRE}$ overvoltage reaction time	—	—	314	$\mu\text{s}$	
$t_{CORE\_UV}$	$V_{CORE}$ FB undervoltage filtering time	4.0	—	10	$\mu\text{s}$	
$t_{CORE\_UV\_R}$	$V_{CORE}$ FB undervoltage reaction time	—	—	15	$\mu\text{s}$	

**Table 6. Dynamic electrical characteristics ...continued**

$T_A = -40\text{ °C}$  to  $125\text{ °C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 36 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 36\text{ V}$ , thermal dissipation must be considered (see [Figure 29](#)).

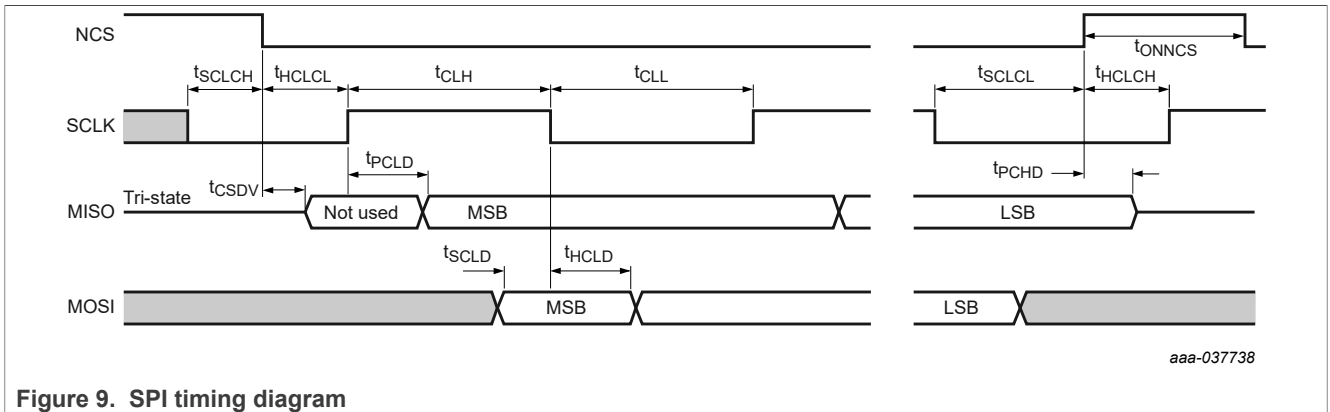
Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
$t_{CORE\_OV}$	$V_{CORE}$ FB overvoltage filtering time	128	—	234	$\mu\text{s}$	
$t_{CORE\_OV\_R}$	$V_{CORE}$ FB overvoltage reaction time	—	—	314	$\mu\text{s}$	
$t_{CCA\_UV}$	$V_{CCA}$ undervoltage filtering time	4.0	—	10	$\mu\text{s}$	
$t_{CCA\_UV\_R}$	$V_{CCA}$ undervoltage reaction time	—	—	15	$\mu\text{s}$	
$t_{CCA\_OV}$	$V_{CCA}$ overvoltage filtering time	128	—	234	$\mu\text{s}$	
$t_{CCA\_OV\_R}$	$V_{CCA}$ overvoltage reaction time	—	—	314	$\mu\text{s}$	
$t_{AUX\_UV}$	$V_{AUX}$ undervoltage filtering time	4.0	—	10	$\mu\text{s}$	
$t_{AUX\_UV\_R}$	$V_{AUX}$ undervoltage reaction time	—	—	15	$\mu\text{s}$	
$t_{AUX\_OV}$	$V_{AUX}$ overvoltage filtering time	128	—	234	$\mu\text{s}$	
$t_{AUX\_OV\_R}$	$V_{AUX}$ overvoltage reaction time	—	—	314	$\mu\text{s}$	
<b>Digital input – multi-purpose IOs</b>						
$F_{IO\_IN}$	Digital input frequency range	0.0	—	100	kHz	
<b>Analog multiplexer</b>						
$t_{MUX\_READY}$	SPI selection to data ready to be sampled on Mux_out • $V_{DDIO} = 5.0\text{ V}$ , $C_{MUX\_OUT} = 1.0\text{ nF}$	—	—	10	$\mu\text{s}$	
<b>Interrupt</b>						
$t_{INTB\_LG}$	INTB pulse duration (long)	90	100	—	$\mu\text{s}$	
$t_{INTB\_ST}$	INTB pulse duration (short)	20	25	—	$\mu\text{s}$	
<b>Long duration timer</b>						
$CLK_{LDT}$	Long duration timer oscillator	31129	32768	34407	Hz	
$CLK_{LDT\_ \%}$	Long duration timer oscillator accuracy • from $-40\text{ °C}$ to $125\text{ °C}$ • from $-20\text{ °C}$ to $85\text{ °C}$ and calibration	-5.0 -2.0	— —	5.0 2.0	%	
<b>CAN dynamic characteristics (FD 2.0 Mbit/s)</b>						
$t_{DOUT}$	TXD dominant state timeout	0.8	—	5.0	ms	
$t_{DOM}$	Bus dominant clamping detection	0.8	—	5.0	ms	
$t_{LOOP}$	Propagation loop delay TXD to RXD • $R_{LOAD} = 120\ \Omega$ , C between CANH and CANL = 100 pF, C at RXD < 15 pF	—	—	255	ns	
$t_{1PWU}$	First pulse wake-up time	0.5	—	3.5	$\mu\text{s}$	
$t_{3PWU}$	Second and third pulse wake-up time	0.5	—	1.0	$\mu\text{s}$	
$t_{3PTO1}$	Multiple pulse wake-up timeout (short)	100	120	—	$\mu\text{s}$	
$t_{3PTO2}$	Multiple pulse wake-up timeout (long)	2400	2800	—	$\mu\text{s}$	
$t_{CAN\_READY}$	Delay to enable CAN by SPI command (NCS rising edge) to CAN to transmit (device in normal mode and CAN interface in TX/RX mode)	—	—	100	$\mu\text{s}$	[3]
$t_{BIT(BUS)}$	Transmitted recessive bit width at 2.0 Mbit/s	435	—	530	ns	
$t_{BIT(RXD)}$	Received recessive bit width at 2.0 Mbit/s	400	—	550	ns	
$t_{REC}$	Receiver timing symmetry at 2.0 Mbit/s	-65	—	40	ns	

**Table 6. Dynamic electrical characteristics ...continued**

$T_A = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 36 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 36\text{ V}$ , thermal dissipation must be considered (see [Figure 29](#)).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
<b>LIN dynamic characteristics (when 7.0 V &lt; V<sub>SUP</sub>1, 2, 3 &lt; 18 V, unless otherwise specified)</b>						
t <sub>RX_PD</sub>	Receiver propagation delay (T <sub>RX_PD</sub> = MAX (t <sub>REC_PDR</sub> , t <sub>REC_PDF</sub> ))	—	—	6.0	μs	
t <sub>RX_SYM</sub>	Symmetry of receiver propagation delay (T <sub>RX_SYM</sub> = t <sub>REC_PDF</sub> - t <sub>REC_PDR</sub> )	-2.0	—	2.0	μs	
t <sub>BUS_WU</sub>	BUS wake-up filter time	—	—	250	μs	
t <sub>XD_DOM</sub>	TXD_L permanent dominant state detection	—	5.0	—	ms	
t <sub>LIN_SHORT_GND</sub>	LIN Short-circuit to GND deglitcher	—	15	—	ms	
BD <sub>FAST</sub>	Fast baud rate	—	—	100	KB/s	
D1	Duty cycle D1 TH <sub>REC</sub> (max) = 0.744 x V <sub>SUP</sub> , TH <sub>DOM</sub> (max) = 0.581 x V <sub>SUP</sub> V <sub>SUP</sub> 7.0 V to 18 V, t <sub>BIT</sub> = 50 μs, D1 = t <sub>BUS-rec</sub> (min)/(2t <sub>BIT</sub> )	0.396	—	—	%	[4]
D2	Duty cycle D2 TH <sub>REC</sub> (min) = 0.422 x V <sub>SUP</sub> , TH <sub>DOM</sub> (min) = 0.284 x V <sub>SUP</sub> V <sub>SUP</sub> 7.6 V to 18 V, t <sub>BIT</sub> = 50 μs, D2 = t <sub>BUS-rec</sub> (max)/(2t <sub>BIT</sub> )	—	—	0.581	%	35 <sup>[4]</sup>
D3	Duty cycle D3 TH <sub>REC</sub> (max) = 0.778 x V <sub>SUP</sub> , TH <sub>DOM</sub> (max) = 0.616 x V <sub>SUP</sub> V <sub>SUP</sub> 7.0 V to 18 V, t <sub>BIT</sub> = 96 μs, D3 = t <sub>BUS-rec</sub> (min)/(2t <sub>BIT</sub> )	0.417	—	—	%	35 <sup>[4]</sup>
D4	Duty cycle D4 TH <sub>REC</sub> (min) = 0.389 x V <sub>SUP</sub> , TH <sub>DOM</sub> (min) = 0.251 x V <sub>SUP</sub> V <sub>SUP</sub> 7.6 V to 18 V, t <sub>BIT</sub> = 96 μs, D4 = t <sub>BUS-rec</sub> (max)/(2t <sub>BIT</sub> )	—	—	0.590	%	35 <sup>[4]</sup>

- [1] This timing is not guaranteed in case of fault during startup phase (after power-on reset or from LPOFF).
- [2] Guaranteed by characterization.
- [3] For proper CAN operation, TXD must be set to high level before CAN enable by the SPI, and must remain high for at least T<sub>CAN\_READY</sub>.
- [4] LIN Driver, bus load conditions (CBUS, RBUS): 1.0 nF; 1.0 kΩ / 6.8 nF; 660 Ω / 10 nF; 500 Ω.



**Figure 9. SPI timing diagram**

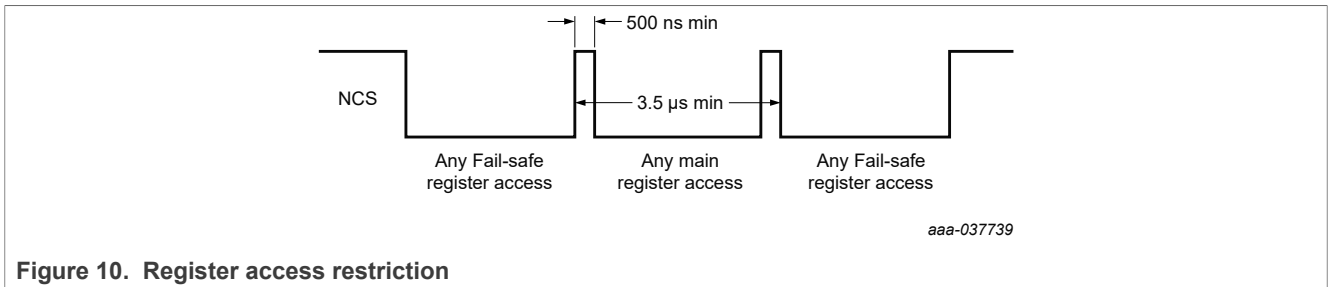


Figure 10. Register access restriction

## 11 Functional pin description

### 11.1 Introduction

The FS6500/FS4500 is the fourth generation of the system basis chip, combining:

- High efficiency switching voltage regulator for MCU, and linear voltage regulators for integrated CAN FD interface.
- External ICs such as sensors, accurate reference voltage for A to D converters, and keep alive memory supply in low-power mode for MCU static RAM.
- Built-in CAN flexible data interface at 2.0 Mbit/s (ISO 11898-2<sup>(12)</sup> and -5<sup>(13)</sup>), and LIN interface (LIN up to Rev. 2.2<sup>(22), (23)</sup>/SAEJ2602-2<sup>(24)</sup>), with local and bus failure diagnostic, protection, and fail-safe operation mode.
- Low-power mode, with ultra low-current consumption.
- Various wake-up capabilities.
- Long duration timer available in normal and low-power mode.
- Enhanced safety features with multiple fail-safe outputs and a scheme to support ASIL B applications.

### 11.2 Power supplies (VSUP1, VSUP2, VSUP3)

VSUP1 and VSUP2 are the input pins for the internal supply dedicated to the SMPS regulators. VSUP3 is the input pin for internal voltage reference. VSUP1, 2, and 3 are robust against ISO 7637<sup>(14)</sup> pulses. VSUP1, 2, and 3 must be connected to the same supply (Figure 70).

### 11.3 V<sub>SENSE</sub> input (VSENSE)

This pin must be connected to the battery line (before the reverse battery protection diode), via a serial resistor. It incorporates a threshold detector to sense the battery voltage, and provide a battery early warning. It also includes a resistor divider to measure VSENSE voltage via the MUX-OUT pin. The VSENSE pin is robust against ISO 7637<sup>(14)</sup> pulses.

### 11.4 Pre-regulator (VPRE)

A highly flexible SMPS pre-regulator is implemented in the FS6500/FS4500. It can be configured as a 'non-inverting buck-boost converter' (Figure 31) or 'standard buck converter' (Figure 30), depending on the external configuration (connection of pin GATE\_LS). The configuration is detected automatically during start-up sequence.

The SMPS pre-regulator is working in current mode control and the compensation network is fully integrated in the device. The high-side switching MOSFET is also integrated to make the current control easier. The pre-regulator delivers a typical output voltage of 6.5 V, which is used internally. Current limitation, overcurrent, overvoltage, and undervoltage detectors are provided. VPRE is enabled by default.

## 11.5 VCORE output (from 1.0 V to 5.0 V range)

The VCORE block of the FS6500 series is an SMPS regulator. The voltage regulator is a step down DC–DC converter operating in voltage control mode. The stability of the converter is done externally, by using the COMP\_CORE pin. The VCORE block of the FS4500 series is a linear regulator. In this case, BOOT\_CORE and COMP\_CORE pins must be left open.

The output voltage of FS6500/FS4500 is configurable to any voltage from a 1.0 V to 5.0 V range using an external resistor divider connected between VCORE and the feedback pin (FB\_CORE) (as example in [Figure 1](#), or [Figure 70](#)). Current limitation, overvoltage, and undervoltage detectors are provided. VCORE can be turned on or off via a SPI command, however it is not recommended to turn off VCORE with the SPI when VCORE is configured safety critical (both overvoltage and undervoltage have an impact on fail-safe outputs). VCORE overvoltage information disables VCORE. Diagnostics are reported in the dedicated register and generate an Interrupt. VCORE is enabled by default. For safety purpose, a second resistor bridge (R3/R4 duplicated) connected to FCRBM should be used to detect an external resistor drift.

## 11.6 VCCA output, 5.0 V, or 3.3 V selectable

The VCCA voltage regulator is used to provide an accurate voltage output (5.0 V, 3.3 V) selectable through an external resistor connected to the SELECT pin.

The VCCA output voltage regulator can be configured using an internal transistor delivering very good accuracy ( $\pm 1.0\%$  for 5.0 V and 3.3 V configuration), with a limited current capability (100 mA) for an analog to digital converter, or with an external PNP transistor, giving higher current capability (up to 300 mA) with lower output voltage accuracy ( $\pm 3.0\%$  for 300 mA) when using a local ECU supply.

Current limitation, overvoltage, and undervoltage detectors are provided. VCCA can be turned on or off via a SPI command, however it is not recommended to turn off VCCA with the SPI when VCCA is configured safety critical (both overvoltage and undervoltage have an impact on fail-safe outputs). VCCA overcurrent (with the use of external PNP only) and overvoltage information disables VCCA. Diagnostics are reported in the dedicated register and generate an Interrupt. VCCA is enabled by default.

## 11.7 VAUX output, 5.0 V, or 3.3 V selectable

The VAUX pin provides an auxiliary output voltage (5.0 V, 3.3 V) selectable through an external resistor connected to SELECT pin. It uses an external PNP ballast transistor for flexibility and power dissipation constraints. The VAUX output voltage regulator can be used as 'auxiliary supply' (local ECU supply) or 'sensor supply' (external ECU supply) with the possibility to be configured as a tracking regulator following VCCA.

Current limitation, overvoltage, and undervoltage detectors are provided. VAUX can be turned on or off via a SPI command, however it is not recommended to turn off VAUX with the SPI when VAUX is configured safety critical (both overvoltage and undervoltage have an impact on fail-safe outputs).  $V_{AUX}$  overcurrent and overvoltage information disables VAUX, reported in the dedicated register, and generates an Interrupt. VAUX is enabled by default.

## 11.8 SELECT input pin

### 11.8.1 VCCA, VAUX voltage configuration

VCCA and VAUX output voltage configurations are set by connecting an external resistor between the SELECT pin and Ground or the SELECT pin and VPRE. According to the value of this resistor, the voltage of VCCA and VAUX are configured after each power-on reset, and after a wake-up event when the device is in LPOFF. Information latches until the next hardware configuration read. Regulator voltage values can be read on the dedicated register via the SPI. See [Figure 72](#).

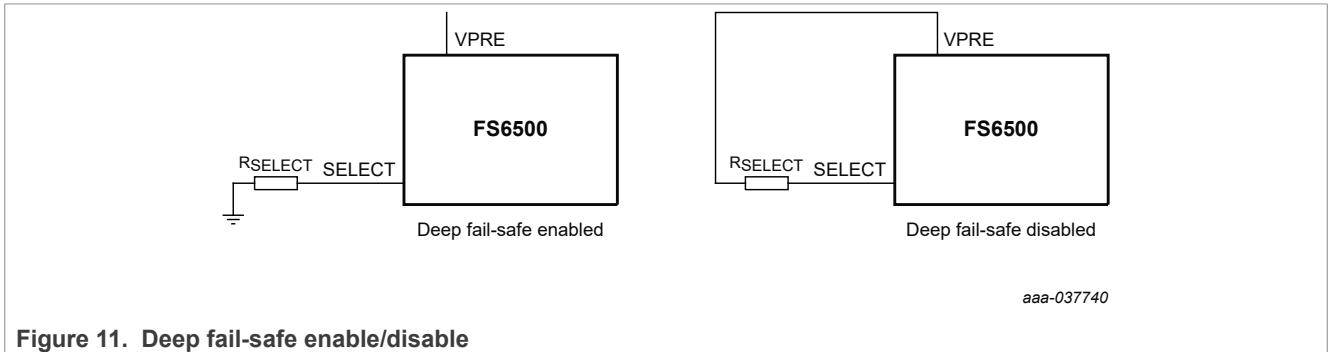
**Table 7. V<sub>CCA</sub>/V<sub>AUX</sub> voltage selection**

V <sub>CCA</sub> (V)	V <sub>AUX</sub> (V)	R select	Recommended value <sup>[1]</sup>
3.3	3.3	<6.0 kΩ	5.1 kΩ ±5.0 %
5.0	5.0	10.8 << 13.2 kΩ	12 kΩ ±5.0 %
3.3	5.0	21.6 << 26.2 kΩ	24 kΩ ±5.0 %
5.0	3.3	45.9 << 56.1 kΩ	51 kΩ ±5.0 %

[1] If the SELECT pin is detected open, the VCCA and VAUX regulators start at their minimum output voltage 3.3 V.

**11.8.2 Deep fail-safe configuration**

Deep fail-safe function is enabled when the SELECT pin is connected to ground and disabled when the SELECT pin is connected to VPRE. The configuration is done after each power-on reset, and after a wake-up event when device is in LPOFF by both the main and the fail-safe logics. The Information is latched until the next hardware configuration read (Figure 11).



**Figure 11. Deep fail-safe enable/disable**

**11.9 CAN\_5V voltage regulator**

The CAN\_5V voltage regulator is a linear regulator dedicated to the internal CAN FD interface. An external capacitor is required. Current limitation, overvoltage, and undervoltage detectors are provided. If the internal CAN transceiver is not used, the CAN\_5V regulator can supply an external load (see Section 12.7.6). CAN\_5V is enabled by default.

**11.10 Interrupt (INTB)**

The INTB output pin generates a low pulse when an Interrupt condition occurs. The INTB behavior as well as the pulse duration are set through the SPI during INIT phase. INTB has an internal pull-up resistor connected to VDDIO.

**11.11 CANH, CANL, TXD, RXD**

These are the pins of the CAN FD physical interface. The CAN FD transceiver provides the physical interface between the CAN FD protocol controller of an MCU and the physical dual wires CAN-bus. The CAN FD interface is connected to the MCU via the RXD and TXD pins.

**11.11.1 TXD**

TXD is the device input pin to control the CAN-bus level. TXD is a digital input with an internal pull-up resistor connected to VDDIO. In the application, this pin is connected to the microcontroller transmit pin. In normal mode, when TXD is high or floating, the CANH and CANL drivers are off, setting the bus in a recessive state.

When TXD is low, the CANH and CANL drivers are activated and the bus is set to a dominant state. TXD has a built-in timing protection disabling the bus when TXD is dominant for more than  $t_{\text{DOUT}}$ . In LPOFF mode, VDDIO is off, pulling this pin to GND.

### 11.11.2 RXD

RXD is the bus output level report pin. In the application, this pin is connected to the microcontroller receive pin. In normal mode, RXD is a push-pull structure. When the bus is in a recessive state, RXD is high. When the bus is dominant, RXD is low. In LPOFF mode, this pin is in the high-impedance state.

### 11.11.3 CANH and CANL

These are the CAN-bus pins. CANL is a low-side driver to GND, and CANH is a high-side driver to CAN\_5V. In normal mode and TXD high, the CANH and CANL drivers are off, and the voltage at CANH and CANL is approximately 2.5 V, provided by the internal bus biasing circuitry. When TXD is low, CANL is pulled to GND and CANH to CAN\_5V, creating a differential voltage on the CAN-bus.

In LPOFF mode, the CANH and CANL drivers are off, and these pins are pulled to GND via the device  $R_{\text{IN\_CHCL}}$  resistors. CANH and CANL have integrated ESD protection and extremely high robustness versus external disturbance, such as EMC and electrical transients. These pins have current limitation and thermal protection.

## 11.12 LIN, TXDL, RXDL

These are the pins of the LIN physical interface. The LIN transceivers provides the physical interface between the MCU and the physical single wire LIN bus. The LIN interface is connected to the MCU via the RXDL and TXDL pins.

### 11.12.1 TXDL

The TXDL input pin is the MCU interface to control the state of the LIN output. TXDL is a digital input with an internal pull-up resistor connected to VDDIO. In the application, this pin is connected to the microcontroller transmit pin.

In normal mode, when TXDL is high or floating, the LIN output transistor is OFF, setting the bus in recessive state. When TXDL is low, the LIN output transistor is on and the bus is set to a dominant state. TXDL has a built-in timing protection disabling the bus when TXDL is dominant for more than  $T_{\text{XD\_DOM}}$ . In LPOFF mode, VDDIO is off, pulling this pin to GND.

### 11.12.2 RXDL

RXDL is the bus output level report pin. In the application, this pin is connected to the microcontroller receive pin. In normal mode, RXD is a push-pull structure. When the bus is in a recessive state, RXD is high. When the bus is dominant, RXD is low. In LPOFF mode, this pin is in the high-impedance state.

### 11.12.3 LIN

This is the LIN bus pin. The LIN driver is a low-side MOSFET with internal overcurrent thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated so no external pull-up components are required for the application in a responder node. An additional pull-up resistor of 1.0 k $\Omega$  must be added when the device is used in the commander node. In normal mode and TXDL high, the LIN transistor is off, and the voltage at LIN is approximately VSUP3, provided by the pull-up resistor with a serial diode structure. When TXD is low, LIN is pulled to GND.

The device has two selectable baud rates: 20 kbit/s for normal baud rate and 10 kbit/s for slow baud rate. An additional fast baud rate (100 kbit/s) is implemented. It can be used to flash the MCU or in the garage for



diagnostic. The LIN consortium specification does not specify electrical parameters for this baud rate. The communication only must be guaranteed. In LPOFF mode, the LIN transistor is off, and this pin is pulled up to VSUP3. LIN has integrated ESD protection and extremely high robustness versus external disturbance, such as EMC and electrical transients.

### 11.13 Multiplexer output MUX\_OUT

The MUX\_OUT pin (Figure 12) delivers analog voltage to the MCU ADC input. The voltage to be delivered to MUX\_OUT is selected via the SPI, from one of the following parameters:

- VSENSE
- VIO\_0
- VKAM
- Internal 2.5 V reference
- Internal die temperature sensor  $T(^{\circ}\text{C}) = (V_{\text{AMUX}} - V_{\text{AMUX\_TP}}) / V_{\text{AMUX\_TP\_CO}} + 165$

Voltage range at MUX\_OUT is from GND to VDDIO (3.3 V or 5.0 V)

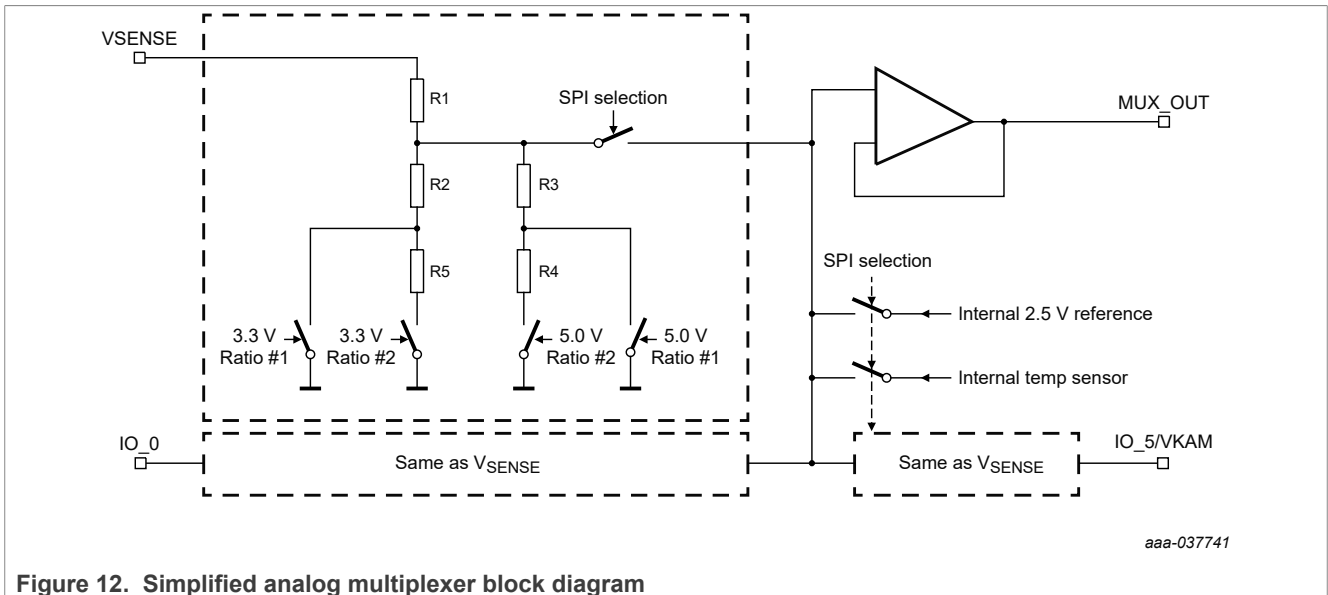


Figure 12. Simplified analog multiplexer block diagram

### 11.14 I/O pins (I/O\_0:I/O\_5)

The FS6500/FS4500 includes five multi-purpose I/Os (I/O\_0 to I/O\_5). I/O\_0 and I/O\_4 are load dump proof and robust against ISO 7637<sup>(14)</sup> pulses. An external serial resistor must be connected to those pins to limit the current during ISO pulses. I/O\_2 and I/O\_3 are not load dump proof. I/O\_5 requires an external protection (resistor and Zener diode) to be load dump proof and robust against ISO 7637<sup>(14)</sup> pulses.

Table 8. I/Os configuration

I/O number	Digital input wake-up capability	Analog input	Output gate driver	VKAM	Ext. IC monitoring
IO_0	X	X			
IO_2	X				
IO_3	X				
IO_4	X		X		X



Table 8. I/Os configuration...continued

I/O number	Digital input wake-up capability	Analog input	Output gate driver	VKAM	Ext. IC monitoring
IO_5	X	X		X	X

- IO\_0 is selectable as follows:

Analog input (load dump proof) sent to the MCU through the MUX\_OUT pin. Wake-up input on the rising or falling edge or based on the previous state. Digital input (logic level) sent to the MCU through the SPI.

**Safety purpose:** IO\_0 is the only wake-up input to resume from deep fail-safe mode.

- IO\_2:3 are selectable as follows:

Digital input (logic level) sent to the MCU through the SPI. Wake-up input on the rising or falling edge or based on the previous state.

- IO\_4 is selectable as follows:

Digital input (logic level) sent to the MCU through the SPI. Wake-up input (load dump proof) on rising or falling edge or based on previous state. Output gate driver (from V<sub>PRE</sub>) for low-side logic level MOSFET.

- IO\_5 is selectable as follows:

Analog input (20 V max.) sent to the MCU through the MUX\_OUT pin. Digital input (logic level) sent to the MCU through the SPI. Wake-up input on rising or falling edge or based on previous state. VKAM output supply.

- IO\_4:5 are selectable as follows:

**Safety purpose:** Digital input (logic level) to perform an IC error monitoring (both IO\_4 AND IO\_5 are used if configured as safety inputs, see Figure 13).

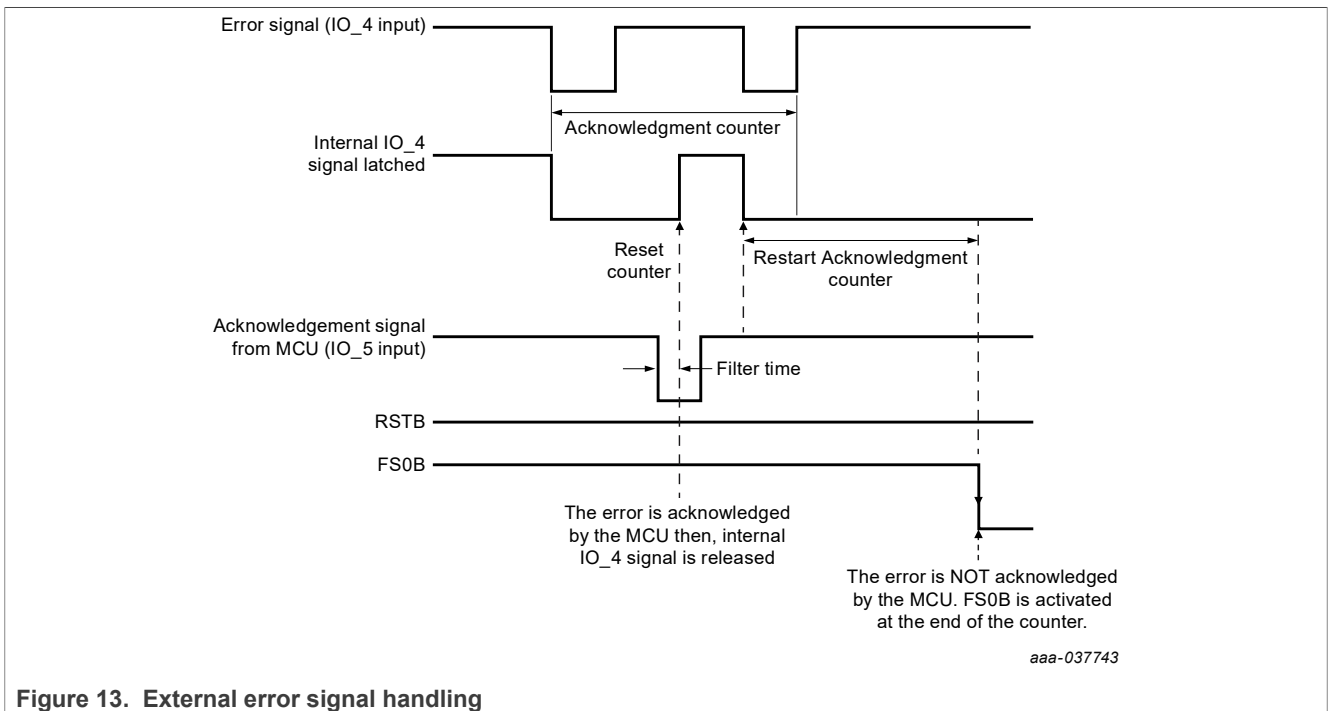


Figure 13. External error signal handling

## 11.15 SAFE output pins (FS0B, FS1B, RSTB)

### 11.15.1 FS0B pin

FS0B pin is the primary safe output pin. FS0B is asserted low when a fault event occurs (see [Section 12.5.5](#)). The objective of this pin is to drive an electrical safe circuitry independent from MCU to deactivate the whole system and set the ECU in a protected and known state.

After each power-on reset or after each wake-up event (LPOFF), the FS0B pin is asserted low. The MCU can decide to release the FS0B pin, when the application is ready to start. An external pull-up circuitry is mandatory connected to VDDIO or VSUP3.

- If the pull-up is connected to VDDIO, the value recommended is 5.0 k $\Omega$ , there is no current in LPOFF since VDDIO is off in LPOFF mode.
- If the pull-up is connected to VSUP3, the value must be above 10 k $\Omega$ , there is a current in the pull-up resistor to consider at application level in LPOFF mode.

### 11.15.2 FS1B pin

FS1B pin is the secondary safe output pin. FS1B is asserted low with a configurable delay ( $t_{\text{DELAY}}$ ) or duration ( $t_{\text{DUR}}$ ) when FS0B is asserted low (see [Section 12.5.6](#)). This pin can be used to:

- Open the phases of a motor after a configurable delay starting when FS0B is asserted, to demagnetize the motor coils and reduce the inductive effect when the switch is open.
- Disable an external physical layer during a configurable duration starting when FS0B is asserted, to avoid miscommunication when the module is in fail mode.
- Be a redundant safe output pin to FS0B when  $t_{\text{DELAY}} = 0$ . In this case, FS1B is asserted at the same time than FS0B.
- Any other use case where a second safety pin is needed.

After each power-on reset or after each wake-up event (LPOFF), the FS1B pin is asserted low. Then the MCU can decide to release the FS1B pin, when the application is ready to start. An external pull-up circuitry is mandatory, connected to VPU\_FS or VDDIO.

### 11.15.3 RSTB pin

The RSTB pin must be connected to MCU and is active low. An external pull-up resistor must be connected to VDDIO. In default configuration, the RST delay time has three possible values depending on the mode and product configuration:

- The longest one is used automatically following a power-on reset or when resulting from LPOFF mode (low-power off).
- The two reset durations are then available in the INIT\_FSSM register, which are 1.0 ms and 10 ms. The configured duration is finally used in the normal operation when a fault occurs leading to a reset activation. The INIT\_FSSM register is available (writing) in the INIT\_FS phase.

## 11.16 VPU\_FS (fail-safe pull-up)

This pin is intended to be the pull-up terminal of FS1B, internally attached to  $V_{\text{PRE}}$  through a reverse diode protection. This independent pull-up (compared to FS0B pull-up) avoids common cause failures between the two safe outputs. When FS1B is used with  $t_{\text{DELAY}} = 0$  or in  $t_{\text{DUR}}$  configuration, a pull-up to VDDIO is also possible, taking into account the common cause failure with the same pull-up as FS0B in the safety analysis.

### 11.17 DEBUG input (entering in debug mode)

The DEBUG pin allows the product to enter debug mode. To activate the debug mode, voltage applied to the DEBUG pin must be within the  $V_{\text{DEBUG\_IL}}$  and  $V_{\text{DEBUG\_IH}}$  range at start-up. If the voltage applied to DEBUG pin is out of these limits, during the SELECT pin configuration, the device settles into normal mode.

In debug mode, the watchdog window is fully open and no watchdog refresh is required. This allows an easy debug of the hardware and software routines (i.e. SPI commands). However, the whole watchdog functionality is kept on (WD refresh counter, WD error counter,...). WD errors are detected and counted with reaction according to WD\_IMPACT bit configuration. When the debug mode is activated, the fail-safe outputs (FS0B, FS1B) are asserted low at start-up. The release procedure and the assertion conditions are the same than in normal mode. When the Debug mode is activated, there is no deep fail-safe state.

The CAN transceiver is set to normal operation mode by default allowing CAN communication without SPI configuration (FS1B\_CAN\_IMP bit = 0). To exit debug mode, the pin must be tied to ground through an external pull-down resistor and a power-on reset or wake-up from LPOFF occurs.

## 12 Functional device operation

### 12.1 Mode and state description of the main state machine

The device has several operation modes. The transition and conditions to enter or leave each mode are illustrated in the functional state diagram ([Figure 15](#)). Two state machines work in parallel. The main state machine controls the power management (VPRE, VCORE, VCCA, VAUX,...) and the fail-safe state machine controls all the safety aspects (WD, RSTB, FS0B, FS1B,...).

#### 12.1.1 Buck or buck boost configuration

An external low-side logic level MOSFET (N-type) is required to operate in non-inverting buck-boost converter. The connection of the external MOSFET is detected automatically during the start-up phase (after a power-on reset or from LPOFF).

- If the external low-side MOSFET is **not** connected (GATE\_LS pin connected to PGND), the product is configured as a standard buck converter.
- If the external low-side MOSFET is connected (GATE\_LS pin connected to external MOSFET gate), the product is configured as a non-inverting buck-boost converter.

The automatic detection is done by pushing 300  $\mu\text{A}$  current on Gate\_LS pin and monitoring the corresponding voltage generated. If a voltage  $>120$  mV is detected before the 120  $\mu\text{s}$  timeout, the non-inverting buck-boost configuration is locked. Otherwise, the standard buck configuration is locked. The boost driver has a current capability of  $\pm 300$  mA.

#### 12.1.2 $V_{\text{PRE}}$ on

Pre-regulator is an SMPS regulator. In this phase, the pre-regulator is switched on and a soft start with a specified duration  $t_{\text{PRE\_SOFT}}$  controls the VPRE output capacitor charge.

#### 12.1.3 SELECT pin configuration

This phase detects the required voltage level on VAUX and VCCA, according to the resistor value connected between the SELECT pin and Ground or VPRE, and configures the deep fail-safe function.

#### 12.1.4 $V_{CORE}/V_{AUX}/V_{CCA}$ on

In this stage, the three regulators  $V_{CORE}$ ,  $V_{AUX}$ ,  $V_{CCA}$  are switched on at the same time with a specified soft start duration. The  $CAN\_5V$  is also started at this time.

#### 12.1.5 INIT main

This mode is automatically entered after the device is 'powered on'. When RSTB is released, initialization phase starts where the device can be configured via the SPI. During INIT phase, some registers can only be configured in this mode (see [Table 19](#) and [Table 20](#)). Other registers can be written in this mode, and also in normal mode.

Once the INIT registers configurations are complete, a last register called 'INIT\_INT' must be configured to switch to normal mode. Writing data in this register (even same default values), automatically locks the INIT registers, and the product switches automatically to normal mode in the main state machine.

#### 12.1.6 Normal

In this mode, all device functions are available. This mode is entered by a SPI command from the INIT phase by writing in the INIT\_INT register. While in normal mode, the device can be set to low-power mode (LPOFF) using secured SPI command.

#### 12.1.7 Low-power mode off

The main state machine has three LPOFF modes with different conditions to enter and exit each LPOFF mode, as described hereafter. After wake-up from LPOFF, all the regulators are enabled by default. In LPOFF, all the regulators are switched off, except  $V_{KAM}$ . The register configuration and the ISO pulse requirement are valid for the three LPOFF modes.

##### 12.1.7.1 LPOFF - sleep

Entering in low-power mode LPOFF - sleep is only available if the product is in normal mode by sending a secured SPI command. In this mode, all the regulators are turned off and the MCU connected to the  $V_{CORE}$  regulator is unsupplied. Only  $V_{KAM}$  is available if  $V_{KAM}$  is used (specific part number for  $V_{KAM}$  on by default).

Once the FS6500/FS4500 is in LPOFF - sleep, the device monitors external events to wake-up and leave the low-power mode. The wake-up events can occur and depending on the device configuration from:

- Physical layer (CAN or LIN)
- I/O inputs
- Timer

When a wake-up event is detected, the device starts the main state machine again by detecting the  $V_{PRE}$  configuration (buck or buck-boost), the wake-up source is reported to the dedicated SPI register, and the fail-safe state machine is also restarted.

##### 12.1.7.2 LPOFF - auto WU

LPOFF - auto WU is entered when the device is in the INIT or normal mode and if the  $V_{PRE}$  voltage level is passing the  $V_{PRE\_UV\_4P3}$  threshold (typ 4.3 V). It can be also entered by sending a secured SPI command if the product is in normal mode. It allows a POR and complete restart of the fail-safe state machine. After 1.0 ms, the device attempts to recover by switching on  $V_{PRE}$  again.

**12.1.7.3 LPOFF - deep FS**

LPOFF - deep FS is entered when the device is in deep fail-safe and if the key is off (IO\_0 is low). To exit this mode, a transition to high level on IO\_0 is required. IO\_0 is usually connected to the key on key off signal (see [Section 12.3](#)).

**12.1.7.4 Register configuration in LPOFF**

In LPOFF, the register settings of the main state machine are kept because the internal 2.5 V main digital regulator is available for wake-up operation. However, the register settings of the fail-safe state machine are erased because the 2.5 V fail-safe digital regulator is not available in LPOFF. As a consequence, after a wake-up event, the configuration of the fail-safe registers must be done again during initialization phase (256 ms open window).

**12.1.7.5 ISO pulse in LPOFF**

If the application has to sustain ISO pulses on V<sub>BAT</sub> in LPOFF mode, the connection of an external Zener diode and a serial resistor to the ground is mandatory (see [Figure 14](#)). During repetitive ISO pulses on V<sub>BAT</sub>, the capacitors connected on V<sub>SUP</sub> line are more and more charged and cannot be discharged due to the extremely low-current needed to maintain wake-up capabilities on IOs, CAN, and LIN. As a consequence, if a leakage path is not created artificially with those discrete components, the voltage on V<sub>SUP</sub> line can exceed the absolute maximum rating supported by this pin.

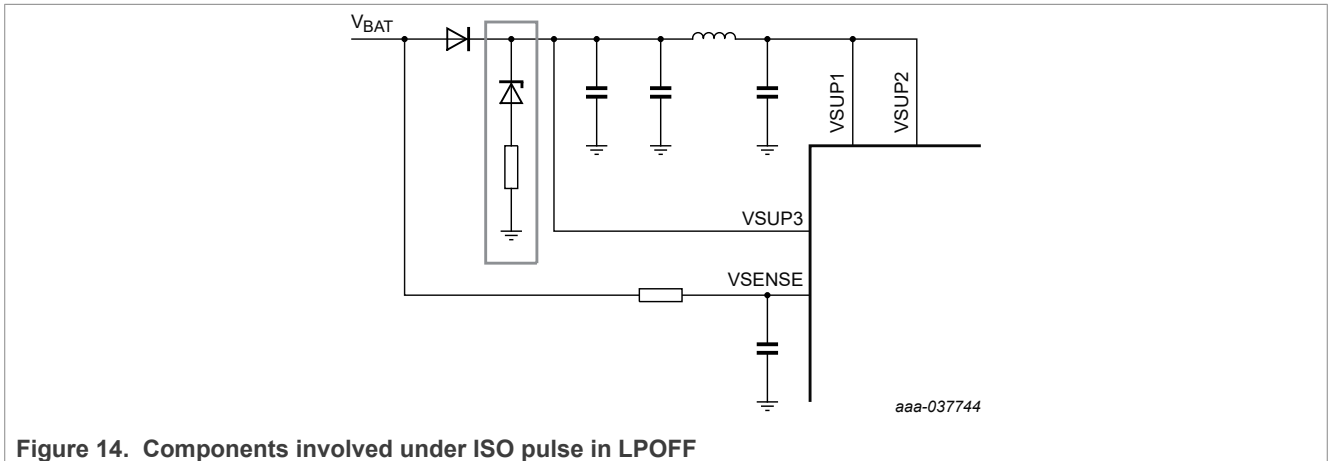


Figure 14. Components involved under ISO pulse in LPOFF

**12.2 Mode and state description of fail-safe state machine**

**12.2.1 Select pin configuration**

This phase detects the required voltage level to apply on VAUX and VCCA according to the resistor value connected between the SELECT pin and Ground or VPRE, and the deep fail-safe configuration. This mode is the equivalent mode seen in the main state machine. In the fail-safe machine this detection is used to internally set the UV/OV threshold on VCCA and VAUX for the voltage supervision, and to enable/disable the deep fail-safe feature.

**12.2.2 ABIST**

Included in the fail-safe machine, the analog built-in self-test (ABIST) verifies the correct functionality of the analog part of the device like the overvoltage and undervoltage detections of the voltage supervisor and the fail-

safe outputs feedback. ABIST fail does not gate the RSTB pin release, but prevents the FS0B and FS1B pins release. It allows the MCU diagnostic, keeping the application in safe state.

**12.2.2.1 ABIST1**

The first ABIST1 ([Table 9](#)) is always run at start-up and after each wake-up event when device is in LPOFF mode.

**Table 9. Regulators and fail-safe pins checked during ABIST1**

Parameters	Overvoltage	Undervoltage	OK/NOK
VPRE	X		
VCORE (including FCRBM)	X	X	
VCCA	X	X	
RSTB			X
FS0B			X

**12.2.2.2 ABIST2**

The second ABIST2 ([Table 10](#)) is run on demand by a SPI command from the MCU. ABIST2 must be executed and pass for FS1B and VAUX, when VAUX is declared safety critical (overvoltage and/or undervoltage have an impact on fail-safe outputs) to release the FS0B pin. Consequently, ABIST2 must be executed at start-up and after each wake-up event when device is in LPOFF mode, to release the fail-safe pin FS0B.

**Table 10. Regulators and fail-safe pins checked during ABIST2**

Parameters	Overvoltage	Undervoltage	OK/NOK
VAUX	X	X	
FS1B			X

**12.2.3 Release RSTB**

In this state, the device releases the RSTB pin.

**12.2.4 INIT\_FS**

This mode is automatically entered after the device is 'powered on' and the built-in self-test (analog ABIST1) has been executed. This INIT\_FS mode starts as soon as RSTB is released.

In this mode, the device can be configured via the SPI within a maximum time of 256 ms, including first watchdog refresh. Some registers can only be configured in this mode and is locked when leaving INIT\_FS mode (see [Table 19](#) and [Table 20](#)). It is recommended, to configure the device first before sending the first WD refresh. As soon as the first good watchdog refresh is sent by the MCU, the device leaves this mode and goes into normal WD mode.

**12.2.5 Normal WD**

In this mode, the device waits for a periodic watchdog refresh coming from the MCU, within a specific configured window timing. Configuration of the watchdog window period can be set during INIT\_FS phase or in this mode. This mode is exited if a fault occurs leading to an RSTB activation (external reset request included).

### 12.2.6 Assert RSTB

When the reset pin is asserted low by the device, a delay runs, to release RSTB, if there are no faults present. The reset low duration time is configurable via the SPI in the INIT\_FSSM register, which is accessible for writing only in the INIT\_FS phase.

### 12.2.7 Assert FSxB and ABIST2

These functions are executed in parallel to INIT\_FS or normal WD states of the fail-safe state machine.

## 12.3 Deep fail-safe state

When the deep fail-safe function is enabled, the fail-safe state machine monitors and counts the number of faults happening, in case of fault detection (see [Section 12.5.3](#)). As soon as either the fault error counter reaches its final value or the RESET pin remains asserted low for more than 8.0 s, the device moves to deep fail-safe state in the functional state diagram ([Figure 15](#)).

When the device is in deep fail-safe state, all the regulators are off (except VKAM if VKAM was on), RSTB, FS0B, and FS1B are activated. To exit this state, a key off/key on action is needed. IO\_0 is usually connected to key signal. Key off (IO\_0 low) moves the device to LPOFF-deep FS, and key on (IO\_0 high) wakes up the device.

During power up phase, the 8.0 s timer starts when the fail-safe state machine enters in the 'Wait\_V<sub>PRE</sub>' state and stops when the RSTB pin is released. During 'INIT\_FS' state, the 8.0 s timer can be disabled in the register INIT\_FS\_IMPACT. During 'normal WD' state, the 8.0 s timer is activated at each RSTB pin assertion.

12.4 Functional state diagram

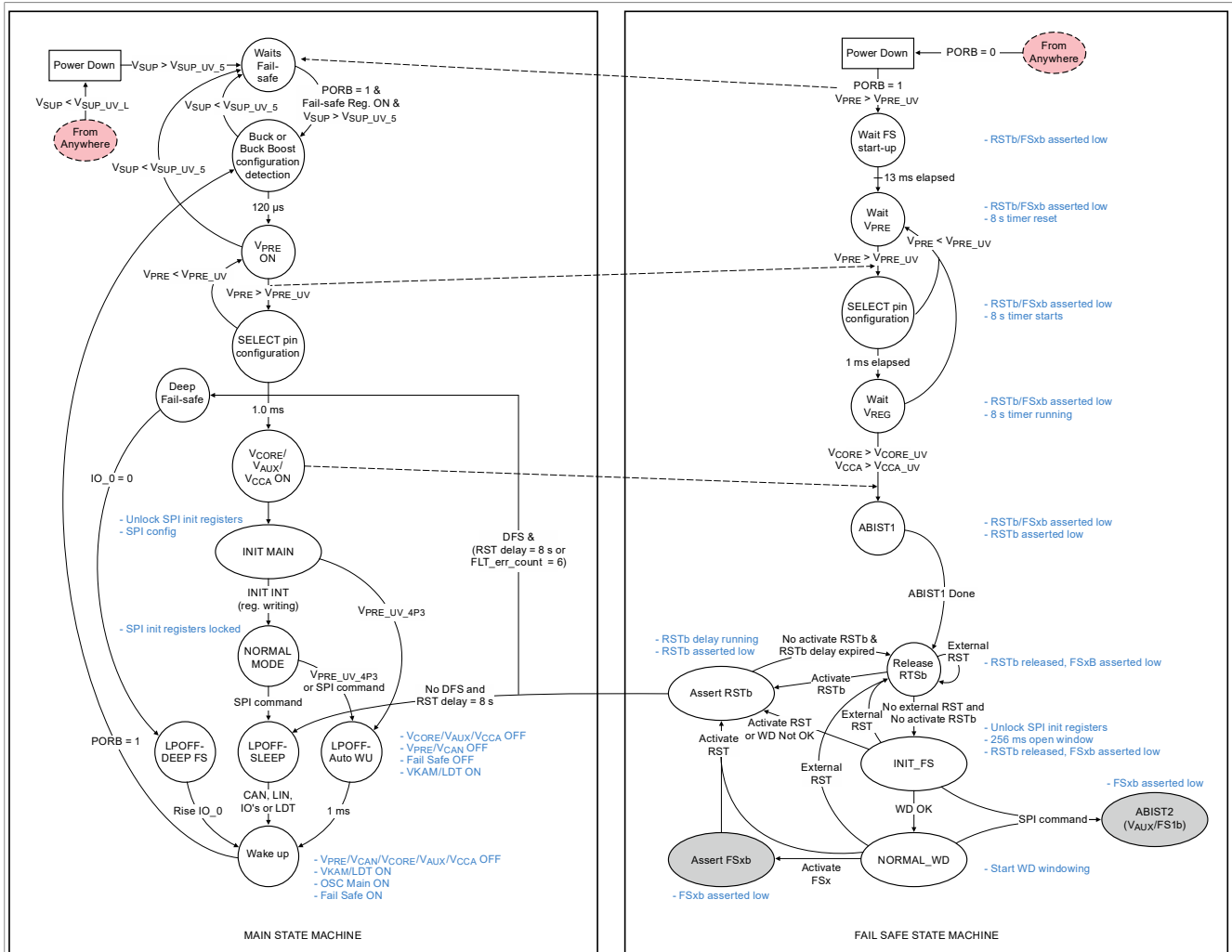


Figure 15. Simplified state diagram

12.5 Fail-safe machine

To fulfill safety critical applications, the FS6500/FS4500 integrates a dedicated fail-safe machine (FSM). The FSM is composed of three main sub-blocks: the voltage supervisor (VS), the fail-safe state machine (FSSM), and the fail-safe output driver (FSO). The FSM is electrically independent from the rest of the circuitry, to avoid common cause failure.

For this reason, the FSM has its own voltage regulators (analog and digital), dedicated band gap, and its own oscillator. Three power supply pins (VSUP 1, 2, and 3) are used to overtake a pin lift issue. The internal voltage regulators are directly connected on VSUP (one bonding wire per pin is used). Additionally, the ground connection is redundant as well to avoid any loss of ground.

All the voltages generated in the device are monitored by the voltage supervisor (under and overvoltage) owing to a dedicated internal voltage reference (different from the one used for the voltage regulators). The result is reported to the MCU through the SPI and delivered to the fail-safe state machine (FSSM) for action, in case of a fault. All the safety relevant signals feed the FSSM, which handles the error handling and controls the fail-safe outputs.



There are three fail-safe outputs: RSTB (asserted low to reset the MCU), FS0B, and FS1B (asserted low to control any fail-safe circuitry). The fail-safe machine is in charge of bringing and maintaining the application in a fail-safe state.

12.5.1 Fail-safe machine state diagram

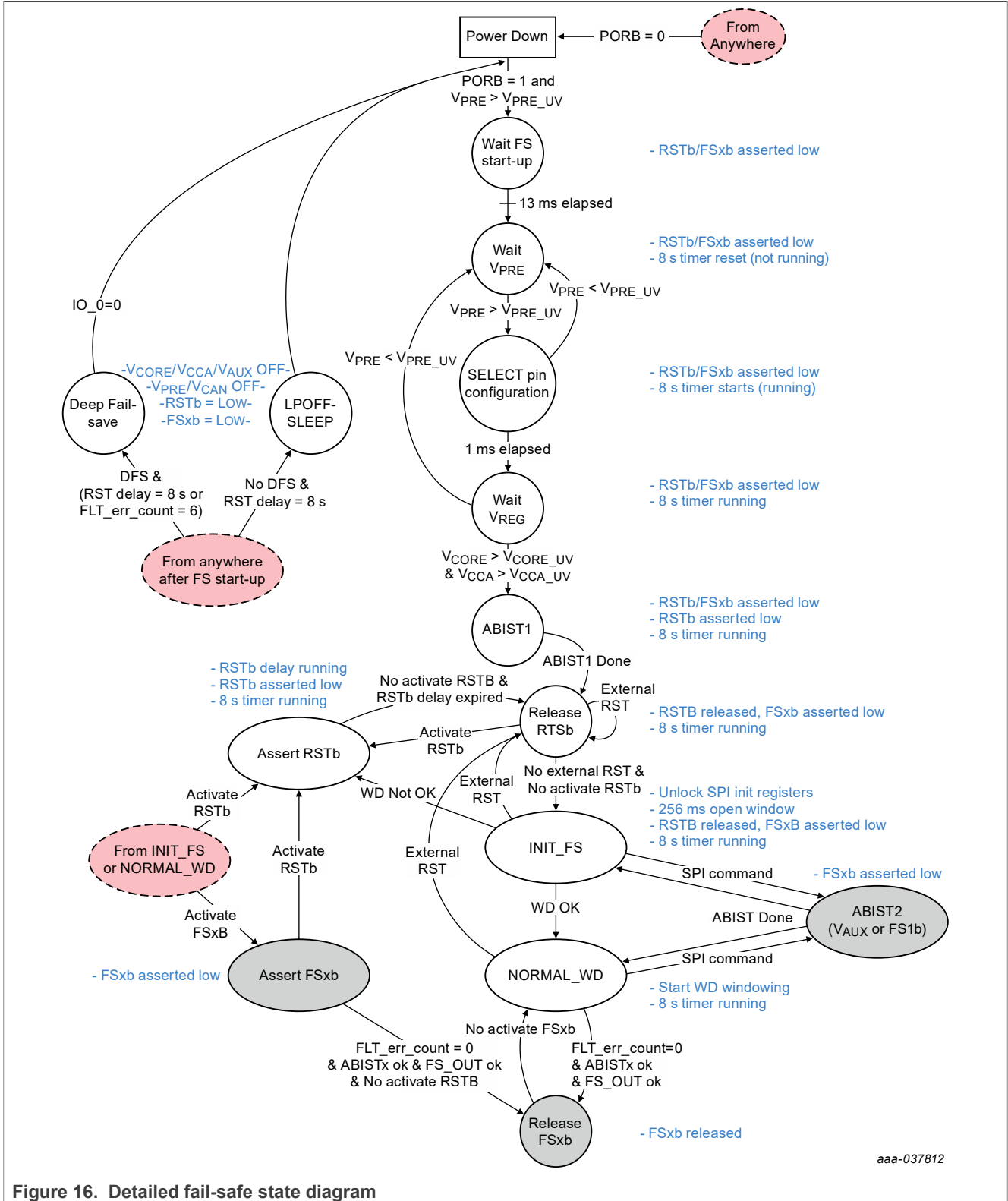


Figure 16. Detailed fail-safe state diagram

## 12.5.2 Watchdog operation

A simple windowed watchdog is implemented in the FS6500/FS4500. The watchdog must be continuously triggered by the MCU in the open watchdog window, otherwise an error is generated. The error handling and watchdog operations are managed by the fail-safe state machine. For debugging purpose, this functionality can be inhibited by setting the right voltage on the DEBUG pin at start-up.

The watchdog window duration is selectable through the SPI during the INIT\_FS phase or in normal mode. The following values are available: 1.0 ms, 2.0 ms, 3.0 ms, 4.0 ms, 6.0 ms, 8.0 ms, 12 ms, 16.0 ms, 24 ms, 32 ms, 64 ms, 128 ms, 256 ms, 512 ms, and 1024 ms. The watchdog can also be inhibited through the SPI register in INIT\_FS phase to allow "reprogramming" (i.e. at vehicle level thru CAN).

The MCU must write in the WD\_ANSWER register during the OPEN watchdog window. In that case, the watchdog window is restarted. If the WD\_ANSWER is accessed during the CLOSED watchdog window, the WD error counter is incremented and the watchdog window is restarted. Anything can be written in the WD\_ANSWER register to refresh the watchdog, regardless of the LFSR register value.

### 12.5.2.1 Normal operation (first watchdog refresh)

At power up, when the RSTB is released as high (after around 16.5 ms), the INIT phase starts for a maximum duration of 256 ms and this is considered as a fully open watchdog window. During this initialization phase, the MCU can configure the product, and no WD error will be detected.

When the configuration is done, the MCU accesses the WD\_ANSWER SPI register to send the first WD refresh. When the watchdog is properly refreshed during the open window, the 256 ms open window is stopped and the initialization phase is finished. If the watchdog is not refreshed during this 256 ms open window (INIT\_FS phase), the device asserts the RSTB, FS0B, and the fault error counter is incremented by '1'.

After a good watchdog refresh, the device enters the Normal WD refresh mode, where open and closed windows are defined either by the configuration made during initialization phase in the WD\_WINDOW register ([Table 88](#)), or by the default value already present in this register (3.0 ms).

### 12.5.2.2 Normal watchdog refresh

The watchdog must be refreshed during every open window of the window period configured in the register WD\_ANSWER. Any WD refresh restarts the window. This ensures the synchronization between MCU and FS6500/FS4500.

The duration of the 'window' is selectable through the SPI with no access restriction, meaning the window duration can be changed in the INIT phase or normal mode. Doing the change in normal operation allows the system integrator to configure the watchdog window duration on the fly:

- The new WD window duration (except after disable) is taken into account when a proper write access in the WD\_ANSWER register occurs or when the previous WD window is finished without any writing (WD timeout).
- The new WD window duration after disable is taken into account when the SPI command is validated.

The duty cycle of the window is set to 50 %  $\pm$ 10 % and is not modifiable.

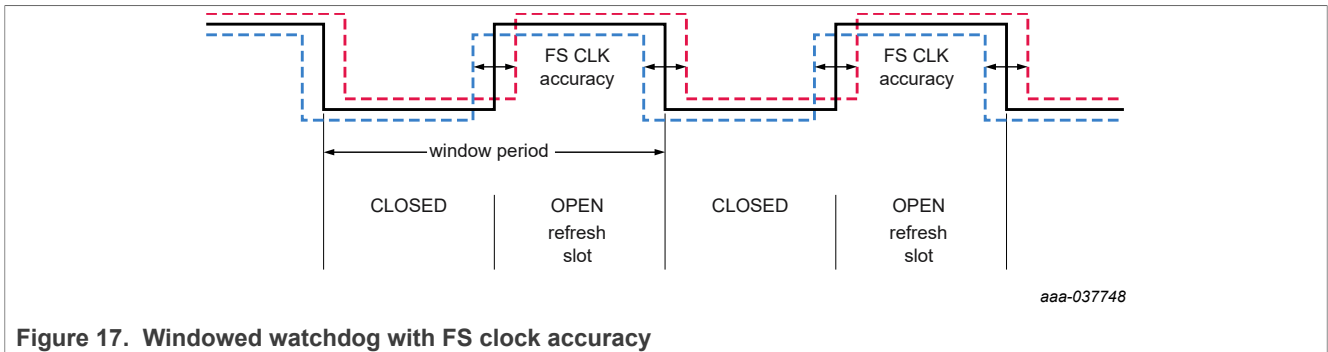


Figure 17. Windowed watchdog with FS clock accuracy

### 12.5.2.3 Watchdog in debug mode

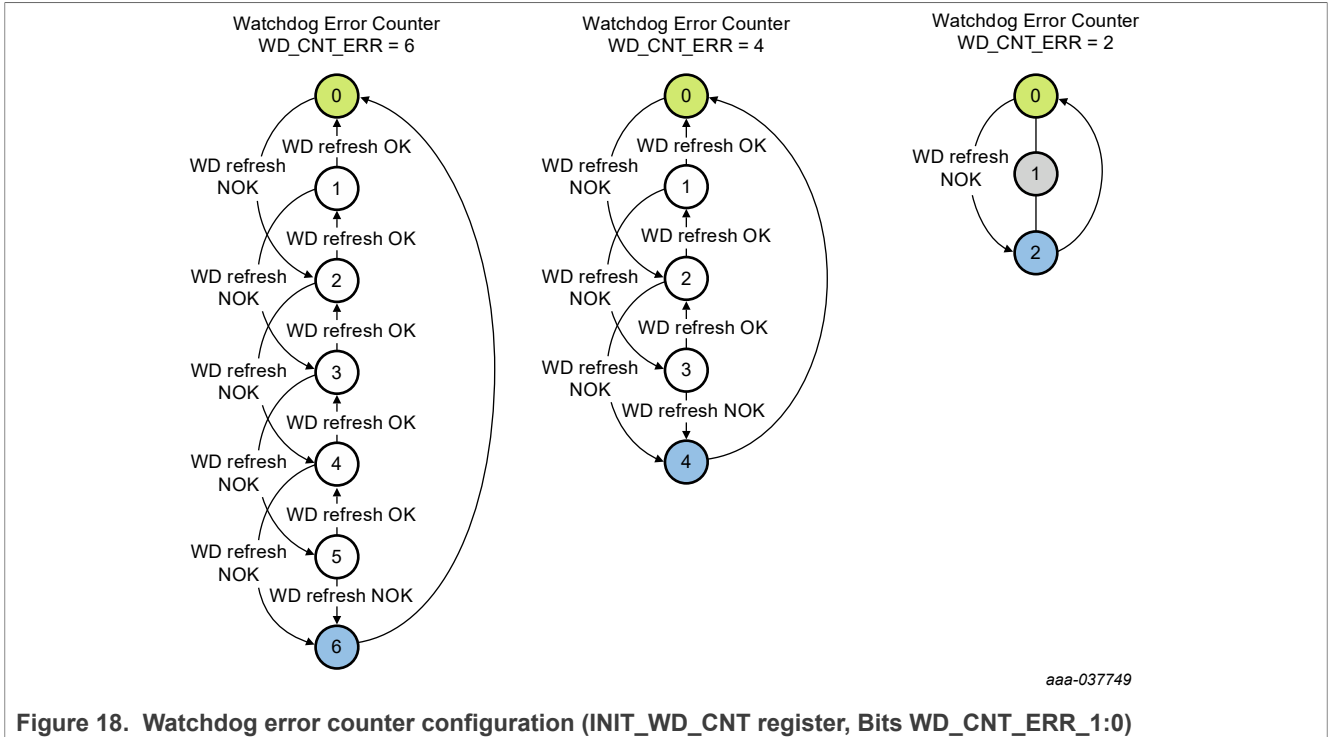
When the device is in debug mode (entered via the DEBUG pin), the watchdog continues to operate, but does not affect the device operation by asserting a reset of the fail-safe pins. For the user, operation appears without the watchdog. If needed and to debug the watchdog itself, the user can operate as in normal mode and check the watchdog refresh counter, the watchdog error counter, and the reset counter. This allows the user to debug their software and ensure a good watchdog strategy in the application.

### 12.5.2.4 Wrong watchdog refresh handling

Error counters and strategy are implemented in the device to manage wrong watchdog refreshes from the MCU. According to consecutive numbers of wrong watchdog refreshes, the device can decide to assert the RSTB and/or FS0B pin, depending on the safety configuration set during the INIT\_FS phase (WD\_IMPACT bit in INIT\_SF\_IMPACT register, [Table 86](#)).

### 12.5.2.5 Watchdog error counter

The watchdog error counter is implemented in the device to filter the incorrect watchdog refresh. Each time a watchdog failure occurs, the device increments this counter by 2. The WD error counter is decremented by 1 each time the watchdog is properly refreshed. This principle ensures a cyclic 'OK/NOK' behavior converges to a failure detection. To allow flexibility in the application, the maximum value of this counter is configurable in the INIT\_WD\_CNT register, but only when device is in INIT\_FS mode.



### 12.5.2.6 Watchdog refresh counter

The watchdog refresh counter is used to decrement the fault error counter. Each time the watchdog is properly refreshed, the watchdog refresh counter is incremented by '1'. Each time the watchdog refresh counter reaches '6' and if next WD refresh is also good, the fault error counter is decremented by '1' (case with WD\_CNT\_RFR\_1:0 configured at 6).

Whatever the position the watchdog refresh counter is in, each time there is a wrong refresh watchdog, the watchdog refresh counter is reset to '0'. To allow flexibility in the application, the maximum value of this watchdog refresh counter is configurable in the INIT\_WD\_CNT register, but only when device is in INIT\_FS mode.

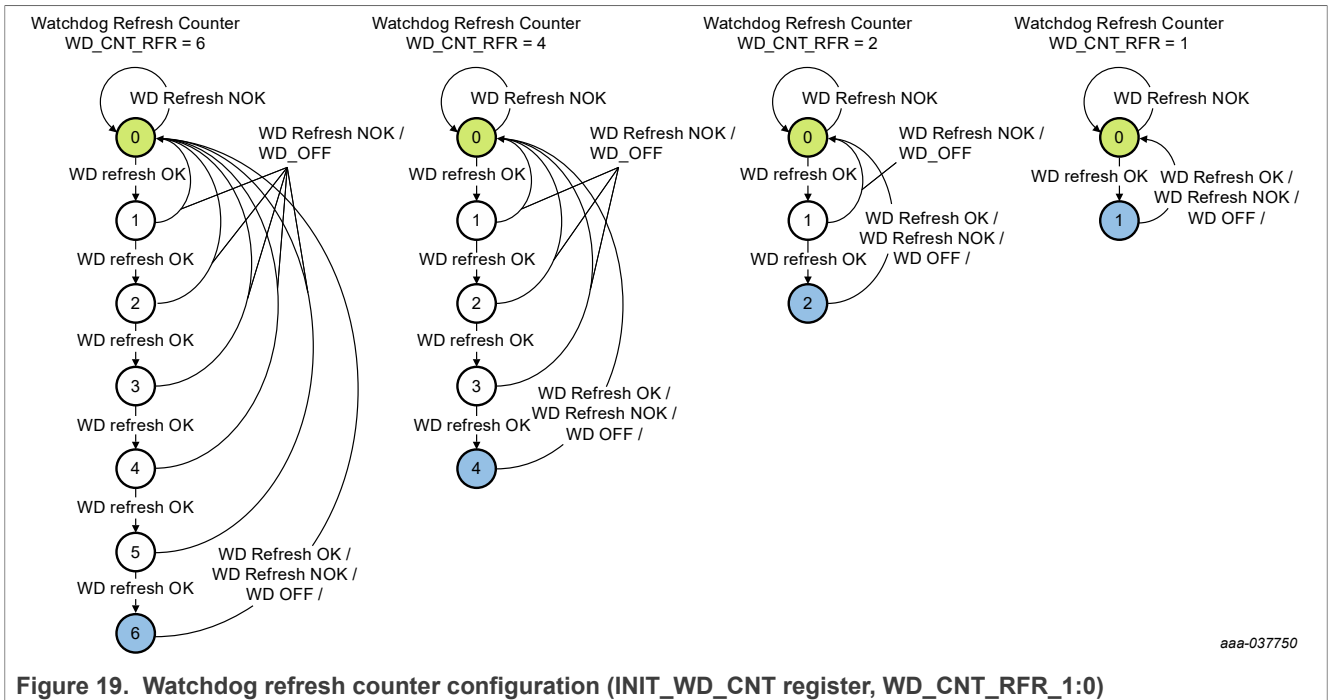


Figure 19. Watchdog refresh counter configuration (INIT\_WD\_CNT register, WD\_CNT\_RFR\_1:0)

Table 11. Watchdog error table

		Window	
		CLOSED	OPEN
SPI	Valid write access to WD_ANSWER	WD_NOK	WD_OK
	No write access to WD_ANSWER (timeout)	No_issue	WD_NOK

Any access to the watchdog register during the 'closed' watchdog window is considered as a wrong watchdog refresh. Watchdog timeout, meaning no WD refresh during closed or open windows, is considered as a wrong WD refresh.

### 12.5.3 Fault error counter

The fault error counter manages and counts the number of faults occurring in the application. This counter is incremented not only for the fault linked to consecutive wrong refresh watchdogs, but also for other sources of fault (undervoltage, overvoltage, external reset,...).

The fault error counter is incremented by 1, each time RSTB and/or FS0B pin is asserted. When FS0B is asserted, the fault error counter is incremented by 1, every time the watchdog error counter maximum value is reached. The fault error counter has two output values (intermediate and final).

- The intermediate value can be used to force the FS0B activation or to generate a RSTB pulse depending on the FLT\_ERR\_IMP\_1:0 bit configuration in INIT\_FAULT register.
- The final value is used to handle the transition to deep fail-safe when the SELECT pin is connected to Ground. If the SELECT pin is connected to VPRE, the main state machine remains in normal mode and the regulators remain on.

The intermediate value of the fault error counter is configurable to '1' or '3' using the FLT\_ERR\_FS bit in the INIT\_FAULT register (Table 83). The final value of the fault error counter is based on the intermediate configuration. This configuration must be done during INIT\_FS phase.

- FLT\_ERR\_FS = 0/Intermediate = 3; Final = 6 (Figure 20).
- FLT\_ERR\_FS = 1/Intermediate = 1; Final = 2 (Figure 21).

In any condition, if the RSTB pin is asserted low for a duration longer than eight seconds, the device goes to:

- Deep fail-safe if the DFS function is enabled (SELECT pin connected to ground)
  - LPOFF-sleep if the DFS function is disabled (SELECT pin connected to VPRES)
- The following faults lead to an increment of the fault error counter and can be configured:

- Watchdog error counter = max value (6 by default)
- V<sub>CORE</sub>, V<sub>CCA</sub>, V<sub>AUX</sub> undervoltage
- V<sub>CORE</sub>, V<sub>CCA</sub>, V<sub>AUX</sub> overvoltage
- FCRBM follows V<sub>CORE</sub> configuration
- IO\_45 error detection (external IC error)

The following faults lead to an increment of the fault error counter and cannot be configured:

- VPRES overvoltage
- Watchdog refresh not OK or watchdog timeout during INIT phase
- SPI DED
- ABIST1, ABIST2 fail
- RSTB short to high (by cascaded effect of FS0B assertion)
- External reset (except reset extension by MCU after reset assertion by the device)

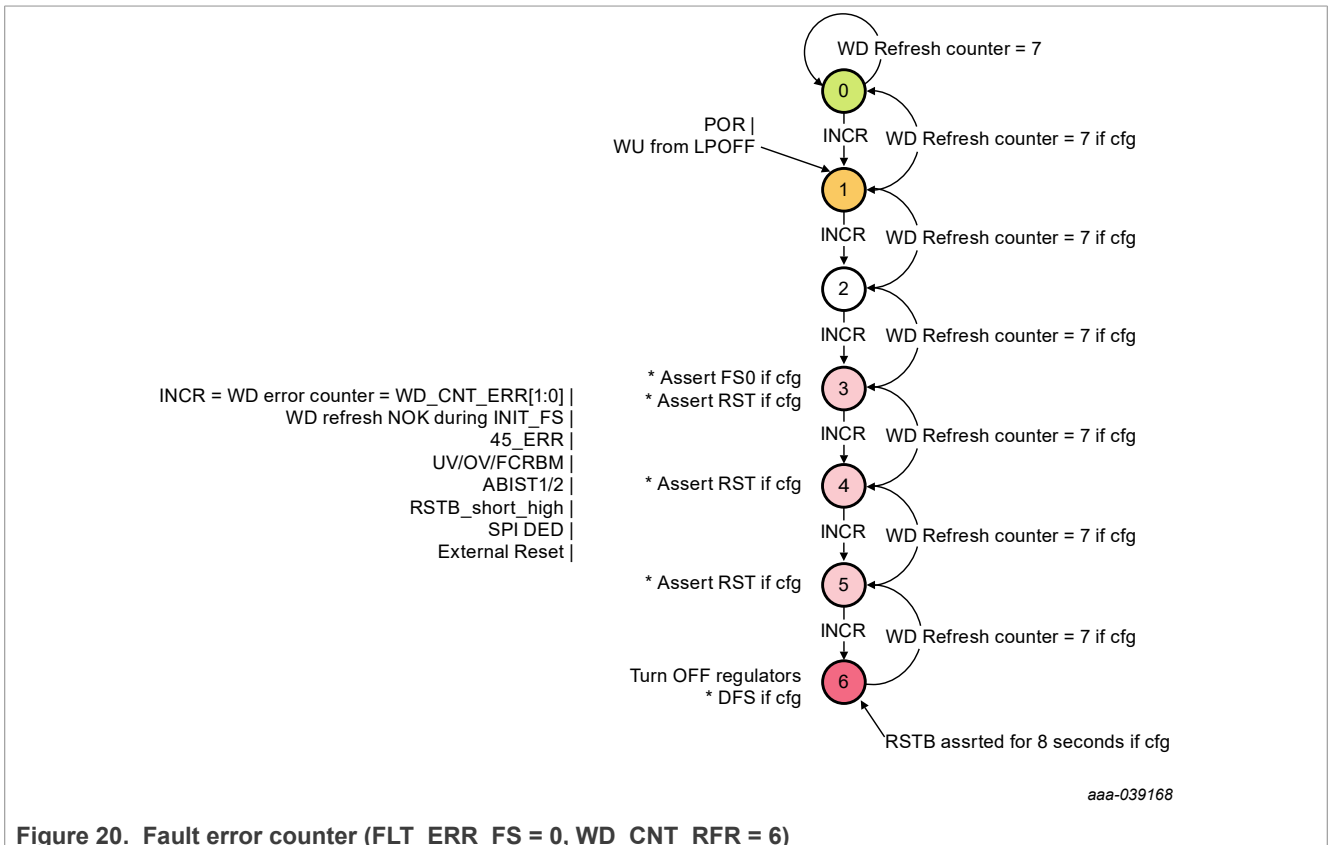
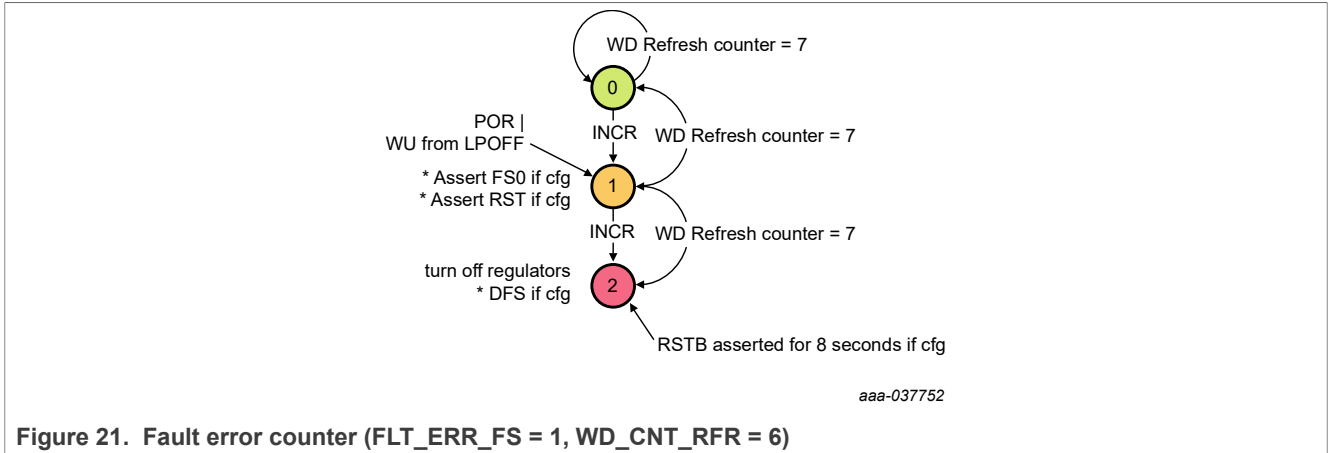


Figure 20. Fault error counter (FLT\_ERR\_FS = 0, WD\_CNT\_RFR = 6)



12.5.3.1 Fault error counter intermediate value

Figure 22 illustrates the fault error counter increment when the watchdog error counter maximum value is reached.

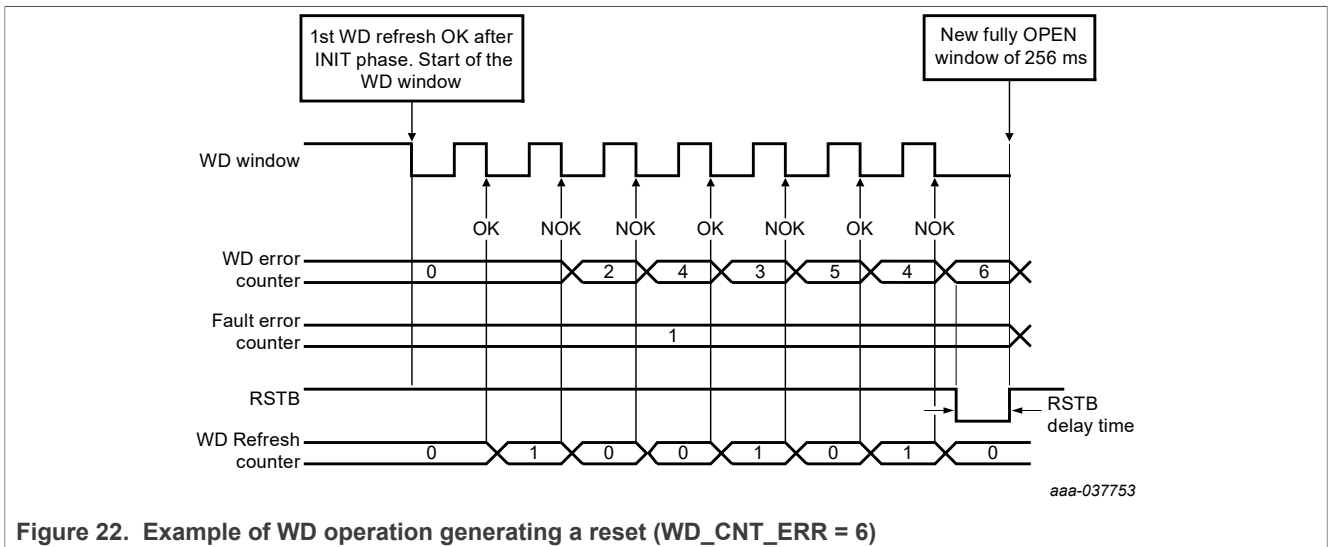


Figure 23 illustrates the RSTB and FS0B possible behavior at the fault error counter intermediate value depending on WD\_IMPACT\_1:0 and FLT\_ERR\_IMP\_1:0 bits configurations:

- #1, WD\_IMPACT\_1:0 = '01' and FLT\_ERR\_IMP\_1:0 = '01': WD impact on RSTB only and FS0B is asserted low if FLT\_ERR\_CNT ≥ intermediate value
- #2, WD\_IMPACT\_1:0 = '10' and FLT\_ERR\_IMP\_1:0 = '10': WD impact on FS0B only and RSTB is asserted low if FLT\_ERR\_CNT ≥ intermediate value and WD error counter = WD\_CNT\_ERR[1:0]



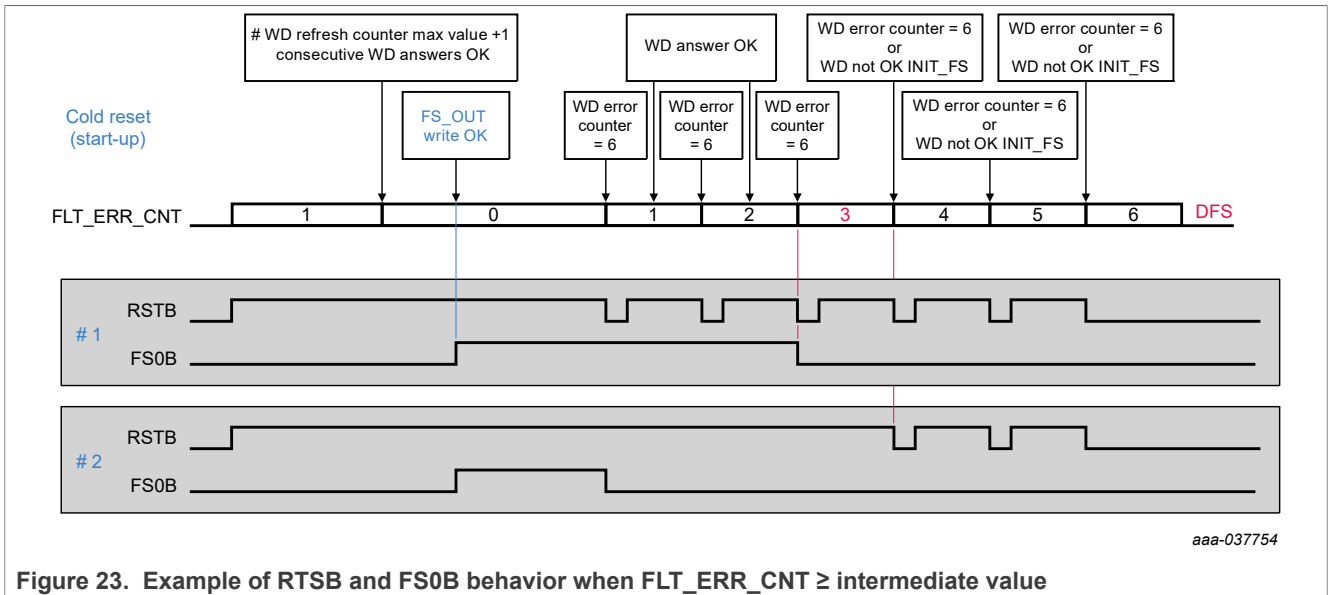


Figure 23. Example of RTSB and FS0B behavior when FLT\_ERR\_CNT ≥ intermediate value

### 12.5.3.2 Fault error counter at start-up or resuming from LPOFF mode

At start-up or when resuming from LPOFF mode, the fault error counter starts at level 1 and FS0B is asserted low. To release FS0B, the fault error counter must go back to a '0' value due to several consecutive good watchdog refreshes. The right command is sent to the RELEASE\_FSxB register (Figure 25). With the default watchdog refresh counter configuration (WD\_RFR\_CNT = 6), seven consecutive good watchdog refreshes decrease the fault error counter to 0 (Figure 24).

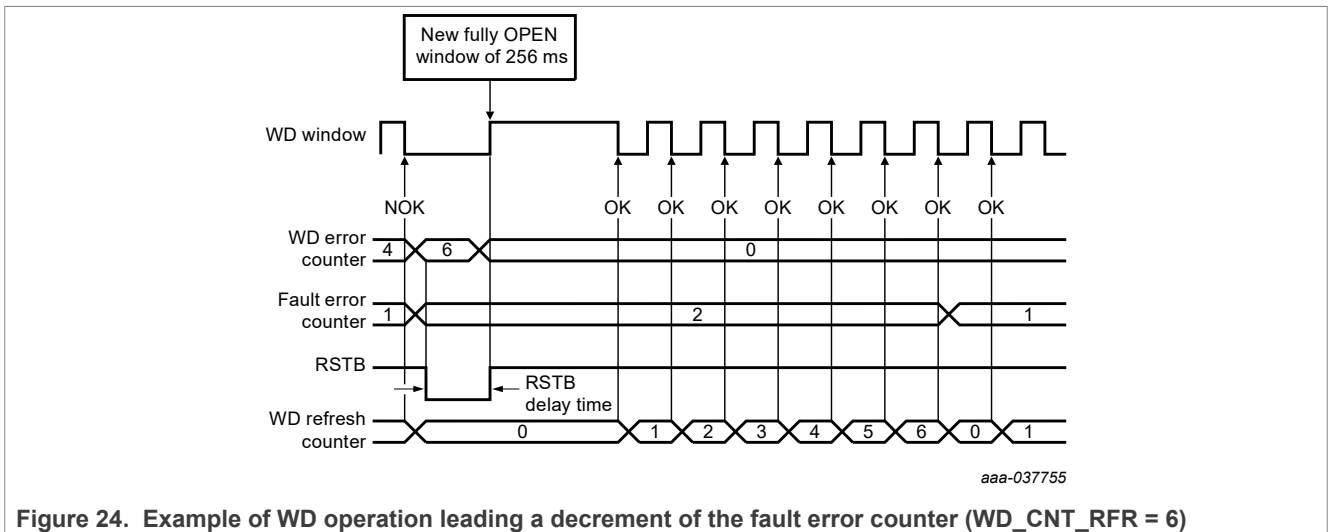


Figure 24. Example of WD operation leading a decrement of the fault error counter (WD\_CNT\_RFR = 6)

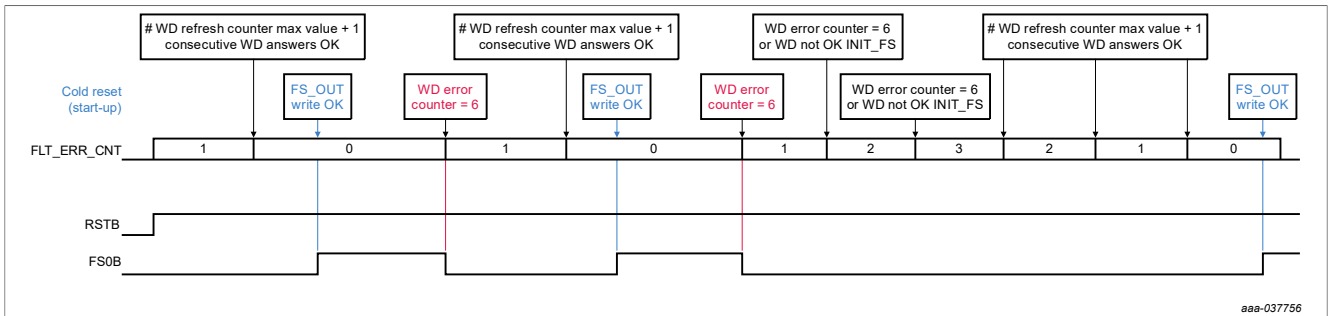


Figure 25. Fault error counter and FS0B deactivation sequence (FLT\_ERR\_FS = 0 and WD\_CNT\_ERR = 6)

### 12.5.4 RESET (RSTB) activation

The activation of RSTB depends on the fail-safe state machine configuration performed during the INIT\_FS phase.

The following faults impact on RSTB activation can be configured:

- Watchdog error counter = max value (6 by default)
- VCORE, VCCA, VAUX undervoltage
- VCORE, VCCA, VAUX overvoltage
- FCRBM follows VCORE configuration
- Fault error counter level

The following faults impact on RSTB activation cannot be configured:

- VPRE overvoltage
- Watchdog refresh not OK or watchdog timeout during INIT phase
- FS0B short to high
- RSTB pulse requested by SPI

### 12.5.5 Fail-safe output (FS0B) activation

The activation of FS0B depends on the fail-safe state machine configuration performed during the INIT\_FS phase.

The following faults impact on FS0B activation can be configured:

- Watchdog error counter = max value (6 by default)
- VCORE, VCCA, VAUX undervoltage
- VCORE, VCCA, VAUX overvoltage
- FCRBM follows VCORE configuration
- IO\_45 error detection (external IC error)
- Fault error counter level

The following faults impact on FS0B activation cannot be configured:

- VPRE overvoltage
- Watchdog refresh not OK or watchdog timeout during INIT phase
- ABIST1/2 fail
- RSTB, FS1B short to high
- FS0B low requested by SPI
- SPI DED

12.5.6 Fail-safe output (FS1B) activation

The activation of FS1B follows the activation of FS0B with a configurable delay ( $t_{DELAY}$ ) or for a configurable duration ( $t_{DUR}$ ).

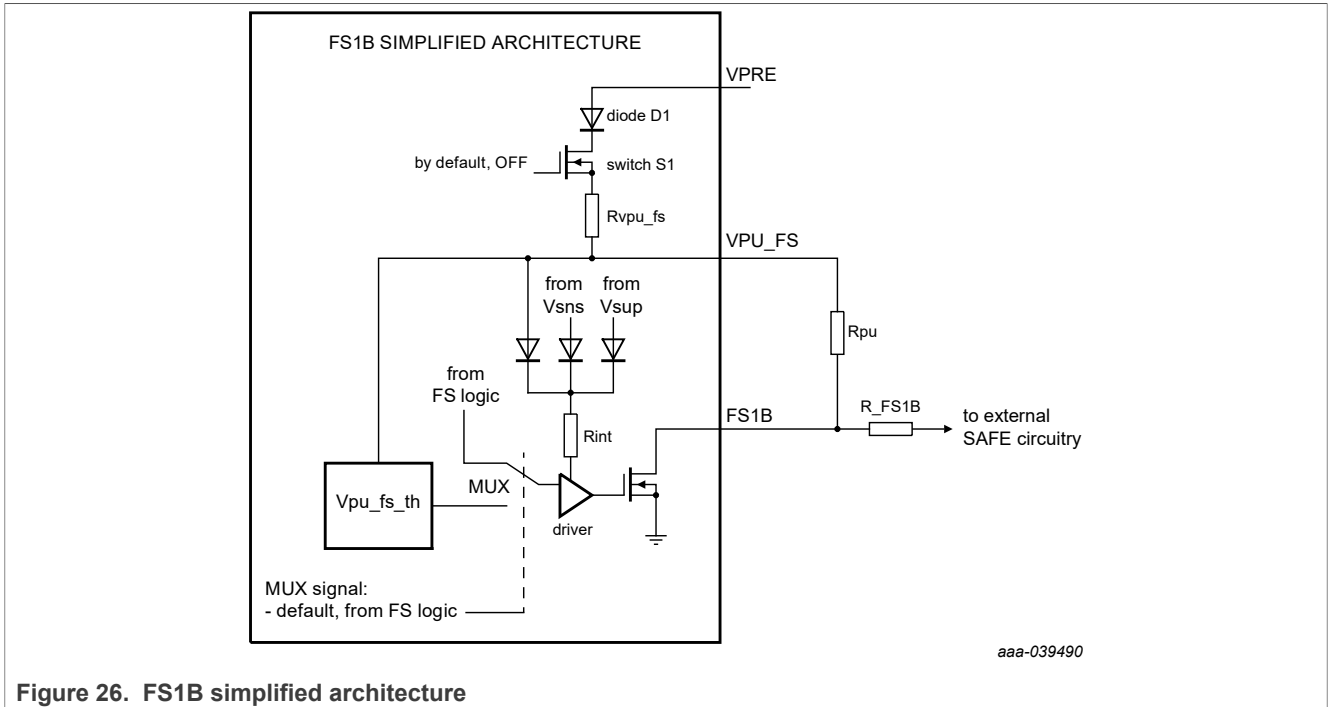


Figure 26. FS1B simplified architecture

VPU\_FS is internally connected to VPRES with a reverse diode protection and protected against short-circuit by  $R_{VPU\_FS}$ . The  $R_{FS1B}$  resistor is needed to be robust against ISO 7637<sup>(14)</sup> pulses.

12.5.6.1  $t_{DELAY}$  operation

In  $t_{DELAY}$  configuration, FS1B is asserted low with a delay after FS0B is activated, and remains asserted until it is released by the SPI.

The delay between FS0B and FS1B activation is configurable via the SPI from 0 ms to 3150 ms with the combination of FS1B\_TIME\_3:0 and FS1B\_TIME\_RANGE bits. This digital delay is generated by the fail-safe logic with an accuracy of  $\pm 10\%$ . FS1B can be activated at the same time as FS0B if  $t_{DELAY} = 0$  or after a programmable delay if  $t_{DELAY} > 0$  (Figure 27).

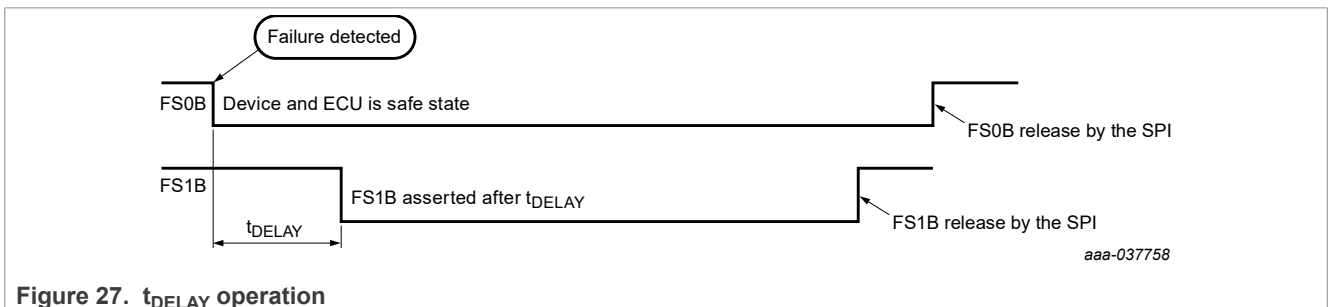


Figure 27.  $t_{DELAY}$  operation

To avoid common cause failures between the two safe outputs (FS0B and FS1B), the VPU\_FS pin must be used as a FS1B pull-up (Figure 26).

The switch S1 is opened by default and must be closed by a SPI command, due to the FS1B\_DLY\_REQ bit in the SF\_OUTPUT\_REQUEST register, before releasing the FS1B pin.

### 12.5.6.2 t<sub>DURATION</sub> operation

In t<sub>DURATION</sub> configuration, FS1B is asserted low at the same time as FS0B for a configurable duration, and is automatically released after t<sub>DURATION</sub> timing (Figure 28). The FS1B activation duration is configurable via the SPI from 0 ms to 3150 ms with the combination of the FS1B\_TIME\_3:0 and FS1B\_TIME\_RANGE bits. This digital duration is generated by the fail-safe logic with an accuracy of ±10 %.

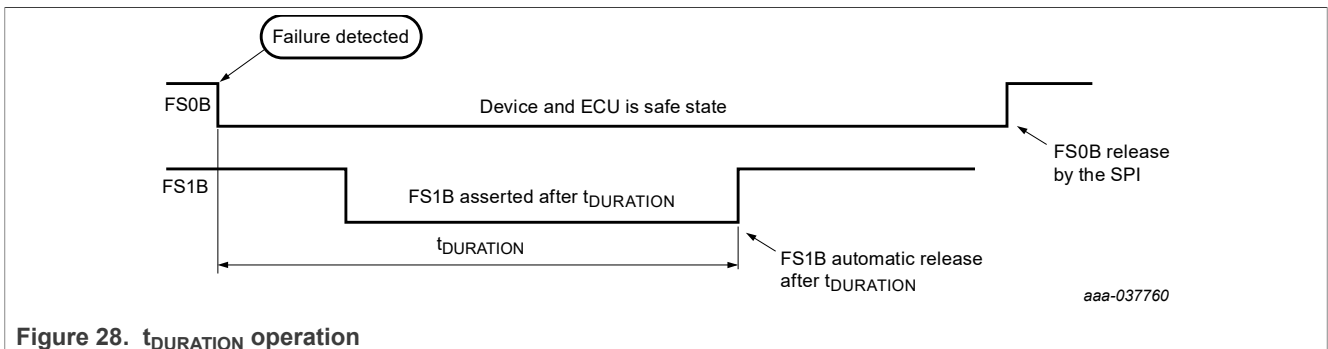


Figure 28. t<sub>DURATION</sub> operation

### 12.5.7 Fail-safe outputs (FS0B and FS1B) release

When the fail-safe outputs FS0B and consequently FS1B are asserted low by the device due to a fault, some conditions must be validated before allowing these pins to be released by the device. These conditions are:

- ABIST2\_FS1B\_OK=1 if part number with FS1B
- ABIST2\_VAUX\_OK=1 except if VAUX\_FS\_OV\_1:0=VAUX\_FS\_UV\_1:0="00"
- Fault is removed
- Fault error counter must be at '0'
- Close the S1 switch (FS1B\_DLY\_DRV bit = 1)
- RELEASE\_FSxB register must be filled with the right value

#### 12.5.7.1 RELEASE\_FSxB register

When a fault is removed and the fault error counter changes back to level '0', a right word must be filled in the RELEASE\_FSxB register. The value depends on the current LFSR. LSB, MSB must be swapped, and a negative operation per bit must be applied.

FS0B and FS1B can be released independently or at the same time, depending on the configuration of the first three bits of the RELEASE\_FSxB register (Table 12). The RELEASE\_FSxB write command should be done after an LFSR read command. If FS0B and FS1B are released sequentially, the procedure must be done a first time for FS0B, and a second time for FS1B.

**Note:** The LFSR register is used to secure the release of FSxB pins. It can be configured during the INIT phase but can also be written at any moment in Normal mode. It is impossible to write 0xFFFF and 0x0000 in LFSR register. A communication error is reported in case of 0x0000 and 0xFFFF write tentative and the configuration is ignored.

**Table 12. RELEASE\_FSxB register based on LFSR value**

	LFSR_7:0	b7	b6	b5	b4	b3	b2	b1	b0
Release FS0B	RELEASE_FSxB_7:0	0	1	1	$\overline{b0}$	$\overline{b1}$	$\overline{b2}$	$\overline{b3}$	$\overline{b4}$
Release FS1B	RELEASE_FSxB_7:0	1	1	0	$\overline{b3}$	$\overline{b4}$	$\overline{b5}$	$\overline{b6}$	$\overline{b7}$
Release FS0B and FS1B	RELEASE_FSxB_7:0	1	0	1	$\overline{b0}$	$\overline{b1}$	$\overline{b2}$	$\overline{b6}$	$\overline{b7}$

**12.5.8 SPI DED**

Some SPI registers affect some safety critical aspects of the fail-safe functions, and therefore are required to be protected against SEU (single event upset). Only fail-safe registers are concerned. During INIT\_FS mode, access to fail-safe registers for product configuration is open. Once the INIT\_FS phase is over, the Hamming circuitry is activated to protect registers content.

At this stage, if there is one single bit flip, the detection is made due to Hamming code, the error is corrected automatically (fully transparent for the user), and a flag is sent. If there are two errors (DED - dual error detection), the detection is made due to Hamming code but detected errors cannot be corrected. The flag is sent and FS0B is activated.

**12.6 Input voltage range**

Due to the flexibility of the pre-regulator, the device can cover a wide battery input voltage range. However, a more standard voltage range can still be covered using only the buck configuration.

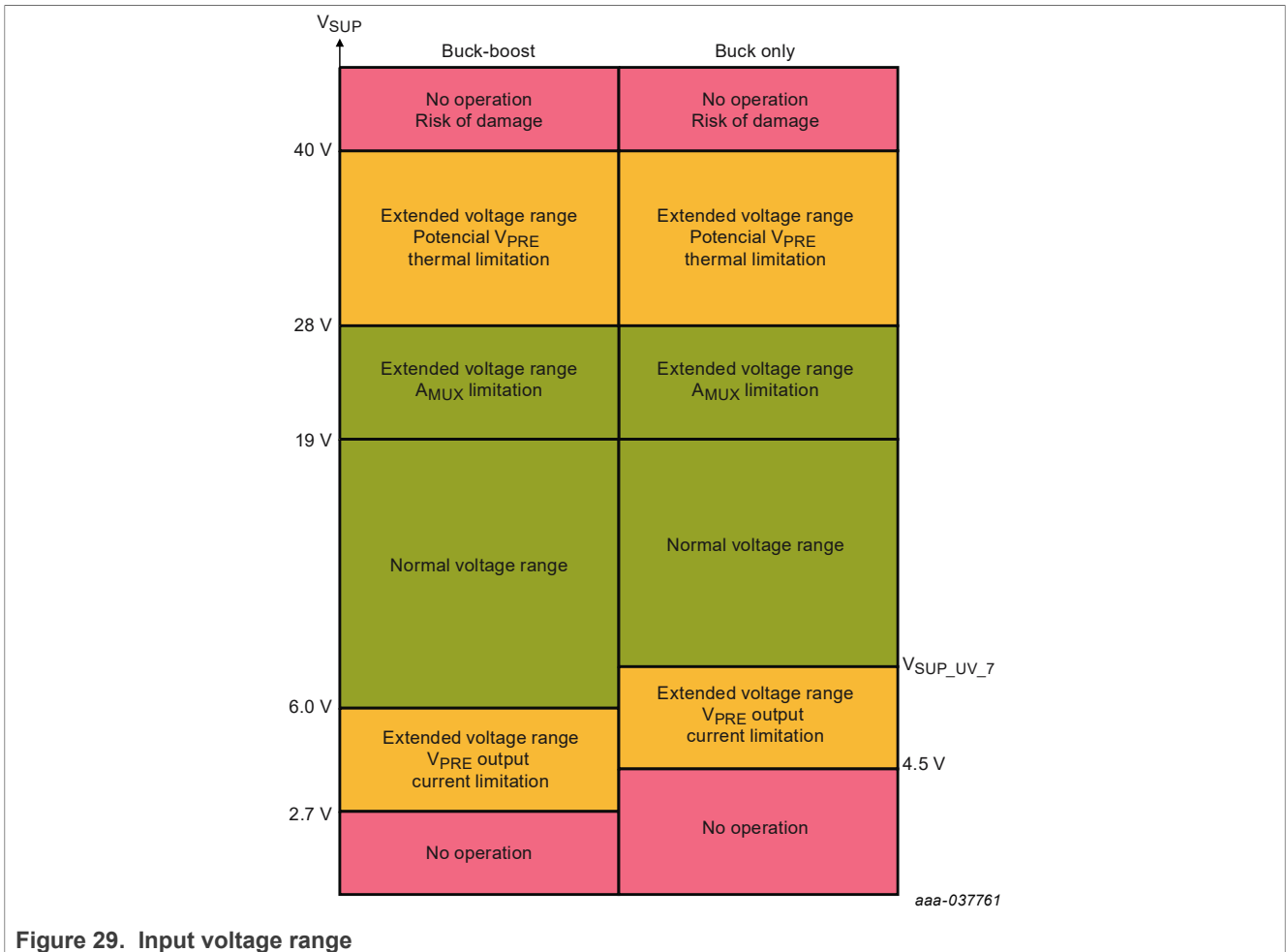


Figure 29. Input voltage range

- $V_{SUP} > 28\text{ V}$ : Potential  $V_{PRE}$  thermal limitation

$R_{DS(on)}$ , Current limitation and overcurrent detection are specified for  $V_{SUP} < 28\text{ V}$ .

- $V_{SUP} > 19\text{ V}$ : MUX\_OUT limitation

$V_{SENSE}$  and IO\_0 maximum analog input voltage range is 19 V. Internal 2.5 V reference voltage accuracy degraded.

- Buck only,  $V_{SUP} < V_{SUP\_UV\_7}$ :

CAN communication is guaranteed for  $V_{SUP} > 6.0\text{ V}$ . LIN communication stopped when  $V_{SUP} < 7.0\text{ V}$  if LIN\_J2602\_DIS bit is not set. For  $V_{CCA}$  and  $V_{AUX}$  5.0 V configuration, undervoltage triggers at low  $V_{SUP}$  (See Section 9,  $V_{CCA\_UV\_5}$  and  $V_{AUX\_UV\_5}$ ).

### 12.7 Power management operation

A thermal sensor is implemented as close as possible to the pass transistor of each regulator ( $V_{PRE}$ ,  $V_{CORE}$ ,  $V_{CCA}$ ,  $V_{CAN}$ ) and an associated individual thermal shutdown ( $T_{SD}$ ) protects these regulators independently. When the  $T_{SD}$  threshold of a specific regulator is reached, this regulator only is switched off and the information is reported in the main state machine. The regulator restarts automatically when the junction temperature of the pass transistor decrease below the  $T_{SD}$  threshold.

12.7.1 VPRE voltage pre-regulator

A highly flexible SMPS pre-regulator is implemented in the FS6500/FS4500. Depending on the input voltage requirement, the device can be configured as 'non-inverting buck-boost converter' (Figure 31) or 'standard buck converter' (Figure 30). An external logic level MOSFET (N-type) is required to operate in 'non-inverting buck-boost converter'. The connection of the external MOSFET is detected automatically during the start-up phase.

The converter operates in current control mode in any configuration. The high-side switching MOSFET is integrated to make the current control easier. The PWM frequency is fixed at a typical 440 kHz. The compensation network is fully integrated. The VPRE output voltage is regulated between 6.0 V and 7.0 V.

If the full current capability is not used for V CORE, VCCA, VAUX, and CAN\_5V, an additional external LDO can be connected to VPRE to fulfill application needs, while the current load remains below the maximum current capability in all conditions.

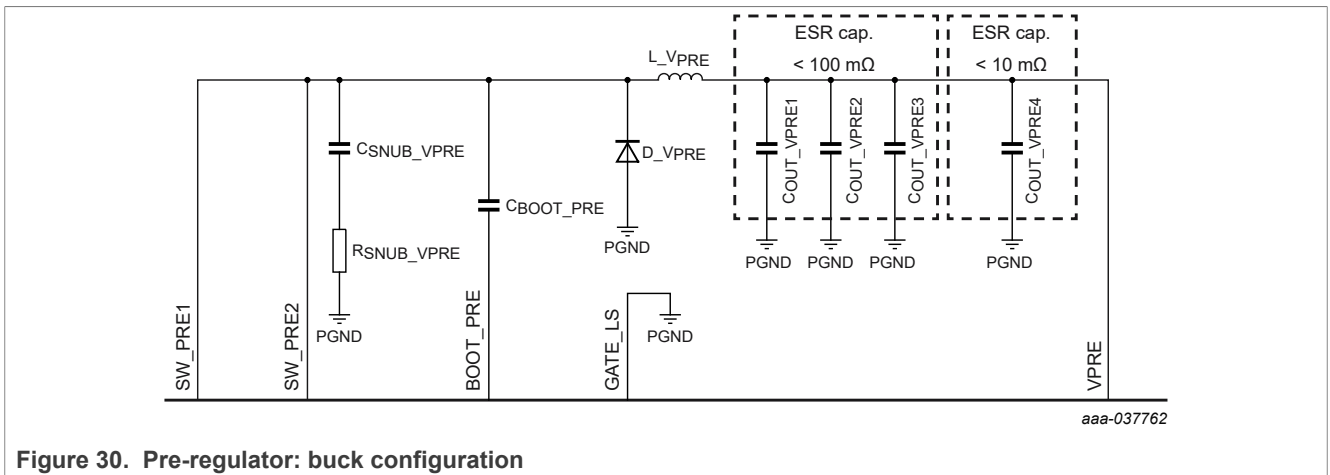


Figure 30. Pre-regulator: buck configuration

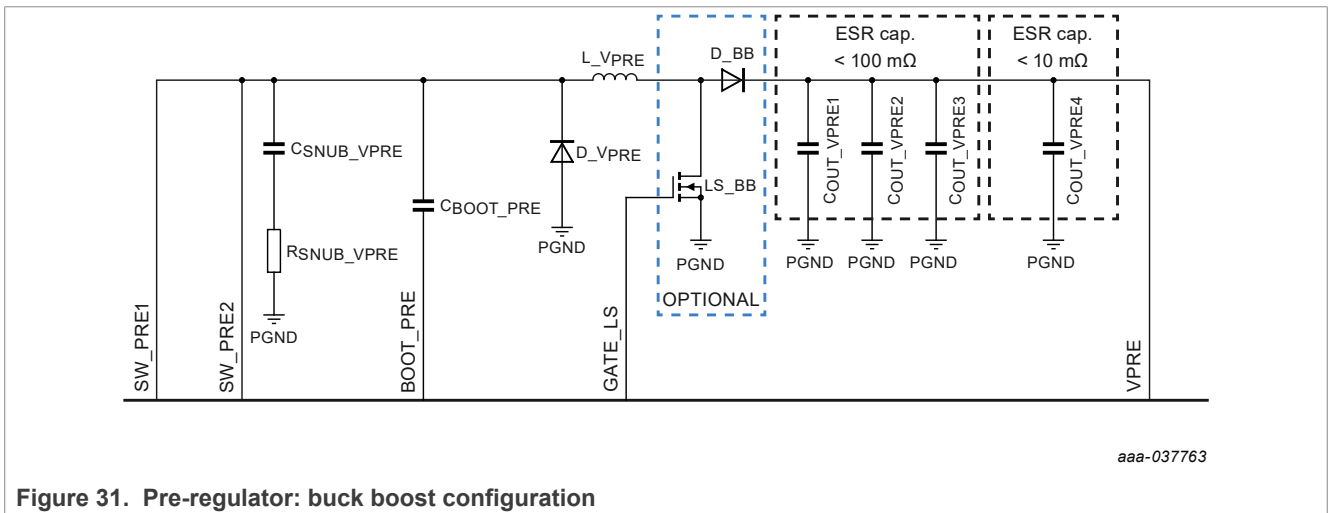
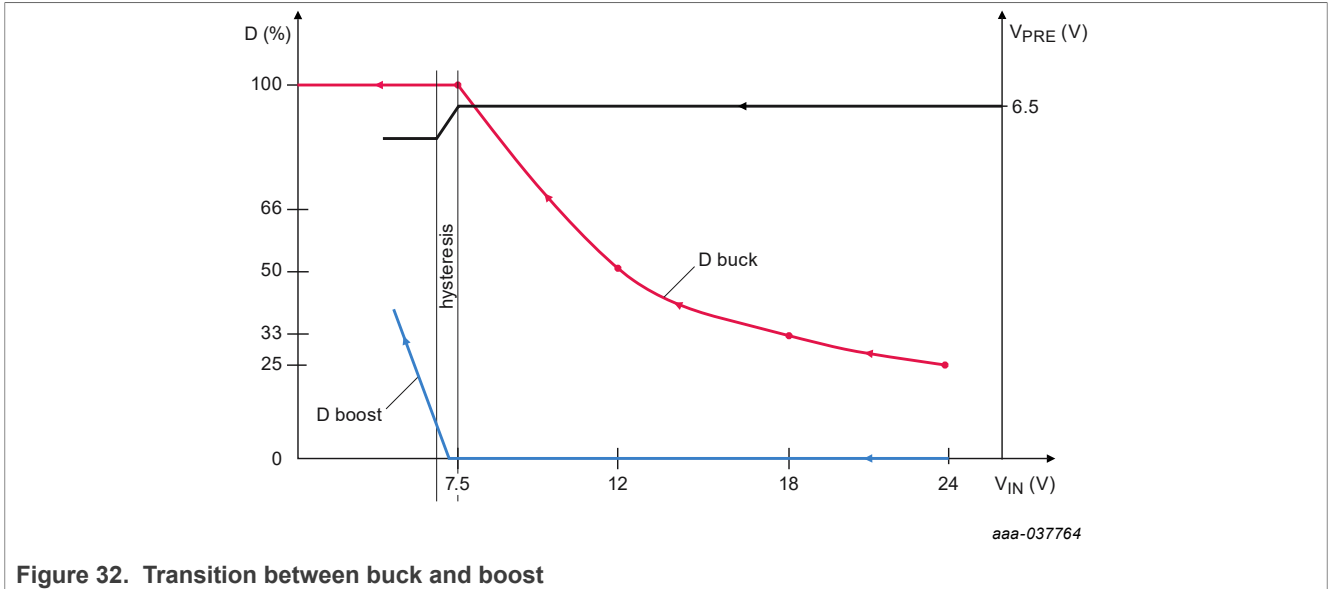


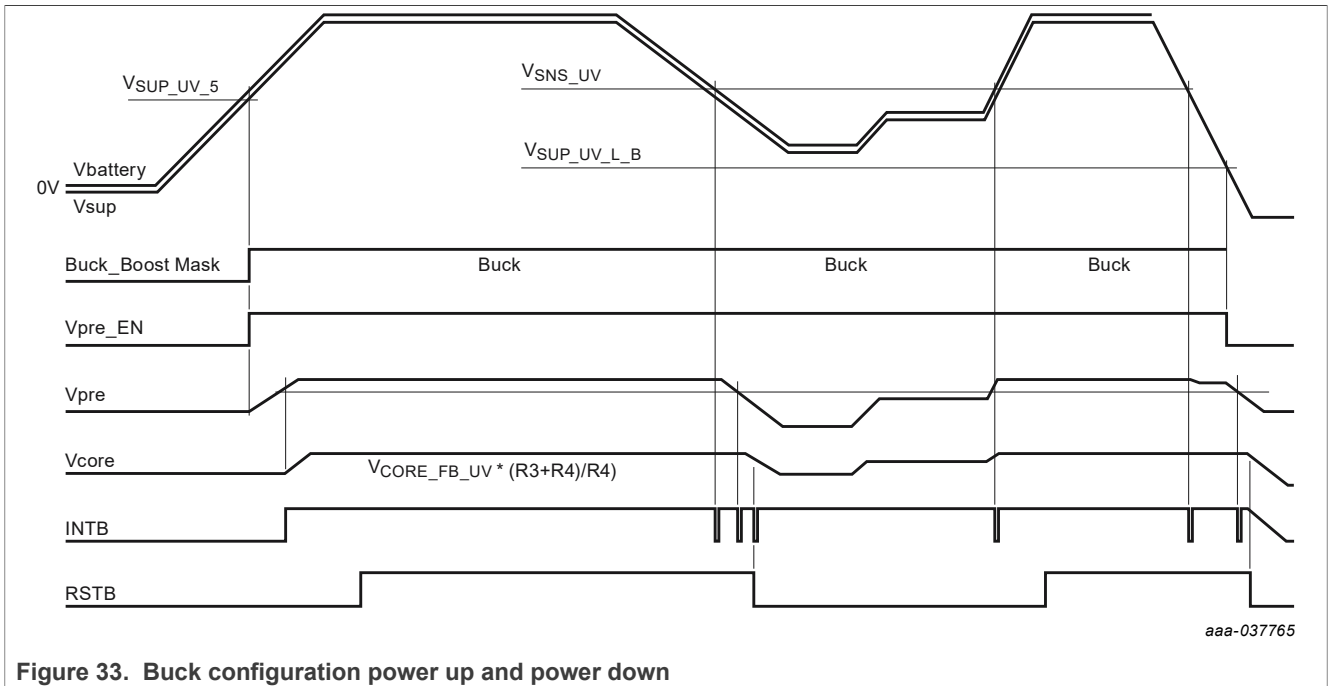
Figure 31. Pre-regulator: buck boost configuration

When the converter is set up to work in boost mode at low VSUP, the transition between buck and boost mode is automatically handled by the device at the VSUP\_UV\_7 threshold. Transition between buck mode and boost mode is based on hysteresis (Figure 32).

- When VSUP > VSUP\_UV\_7, the converter works in buck mode and the VPRE output is regulated at 6.5 V typ.
- When VSUP < VSUP\_UV\_7, the converter works in boost mode and the VPRE output is regulated at 6.3 V typ.



12.7.1.1 Power up and power down sequence





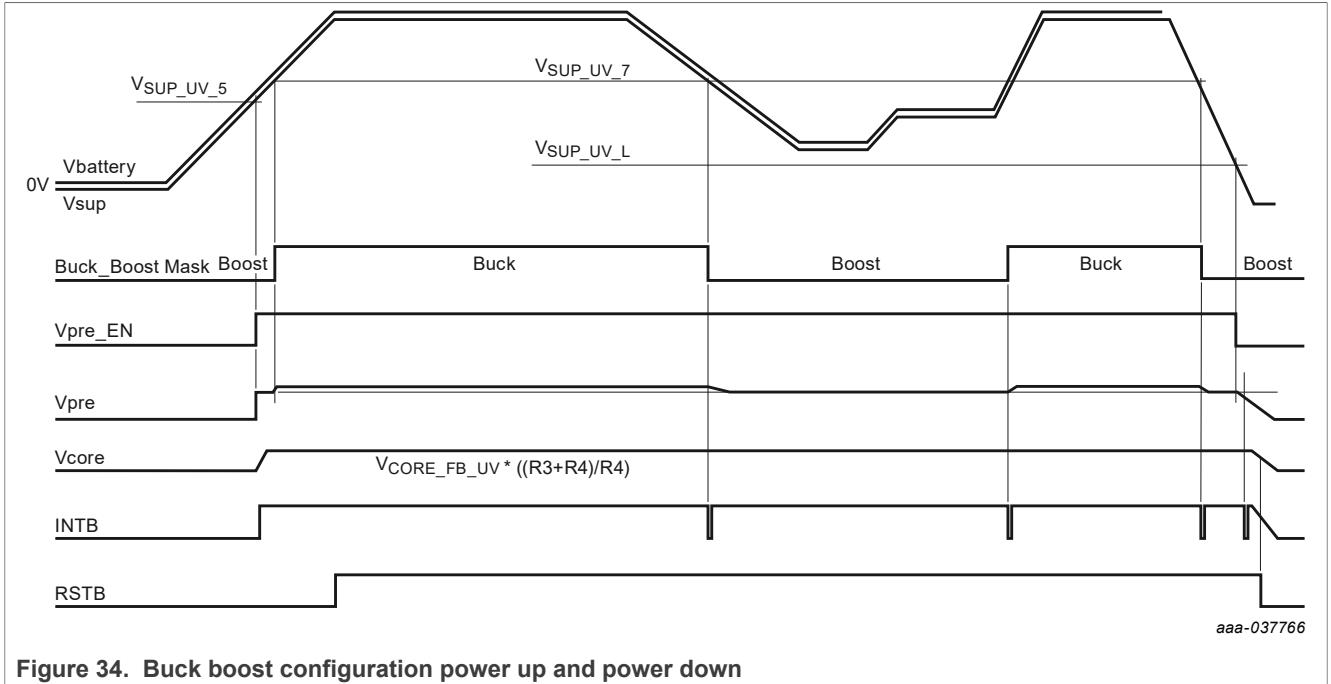


Figure 34. Buck boost configuration power up and power down

### 12.7.1.2 Cranking management

When VPRE is set up to work in buck only mode, the application can work down to  $V_{SUP} = V_{SUP\_UV\_L\_B} = 4.5\text{ V}$  with a minimum of 500 mA current guaranteed on VPRE.

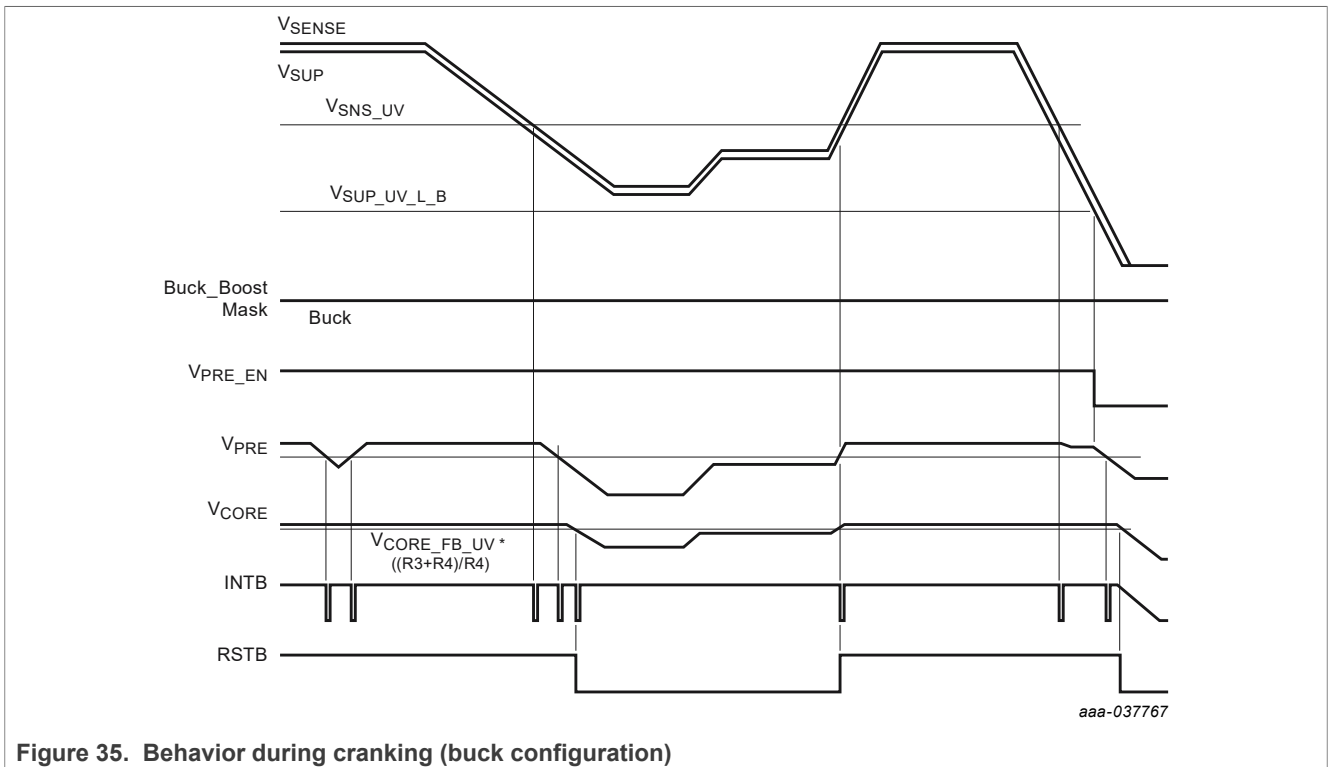
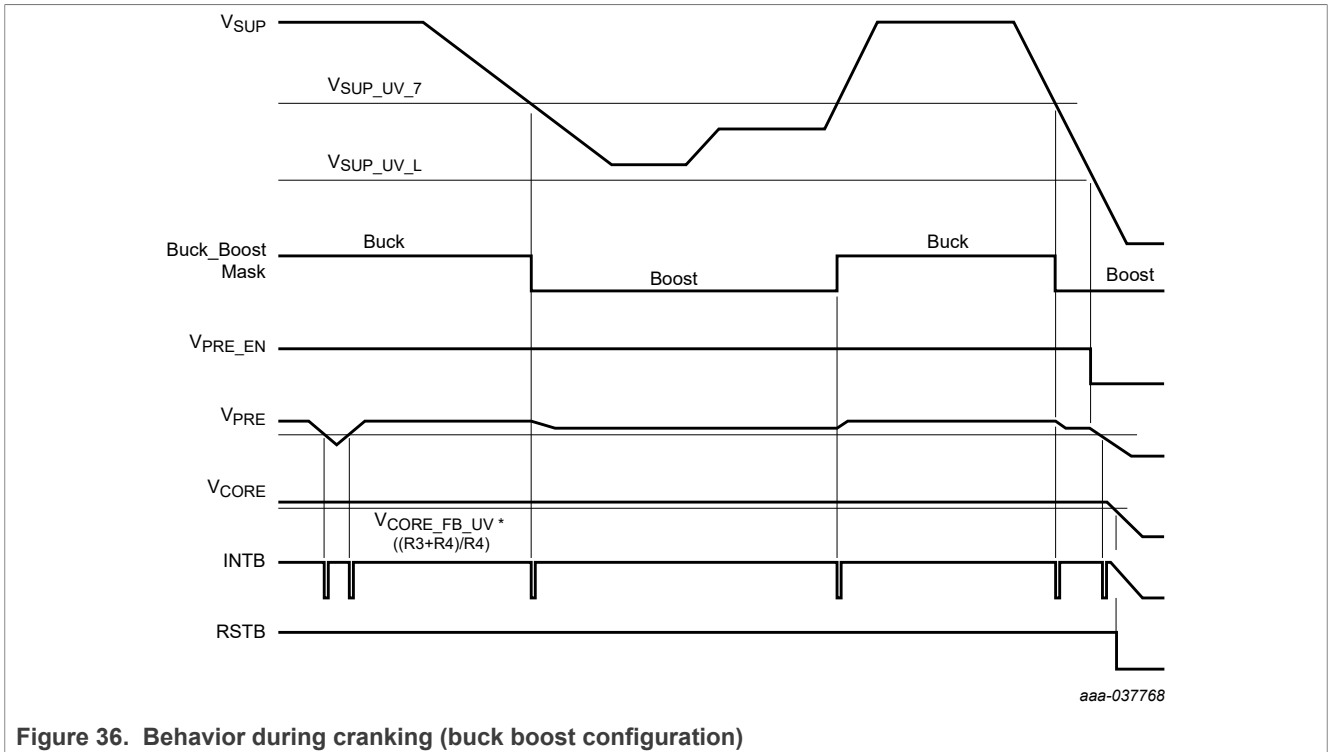


Figure 35. Behavior during cranking (buck configuration)

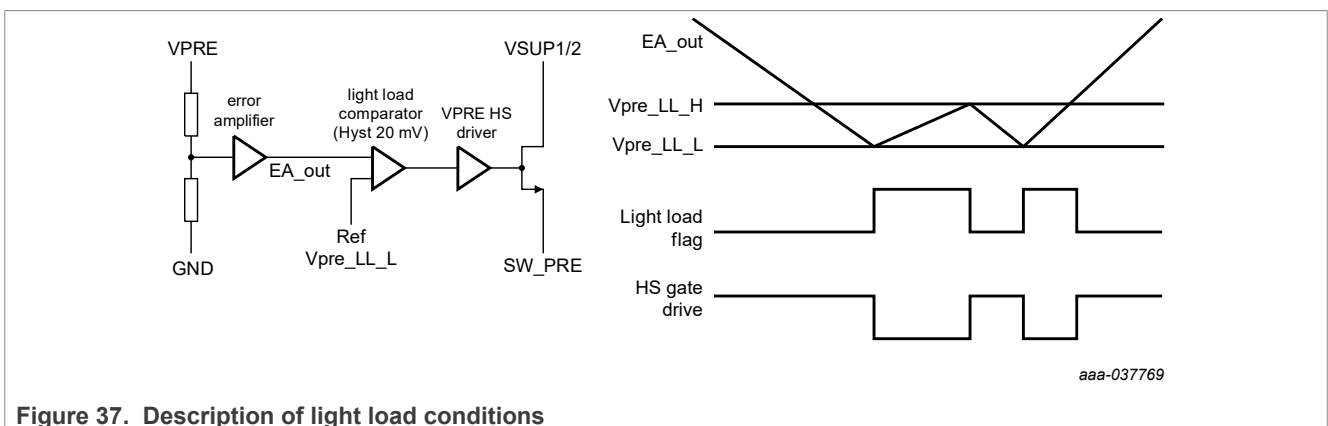
When VPRE is set up to work in buck-boost mode, the application can work down to VSUP = VSUP\_UV\_L = 2.7 V with a minimum of 300 mA current guaranteed on VPRE. The buck-boost configuration helps to pass the LV124 specification requiring a minimum of 3.2 V on VBAT supply during cold cranking conditions.



### 12.7.1.3 Light load condition

To improve the converter efficiency and avoid any unwanted output voltage increase, the VPRE voltage regulator operates in pulse skipping mode during light load conditions.

The transition between normal mode and pulse skipping mode is based on the comparison between the error amplifier output (EA\_out) and pre-defined thresholds VPRE\_LL\_H and VPRE\_LL\_L. When the error amplifier output reaches VPRE\_LL\_L, the VPRE high-side transistor is switched off. When the error amplifier output reaches VPRE\_LL\_H, the VPRE high-side transistor is switched on again for the next switching period (Figure 37).



12.7.1.4 Input power feed forward condition

To improve the converter efficiency during high input power conditions, the VPRE switching frequency is reduced from 440 kHz to 220 kHz, when  $V_{SUP} > V_{SUP\_IPFF}$ , to decrease the switching losses. The transition between the two frequencies is transparent for the application.

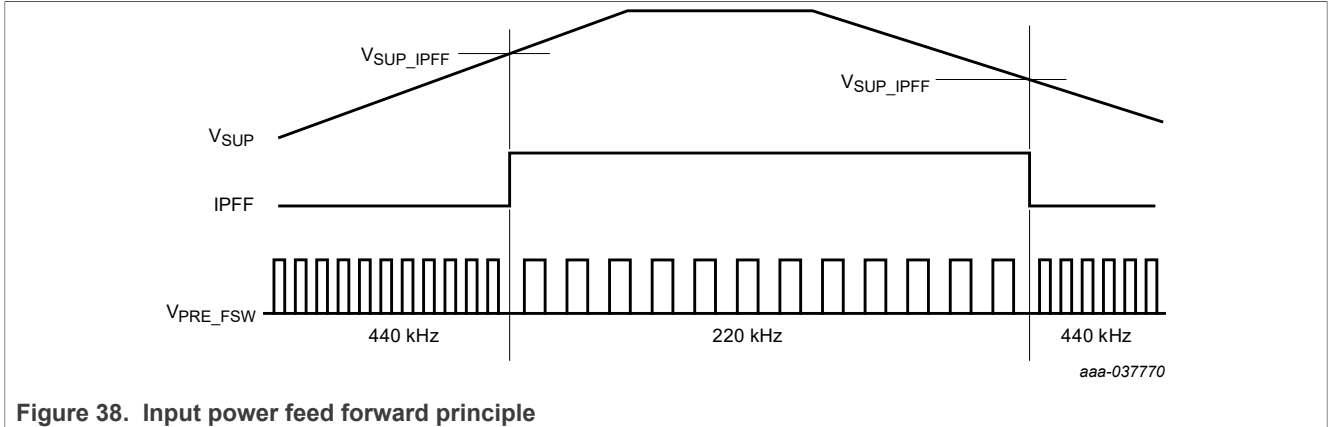


Figure 38. Input power feed forward principle

12.7.1.5 Overcurrent detection and current limitation

12.7.1.5.1 Overcurrent protection:

To ensure the integrity of the high-side MOSFET, an overcurrent detection is implemented. The regulator is switched off by the main state machine when the  $I_{PRE\_OC}$  overcurrent detection threshold is reached three consecutive times. The overcurrent detection is blanked when the pass transistor is switched on during  $t_{PRE\_OC}$  to avoid parasitic switch off of the high-side gate driver.

The VPRE output voltage decrease causes an undervoltage condition on one of the cascaded regulators (VCORE, VCCA, VAUX) and brings the device into fail-safe state. The overcurrent protects the regulator in case the SW\_PRE pin is shorted to GND. The overcurrent works in buck mode only.

12.7.1.5.2 Current limitation:

A current limitation is also implemented to avoid uncontrolled power dissipation inside the device (duty cycle control) and limits the current. VPRE current limitation is automatically set based on the buck or buck-boost configuration. In buck only mode, the lowest current limitation  $I_{PRE\_LIM2}$  is applied while in buck-boost mode, the highest current limitation  $I_{PRE\_LIM1}$  is applied. The current limitation is blanked when the pass transistor is switched on during  $t_{PRE\_BLK\_LIM}$  to allow short-circuit detection on the SW\_PRE pin.

When  $I_{PRE\_LIM}$  threshold is reached during buck mode, the high-side integrated MOSFET is switched off. When the  $I_{PRE\_LIM}$  threshold is reached during boost mode, the external low-side MOSFET is switched off. In both cases, the MOSFET is not switched on again before the next rising edge of the switching clock.

The current limitation induces a duty cycle reduction and leads to the VPRE output voltage gradually dropping, which may cause an undervoltage condition on one of the cascaded regulators (VCORE, VCCA, VAUX) and bring the device to the fail-safe state. The current limitation does not switch off the regulator. The current limitation protects the regulator when the VPRE pin is shorted to GND.

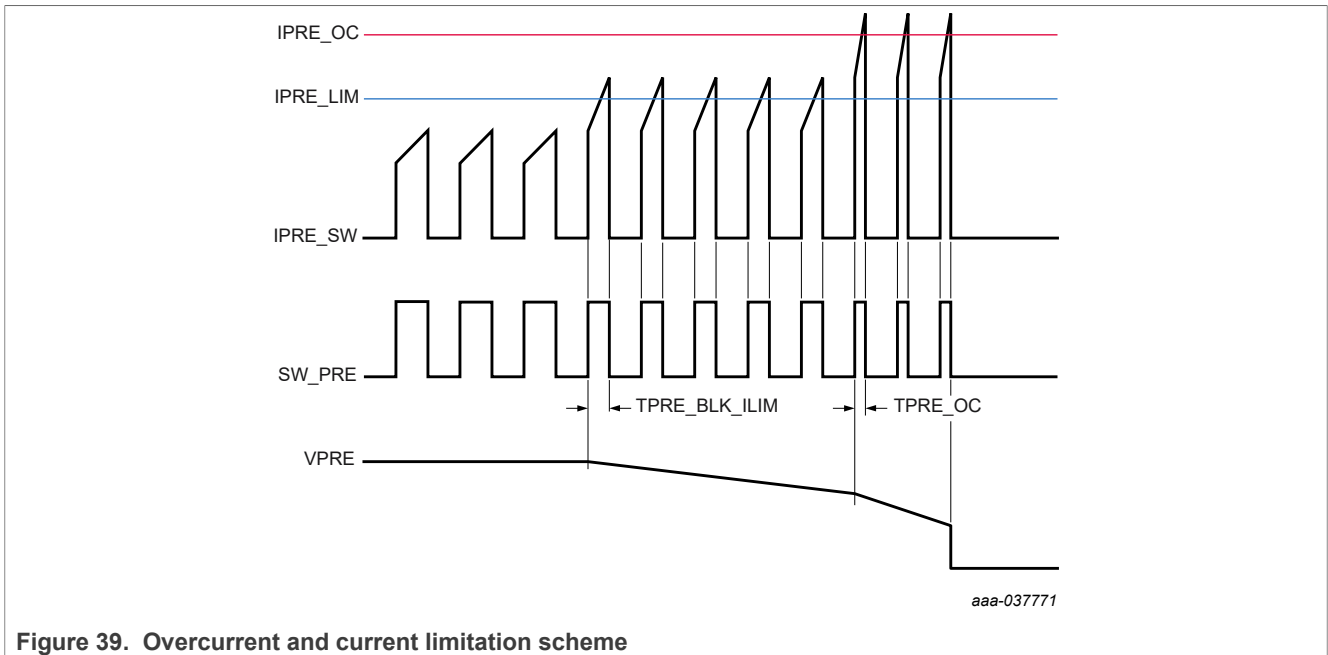


Figure 39. Overcurrent and current limitation scheme

### 12.7.1.6 VPRE voltage monitoring

The overvoltage detection switches off the regulator. The undervoltage detector is disabled when the regulator is switched off, reporting an undervoltage. Diagnostic is reported in the dedicated register and generates an Interrupt. The undervoltage detection does not switch off the regulator. However,  $V_{PRE}$  decrease may induce an undervoltage on a regulator attached to  $V_{PRE}$  ( $V_{CORE}$ ,  $V_{CCA}$ ,  $V_{AUX}$ , or  $CAN\_5V$ ), and bring the application in fail-safe state depending on the supervisor configuration (registers `INIT_VCORE_OVUV_IMPACT`, `INIT_VCCA_OVUV_IMPACT`, `INIT_VAUX_OVUV_IMPACT`).

### 12.7.1.7 VPRE efficiency

$V_{PRE}$  efficiency versus current load is given for information based on typical external component criteria described in [Figure 40](#), close to the graph and at typical automotive  $V_{SUP}$  voltage (14 V). The efficiency is valid in buck mode only and above a 200 mA load on  $V_{PRE}$ , to be in continuous mode on the 22  $\mu$ H inductor. The efficiency is calculated and has to be verified by measurement at the application level.

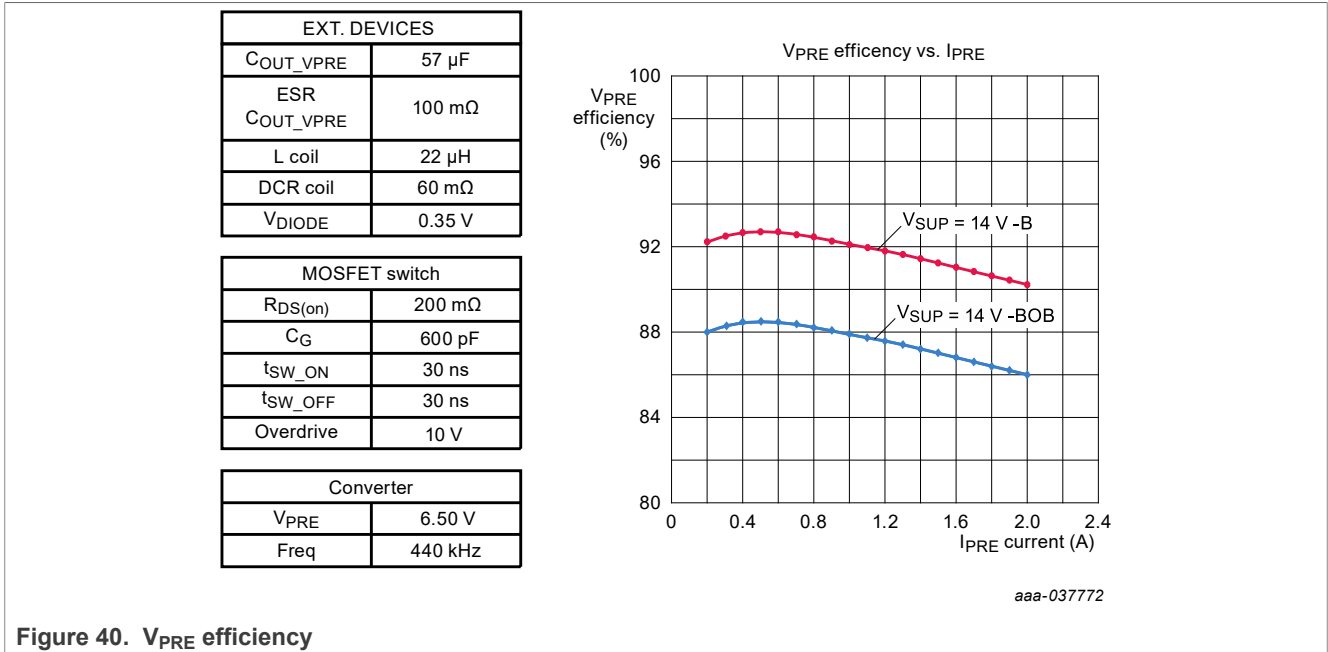


Figure 40. V<sub>PRE</sub> efficiency

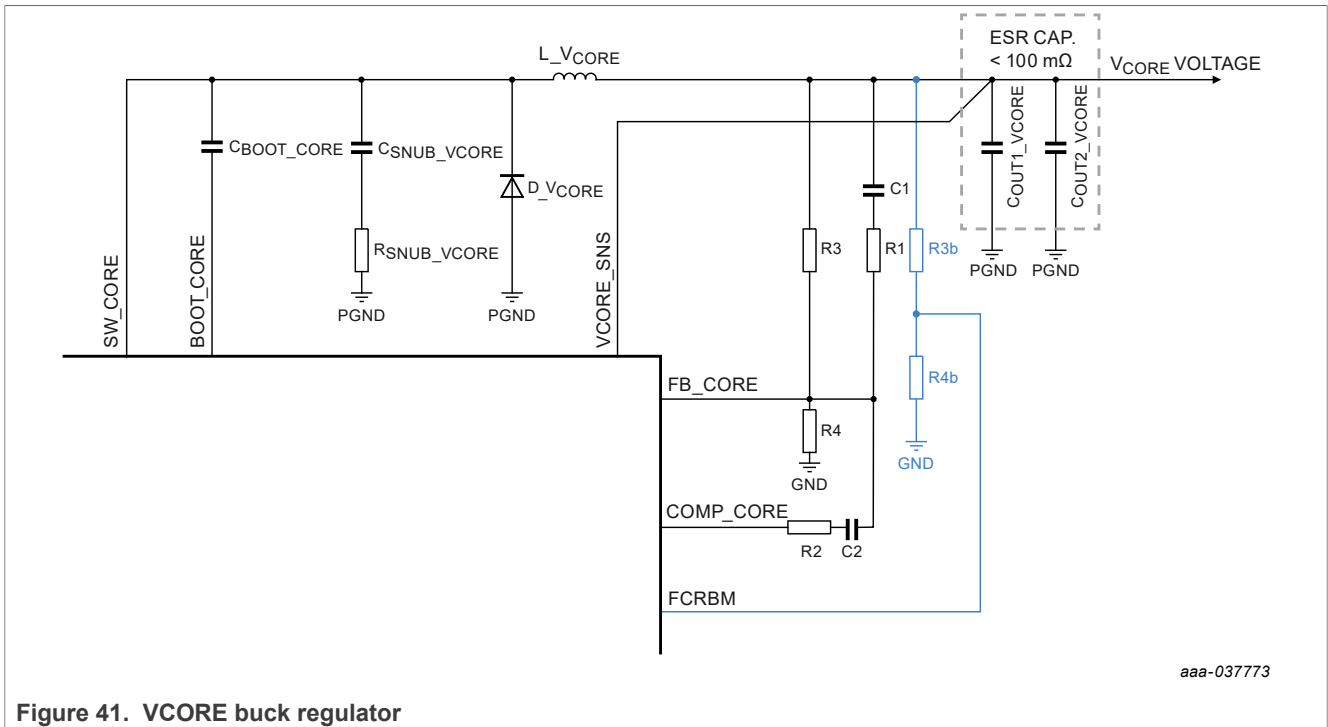
### 12.7.2 V<sub>CORE</sub> voltage regulator

This voltage regulator is a step-down DC–DC converter in the FS6500 series and a linear regulator in the FS4500 series.

#### 12.7.2.1 V<sub>CORE</sub> DC–DC converter

The FS6500 voltage regulator is a step-down DC–DC converter operating in voltage control mode. The high-side switching MOSFET, connected to V<sub>PRE</sub>, is integrated in the device, and the PWM frequency is fixed at 2.4 MHz typical. The output voltage is configurable from a 1.0 V to 5.0 V range, and adjustable around these voltages with an external resistor divider (R<sub>3</sub>/R<sub>4</sub>) connected between V<sub>CORE</sub> and the feedback pin (FB<sub>CORE</sub>) (Figure 41).  $V_{CORE} = V_{CORE\_FB} \times ((R_3 + R_4)/R_4)$ .

The voltage accuracy is ±2.0 % (without the external resistor bridge R<sub>3</sub>/R<sub>4</sub> accuracy) and the max output current is 2.2 A. The stability of the overall converter is done by an external compensation network (R<sub>1</sub>/C<sub>1</sub>/R<sub>2</sub>/C<sub>2</sub>) connected to the pin COMP<sub>CORE</sub>. It is recommended to use 1.0 % accuracy resistors and set R<sub>4</sub> = 8.06 kΩ and adjust R<sub>3</sub> to obtain the final V<sub>CORE</sub> voltage needed for the MCU core supply.



aaa-037773

Figure 41. Vcore buck regulator

### 12.7.2.2 Light load condition

To improve the converter efficiency and avoid any unwanted output voltage increase, the Vcore voltage regulator operates in pulse skipping mode during light load conditions. The principle is the same as the VPRE implementation described in detail in [Section 12.7.1.3](#).

### 12.7.2.3 Current limitation

A current limitation is implemented to avoid uncontrolled power dissipation inside the device (duty cycle control) and limits the current below  $I_{CORE\_LIM}$ . The current limitation is banked when the pass transistor is switched on during  $t_{CORE\_BLK\_LIM}$  to avoid parasite detection. When the  $I_{CORE\_LIM}$  threshold is reached, the high-side integrated MOSFET is switched off. The MOSFET is not switched on again before the next rising edge of the switching clock.

The current limitation induces a duty cycle reduction and leads to the Vcore output voltage to fall gradually and may cause an undervoltage condition, bringing the device into a fail-safe state. The current limitation does not switch off the regulator.

### 12.7.2.4 Voltage monitoring

The overvoltage detection switches off the regulator. The regulator remains on during an undervoltage detection. Diagnostic is reported in the dedicated register, generates an interrupt, and may bring the application into the fail-safe state, depending on the supervisor configuration (register INIT\_VCORE\_OVUV\_IMPACT).

For safety purposes, the FCRBM pin monitors the external resistor bridge (R3/R4) used to set up the final Vcore voltage through a second resistor bridge (R3b/R4b) to detect an external resistor drift or disconnection. The monitoring compares the FB\_CORE and FCRBM pins ([Figure 42](#)) and triggers when  $FB\_CORE - FCRBM > \pm 150\text{ mV max}$ .

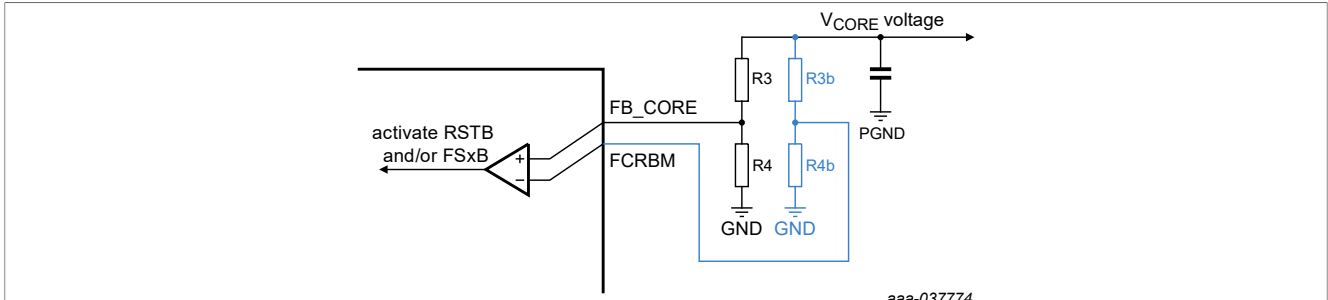


Figure 42. Feedback core resistor bridge monitoring (FCRBM)

If the second resistor bridge (R3b/R4b) is not mounted, FCRBM must be connected directly to FB\_CORE to satisfy  $V_{FB\_CORE} = V_{FCRBM}$  in all conditions.

12.7.2.5 V<sub>CORE</sub> efficiency

V<sub>CORE</sub> efficiency versus current load is given for information based on typical external component criteria described in Figure 43, close to the graph and at three typical V<sub>CORE</sub> voltages (5.0 V, 3.3 V, and 1.2 V), covering most of the MCU supply ranges. The efficiency is valid above a 200 mA load on V<sub>CORE</sub> to be in continuous mode in the 2.2 μH inductor. The efficiency is calculated and has to be verified by measurement at the application level. One major contributor degrading the efficiency at V<sub>CORE</sub> = 1.2 V is the external diode during the recirculation phase. The lower the diode forward voltage (V<sub>F</sub>) is, the better the efficiency.

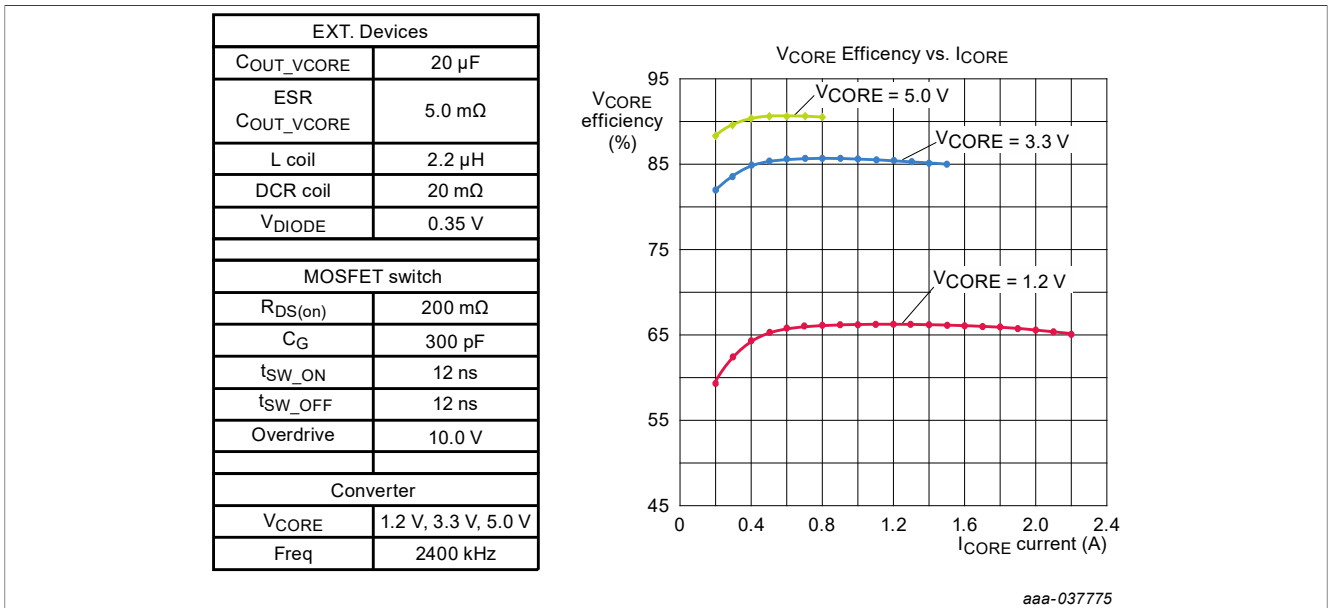


Figure 43. V<sub>CORE</sub> efficiency

12.7.2.6 V<sub>CORE</sub> linear regulator

The FS4500 voltage regulator is a linear regulator. The pass device, connected to V<sub>PRE</sub>, is integrated. The output voltage range is configurable from 1.0 V to 5.0 V, and adjustable around these voltages with an external resistor divider (R3/R4) connected between V<sub>CORE</sub> and the feedback pin (FB\_CORE) (see Figure 44).  $V_{CORE} = V_{CORE\_FB} \times ((R3 + R4)/R4)$ .

The voltage accuracy is ±2.0 % (without the external resistor bridge R3/R4 accuracy) and the max. output current is 0.5 A. In this case, the BOOT\_CORE and COMP\_CORE pins (used in buck converter mode only)

must be left open. It is recommended to use 1.0 % accuracy resistors and set  $R4 = 8.06 \text{ k}\Omega$  and adjust  $R3$  to obtain the final  $V_{\text{CORE}}$  voltage needed for the MCU core supply. When  $V_{\text{CORE}}$  is used in linear mode, the power dissipation must be taken into account at low-voltage.

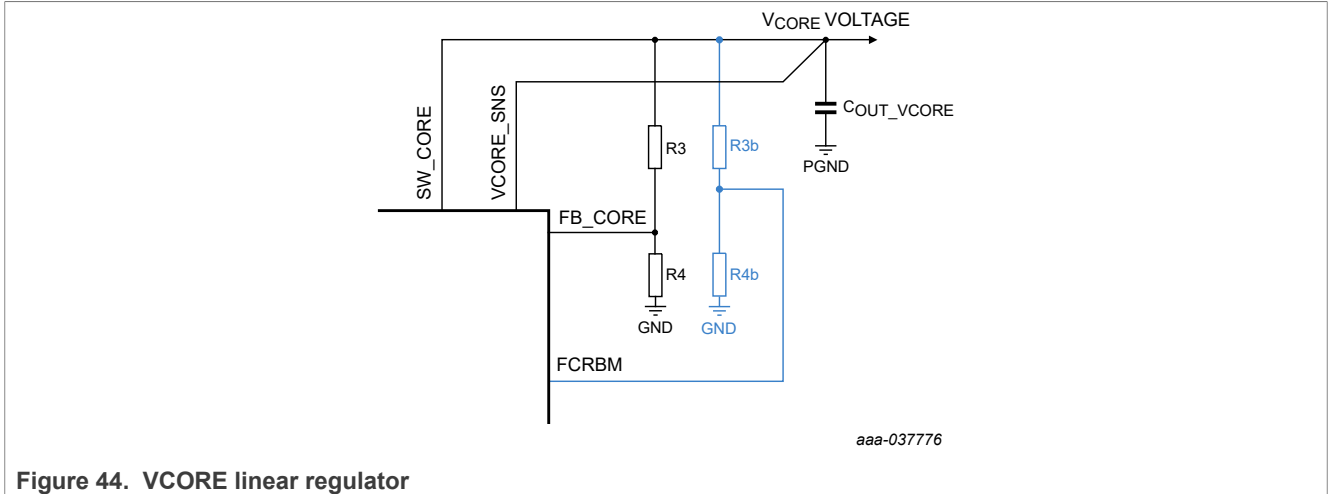


Figure 44. V<sub>CORE</sub> linear regulator

12.7.2.7 Current limitation

Similar to the buck converter mode, a current limitation is implemented to avoid uncontrolled power dissipation inside the device (see Section 12.7.2.3).

12.7.2.8 Voltage monitoring

The linear regulator has the same voltage monitoring than the DC–DC buck converter (see Section 12.7.2.4).

12.7.3 Charge pump and bootstrap

Both switching MOSFETs of VPRE and V<sub>CORE</sub> SMPS are driven by external bootstrap capacitors. Additionally, a charge pump is implemented to ensure 100 % duty cycle for both converters. Each converter uses a 100 nF external capacitor minimum to operate properly.

12.7.4 VCCA voltage regulator

VCCA is a linear voltage regulator mainly dedicated to supply the MCU I/Os, especially the ADC. The output voltage is selectable at 5.0 V, or 3.3 V. Since this output voltage can be used to supply MCU I/Os, the output voltage selection is done using an external resistor connected to the SELECT pin and ground or VPRE. When VCCA is used with the internal MOS transistor, the VCCA\_E pin must be connected to VPRE. The voltage accuracy is ±1.0 % for 5.0 V and 3.3 V configuration with an output current capability at 100 mA.

When VCCA is used with an external PNP transistor to boost the current capability up to 300 mA, the connection is detected automatically during the start-up sequence of the FS6500/FS4500. In such condition, the internal pass transistor is switched off and all the current is driven through the external PNP to reduce the internal power dissipation. The output voltage accuracy with an external PNP is reduced to ±3.0 % at 300 mA current load. The VCCA output voltage is used as a reference for the auxiliary voltage supply (V<sub>AUX</sub>) when VAUX is configured as a tracking regulator.



### 12.7.4.1 Current limitation

A current limitation is implemented to avoid uncontrolled power dissipation of the internal MOSFET or external PNP transistor. By default, the current limitation threshold is selected based on the auto detection of the external PNP during start-up phase.

- When the internal MOSFET transistor is used, the current is limited to  $I_{CCA\_LIM\_INT}$  and the regulator is kept on
- When the external PNP transistor is used, the current is limited to  $I_{CCA\_LIM\_OUT}$  and the regulator is switched off after a dedicated duration  $t_{CCA\_LIM\_OFF}$  under current limitation. A SPI command is needed to restart the regulator.

In case of an external PNP configuration only, the lowest current limitation threshold can be selected by the SPI in the register `INIT_VREG` instead of the highest one. A current limitation foldback scheme is implemented to reduce the current limitation to  $I_{CCA\_LIM\_FB}$  when  $V_{CCA}$  is below  $V_{CCA\_LIM\_FB}$ , limiting the power dissipation in the external PNP transistor during a short-circuit to GND of the  $V_{CCA}$  pin.

### 12.7.4.2 Voltage monitoring

The overvoltage detection switches off the regulator. The regulator remains on if an undervoltage is detected. A diagnostic is reported in the dedicated register, generating an Interrupt and may bring the application into fail-safe state, depending on the supervisor configuration (register `INIT_VCCA_OVUV_IMPACT`).

### 12.7.5 VAUX voltage regulator

VAUX is a highly flexible linear voltage regulator, which can be used either as an auxiliary supply dedicated to additional device in the ECU or as a sensor supply (i.e. outside the ECU). An external PNP transistor must be used (no internal current capability).

If VAUX is not used in the application, the VAUX, VAUX\_E, and VAUX\_B pins must be left open. It is recommended to turn the  $V_{AUX}$  driver off and disable the  $V_{AUX}$  safety impact by the SPI (`VAUX_EN=0` in `REG_MODE` register and all bits of `INIT_VAUX_OVUV_IMPACT` register at 0).

If VAUX is used as an auxiliary supply, the output voltage is selectable between 5.0 V and 3.3 V. Since this voltage rail can be used to supply MCU IOs, the selection is done with an external resistor connected between the SELECT pin and ground or VPRE. In such case, the voltage accuracy is  $\pm 3.0\%$ , with a maximum output current capability of 400 mA.

If VAUX is used as a sensor supply rail, the output voltage is selectable between 5.0 V and 3.3 V.  $V_{CCA}$  can be used as reference for the sensor supply used as tracker. In this case, the  $V_{AUX}$  voltage must match  $V_{CCA}$ , limiting the resistor configuration at the SELECT pin to 5.1 k $\Omega$  ( $V_{AUX} = V_{CCA} = 3.3$  V) and 12 k $\Omega$  ( $V_{AUX} = V_{CCA} = 5.0$  V). The tracker mode selection is done during the INIT phase and secured (bit `VAUX_TRK_EN` in the `INIT_VREG` register). The tracking accuracy is  $\pm 15$  mV.

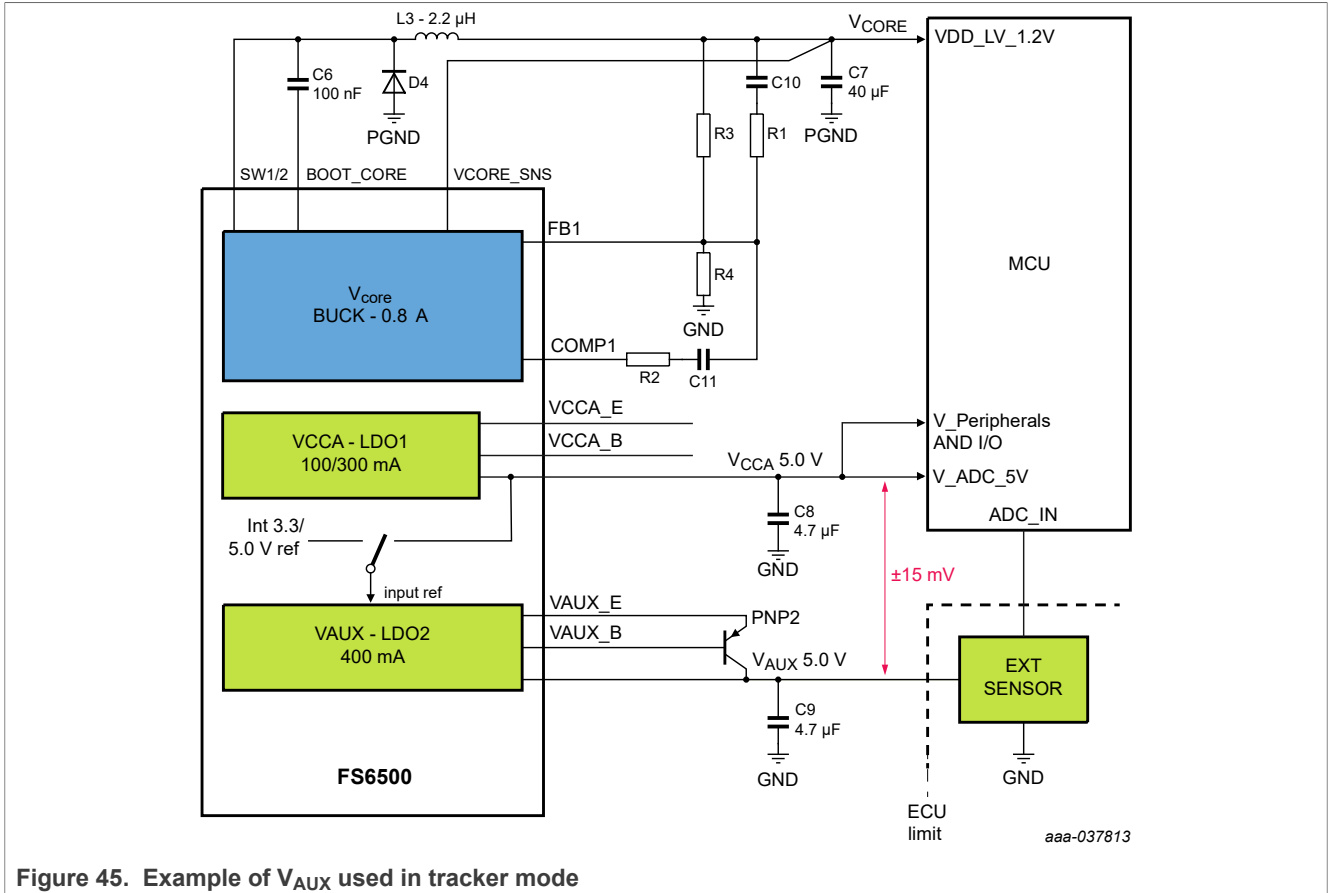


Figure 45. Example of  $V_{AUX}$  used in tracker mode

### 12.7.5.1 Current limitation

A current limitation is implemented to avoid uncontrolled power dissipation of the external PNP transistor. The current is limited to  $I_{AUX\_LIM}$  and the regulator is switch off after a dedicated duration  $t_{AUX\_LIM\_OFF}$  under current limitation. A SPI command is needed to restart the regulator. A current limitation foldback scheme is implemented to reduce the current limitation to  $I_{AUX\_LIM\_FB}$  when  $V_{AUX}$  is below  $V_{AUX\_LIM\_FB}$ , limiting the power dissipation in the external PNP transistor during a short-circuit to GND of the VAUX pin.

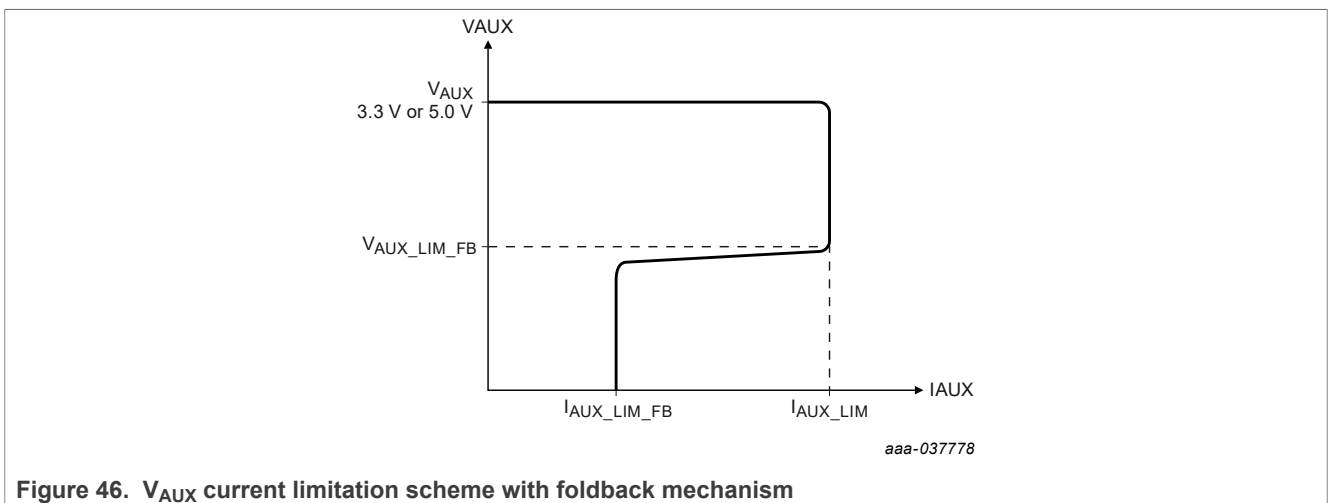


Figure 46.  $V_{AUX}$  current limitation scheme with foldback mechanism

**12.7.5.2 Voltage monitoring**

The overvoltage detection switches off the regulator. The regulator remains on if an undervoltage is detected. A diagnostic is reported in the dedicated register, generating an interrupt and may bring the application into the fail-safe state, depending on the supervisor configuration (register INIT\_VAUX\_OVUV\_Impact).

**12.7.6 CAN\_5V voltage regulator**

The CAN\_5V voltage regulator is a linear regulator fully dedicated to the internal CAN interface. By default, the CAN\_5V regulator and the undervoltage detector are enabled and the overvoltage detector is disabled. The overvoltage detector can be enabled by the SPI during INIT\_MAIN state.

If the overvoltage detector is enabled, the CAN\_5V regulator switches off when an overvoltage is detected. The undervoltage detector is disabled when the regulator is switched off reporting an undervoltage. A diagnostic is reported in the dedicated register, generating an Interrupt. The CAN\_5V regulator is not a safety regulator. Consequently, the CAN\_5V voltage monitoring (overvoltage, undervoltage) never asserts the RSTB or FS0B fail-safe pins.

If the FS6500/FS4500 internal CAN FD transceiver is not used in the application, the CAN\_5V regulator can be used to supply an external standalone CAN or FLEX-RAY transceiver, provided the current load remains below the maximum current capability in all conditions. In this case, the internal CAN FD transceiver must be put into sleep mode without wake-up capability.

**12.7.7 VKAM**

The keep alive memory supply is shared with IO\_5 pin. When VKAM is used, IO\_5 is not available and vice versa. Depending on the part number selection (Section 5.2), VKAM can be on or off by default.

- If VKAM is on by default, VKAM starts as soon as VSUP3 is > 4.5 V. VKAM can still be turned off/on by the SPI.
- If VKAM is off by default, VKAM is turned on/off by the SPI.

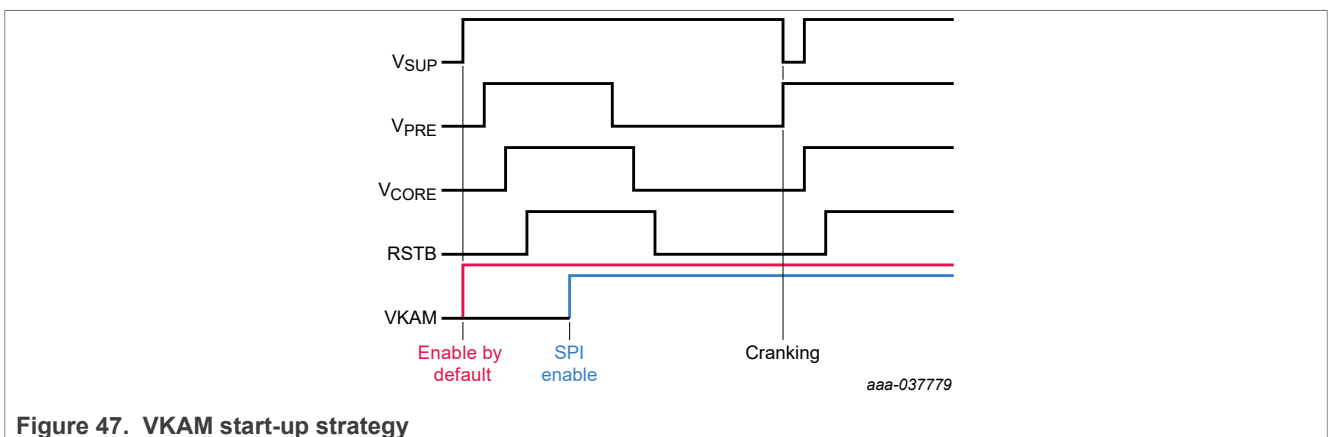


Figure 47. VKAM start-up strategy

VKAM is the only supply available in low-power mode (LPOFF). VKAM can be used to supply the MCU static RAM or any other external IC which does not exceed the current capability. A current limitation is implemented. Neither voltage monitoring, nor thermal shutdown are implemented. VKAM can be selected at the MUX\_OUT pin to be monitored by the MCU ADC. The VKAM supply is available down to  $V_{SUP} = V_{SUP\_UV\_L} = 2.7\text{ V}$  when the device is in normal mode, and down to  $V_{SUP} = 4.5\text{ V}$  when the device is in low-power mode off.

12.7.8 Power dissipation

The FS6500/FS4500 provides high performance SMPS and linear regulators to supply high end MCUs in automotive applications. Each regulator can deliver:

- $V_{PRE}$  (6.5 V) up to 2.0 A
- $V_{CORE}$  (from 1.0 V to 5.0 V range) up to 2.2 A
- $V_{CCA}$  (3.3 V or 5.0 V) up to 100 mA (with internal MOS) or up to 300 mA (with external PNP)
- $V_{AUX}$  (3.3 V or 5.0 V) up to 400 mA (with external PNP)
- $V_{CAN}$  (5.0 V) up to 100 mA

A thermal dissipation analysis has to be performed based on the application use case to ensure the maximum silicon junction temperature does not exceed 150 °C.

Two use cases covering the two main  $V_{CORE}$  voltage configurations are provided in [Figure 48](#).

- use case 1:  $V_{CORE} = 3.3\text{ V}$ ,  $I_{CORE} = 0.7\text{ A}$ ,  $V_{CCA}$  with int. MOS
- use case 2:  $V_{CORE} = 1.2\text{ V}$ ,  $I_{CORE} = 1.4\text{ A}$ ,  $V_{CCA}$  with ext. PNP

Both use cases have a total internal power dissipation below 0.9 W. A junction to ambient thermal resistivity of 30 °C/W allows the application to work up to an ambient temperature of 125 °C. A good soldering of the package expose pad is highly recommended to achieve such thermal performance.

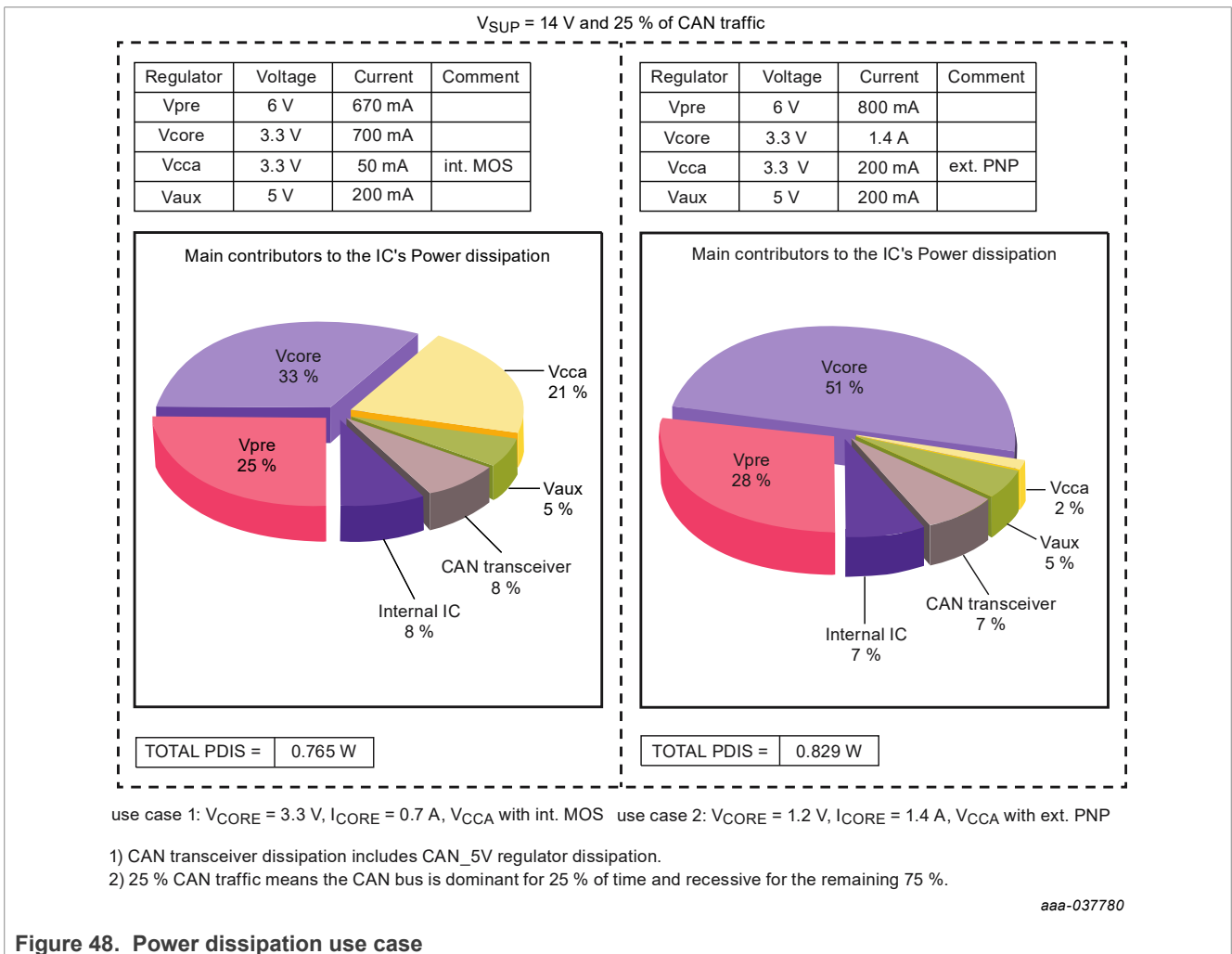
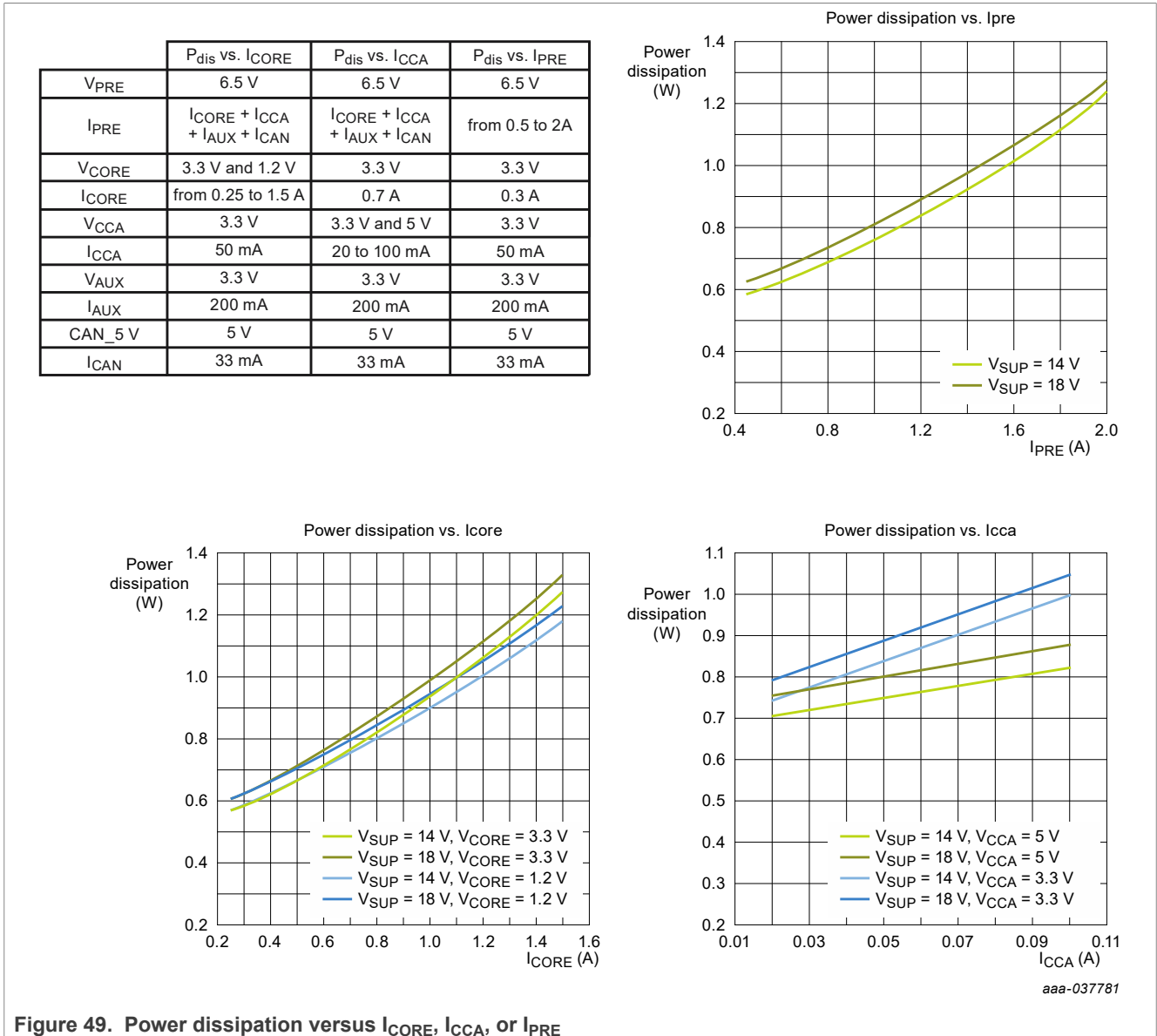


Figure 48. Power dissipation use case

The main contributors to the device power dissipation are the  $V_{PRE}$ ,  $V_{CORE}$ , and  $V_{CCA}$  (when used with an internal PMOS) regulators. In comparison, the power dissipation from the Internal IC, VAUX, and CAN transceiver are negligible.  $V_{PRE}$  power dissipation is mainly induced by the loading of the regulators it is supplying, mainly  $V_{CORE}$ ,  $V_{CCA}$ , and  $V_{AUX}$  which are application dependent. The total device power dissipation, depending on the variation of these three regulators, is detailed in Figure 49 with the environmental conditions in the associated table.



12.7.9 Start-up sequence

To provide a safe and well known start-up sequence, the FS6500/FS4500 includes an undervoltage lockout. This  $V_{SUP\_UV\_5}$  undervoltage lockout applies when the device is under a power-on reset condition or released from LPOFF. All the different voltage rails start automatically as described in Figure 50.

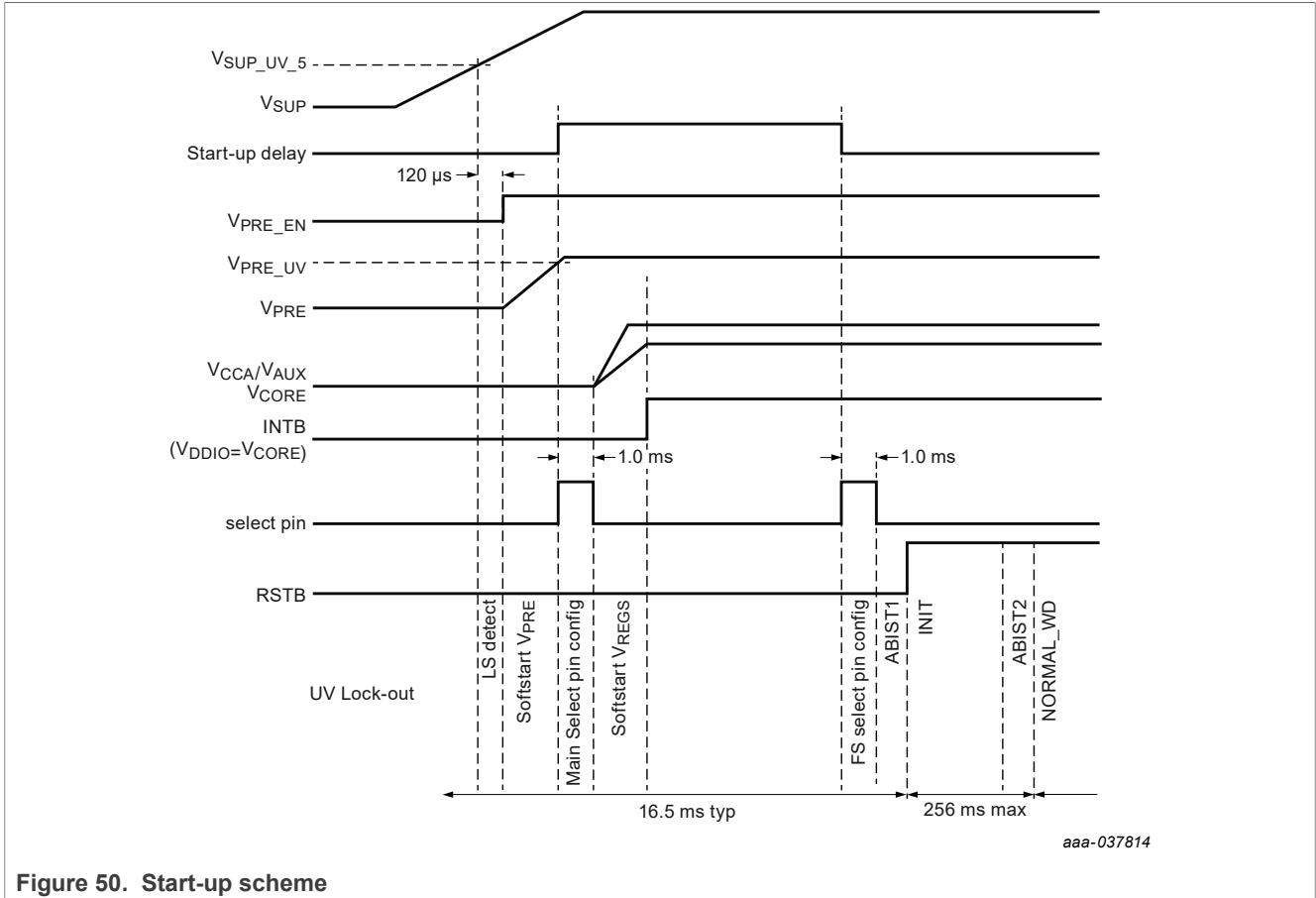


Figure 50. Start-up scheme

The final value of  $V_{AUX}$  and  $V_{CCA}$  depends on the hardware configuration (resistor values at the SELECT pin). The typical start-up sequence takes around 16.5 ms to release RSTB. RSTB can be pulled low after those 16.5 ms by the MCU, if it is not ready to run after power up. See [Section 12.7.7](#) for the VKAM start-up sequence.

### 12.8 Long duration timer

The device includes a long duration timer, with an integrated oscillator. The timer is configurable by the SPI and can operate in normal mode and low-power mode. It provides several functions and offers a large range of counting periods, as well as a calibration mechanism, for internal oscillator compensation.

The timer is not part of the safety circuitry. However it can be activated in normal mode, and all prescaler options can be selected, to allow timer circuitry verification. The timer is based on a 24-bit counter, with a 32768 Hz oscillator, allowing a 1.0 s timebase.

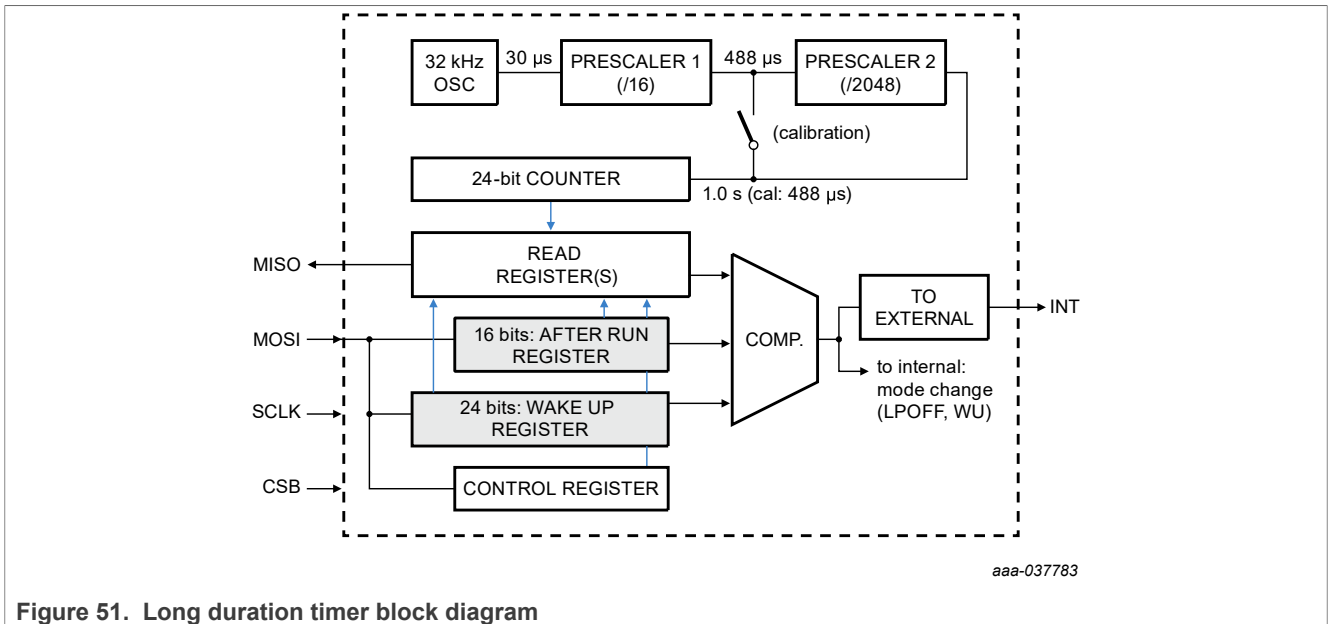


Figure 51. Long duration timer block diagram

### 12.8.1 Timer characteristics

In normal operation, the timer can count up to 194 days, with 1 second resolution. In calibration mode, the prescaler 2 is bypassed and the timer can count up to 2.28 hours, with 488 μs resolution. The calibration principle consists in activation of the counter for a dedicated and accurate duration, due to the MCU accurate clock and timing. The MCU then reads back the timer count, compares the count versus the accurate time of activation, then calculates a time offset. It is recommended to perform the calibration between -20 °C and +85 °C.

Table 13. Long duration timer characteristics

	Osc freq	Osc period	Prescaler	Counter resolution	Max count	
Operation	32768 Hz	30.52 μs	16 x 2048	1 s	4660 Hrs	194 days
Calibration	32768 Hz	30.52 μs	16	488 μs	8192 s	2.28 Hrs

### 12.8.2 Calibration procedure

The calibration procedure consists of activating the counter for a specific duration and comparing the result with the MCU's accurate clock and timing. Once the timer expires, the MCU reads back its final value to compare with its own accurate time of activation and to calculate a time offset. NXP recommends performing the calibration between -20 °C and 85 °C.

Calibration example:

- Select the timer function 1 and set the after run value to 65535 (~32 s).
- Start the counter.
- Read the counter when the MCU RTC reaches 20 s (must be less than 30 s with ±5.0 % oscillator accuracy).
- If the oscillator period is at exact typical value (absolutely no deviation error), expected reading is 40960.
- The exact reading calculates the error correction factor  $ECF = \frac{\text{exact\_reading}}{\text{expected\_reading}}$ .
- $ECF < 1$  if the oscillator is faster than the exact typical value.
- $ECF > 1$  if the oscillator is slower than the exact typical value.

- After calibration, the new after run or wake-up values to set the counter are "after run x ECF" and "wake-up x ECF".

12.8.3 Timer functions

- **Function 1:** In normal mode, count and generate a flag or an Interrupt when the counter reaches the after run value.
- **Function 2:** In normal mode, count until the counter reaches the after run value and enters into low-power mode.
- **Function 3:** In normal mode, count until the counter reaches the after run value and enters into low-power mode. Once in low-power mode, count until the counter reaches the wake-up value and wakes up.
- **Function 4:** In low-power mode, count until the counter reaches the wake-up value and wakes up.
- **Function 5:** In low-power mode, count and do not wake-up unless the counter overflow occurs, or if the device wakes up by another source (CAN, LIN, IO).

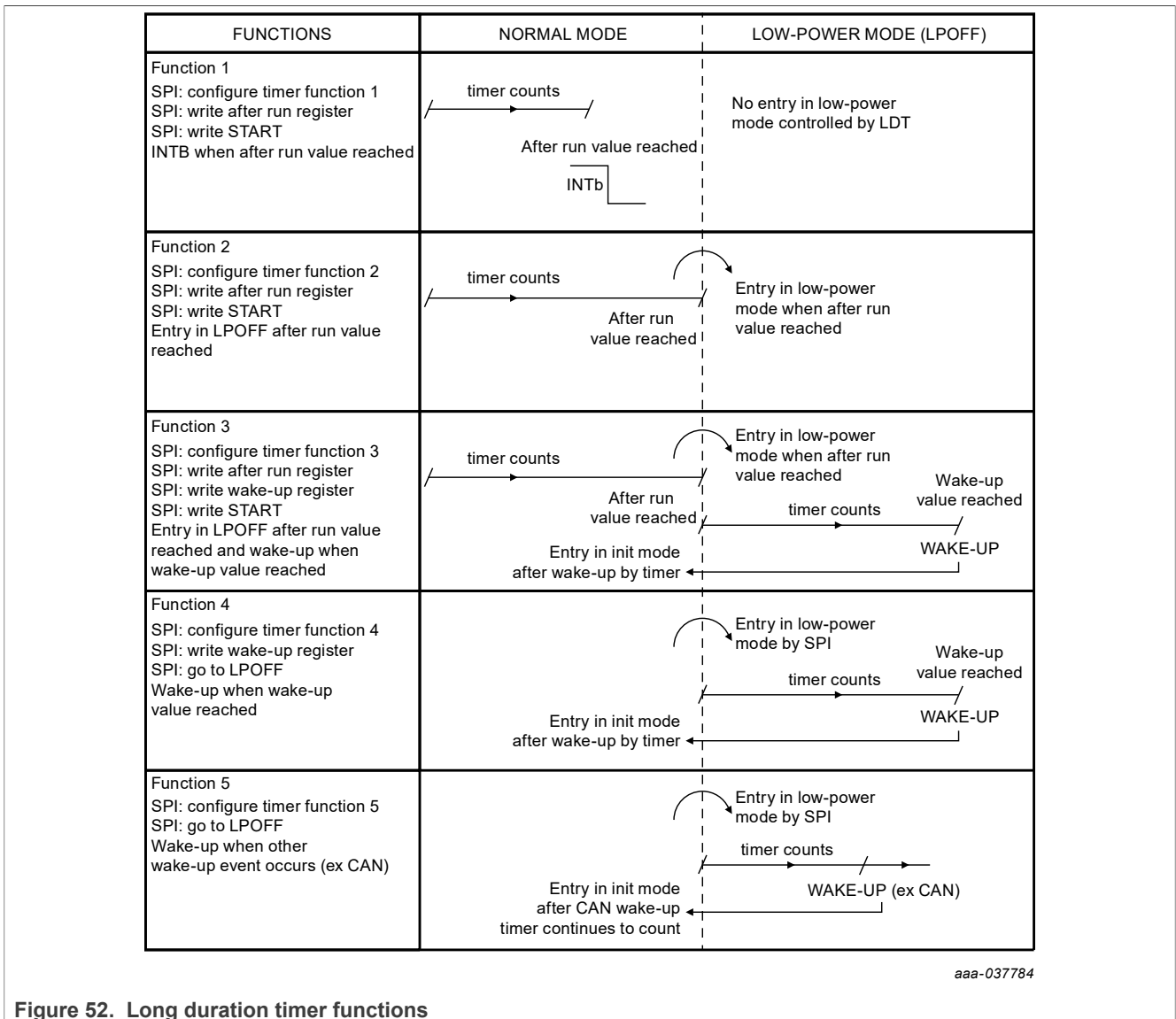


Figure 52. Long duration timer functions



12.8.4 Timer operation

The timer is configured and operates with the LONG\_DURATION\_TIMER register. The 16-bit after-run value and the 24-bit wake-up value are configured and read in the corresponding registers.

Figure 53 describes the independent state machine of long duration timer (LDT). After a POR of the device, the LDT is in idle mode waiting for configuration. The after-run timer function starts when the LDT\_ENABLE bit is set by SPI. The wake-up timer function starts when the device enters in LPOFF mode.

- When function 1 is selected and the counter reaches the after run value (EOT), an interrupt is generated and the counter is stopped. The counter must be disabled (~ENABLE) before reading its value and enabled again.
- When function 2 is selected and the counter reaches the after run value (EOT), the device goes to LPOFF mode and the counter is stopped. The counter must be disabled (~ENABLE) before reading its value and enabled again.
- When function 3 is selected and the counter reaches the after run value (EOT), the device goes to LPOFF mode. The counter is reset and restart to count. When the counter reaches the wake-up value (EOT), the device wakes up and the counter is stopped. The counter must be disabled (~ENABLE) before reading its value and enabled again.
- When function 4 is selected and the counter reaches the wake-up value (EOT), the device wakes up and the counter is stopped. The counter must be disabled (~ENABLE) before reading its value and enabled again.
- When function 5 is selected and the counter overflows (OVRFLW), the device wakes up and the counter is stopped. The counter must be disabled (~ENABLE) before reading its value and enabled again. Overflow means counter max value is reached (all 24 bits at logic 1).
- When function 5 is selected and the devices wakes up by CAN, LIN, or IO, the counter is running. The counter must be disabled (~ENABLE) before reading its value and enabled again.

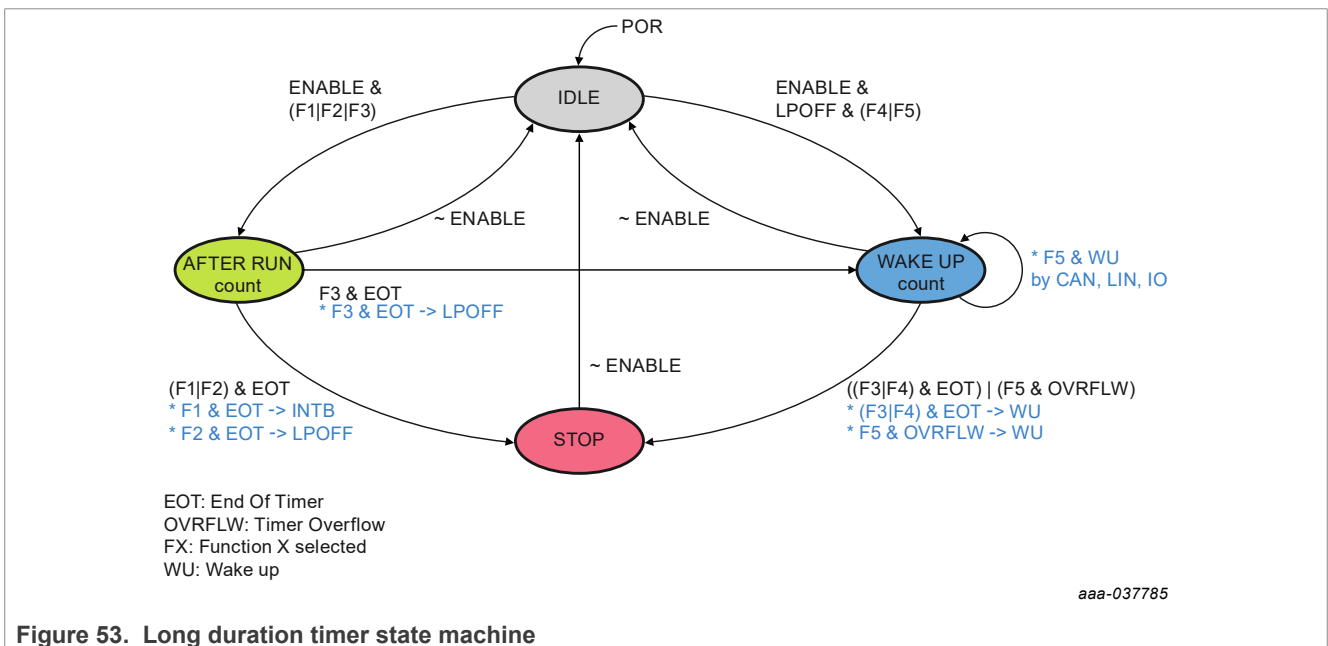


Figure 53. Long duration timer state machine

12.9 CAN transceiver

The CAN (controller area network) transceiver provides the physical interface between the CAN protocol controller of an MCU and the physical dual wires CAN-bus. The FS6500/FS4500 integrated CAN interface is compliant with flexible data standard at 2.0 Mbit/s. It offers excellent EMC and ESD performance, and meets the ISO 11898-2<sup>(12)</sup> and ISO 11898-5<sup>(13)</sup> standards.

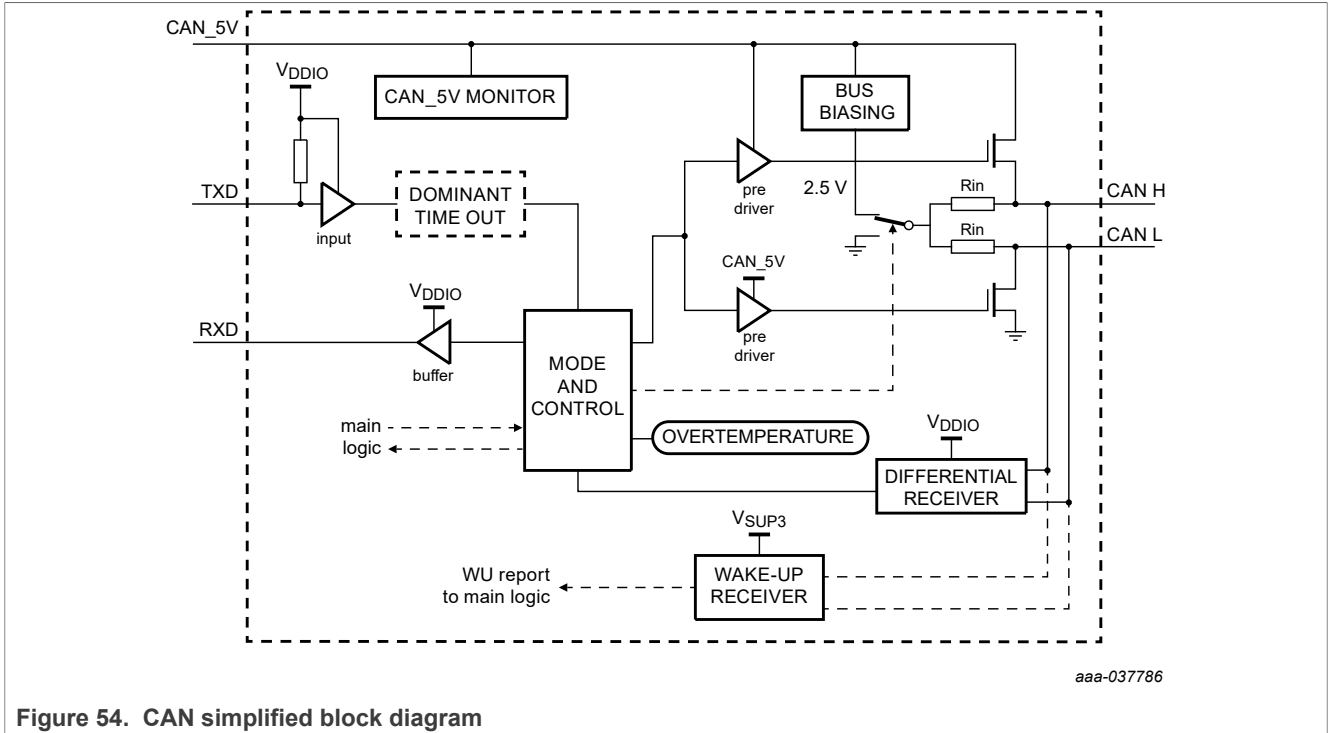


Figure 54. CAN simplified block diagram

### 12.9.1 Operating modes

#### 12.9.1.1 Normal mode

When the CAN mode bit configuration is '11' (CAN in normal operation), the device is able to transmit information from TXD to the bus and report the bus level to the RXD pin. When TXD is high, CANH and CANL drivers are off and the bus is in the recessive state (unless it is in an application where another device drives the bus to the dominant state). When TXD is low, the CANH and CANL drivers are on and the bus is in the dominant state. When the CAN mode bit configuration is '01' (CAN in listen only), the device is only able to report the bus level to the RXD pin. The TXD driver is off and the device is not able to transmit information from TXD to the bus. TXD is maintained high by an internal pull-up resistor TXD<sub>PULL-UP</sub> connected to VDDIO.

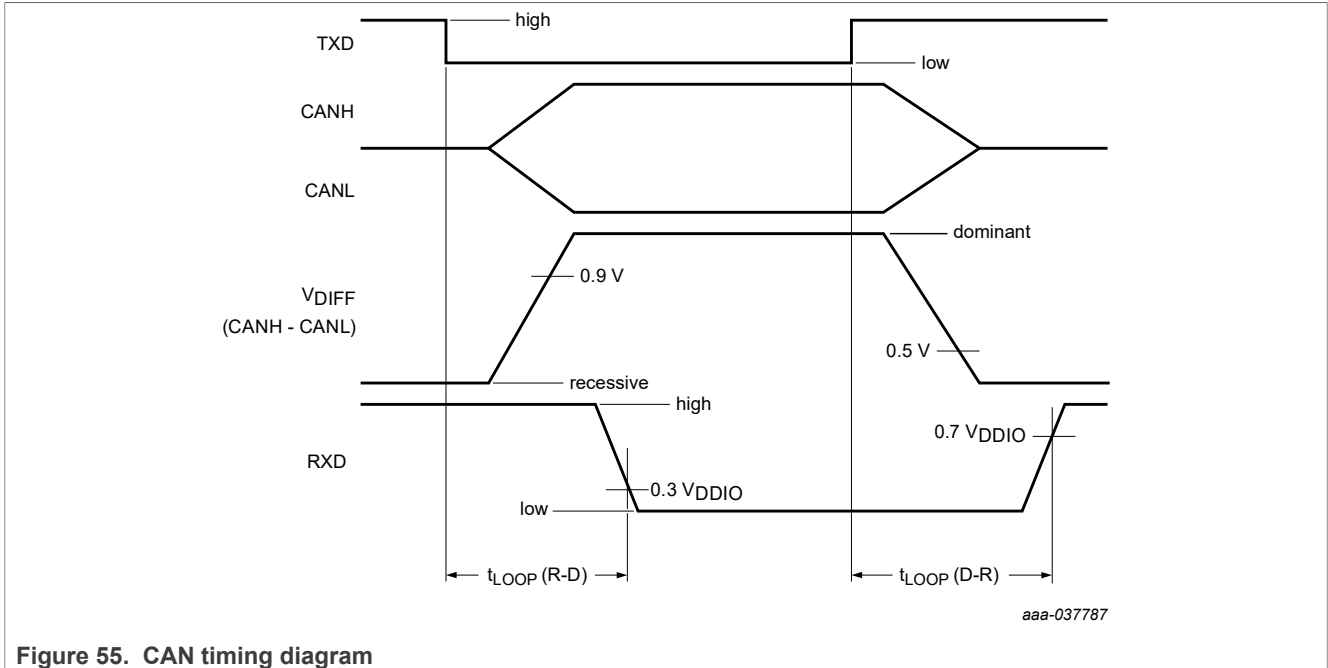


Figure 55. CAN timing diagram

12.9.1.2 Sleep mode

When the device is in LPOFF mode, the CAN transceiver is automatically set in sleep mode with or without wake-up capability, depending on the CAN mode bit configuration. In this case, the CANH and CANL pins are pulled down to GND via the internal R<sub>IN</sub> resistor, the TXD and RXD pins are pulled to GND, and both driver and receiver are off. The CAN mode is automatically changed to sleep with wake-up capability if not configured to sleep without wake-up capability when the device enters LPOFF. After LPOFF, the initial CAN mode prior to enter LPOFF is restored (Figure 56).

CAN state before entering LPOFF		CAN state after LPOFF		CAN state after entering LPOFF	
CAN_mode [1:0]	CAN state	CAN_mode [1:0]	CAN state	CAN_mode [1:0]	CAN state
00	Sleep, no wake-up capability	00	Sleep, no wake-up capability	00	Sleep, no wake-up capability
01	Listen only	10	Sleep, wake-up capability	01	Listen only
10	Sleep, wake-up capability			10	Sleep, wake-up capability
11	Normal			11	Normal

aaa-037788

Figure 56. CAN transition when device goes to LPOFF

12.9.2 Fault detection

12.9.2.1 TXD permanent dominant (timeout)

If TXD is set low for a time longer than t<sub>DOUT</sub>, the CAN drivers are disabled and the CAN-bus returns to the recessive state. The CAN receiver continues to operate. This prevents the bus to be set in the dominant state permanently in case a failure sets the TXD input to a permanent low level.

The CAN\_MODE MSB bit is set to 0 and the flag TXD\_dominant is reported in the DIAG\_CAN\_1 register. The device recovers from this error detection after setting the CAN\_MODE to normal operation and when a high level is detected on TXD. The TXD failure detection is operating when the CAN transceiver is in normal mode and listen only mode.

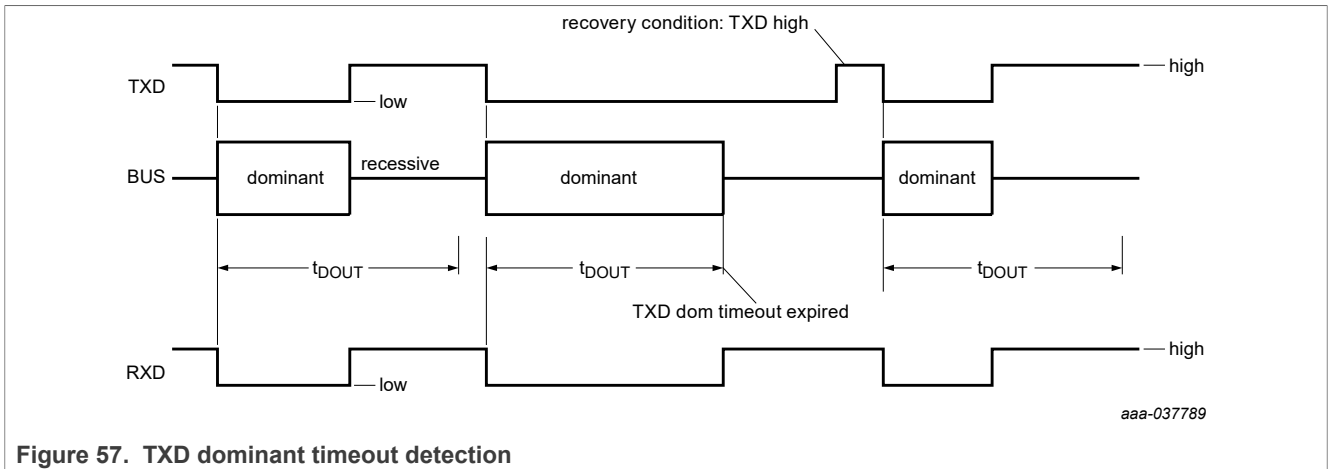


Figure 57. TXD dominant timeout detection

### 12.9.2.2 RXD permanent recessive

If RXD is detected high for seven consecutive receive/dominant cycles, the CAN drivers and receiver are disabled and the CAN-bus returns to the recessive state. This prevents a CAN protocol controller from starting a CAN message on the TXD pin, while RXD is shorted to a recessive level and seen from a CAN controller as a bus idle state.

The CAN\_MODE MSB bit is set to 0 and the flag RXD\_REC is reported in the DIAG\_CAN\_1 register. The device recovers from this error detection after setting the CAN\_MODE to normal operation. The RXD failure detection is operating when the CAN transceiver is in normal mode and listen only mode.

### 12.9.2.3 CAN-bus short-circuits

CANL/CANH short to GND and CANL/CANH short to the battery are detected and reported to the device main logic. The CAN driver and receiver are not disabled. They are detected and reported to the device main logic.

CANL short to GND is detected when CANL is < 0.5 V, 500 ns after TXD is activated low, and five consecutive times, as illustrated for CANL short to GND on Figure 58. CANH short to the battery is detected when CANH is > 5.2 V, 500 ns after TXD is activated low, and five consecutive times. CANL short to the battery and CANH short to GND are detected when  $I_{CANL}$  or  $I_{CANH} > 75$  mA (typ), 500 ns after TXD is activated low, and five consecutive times.

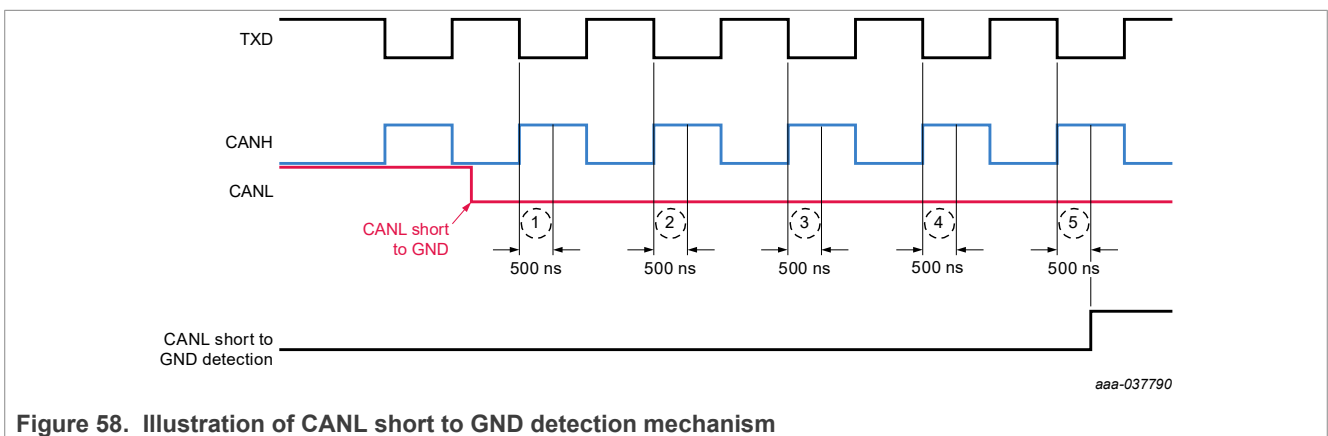


Figure 58. Illustration of CANL short to GND detection mechanism

If the CAN-bus is dominant for a time longer than  $t_{DOM}$ , due for instance to an external short-circuit from another CAN node, the flag CAN\_DOM is reported in the DIAG\_CAN\_1 register. This failure does not disable the bus

driver. The CAN-bus dominant failure detection is operating when the CAN transceiver is in normal mode and listen only mode.

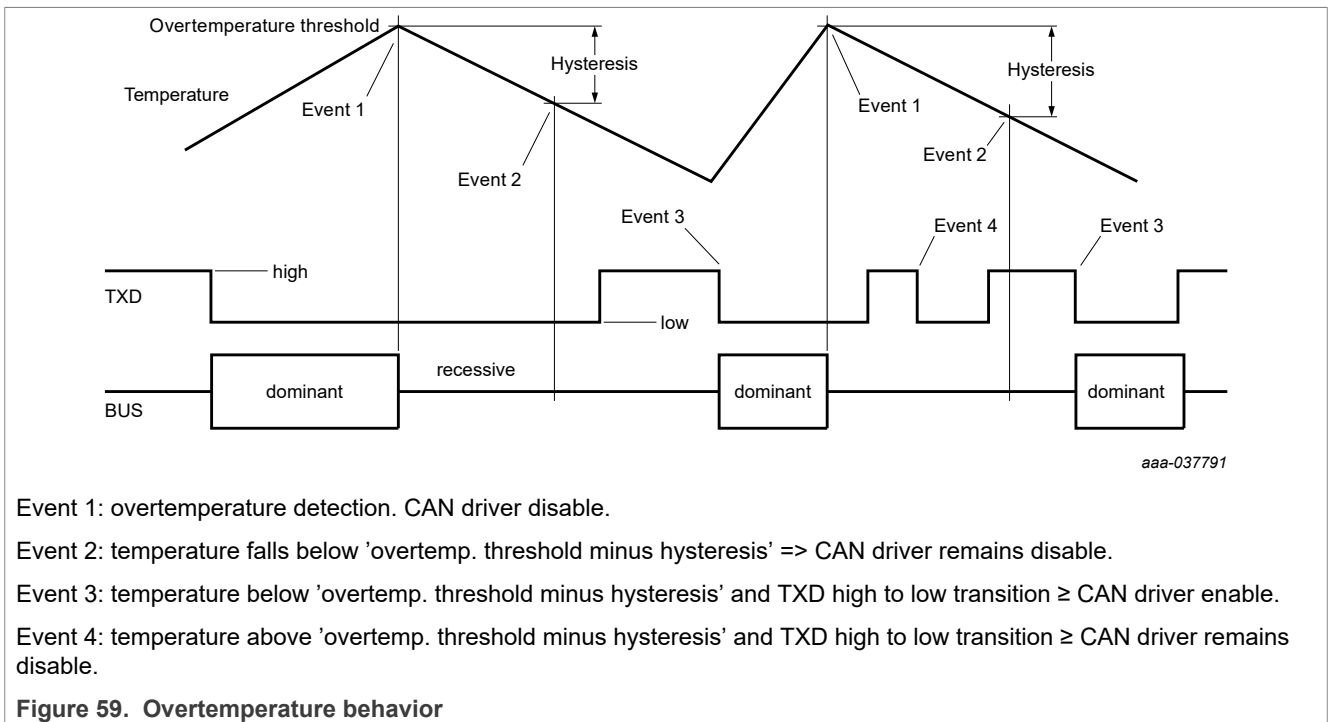
12.9.2.4 CAN current limitation

The current flowing in and out of the CANH and CANL driver is limited to 100 mA, in case of a short-circuit (parameters  $I_{CANL-SK}$  and  $I_{CANH-SC}$ ).

12.9.2.5 CAN overtemperature

If the driver temperature exceeds the TSD ( $T_{OT}$ ), the CAN drivers are disabled and the CAN-bus returns to the recessive state. The CAN receiver continues to operate. The CAN\_MODE MSB bit is set to 0 and the flag CAN\_OT is reported in the DIAG\_CAN\_LIN register.

A hysteresis is implemented in this protection feature. The device overtemperature and recovery conditions are shown in Figure 59. The CAN drivers remain disabled until the temperature has fallen below the OT threshold minus hysteresis. The device recovers from this error detection after setting the CAN\_MODE to normal operation and when a high level is detected on TXD.



12.9.2.6 Distinguish CAN diagnostics and CAN errors

The CAN errors can generate an interruption while the CAN diagnostics are reported in the digital for information only. The interruption generated by the CAN errors can be inhibited setting the INT\_INH\_CAN bit in the INIT\_INH\_INT register. The list of CAN diagnostic and CAN error bits is provided in Table 14.

Table 14. CAN diagnostic and CAN error bits

Register	Bit	Flag type	Effect
DIAG_CAN_FD	CANH_BATT	Diagnostic	No impact on CAN transceiver
	CANH_GND	Diagnostic	No impact on CAN transceiver
	CANL_BATT	Diagnostic	No impact on CAN transceiver
	CANL_GND	Diagnostic	No impact on CAN transceiver
	CAN_DOM	Error	Turn off CAN transceiver
	RXD_REC	Error	Turn off CAN transceiver
	TXD_DOM	Error	Turn off CAN transceiver
DIAG_CAN_LIN	CAN_OT	Error	Turn off CAN transceiver
	CAN_OC	Diagnostic	No impact on CAN transceiver

### 12.9.3 Wake-up mechanism

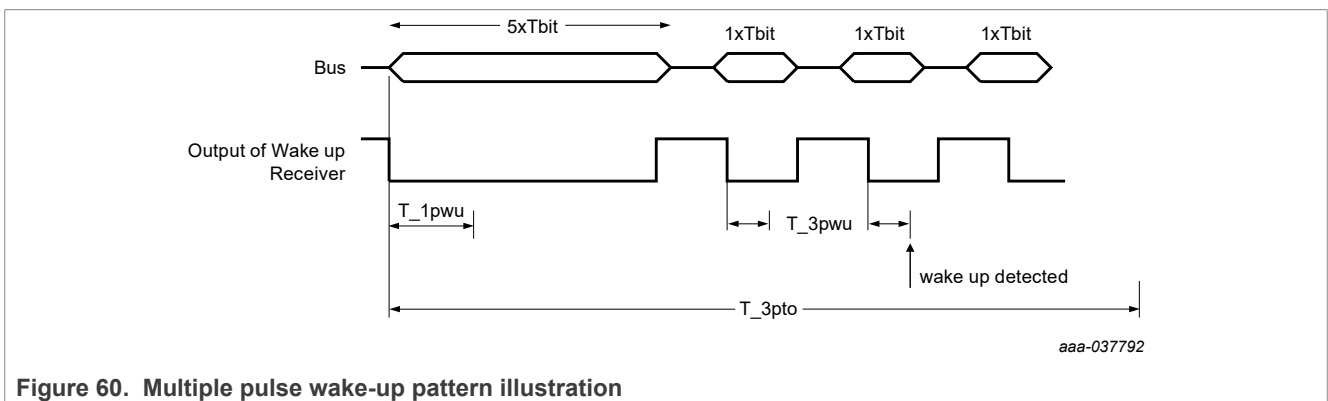
The device includes bus monitoring circuitry to detect and report bus wake-ups when the device is in LPOFF and when CAN mode configuration is different from sleep/no wake-up capability. Multiple dominant pulse wake-up detection is implemented. The event must occur within the  $t_{3PTOX}$  timeout.  $t_{3PTOX} = t_{3PTO1}$  or  $t_{3PTO2}$ , depending on the SPI selection. The wake-up events are reported in the WU\_SOURCE register.

#### 12.9.3.1 Multiple pulse detection

To activate wake-up report, three events must occur on the CAN-bus:

- event 1: a dominant level longer than  $t_{1PWU}$  followed by
- event 2: a dominant level longer than  $t_{3PWU}$  followed by
- event 3: a dominant level longer than  $t_{3PWU}$ .

The three events and the timeout function avoiding a permanent dominant state on the bus generates permanent wake-up situation which would prevent system to enter in low-power mode.



### 12.10 LIN transceiver

The local interconnect network (LIN) is a serial communication protocol, designed to support automotive networks in conjunction with a controller area network (CAN). The LIN transceiver is operational from a  $V_{SUP}$  of 7.0 V to 18 V DC, and compatible with LIN protocol specification 2.0, 2.1<sup>(22)</sup>, 2.2<sup>(23)</sup>, and SAEJ2602-2<sup>(24)</sup>.

12.10.1 Simplified block diagram

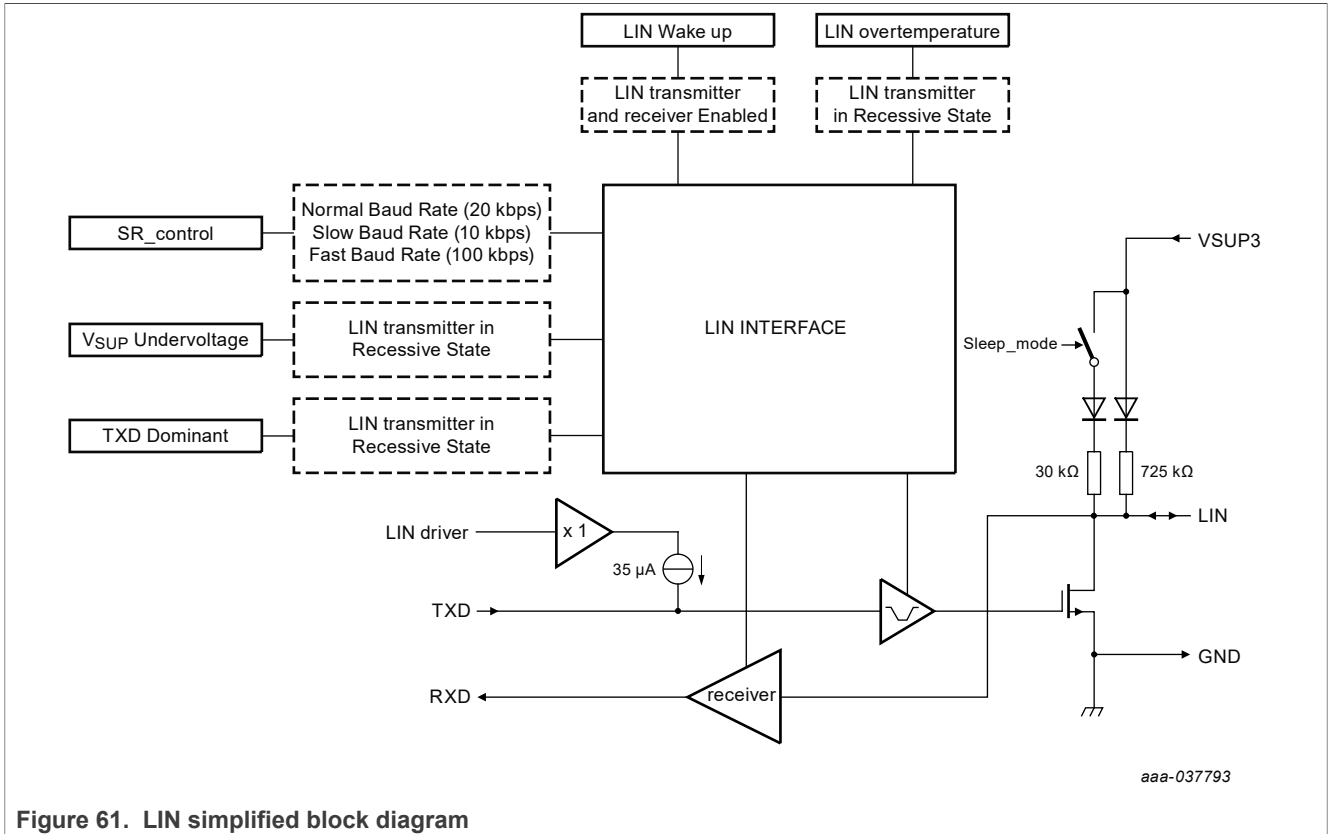


Figure 61. LIN simplified block diagram

12.10.2 Operating modes

12.10.2.1 Normal mode

When the LIN mode bit configuration is '11' (LIN in normal operation), the device is able to transmit information from TXDL to the bus and report the bus level to the RXDL pin. When TXDL is high, the LIN driver is off and the bus is in the recessive state (unless it is in an application where another device drives the bus to the dominant state). When TXDL is low, the LIN driver is on and the bus is in the dominant state.

When the LIN mode bit configuration is '01' (LIN in listen only), the device is only able to report the bus level to the RXDL pin. The TXDL driver is off and the device is not able to transmit information from TXDL to the bus. TXDL is maintained high by the internal pull-up resistor TXDLPULL-UP connected to VDDIO.

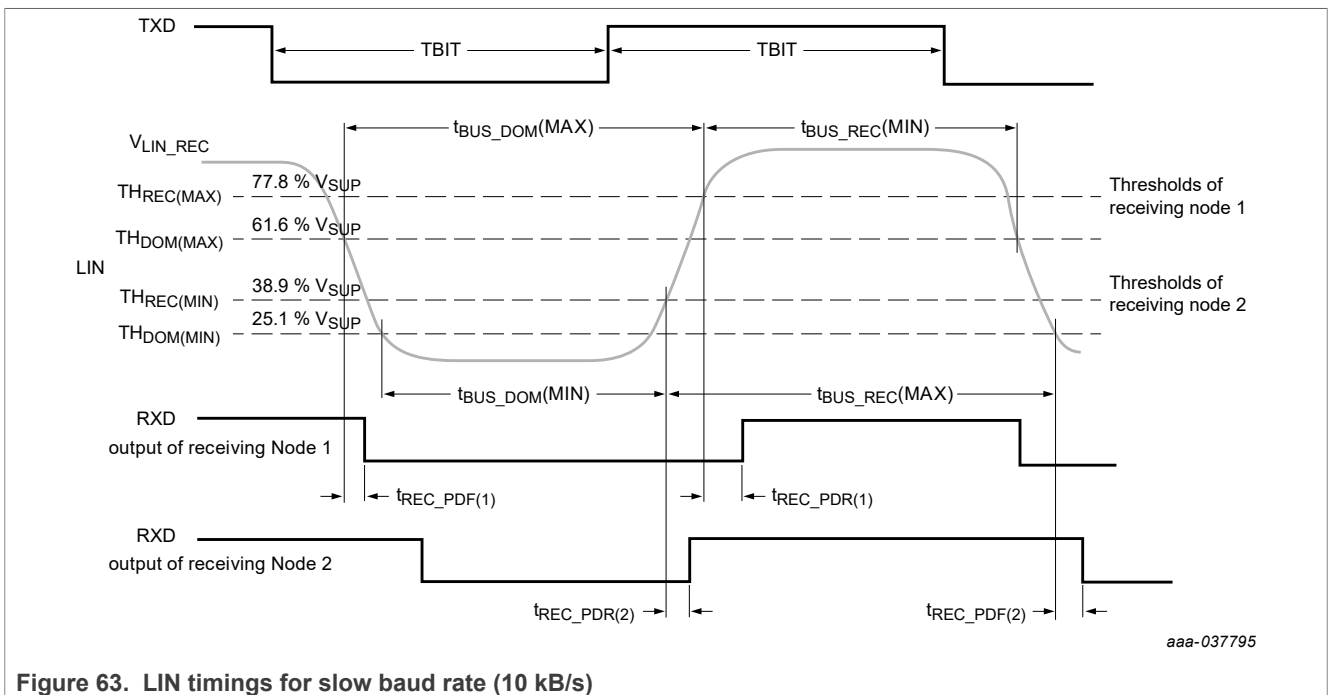
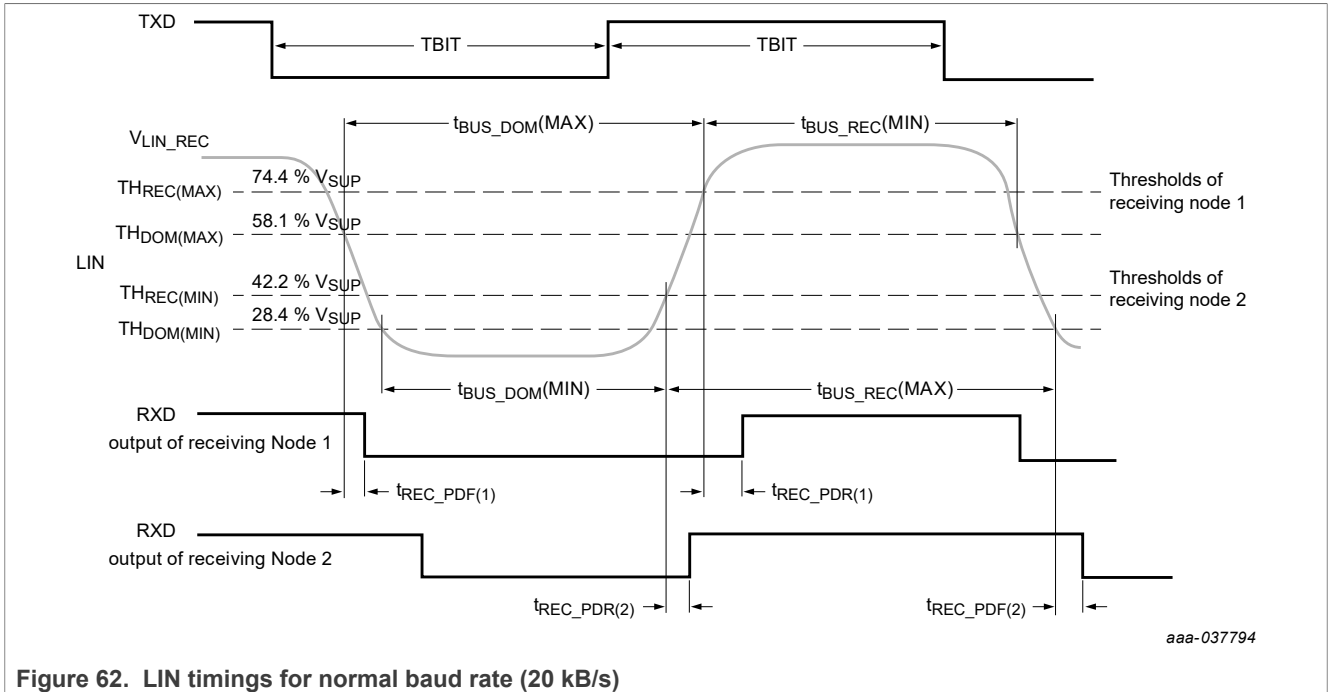
12.10.2.2 Sleep mode

When the device is in LPOFF mode, the LIN transceiver is automatically set into sleep mode with or without wake-up capability, depending on the LIN mode bit configuration. In this case, the LIN pin is pulled up to VSUP via the internal resistor and diode structure, the TXDL and RXDL pins are driven to GND.

12.10.3 Baud rate selection

The device has two selectable baud rates: 20 kB/s for normal baud rate and 10 kB/s for slow baud rate. An additional fast baud rate (100 kB/s) can be used to flash the MCU, or in the garage for diagnostic. The LIN consortium specification does not specify electrical parameters for this baud rate. The communication only

is guaranteed. The baud rate selection is done by the SPI setting during the INIT phase of the main logic. Depending on the baud rate setting, the corresponding LIN slope control is automatically selected.





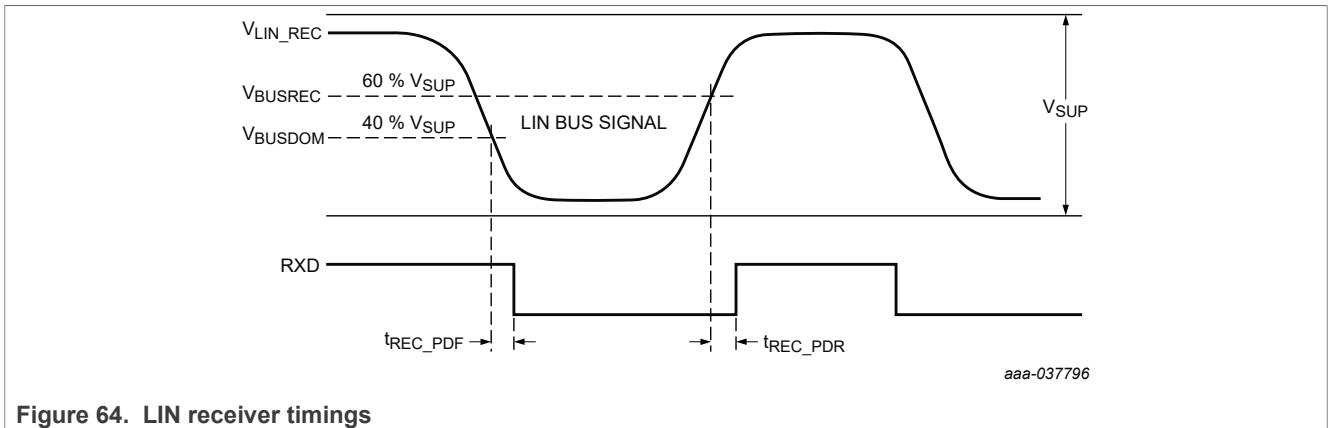


Figure 64. LIN receiver timings

12.10.4 Fault detection

12.10.4.1 VSUP undervoltage

A  $V_{SUP}$  undervoltage ( $V_{LIN\_UV}$ ) detection is implemented to be compliant with SAEJ2602-2<sup>(24)</sup> standard. At low  $V_{SUP}$  voltage ( $V_{SUP} < V_{LIN\_UV}$ ), the LIN bus goes into recessive state to avoid wrong communication.

12.10.4.2 TXDL permanent dominant (timeout)

If TXDL is set low for a time longer than the  $t_{XD\_DOM}$  parameter, the LIN driver is disabled and the LIN bus returns to the recessive state. This prevents the bus from being set in dominant state permanently, in case a failure sets the TXDL input permanently to a low level.

The LIN receiver continues to operate. The LIN\_mode MSB bit is set to 0 and the TXDL\_DOM flag is reported in the DIAG\_CAN\_LIN register. The device recovers from this error detection after setting the LIN\_mode to normal operation, and when a high level is detected on TXDL. The TXDL failure detection is operating when the LIN transceiver is in normal mode and listen only mode.

12.10.4.3 RXDL permanent recessive

If RXDL is detected high for seven consecutive receive/dominant cycles, the LIN driver and receiver are disabled and the LIN bus returns to the recessive state. The LIN\_mode MSB bit is set to 0 and the RXDL\_REC flag is reported in the DIAG\_CAN\_LIN register. The device recovers from this error detection after setting the LIN\_mode to normal operation, and after a LIN dominant transition. The RXDL failure detection is operating when the LIN transceiver is in normal mode and listen only mode.

12.10.4.4 LIN bus short-circuit

If the LIN bus is dominant for a time longer than  $t_{LIN\_SHORT\_GND}$ , due for instance to an external short-circuit to GND, the detection is reported to the device main logic. The BUS bus failure detection is operating when the LIN transceiver is in normal mode and listen only mode.

12.10.4.5 LIN current limitation

In case of a LIN short-circuit to the battery, the current flowing out of the LIN driver is limited to 200 mA ( $I_{BUS\_LIM}$ ), and the LIN driver is not shutdown. The LIN bus goes into the recessive state when the current limitation occurs and returns in the same functional mode as before the failure when the current fell below the current limitation value.

12.10.4.6 LIN overtemperature

If the driver temperature exceeds TSD ( $t_{LIN\_SD}$ ), the LIN driver is disabled and the LIN bus returns to the recessive state. The LIN receiver continues to operate. The LIN\_mode MSB bit is set to 0 and the LIN\_OT flag is reported in the DIAG\_CAN\_LIN register. A hysteresis is implemented in this protection feature. The LIN driver remains disabled until the temperature has fallen below the OT threshold minus hysteresis. The device recovers from this error detection after setting the LIN\_mode to normal operation, and when a high level is detected on TXDL.

12.10.4.7 LIN errors

The interruption generated by the LIN errors can be inhibited setting INT\_INH\_LIN bit in INIT\_INH\_INT register. The list of LIN error bits is provided in [Table 15](#).

Table 15. LIN error bits

Register	Bit	Flag type	Effect
DIAG_CAN_LIN	LIN_DOM	Error	No impact on LIN transceiver
	RXDL_REC	Error	Turn off LIN transceiver
	TXDL_DOM	Error	Turn off LIN transceiver
	LIN_OT	Error	Turn off LIN transceiver

12.10.5 Wake-up mechanism

The device can wake-up by a LIN dominant pulse longer than  $t_{BUS\_WU}$ . Dominant pulse means: a recessive to dominant transition, wait for  $t > t_{BUS\_WU}$ , then a dominant to recessive transition.

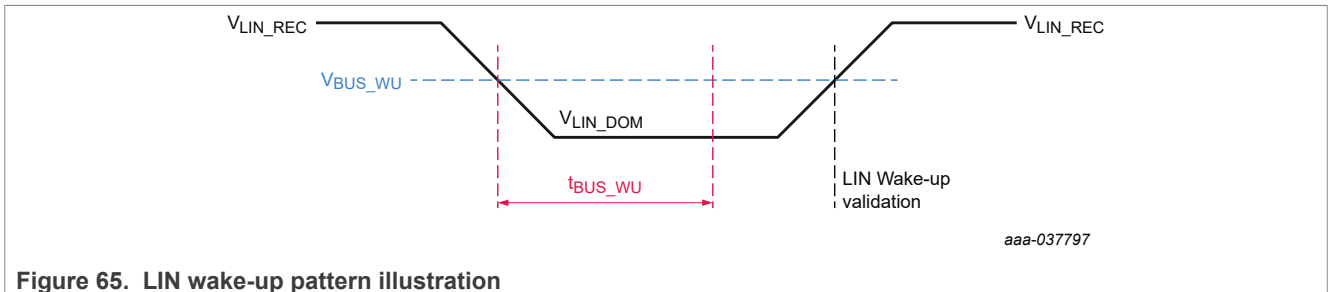


Figure 65. LIN wake-up pattern illustration

## 13 Serial peripheral interface

### 13.1 High-level overview

#### 13.1.1 SPI

The device uses a 16-bit SPI, with the following arrangement:

MOSI, primary out, secondary in bits:

- Bit 15 read/write
- Bit 14 main or fail-safe register target
- bit 13 to 9 (A4 to A0) to select the register address. Bit 8 is a parity bit in write mode, next bit (=0) in read mode.
- bit7 to 0 (D7 to D0): control bits

MISO, primary in, secondary out bits:

- bits 15 to 8 (S15 to S8) are device status bits
- bits 7 to 0 (Do7 to Do0) are either extended device status bits, device internal control register content or device flags.

[Figure 66](#) is an overview of the SPI implementation.

#### 13.1.2 Parity bit 8 calculation

The parity bit 8 is used in write mode only (bit 15 = 1). It is calculated based on the number of logic ones contained in the bit 15–9, 7–0 sequence (this is the whole 16-bits of the write command except bit 8). In read mode, the parity bit should be set to 0.

Bit 8 must be set to 0 if the number of ones is odd.

Bit 8 must be set to 1 if the number of ones is even.

#### 13.1.3 Device status on MISO

When a write operation is performed to store data or a control bit in the device, the MISO pin reports a 16-bit fixed device status composed of two bytes: device fixed status (bits 15 to 8) + extended device status (bits 7 to 0). In a read operation, MISO reports the fixed device status (bits 15 to 8), and the next eight bits are content of the selected register. A standard serial peripheral interface (SPI) is integrated to allow bidirectional communication between the FS6500/FS4500 and the MCU. The SPI is used for configuration and diagnostic purposes.

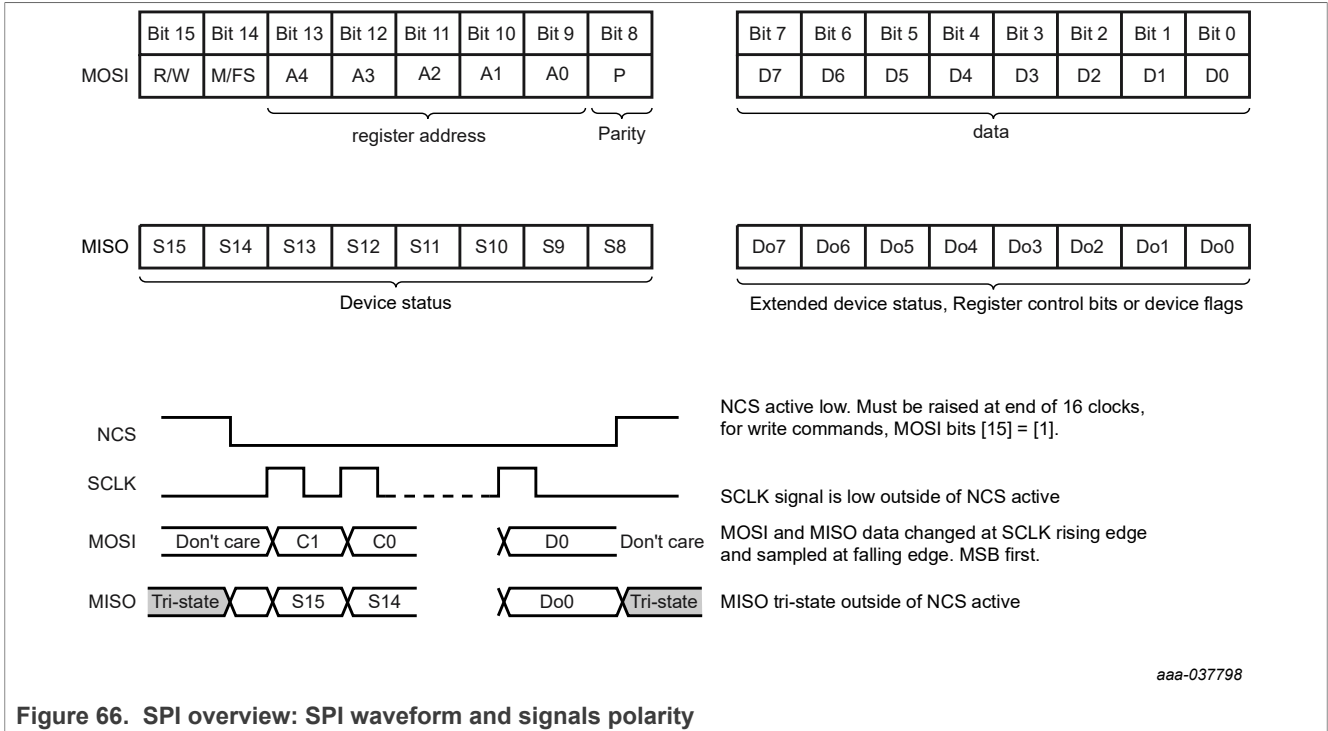


Figure 66. SPI overview: SPI waveform and signals polarity

The device contains several registers. Their address is coded on 7 bits (bits 15 to 9). Each register controls or reports part of the device function. Data can be written to the register, to control the device operation or set default value or behavior. Every register can also be read back to ensure its content (default setting or value previously written) is correct.

### 13.1.4 Register description

Although the minimum time between two NCS low sequences is defined by  $t_{ONNCS}$  (Figure 9), two consecutive accesses to the fail-safe registers must be done with a 3.5  $\mu$ s minimum NCS high time in between. Although the minimum time between two fail-safe registers accesses is 3.5  $\mu$ s, some SPI accesses to the main registers can be done in between (Figure 10).

## 13.2 Detailed operation

### 13.2.1 SPI command organization

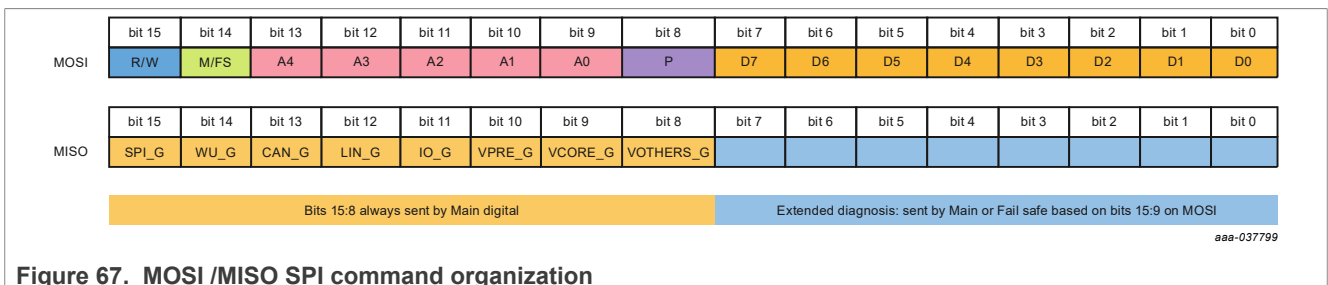


Figure 67. MOSI /MISO SPI command organization

Table 16. MOSI bits description

R/W	Description	Set if it is a read or write command
	0	Read
	1	Write
M/FS	Description	Split the addresses between fail-safe state machine and main logic
	0	Main
	1	Fail-safe
A4:0	Description	Set the address to read or write
	0	See register mapping
	1	
P	Description	Parity bit (only use in write mode). Set to 0 in read mode
	0	Number of '1' (bit 15:9 and bit 7:0) is odd
	1	Number of '1' (bit 15:9 and bit 7:0) is even
D7:0	Description	Data in write mode. Must be set to 00h in read mode
	0	See register details
	1	

13.2.2 Main logic general diagnostic

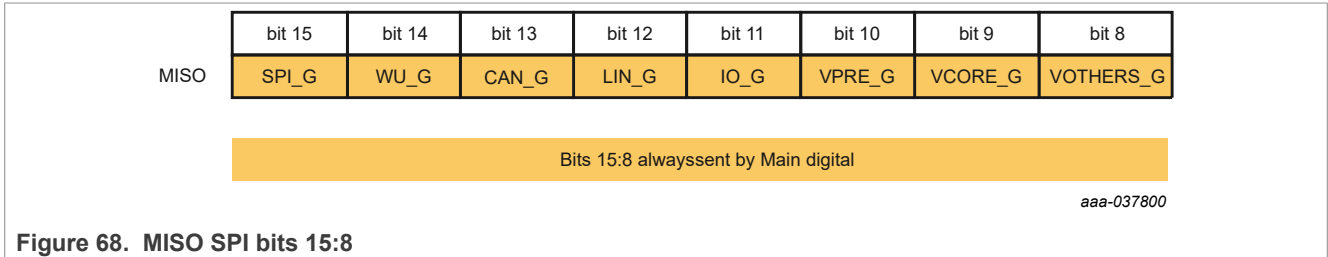


Figure 68. MISO SPI bits 15:8

Table 17. MISO bits description

SPI_G <sup>[1]</sup>	Description	Report an error in the SPI communication
	0	No failure
	1	Failure
	Reset condition	Power on reset/read
WU_G <sup>[2]</sup>	Description	Report a wake-up event. Logical OR of all wake-up sources
	0	No WU_G event
	1	WU_G event
	Reset condition	Power on reset/when initial event cleared on read
CAN_G <sup>[3]</sup>	Description	Report a CAN event (diagnostic)
	0	No event
	1	CAN event
	Reset Condition	Power on reset/when initial event cleared on read

Table 17. MISO bits description...continued

LIN_G <sup>[4]</sup>	Description	Report a LIN event (diagnostic)
	0	No event
	1	LIN event
	Reset condition	Power on reset/when initial event cleared on read
IO_G <sup>[5]</sup>	Description	Report a change in IOs state
	0	No IO transition
	1	IO transition
	Reset condition	Power on reset/when initial event cleared on read
VPRE_G <sup>[6]</sup>	Description	Report an event from V <sub>PRE-REGULATOR</sub> and battery monitoring (status change or failure)
	0	No event
	1	Event occurred
	Reset condition	Power on reset/when initial event cleared on read
VCORE_G <sup>[7]</sup>	Description	Report an event from V <sub>CORE</sub> regulator (status change or failure)
	0	No event
	1	Event occurred
	Reset condition	Power on reset/when initial event cleared on read
VOTHERS_G <sup>[8]</sup>	Description	Report an event from V <sub>CCA</sub> , V <sub>AUX</sub> , or V <sub>CAN</sub> regulators (status change or failure)
	0	No event
	1	Event occurred
	Reset condition	Power on reset/when initial event cleared on read

- [1] SPI\_G = SPI\_ERR or SPI\_CLK or SPI\_REQ or SPI\_PARITY or SPI\_FS\_ERR or SPI\_FS\_CLK or SPI\_FS\_REQ or SPI\_FS\_PARITY
- [2] WU\_G = IO\_5\_WU or IO\_4\_WU or IO\_3\_WU or IO\_2\_WU or IO\_0\_WU or PHY\_WU
- [3] CAN\_G = CANH\_BATT or CANH\_GND or CANL\_BATT or CANL\_GND or CAN\_DOM or RXD\_REC or TXD\_DOM or CAN\_OT or CAN\_OC
- [4] LIN\_G = LIN\_OT or RXDL\_REC or TXDL\_DOM or LIN\_DOM
- [5] IO\_G = IO\_5 or IO\_4 or IO\_3 or IO\_2 or IO\_0
- [6] VPRE\_G = VSNS\_UV or VSUP\_UV\_7 or IPFF or ILIM\_PRE or TWARN\_PRE or BOB or !VPRE\_STATE or VPRE\_OV or VPRE\_UV
- [7] VCORE\_G = TWARN\_CORE or !VCORE\_STATE or VCORE\_OV or VCORE\_UV
- [8] VOTHERS\_G = ILIM\_CCA or TWARN\_CCA or TSD\_CCA or ILIM\_CCA\_OFF or VCCA\_UV or VCCA\_OV or ILIM\_AUX or TSD\_AUX or ILIM\_AUX\_OFF or VAUX\_OV or VAUX\_UV or ILIM\_CAN or VCAN\_UV or VCAN\_OV or TSD\_CAN

13.2.3 Fail-safe logic general diagnostic

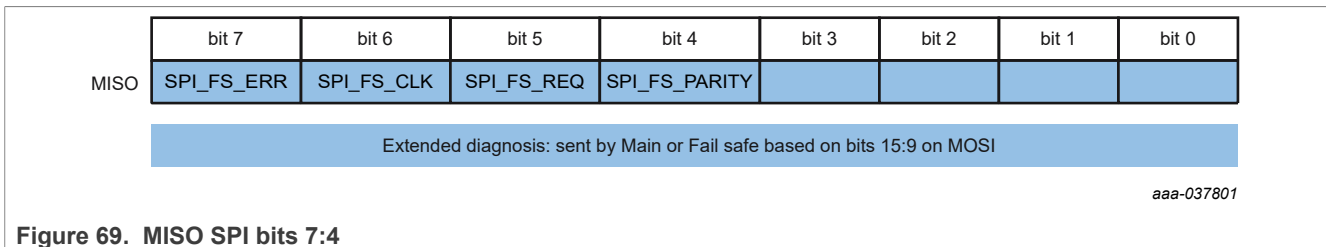


Figure 69. MISO SPI bits 7:4

**Table 18. MISO bits description**

SPI_FS_ERR	Description	Secured SPI communication check, concerns fail-safe logic only.
	0	<b>No error</b>
	1	Error detected in the secured bits
	Reset condition	Power on reset
SPI_FS_CLK	Description	SCLK error detection, concerns internal error in fail-safe logic only and external errors (at pin level) for both main and fail-safe logics. Other errors flagged by SPI_CLK_bit
	0	<b>16 clock cycles during NCS low</b>
	1	Wrong number of clock cycles (<16 or >16)
	Reset condition	Power on reset
SPI_FS_REQ	Description	Invalid SPI access (wrong write or read, write to INIT registers in normal mode, wrong address), concerns fail-safe Logic only
	0	<b>No error</b>
	1	SPI violation
	Reset condition	Power on reset
SPI_FS_PARITY	Description	SPI parity bit error detection, concerns fail-safe logic only
	0	<b>Parity bit OK</b>
	1	Parity bit error
	Reset condition	Power on reset

**13.2.4 Main logic register address table**

[Table 19](#) is a list of device registers and addresses coded in bits 13 to 9 in MOSI for main logic.

**Table 19. Register mapping of main logic**

Register	Address							Write description	Table ref.
	FS/M	A4	A3	A2	A1	A0	Hex		
INIT_VREG	0	0	0	0	0	1	#1(01h)	Write during INIT phase then read only	<a href="#">Table 22</a>
INIT_WU1	0	0	0	0	1	0	#2(02h)	Write during INIT phase then read only	<a href="#">Table 24</a>
INIT_WU2	0	0	0	0	1	1	#3(03h)	Write during INIT phase then read only	<a href="#">Table 26</a>
INIT_INT	0	0	0	1	0	0	#4(04h)	Write during INIT phase then read only	<a href="#">Table 28</a>
INIT_INH_INT	0	0	0	1	0	1	#5(05h)	Write during INIT phase then read only	<a href="#">Table 30</a>
LONG_DURATION_TIMER	0	0	0	1	1	0	#6(06h)	Write during normal and read	<a href="#">Table 32</a>
NOT USED	0	0	0	1	1	1	#7(07h)	N/A	N/A
HW_CONFIG	0	0	1	0	0	0	#8(08h)	Read only	<a href="#">Table 34</a>
WU_SOURCE	0	0	1	0	0	1	#9(09h)	Read only	<a href="#">Table 36</a>
DEVICE_ID	0	0	1	0	1	0	#10(0Ah)	Read only	<a href="#">Table 38</a>
IO_INPUT	0	0	1	0	1	1	#11(0Bh)	Read only	<a href="#">Table 40</a>
DIAG_VPRE	0	0	1	1	0	0	#12(0Ch)	Read only	<a href="#">Table 42</a>
DIAG_VCORE	0	0	1	1	0	1	#13(0Dh)	Read only	<a href="#">Table 44</a>
DIAG_VCCA	0	0	1	1	1	0	#14(0Eh)	Read only	<a href="#">Table 46</a>
DIAG_VAUX	0	0	1	1	1	1	#15(0Fh)	Read only	<a href="#">Table 48</a>
DIAG_VSUP_VCAN	0	1	0	0	0	0	#16(10h)	Read only	<a href="#">Table 50</a>
DIAG_CAN_FD	0	1	0	0	0	1	#17(11h)	Read only	<a href="#">Table 52</a>

Table 19. Register mapping of main logic ...continued

Register	Address							Write description	Table ref.
	FS/M	A4	A3	A2	A1	A0	Hex		
DIAG_CAN_LIN	0	1	0	0	1	0	#18(12h)	Read only	<a href="#">Table 54</a>
DIAG_SPI	0	1	0	0	1	1	#19(13h)	Read only	<a href="#">Table 56</a>
NOT USED	0	1	0	1	0	0	#20(14h)	N/A	N/A
MODE	0	1	0	1	0	1	#21(15h)	Write during normal and read	<a href="#">Table 58</a>
REG_MODE	0	1	0	1	1	0	#22(16h)	Write during normal and read	<a href="#">Table 60</a>
IO_OUT_AMUX	0	1	0	1	1	1	#23(17h)	Write during normal and read	<a href="#">Table 62</a>
CAN_LIN_MODE	0	1	1	0	0	0	#24(18h)	Write during normal and read	<a href="#">Table 64</a>
NOT USED	0	1	1	0	0	1	#25(19h)	N/A	N/A
LDT_AFTER_RUN_1	0	1	1	0	1	0	#26(1Ah)	Write during normal and read	<a href="#">Table 66</a>
LDT_AFTER_RUN_2	0	1	1	0	1	1	#27(1Bh)	Write during normal and read	<a href="#">Table 68</a>
LDT_WAKE_UP_1	0	1	1	1	0	0	#28(1Ch)	Write during normal and read	<a href="#">Table 70</a>
LDT_WAKE_UP_2	0	1	1	1	0	1	#29(1Dh)	Write during normal and read	<a href="#">Table 72</a>
LDT_WAKE_UP_3	0	1	1	1	1	0	#30(1Eh)	Write during normal and read	<a href="#">Table 74</a>

### 13.2.5 Fail-safe logic register address table

[Table 20](#) is a list of device registers and addresses coded in bits 13 to 9 in MOSI for fail-safe logic

Table 20. Register mapping of fail-safe logic

Register	Address							Write description	Table ref.
	FS/M	A4	A3	A2	A1	A0	Hex		
INIT_FS1B_TIMING	1	0	0	0	0	1	#33(21h)	Write during INIT phase then read only	<a href="#">Table 76</a>
BIST	1	0	0	0	1	0	#34(22h)	Write (No restriction) and read	<a href="#">Table 78</a>
INIT_SUPERVISOR	1	0	0	0	1	1	#35(23h)	Write during INIT phase then read only	<a href="#">Table 80</a>
INIT_FAULT	1	0	0	1	0	0	#36(24h)	Write during INIT phase then read only	<a href="#">Table 82</a>
INIT_FSSM	1	0	0	1	0	1	#37(25h)	Write during INIT phase then read only	<a href="#">Table 84</a>
INIT_SF_IMPACT	1	0	0	1	1	0	#38(26h)	Write during INIT phase then read only	<a href="#">Table 86</a>
WD_WINDOW	1	0	0	1	1	1	#39(27h)	Write (no restriction) and read	<a href="#">Table 88</a>
LFSR	1	0	1	0	0	0	#40(28h)	Write (no restriction) and read	<a href="#">Table 90</a>
WD_ANSWER	1	0	1	0	0	1	#41(29h)	Write (no restriction) and read	<a href="#">Table 92</a>
RELEASE_FSxB	1	0	1	0	1	0	#42(2Ah)	Write (no restriction) and read	<a href="#">Table 94</a>
SF_OUTPUT_REQUEST	1	0	1	0	1	1	#43(2Bh)	Write (no restriction) and read	<a href="#">Table 96</a>
INIT_WD_CNT	1	0	1	1	0	0	#44(2Ch)	Write during INIT phase then read only	<a href="#">Table 98</a>
DIAG_SF_IOs	1	0	1	1	0	1	#45(2Dh)	Read only	<a href="#">Table 100</a>
WD_COUNTER	1	0	1	1	1	0	#46(2Eh)	Read only	<a href="#">Table 102</a>
DIAG_SF_ERR	1	0	1	1	1	1	#47(2Fh)	Read only	<a href="#">Table 104</a>
NOT USED	1	1	0	0	0	0	#48(30h)	N/A	N/A
INIT_VCORE_OVUV_IMPACT	1	1	0	0	0	1	#49(31h)	Write during INIT phase then read only	<a href="#">Table 106</a>
INIT_VCCA_OVUV_IMPACT	1	1	0	0	1	0	#50(32h)	Write during INIT phase then read only	<a href="#">Table 108</a>
INIT_VAUX_OVUV_IMPACT	1	1	0	0	1	1	#51(33h)	Write during INIT phase then read only	<a href="#">Table 110</a>
DEVICE_ID_FS	1	1	0	1	0	0	#52(34h)	Read only	<a href="#">Table 112</a>

### 13.2.6 Secured SPI command

Some SPI commands must be secured to avoid unwanted change of the critical bits. The secured bits in the fail-safe machine and the main state machine are calculated from the data bits sent as follows:



**Table 21. Secured SPI**

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data 3	Data 2	Data 1	Data 0	Secure 3	Secure2	Secure 1	Secure 0

- Secure 3 = NOT(Bit5)
- Secure 2 = NOT(Bit4)
- Secure 1 = Bit7
- Secure 0 = Bit6

### 13.3 Detail of main logic register mapping

#### 13.3.1 INIT\_VREG

**Table 22. INIT\_VREG register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	0	0	1	P	ICCA_LIM	TCCA_LIM_OFF	IPFF_DIS	VCAN_OV_MON	0	TAUX_LIM_OFF	VAUX_TRK_EN	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	ICCA_LIM	TCCA_LIM_OFF	IPFF_DIS	VCAN_OV_MON	RES_ERVED	TAUX_LIM_OFF	VAUX_TRK_EN	BAT_FAIL
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	ICCA_LIM	TCCA_LIM_OFF	IPFF_DIS	VCAN_OV_MON	RES_ERVED	TAUX_LIM_OFF	VAUX_TRK_EN	BAT_FAIL

**Table 23. INIT\_VREG description and configuration of the bits (default value in bold)**

ICCA_LIM	Description	Configure the current limitation threshold for VCCA. Only available for external PNP.
	0	<b>ICCA_LIM_OUT</b>
	1	ICCA_LIM_INT
	Reset condition	Power on reset
TCCA_LIM_OFF	Description	Configure the current limitation duration before VCCA is switched off. Only available for external PNP.
	0	10 ms
	1	<b>50 ms</b>
	Reset condition	Power on reset
IPFF_DIS	Description	DISABLE the input power feed forward (IPFF) function of V <sub>PRE</sub>
	0	<b>Enabled</b>
	1	Disabled
	Reset condition	Power on reset

**Table 23. INIT\_VREG description and configuration of the bits (default value in bold) ...continued**

VCAN_OV_MON	Description	CAN_5V overvoltage monitoring
	<b>0</b>	<b>Off.</b> V <sub>CAN_OV</sub> is not monitored. Flag is ignored.
	1	On. V <sub>CAN_OV</sub> is monitored. If OV the CAN_5V regulator is switched off.
	Reset condition	Power on reset
TAUX_LIM_OFF	Description	Configure the current limitation duration before VAUX is switched off.
	0	10 ms
	<b>1</b>	<b>50 ms</b>
	Reset condition	Power on reset
VAUX_TRK_EN	Description	Configure VAUX regulator as a tracker of VCCA
	<b>0</b>	<b>NO tracking.</b>
	1	Tracking mode enabled and latched
	Reset condition	Power on reset
BAT_FAIL <sup>[1]</sup>	Description	Report a battery disconnection (POR of the main logic)
	0	NO POR
	<b>1</b>	<b>POR occurred</b>
	Reset condition	Power on reset
	Clear condition	Read

[1] **BAT\_FAIL** = POR\_M or V<sub>SUP\_UV\_L</sub> or BG\_OK (reset sources of main logic). BAT\_FAIL bit is cleared by a SPI read.

### 13.3.2 INIT\_WU1

**Table 24. INIT\_WU1 register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	0	1	0	P	WU_IO0_1	WU_IO0_0	WU_IO2_1	WU_IO2_0	WU_IO3_1	WU_IO3_0	WU_IO4_1	WU_IO4_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	WU_IO0_1	WU_IO0_0	WU_IO2_1	WU_IO2_0	WU_IO3_1	WU_IO3_0	WU_IO4_1	WU_IO4_0
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	WU_IO0_1	WU_IO0_0	WU_IO2_1	WU_IO2_0	WU_IO3_1	WU_IO3_0	WU_IO4_1	WU_IO4_0

**Table 25. INIT\_WU1 description and configuration of the bits (default value in bold)**

WU_IO0_1:0	Description	IO_0 wake-up configuration
	00	NO wake-up capability
	<b>01</b>	<b>Wake-up on rising edge - or high level</b>
	10	Wake-up on falling edge - or low level
	11	Wake-up on any edge
	Reset condition	Power on reset

**Table 25. INIT\_WU1 description and configuration of the bits (default value in bold)...continued**

WU_IO2_1:0	Description	IO_2 wake-up configuration
	<b>00</b>	<b>NO wake-up capability</b>
	01	Wake-up on rising edge - or high level
	10	Wake-up on falling edge - or low level
	11	Wake-up on any edge
	Reset condition	Power on reset
WU_IO3_1:0	Description	IO_3 wake-up configuration
	<b>00</b>	<b>NO wake-up capability</b>
	01	Wake-up on rising edge - or high level
	10	Wake-up on falling edge - or low level
	11	Wake-up on any edge
	Reset condition	Power on reset
WU_IO4_1:0	Description	IO_4 wake-up configuration
	<b>00</b>	<b>NO wake-up capability</b>
	01	Wake-up on rising edge - or high level
	10	Wake-up on falling edge - or low level
	11	Wake-up on any edge
	Reset condition	Power on reset

**13.3.3 INIT\_WU2**

**Table 26. INIT\_WU2 register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	0	1	1	P	WU_IO5_1	WU_IO5_0	CAN_DIS_CFG	CAN_WU_TO	0	LIN_J2602_DIS	LIN_SR_1	LIN_SR_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	WU_IO5_1	WU_IO5_0	CAN_DIS_CFG	CAN_WU_TO	RESERVED	LIN_J2602_DIS	LIN_SR_1	LIN_SR_0
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	WU_IO5_1	WU_IO5_0	CAN_DIS_CFG	CAN_WU_TO	RESERVED	LIN_J2602_DIS	LIN_SR_1	LIN_SR_0

**Table 27. INIT\_WU2 description and configuration of the bits (default value in bold)**

WU_IO5_1:0	Description	IO_5 wake-up configuration
	<b>00</b>	<b>NO wake-up capability</b>
	01	Wake-up on rising edge - or high level
	10	Wake-up on falling edge - or low level
	11	Wake-up on any edge
	Reset condition	Power on reset
CAN_DIS_CFG	Description	Define CAN behavior when FS1B is asserted low
	<b>0</b>	<b>CAN in RX only mode (when FS1B_CAN_IMPACT = 1 in INIT_FAULT register)</b>
	1	CAN in sleep mode (when FS1B_CAN_IMPACT = 1 in INIT_FAULT register)
Reset condition	Power on reset	
CAN_WU_TO	Description	Define the CAN wake-up timeout
	<b>0</b>	<b>120 µs</b>
	1	2.8 ms
Reset condition	Power on reset	
LIN_J2602_dis	Description	To comply with J2602 standard. Recessive mode when VSUP < 7.0 V
	<b>0</b>	<b>Compliant with J2602 standard</b>
	1	Not compliant with J2602 standard
Reset condition	Power on reset	
LIN_SR_1:0	Description	Configure the LIN slew rate
	<b>00</b>	<b>20 kbit/s</b>
	01	10 kbit/s
	1X	Fast baud rate (Max: 100 kbit/s)
Reset condition	Power on reset	

**13.3.4 INIT\_INT**

**Table 28. INIT\_INT register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	1	0	0	P	INT_DURATION	INT_INH_LIN	INT_INH_ALL	INT_INH_VSNS	INT_INH_VPRE	INT_INH_VCORE	INT_INH_VOTHER	INT_INH_CAN
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	INT_DURATION	INT_INH_LIN	INT_INH_ALL	INT_INH_VSNS	INT_INH_VPRE	INT_INH_VCORE	INT_INH_VOTHER	INT_INH_CAN
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	INT_DURATION	INT_INH_LIN	INT_INH_ALL	INT_INH_VSNS	INT_INH_VPRE	INT_INH_VCORE	INT_INH_VOTHER	INT_INH_CAN

Table 29. INIT\_INT description and configuration of the bits (default value in bold)

INT_DURATION	Description	Define the duration of the interrupt pulse
	<b>0</b>	<b>100 μs</b>
	1	25 μs
	Reset condition	Power on reset
INT_INH_LIN	Description	Inhibit the interrupt for LIN error bits
	<b>0</b>	<b>All INT sources</b>
	1	LIN error bits change INHIBITED
	Reset condition	Power on reset
INT_INH_ALL	Description	Inhibit ALL the interrupt
	<b>0</b>	<b>All INT sources</b>
	1	All INT inhibited
	Reset condition	Power on reset
INT_INH_VSNS	Description	Inhibit the interrupt for V <sub>SNS_UV</sub>
	<b>0</b>	<b>All INT sources</b>
	1	V <sub>SNS_UV</sub> INT inhibited
	Reset condition	Power on reset
INT_INH_VPRE	Description	Inhibit the interrupt for V <sub>PRE</sub> status event
	<b>0</b>	<b>All INT sources</b>
	1	V <sub>PRE</sub> status change inhibited
	Reset condition	Power on reset
INT_INH_VCORE	Description	Inhibit the interrupt for V <sub>CORE</sub> status event
	<b>0</b>	<b>All INT sources</b>
	1	V <sub>CORE</sub> status change inhibited
	Reset condition	Power on reset
INT_INH_VOTHER	Description	Inhibit the interrupt for V <sub>CCA</sub> /V <sub>AUX</sub> and V <sub>CAN</sub> status event
	<b>0</b>	<b>All INT sources</b>
	1	V <sub>CCA</sub> /V <sub>AUX</sub> /V <sub>CAN</sub> status change inhibited
	Reset condition	Power on reset
INT_INH_CAN	Description	Inhibit the interrupt for CAN error bits
	<b>0</b>	<b>All INT sources</b>
	1	CAN error bits change inhibited
	Reset condition	Power on reset

13.3.5 INIT\_INH\_INT

Table 30. INIT\_INH\_INT register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	1	0	1	P	0	0	0	INT_INH_5	INT_INH_4	INT_INH_3	INT_INH_2	INT_INH_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	RES_ERVED	RES_ERVED	RES_ERVED	INT_INH_5	INT_INH_4	INT_INH_3	INT_INH_2	INT_INH_0
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	RES_ERVED	RES_ERVED	RES_ERVED	INT_INH_5	INT_INH_4	INT_INH_3	INT_INH_2	INT_INH_0

Table 31. INIT IO\_WU2 description and configuration of the bits (default value in bold)

INT_INH_5	Description	Inhibit the interrupt pulse for IO_5 (masked in IO_G)
	<b>0</b>	<b>INT not masked</b>
	1	INT masked
	Reset condition	Power on reset
INT_INH_4	Description	Inhibit the interrupt pulse for IO_4 (masked in IO_G)
	<b>0</b>	<b>INT not masked</b>
	1	INT masked
	Reset condition	Power on reset
INT_INH_3	Description	Inhibit the interrupt pulse for IO_3 (masked in IO_G)
	0	INT not masked
	<b>1</b>	<b>INT masked</b>
	Reset condition	Power on reset
INT_INH_2	Description	Inhibit the interrupt pulse for IO_2 (masked in IO_G)
	0	INT not masked
	<b>1</b>	<b>INT masked</b>
	Reset condition	Power on reset
INT_INH_0	Description	Inhibit the interrupt pulse for IO_0 (masked in IO_G)
	<b>0</b>	<b>INT not masked</b>
	1	INT masked
	Reset condition	Power on reset

13.3.6 LONG\_DURATION\_TIMER

Table 32. LONG\_DURATION\_TIMER register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	1	1	0	P	F2	F1	F0	REG_SE	0	MODE	LDT_ENABLE	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	F2	F1	F0	REG_SE	LDT_RUNNING	MODE	LDT_ENABLE	LDT_INT

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	F2	F1	F0	REG_SE	LDT_RUNNING	MODE	LDT_ENABLE	LDT_INT

Table 33. LONG\_DURATION\_TIMER description and configuration of the bits (default value in bold)

F2:F0	Description	Select timer operating function
	000	<b>Function 1: in normal mode count and generate flag or INT when counter reaches the after run value.</b>
	001	Function 2: in normal mode count until after run value is reached, then enters in LPOFF.
	010	Function 3: in normal mode count until after run value is reached, then enters in LPOFF. Once in LPOFF, count until wake-up value is reached and wake-up.
	011	Function 4: in LPOFF, count until wake-up value is reached and wake-up.
	100	Function 5: in LPOFF, count and do not wake-up. Counter value is stored in wake-up register.
	101... 111	N/A
	Reset condition	Power on reset
REG_SE	Description	Counter register selection
	0	<b>Read programmed wake-up register</b>
	1	Read real time counter into wake-up register (after counter is stopped with LDT_ENABLE bit)
Reset condition	Power on reset	
MODE	Description	Operating mode selection
	0	Calibration mode (488 μs resolution)
	1	<b>Normal mode (1 s resolution)</b>
	Reset condition	Power on reset
LDT_ENABLE	Description	LDT counter control
	0	<b>LDT counter stop</b>
	1	LDT counter start
	Reset condition	Power on reset

**Table 33. LONG\_DURATION\_TIMER description and configuration of the bits (default value in bold)...***continued*

LDT_RUNNING	Description	Counter status
	<b>0</b>	<b>Counter not running</b>
	1	Counter running
	Reset condition	Power on reset
LDT_INT	Description	Counter interrupt generation when function 1 is selected
	<b>0</b>	<b>No INT generated</b>
	1	INT generated when counter reach after run value
	Reset condition	Power on reset/read

**13.3.7 HW\_CONFIG**

**Table 34. HW\_CONFIG register description**

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOOTHERS_G	LS_DETECT	RESERVED	VCCA_PNP_DET	VCCA_HW	VAUX_HW	1	DFS_HW1	DBG_HW

**Table 35. HW\_CONFIG description and configuration of the bits (default value in bold)**

LS_DETECT	Description	Report the hardware configuration of V <sub>PRE</sub>
	<b>0</b>	Buck-boost
	1	Buck only
	Reset condition	Power on reset/refresh after LPOFF
VCCA_PNP_DET	Description	Report the connection of an external PNP on V <sub>CCA</sub>
	<b>0</b>	External PNP connected
	1	Internal MOSFET
	Reset condition	Power on reset/refresh after LPOFF
VCCA_HW	Description	Report the hardware configuration for V <sub>CCA</sub>
	<b>0</b>	3.3 V
	1	5.0 V
	Reset condition	Power on reset/refresh after LPOFF
VAUX_HW	Description	Report the hardware configuration for V <sub>AUX</sub>
	<b>0</b>	5.0 V
	1	3.3 V
	Reset condition	Power on reset/refresh after LPOFF
DFS_HW1	Description	Report the deep fail-safe hardware configuration (main logic)
	<b>0</b>	Deep fail-safe disable
	1	Deep fail-safe enable
	Reset condition	Power on reset/refresh after LPOFF



Table 35. HW\_CONFIG description and configuration of the bits (default value in bold)...continued

DBG_HW	Description	Report the configuration of the DEBUG mode
	0	Normal operation
	1	Debug mode selected
	Reset condition	Power on reset/refresh after LPOFF

13.3.8 WU\_SOURCE

Table 36. WU\_SOURCE register description

Read	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	IO_5_WU	IO_4_WU	IO_3_WU	IO_2_WU	IO_0_WU	AUTO_WU	LDT_WU	PHY_WU

Table 37. WU\_SOURCE description and configuration of the bits (default value in bold)

IO_5_WU	Description	Report a wake-up event from IO_5
	0	<b>No wake-up</b>
	1	Wake-up event detected
	Reset condition	Power on reset/read
IO_4_WU	Description	Report a wake-up event from IO_4
	0	<b>No wake-up</b>
	1	Wake-up event detected
	Reset condition	Power on reset/read
IO_3_WU	Description	Report a wake-up event from IO_3
	0	<b>No wake-up</b>
	1	Wake-up event detected
	Reset condition	Power on reset/read
IO_2_WU	Description	Report a wake-up event from IO_2
	0	<b>No wake-up</b>
	1	Wake-up event detected
	Reset condition	Power on reset/read
IO_0_WU	Description	Report a wake-up event from IO_0
	0	<b>No wake-up</b>
	1	Wake-up event detected
	Reset condition	Power on reset/read
AUTO_WU	Description	Report an automatic wake-up event
	0	<b>No wake-up</b>
	1	Wake-up event detected
	Reset condition	Power on reset/read

**Table 37. WU\_SOURCE description and configuration of the bits (default value in bold)...continued**

LDT_WU	Description	Report a wake-up event from long duration timer
	<b>0</b>	<b>No wake-up</b>
	1	Wake-up event detected
	Reset condition	Power on reset/read
PHY_WU	Description	Report a wake-up event from CAN or LIN
	<b>0</b>	<b>No wake-up</b>
	1	Wake-up event detected
	Reset condition	Power on reset/read CAN_WU or/and LIN_WU

**13.3.9 DEVICE\_ID**

**Table 38. DEVICE\_ID register description**

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	VCORE_1	VCORE_0	PHY_1	PHY_0	VKAM	DEV_REV_2	DEV_REV_1	DEV_REV_0

**Table 39. DEVICE\_ID description and configuration of the bits (default value in bold)**

VCORE_1:0	Description	VCORE current capability
	00	1.5 A
	01	0.8 A
	10	0.5 A
	11	2.2 A
	Reset condition	Power on reset
PHY_1:0	Description	CAN or LIN physical layer
	00	No CAN, no LIN
	01	CAN only
	10	LIN only
	11	CAN and LIN
	Reset condition	Power on reset
VKAM	Description	VKAM supply
	0	VKAM off by default
	1	VKAM on by default
	Reset condition	Power on reset

**Table 39. DEVICE\_ID description and configuration of the bits (default value in bold)...continued**

DEV_REV_2:0	Description	Device silicon revision
	000	Silicon Rev. xxx
	...	- For ASIL D devices, DEV_REV_2:0 = 010 - For ASIL B devices, DEV_REV_2:0 = 111;
	111	
	Reset condition	Power on reset

**13.3.10 IO\_INPUT**

**Table 40. IO\_INPUT register description**

Read	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPL_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	IO_5	IO_4	0	IO_3	IO_2	0	0	IO_0

**Table 41. IO\_INPUT description and configuration of the bits**

IO_5	Description	Report IO_5 digital state in normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power on reset/read
IO_4	Description	Report IO_4 digital state in normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power on reset/read
IO_3	Description	Report IO_3 digital state in normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power on reset/read
IO_2	Description	Report IO_2 digital state in normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power on reset/read
IO_0	Description	Report IO_0 digital state in normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power on reset/read

13.3.11 DIAG\_VPRE

Table 42. DIAG\_VPRE register description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	BoB	VPRE_STATE	TWARN_PRE	TSD_PRE	VPRE_OV	VPRE_UV	ILIM_PRE	0

Table 43. DIAG\_VPRE description and configuration of the bits (default value in bold)

BoB	Description	Report a running mode of V <sub>PRE</sub>
	0	<b>Buck</b>
	1	Boost
	Reset condition	Power on reset
VPRE_STATE	Description	Report the activation state of V <sub>PRE</sub> SMPS
	0	SMPS off
	1	<b>SMPS on</b>
	Reset condition	Power on reset
TWARN_PRE	Description	Report a thermal warning from V <sub>PRE</sub>
	0	<b>No thermal warning (T<sub>J</sub> &lt; T<sub>WARN_PRE</sub>)</b>
	1	Thermal warning (T <sub>J</sub> > T <sub>WARN_PRE</sub> )
	Reset condition	Power on reset/read
TSD_PRE	Description	Thermal shutdown of V <sub>PRE</sub>
	0	<b>No TSD (T<sub>J</sub> &lt; T<sub>SD_PRE</sub>)</b>
	1	TSD occurred (T <sub>J</sub> > T <sub>SD_PRE</sub> )
	Reset condition	Power on reset/read
VPRE_OV	Description	V <sub>PRE</sub> overvoltage detection
	0	<b>No overvoltage (V<sub>PRE</sub> &lt; V<sub>PRE_OV</sub>)</b>
	1	Overvoltage detected (V <sub>PRE</sub> > V <sub>PRE_OV</sub> )
	Reset condition	Power on reset/read
VPRE_UV	Description	V <sub>PRE</sub> undervoltage detection
	0	No undervoltage (V <sub>PRE</sub> > V <sub>PRE_UV</sub> )
	1	<b>Undervoltage detected (V<sub>PRE</sub> &lt; V<sub>PRE_UV</sub>)</b>
	Reset condition	Power on reset/read
ILIM_PRE	Description	Report a current limitation condition on V <sub>PRE</sub>
	0	<b>No current limitation (I<sub>PRE_PK</sub> &lt; I<sub>PRE_LIM</sub>)</b>
	1	Current limitation (I <sub>PRE_PK</sub> > I <sub>PRE_LIM</sub> )
	Reset condition	Power on reset/read

**13.3.12 DIAG\_VCORE**

**Table 44. DIAG\_VCORE register description**

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	0	VCORE_STATE	TWARN_CORE	TSD_CORE	VCORE_FB_OV	VCORE_FB_UV	0	0

**Table 45. DIAG\_VCORE description and configuration of the bits (default value in bold)**

VCORE_STATE	Description	Report the activation state of $V_{CORE}$ SMPS
	0	SMPS off
	<b>1</b>	<b>SMPS on</b>
	Reset condition	Power on reset
TWARN_CORE	Description	Report a thermal warning from $V_{CORE}$
	<b>0</b>	<b>No thermal warning (<math>T_J &lt; T_{WARN\_CORE}</math>)</b>
	1	Thermal warning ( $T_J > T_{WARN\_CORE}$ )
	Reset condition	Power on reset/read
TSD_CORE	Description	Thermal shutdown of $V_{CORE}$
	<b>0</b>	<b>No TSD (<math>T_J &lt; T_{SD\_CORE}</math>)</b>
	1	TSD occurred ( $T_J > T_{SD\_CORE}$ )
	Reset condition	Power on reset/read
VCORE_FB_OV	Description	$V_{CORE}$ overvoltage detection
	<b>0</b>	<b>No overvoltage (<math>V_{CORE\_FB} &lt; V_{CORE\_FB\_OV}</math>)</b>
	1	Overvoltage detected ( $V_{CORE\_FB} > V_{CORE\_FB\_OV}$ )
	Reset condition	Power on reset/read
VCORE_FB_UV	Description	$V_{CORE}$ undervoltage detection
	0	No undervoltage ( $V_{CORE\_FB} > V_{CORE\_FB\_UV}$ )
	<b>1</b>	<b>Undervoltage (<math>V_{CORE\_FB} &lt; V_{CORE\_FB\_UV}</math>)</b>
	Reset condition	Power on reset/read

**13.3.13 DIAG\_VCCA**

**Table 46. DIAG\_VCCA register description**

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	0	0	TWARN_CCA	TSD_CCA	VCCA_OV	VCCA_UV	ILIM_CCA	ILIM_CCA_OFF

**Table 47. DIAG\_VCCA description and configuration of the bits (default value in bold)**

TWARN_CCA	Description	Report a thermal warning from V <sub>CCA</sub> . Available only for internal pass MOSFET
	<b>0</b>	<b>No thermal warning</b> ( $T_J < T_{WARN\_CCA}$ )
	1	Thermal warning ( $T_J > T_{WARN\_CCA}$ )
	Reset condition	Power on reset/read
TSD_CCA	Description	Thermal shutdown of V <sub>CCA</sub>
	<b>0</b>	<b>NO TSD</b> ( $T_J < T_{SD\_CCA}$ )
	1	TSD occurred ( $T_J > T_{SD\_CCA}$ )
	Reset condition	Power on reset/read
VCCA_OV	Description	V <sub>CCA</sub> overvoltage detection
	<b>0</b>	<b>No overvoltage</b> ( $V_{CCA} < V_{CCA\_OV}$ )
	1	Overvoltage detected ( $V_{CCA} > V_{CCA\_OV}$ )
	Reset condition	Power on reset/read
VCCA_UV	Description	V <sub>CCA</sub> undervoltage detection
	0	No undervoltage ( $V_{CCA} > V_{CCA\_UV}$ )
	<b>1</b>	<b>Undervoltage detected</b> ( $V_{CCA} < V_{CCA\_UV}$ )
	Reset condition	Power on reset/read
ILIM_CCA	Description	Report a current limitation condition on V <sub>CCA</sub>
	<b>0</b>	<b>No current limitation</b> ( $I_{CCA} < I_{CCA\_LIM}$ )
	1	Current limitation ( $I_{CCA} > I_{CCA\_LIM}$ )
	Reset condition	Power on reset/read
ILIM_CCA_OFF	Description	Maximum current limitation duration. Available only when an external PNP is connected
	<b>0</b>	<b>T<sub>LIMITATION</sub> &lt; T<sub>CCA_LIM_OFF</sub></b>
	1	T <sub>LIMITATION</sub> > T <sub>CCA_LIM_OFF</sub>
	Reset condition	Power on reset/read

**13.3.14 DIAG\_VAUX**

**Table 48. DIAG\_VAUX register description**

Read	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0
MISO	SPL_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	0	0	0	TSD_AUX	VAUX_OV	VAUX_UV	ILIM_AUX	ILIM_AUX_OFF

**Table 49. DIAG\_VAUX description and configuration of the bits (default value in bold)**

TSD_AUX	Description	Thermal shutdown of $V_{AUX}$
	<b>0</b>	<b>No TSD</b> ( $T_J < T_{SD\_AUX}$ )
	1	TSD occurred ( $T_J > T_{SD\_AUX}$ )
	Reset condition	Power on reset/read
VAUX_OV	Description	$V_{AUX}$ overvoltage detection
	<b>0</b>	<b>No overvoltage</b> ( $V_{AUX} < V_{AUX\_OV}$ )
	1	Overvoltage detected ( $V_{AUX} > V_{AUX\_OV}$ )
	Reset condition	Power on reset/read
VAUX_UV	Description	$V_{AUX}$ undervoltage detection
	0	No undervoltage ( $V_{AUX} > V_{AUX\_UV}$ )
	<b>1</b>	<b>Undervoltage detected</b> ( $V_{AUX} < V_{AUX\_UV}$ )
	Reset condition	Power on reset/read
ILIM_AUX	Description	Report a current limitation condition on $V_{AUX}$
	<b>0</b>	<b>No current limitation</b> ( $I_{AUX} < I_{AUX\_LIM}$ )
	1	Current limitation ( $I_{AUX} > I_{AUX\_LIM}$ )
	Reset condition	Power on reset/read
ILIM_AUX_OFF	Description	Maximum current limitation duration
	<b>0</b>	$T_{LIMITATION} < T_{AUX\_LIM\_OFF}$
	1	$T_{LIMITATION} > T_{AUX\_LIM\_OFF}$
	Reset condition	Power on reset/read

**13.3.15 DIAG\_VSUP\_VCAN**

**Table 50. DIAG\_VSUP\_VCAN register description**

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPL_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	VSNS_UV	VSUP_UV_7	IPFF	TSD_CAN	VCAN_OV	VCAN_UV	ILIM_CAN	0

**Table 51. DIAG\_VSUP\_VCAN description and configuration of the bits (default value in bold)**

VSNS_UV	Description	Detection of battery voltage below $V_{SNS\_UV}$
	0	$V_{BAT} > V_{SNS\_UV}$
	<b>1</b>	<b><math>V_{BAT} &lt; V_{SNS\_UV}</math></b>
	Reset condition	Power on reset/read
VSUP_UV_7	Description	Detection of $V_{SUP}$ below $V_{SUP\_UV\_7}$
	0	$V_{SUP} > V_{SUP\_UV\_7}$
	<b>1</b>	<b><math>V_{SUP} &lt; V_{SUP\_UV\_7}</math></b>
	Reset condition	Power on reset/read

**Table 51. DIAG\_VSUP\_VCAN description and configuration of the bits (default value in bold)...continued**

IPFF	Description	Input power feed forward (IPFF)
	<b>0</b>	<b>Normal operation</b>
	1	IPFF mode activated
	Reset condition	Power on reset/read
TSD_CAN	Description	Thermal shutdown of V <sub>CAN</sub>
	<b>0</b>	<b>NO TSD (T<sub>J</sub> &lt; T<sub>SD_CAN</sub>)</b>
	1	TSD occurred (T <sub>J</sub> > T <sub>SD_CAN</sub> )
	Reset condition	Power on reset/read
VCAN_OV	Description	V <sub>CAN</sub> overvoltage detection
	<b>0</b>	<b>No overvoltage (V<sub>CAN</sub> &lt; V<sub>CAN_OV</sub>)</b>
	1	Overvoltage detected (V <sub>CAN</sub> > V <sub>CAN_OV</sub> )
	Reset condition	Power on reset/read
VCAN_UV	Description	V <sub>CAN</sub> undervoltage detection
	0	No undervoltage (V <sub>CAN</sub> > V <sub>CAN_UV</sub> )
	<b>1</b>	<b>Undervoltage detected (V<sub>CAN</sub> &lt; V<sub>CAN_UV</sub>)</b>
	Reset condition	Power on reset/read
ILIM_CAN	Description	Report a current limitation condition on V <sub>CAN</sub>
	<b>0</b>	<b>No current limitation (I<sub>CAN</sub> &lt; I<sub>CAN_LIM</sub>)</b>
	1	Current limitation (I <sub>CAN</sub> > I <sub>CAN_LIM</sub> )
	Reset condition	Power on reset/read

**13.3.16 DIAG\_CAN\_FD**

**Table 52. DIAG\_CAN\_FD register description**

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPL_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	CANH_BATT	CANH_GND	CANL_BATT	CANL_GND	CAN_DOM	0	RXD_REC	TXD_DOM

**Table 53. DIAG\_CAN\_FD description and configuration of the bits (default value in bold)**

CANH_BATT	Description	CANH short-circuit to battery detection
	<b>0</b>	<b>No failure</b>
	1	Failure detected
	Reset condition	Power on reset/read
CANH_GND	Description	CANH short-circuit to GND detection
	<b>0</b>	<b>No failure</b>
	1	Failure detected
	Reset condition	Power on reset/read



**Table 53. DIAG\_CAN\_FD description and configuration of the bits (default value in bold)...continued**

CANL_BATT	Description	CANL short-circuit to battery detection
	<b>0</b>	<b>No failure</b>
	1	Failure detected
	Reset condition	Power on reset/read
CANL_GND	Description	CANL short-circuit to GND detection
	<b>0</b>	<b>No failure</b>
	1	Failure detected
	Reset condition	Power on reset/read
CAN_DOM	Description	CAN-bus dominant clamping detection
	<b>0</b>	<b>No failure</b>
	1	Failure detected
	Reset condition	Power on reset/read
RXD_REC	Description	RXD recessive clamping detection (short-circuit to 5.0 V)
	<b>0</b>	<b>No failure</b>
	1	Failure detected
	Reset condition	Power on reset/read
TXD_DOM	Description	TXD dominant clamping detection (short-circuit to GND)
	<b>0</b>	<b>No failure</b>
	1	Failure detected
	Reset condition	Power on reset/read

**13.3.17 DIAG\_CAN\_LIN**

**Table 54. DIAG\_CAN\_LIN register description**

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPL_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	LIN_DOM	TXDL_DOM	0	RXDL_REC	LIN_OT	0	CAN_OT	CAN_OC

**Table 55. DIAG\_CAN\_LIN description and configuration of the bits (default value in bold)**

LIN_DOM	Description	LIN bus dominant clamping detection
	<b>0</b>	<b>No failure</b>
	1	Failure detected
	Reset condition	Power on reset/read
TXDL_DOM	Description	LIN TXD dominant clamping detection (short-circuit to GND)
	<b>0</b>	<b>No failure</b>
	1	Failure detected
	Reset condition	Power on reset/read

**Table 55. DIAG\_CAN\_LIN description and configuration of the bits (default value in bold)...continued**

RXDL_REC	Description	LIN RXD recessive clamping detection (short-circuit to 5.0 V)
	<b>0</b>	<b>No failure</b>
	1	Failure detected
	Reset condition	Power on reset/read
LIN_OT	Description	LIN overtemperature detection
	<b>0</b>	<b>No failure</b>
	1	Failure detected
	Reset condition	Power on reset/read
CAN_OT	Description	CAN overtemperature detection
	<b>0</b>	<b>No failure</b>
	1	Failure detected
	Reset condition	Power on reset/read
CAN_OC	Description	CAN overcurrent detection
	<b>0</b>	<b>No failure</b>
	1	Failure detected
	Reset condition	Power on reset/read

**13.3.18 DIAG\_SPI**

**Table 56. DIAG\_SPI register description**

Read	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_ERR	0	SPI_CLK	0	SPI_REQ	0	SPI_PARITY	0

**Table 57. DIAG\_SPI description and configuration of the bits (default value in blue)**

SPI_ERR	Description	Secured SPI communication check
	<b>0</b>	<b>No error</b>
	1	Error detected in the secured bits
	Reset condition	Power on reset/read
SPI_CLK	Description	SCLK error detection
	<b>0</b>	<b>16 clock cycles during NCS low</b>
	1	Wrong number of clock cycles (<16 or > 16)
	Reset condition	Power on reset/read
SPI_REQ	Description	Invalid SPI access (wrong write or read, write to INIT registers in normal mode, wrong address)
	<b>0</b>	<b>No error</b>
	1	SPI violation
	Reset condition	Power on reset/read

**Table 57. DIAG\_SPI description and configuration of the bits (default value in blue)...continued**

SPI_PARITY	Description	SPI parity bit error detection
	<b>0</b>	<b>Parity bit OK</b>
	1	Parity bit error
	Reset condition	Power on reset/read

**13.3.19 Mode**

**Table 58. Mode register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	0	1	0	1	P	VKAM_EN	LPOFF_AUTO_WU	GO_LPOFF	INT_REQ	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	VKAM_EN	RESERVED	RESERVED	RESERVED	INIT	NORMAL	DFS	LPOFF
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	VKAM_EN	RESERVED	RESERVED	RESERVED	INIT	NORMAL	DFS	LPOFF

**Table 59. Mode description and configuration of the bits (default value in bold)**

VKAM_EN	Description	V <sub>KAM</sub> control (default state depends on part number)
	<b>0</b>	<b>DISABLED</b>
	1	ENABLED
	Reset condition	Power on reset
LPOFF_AUTO_WU	Description	Configure the device in LPOFF_AUTO_WU
	<b>0</b>	<b>No action</b>
	1	Go to LPOFF mode and wake-up automatically after 1.0 ms
	Reset condition	Power on reset/refresh after LPOFF
GO_LPOFF	Description	Configure the device in LPOFF-SLEEP
	<b>0</b>	<b>No action</b>
	1	Go to LPOFF mode and wait for wake-up event
	Reset condition	Power on reset/refresh after LPOFF
INT_REQ	Description	Request for an INT pulse
	<b>0</b>	<b>No Request</b>
	1	Request for an INT pulse
	Reset condition	Power on reset
INIT	Description	Report if INIT mode of the main logic state machine is entered
	<b>0</b>	<b>Not in INIT mode</b>
	<b>1</b>	<b>INIT mode</b>
	Reset condition	Power on reset

**Table 59. Mode description and configuration of the bits (default value in bold)...continued**

NORMAL	Description	Report if normal mode of the main logic state machine is entered
	<b>0</b>	<b>Not in normal mode</b>
	1	Normal mode
	Reset condition	Power on reset
DFS	Description	Report if the device resumes from deep fail-safe mode
	<b>0</b>	<b>Not in deep fail-safe</b>
	1	Resume from deep fail-safe
	Reset condition	Power on reset/read
LPOFF	Description	Report if the device resumes from LPOFF-sleep or LPOFF_AUTO_WU mode
	<b>0</b>	<b>Not in LPOFF</b>
	1	Resume from LPOFF
	Reset condition	Power on reset/read
Secure 3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

**13.3.20 REG\_MODE**

**Table 60. REG\_MODE register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	0	1	1	0	P	VCORE_EN	VCCA_EN	VAUX_EN	VCAN_EN	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	RES_ERVED	RES_ERVED	RES_ERVED	RES_ERVED	VCORE_EN	VCCA_EN	VAUX_EN	VCAN_EN
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	RES_ERVED	RES_ERVED	RES_ERVED	RES_ERVED	VCORE_EN	VCCA_EN	VAUX_EN	VCAN_EN

**Table 61. REG\_MODE description and configuration of the bits (default value in bold)**

VCORE_EN	Description	V <sub>CORE</sub> control (switch off not recommended if V <sub>CORE</sub> is safety critical)
	<b>0</b>	Disabled
	<b>1</b>	<b>Enabled</b>
	Reset condition	Power on reset
VCCA_EN	Description	V <sub>CCA</sub> control (switch off not recommended if V <sub>CCA</sub> is safety critical)
	<b>0</b>	Disabled
	<b>1</b>	<b>Enabled</b>
	Reset condition	Power on reset

**Table 61. REG\_MODE description and configuration of the bits (default value in bold)...***continued*

VAUX_EN	Description	V <sub>AUX</sub> control (switch off not recommended if V <sub>AUX</sub> is safety critical)
	0	Disabled
	<b>1</b>	<b>Enabled</b>
	Reset condition	Power on reset
VCAN_EN	Description	V <sub>CAN</sub> control
	0	Disabled
	<b>1</b>	<b>Enabled</b>
	Reset condition	Power on reset
Secure 3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

**13.3.21 IO\_OUT\_AMUX**

**Table 62. IO\_OUT\_AMUX register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	0	1	1	1	P	IO_OUT_4_EN	IO_OUT_4	0	0	0	AMUX_2	AMUX_1	AMUX_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	IO_OUT_4_EN	IO_OUT_4	RES_ERVED	RES_ERVED	RES_ERVED	AMUX_2	AMUX_1	AMUX_0
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	IO_OUT_4_EN	IO_OUT_4	RES_ERVED	RES_ERVED	RES_ERVED	AMUX_2	AMUX_1	AMUX_0

**Table 63. IO\_OUT\_AMUX description and configuration of the bits (default value in bold)**

IO_OUT_4_EN	Description	Enable the output gate driver capability for IO_4
	<b>0</b>	<b>High-impedance (IO_4 configured as input)</b>
	1	Enabled (IO_4 configured as output gate driver)
	Reset condition	Power on reset
IO_OUT_4	Description	Configure IO_4 output gate driver state
	<b>0</b>	<b>Low</b>
	1	High
	Reset condition	Power on reset

**Table 63. IO\_OUT\_AMUX description and configuration of the bits (default value in bold)...continued**

AMUX_2:0	Description	Select AMUX output
	<b>000</b>	<b>V<sub>REF</sub></b>
	001	V <sub>SNS</sub> wide range
	010	IO_0 wide range
	011	IO_5 wide range
	100	V <sub>SNS</sub> tight range
	101	IO_0 tight range
	110	IO_5 tight range/VKAM
	111	Die Temperature Sensor
	Reset condition	Power on reset

**13.3.22 CAN\_LIN\_MODE**

**Table 64. CAN\_LIN\_MODE register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	1	0	0	0	P	CAN_MODE_1	CAN_MODE_0	CAN_AUTO_DIS	LIN_MODE_1	LIN_MODE_0	LIN_AUTO_DIS	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	CAN_MODE_1	CAN_MODE_0	CAN_AUTO_DIS	LIN_MODE_1	LIN_MODE_0	LIN_AUTO_DIS	CAN_WU	LIN_WU
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	CAN_MODE_1	CAN_MODE_0	CAN_AUTO_DIS	LIN_MODE_1	LIN_MODE_0	LIN_AUTO_DIS	CAN_WU	LIN_WU

**Table 65. CAN\_LIN\_MODE description and configuration of the bits (default value in bold)**

CAN_MODE_1:0 <sup>[1]</sup>	Description	Configure the CAN mode
	00	Sleep/no wake-up capability
	01	Listen only
	<b>10</b>	<b>Sleep/wake-up capability</b>
	11	Normal operation mode
	Reset condition	Power on reset
CAN_AUTO_DIS	Description	Automatic CAN TX disable
	0	NO auto disable
	<b>1</b>	<b>Reset CAN_MODE from '11' to '01' on CAN_OT or TXD_DOM or RXD_REC event</b>
	Reset condition	Power on reset

**Table 65. CAN\_LIN\_MODE description and configuration of the bits (default value in bold)...continued**

LIN_MODE_1:0	Description	Configure the LIN mode
	00	Sleep/no wake-up capability
	01	Listen only
	<b>10</b>	<b>Sleep/wake-up capability</b>
	11	Normal operation mode
	Reset condition	Power on reset
LIN_AUTO_DIS	Description	Automatic LIN mode disable
	0	No auto disable
	<b>1</b>	<b>Reset LIN_mode from '11' to '01' on LIN_OT or TXDL_DOM or RXDL_REC event</b>
	Reset condition	Power on reset
CAN_WU	Description	Report a wake-up event from the CAN
	<b>0</b>	<b>No wake-up</b>
	1	Wake-up detected
	Reset condition	Power on reset/read
LIN_WU	Description	Report a wake-up event from the LIN
	<b>0</b>	<b>No wake-up</b>
	1	Wake-up detected
	Reset condition	Power on reset/read

[1] CAN mode is automatically configured to 'sleep + wake-up capability[10]' if CAN mode was different than 'sleep + no wake-up capability [00]' before the device enters in LPOFF. After LPOFF, the initial CAN mode prior to enter LPOFF is restored.

### 13.3.23 LDT\_AFTER\_RUN\_1

**Table 66. LDT\_AFTER\_RUN\_1 register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	1	0	1	0	P	B15	B14	B13	B12	B11	B10	B9	B8
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B15	B14	B13	B12	B11	B10	B9	B8
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B15	B14	B13	B12	B11	B10	B9	B8

**Table 67. LDT\_AFTER\_RUN\_1 description and configuration of the bits (default value in bold)**

B15:8	Description	Long duration timer - after run value
	00 to FF	After run value (8 most significant bits)
	Reset condition	Power on reset

**13.3.24 LDT\_AFTER\_RUN\_2**

**Table 68. LDT\_AFTER\_RUN\_2 register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	1	0	1	1	P	B7	B6	B5	B4	B3	B2	B1	B0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B7	B6	B5	B4	B3	B2	B1	B0
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B7	B6	B5	B4	B3	B2	B1	B0

**Table 69. LDT\_AFTER\_RUN\_2 description and configuration of the bits (default value in bold)**

B7:0	Description	Long duration timer - after run value
	00 to FF	After run value (8 least significant bits)
	Reset condition	Power on reset

**13.3.25 LDT\_WAKE\_UP\_1**

**Table 70. LDT\_WAKE\_UP\_1 register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	1	1	0	0	P	B23	B22	B21	B20	B19	B18	B17	B16
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B23	B22	B21	B20	B19	B18	B17	B16
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B23	B22	B21	B20	B19	B18	B17	B16

**Table 71. LDT\_WAKE\_UP\_1 description and configuration of the bits (default value in bold)**

B23:16	Description	Long duration timer – wake-up value
	00 to FF	Wake-up value (8 most significant bits)
	Reset condition	Power on reset

**13.3.26 LDT\_WAKE\_UP\_2**

**Table 72. LDT\_WAKE\_UP\_2 register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	1	1	0	1	P	B15	B14	B13	B12	B11	B10	B9	B8
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B15	B14	B13	B12	B11	B10	B9	B8



Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B15	B14	B13	B12	B11	B10	B9	B8

**Table 73. LDT\_WAKE\_UP\_2 description and configuration of the bits (default value in bold)**

B15:8	Description	Long duration timer – wake-up value
	00 to FF	Wake-up value (8 intermediate bits)
	Reset condition	Power on reset

**13.3.27 LDT\_WAKE\_UP\_3**

**Table 74. LDT\_WAKE\_UP\_3 register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	1	1	1	0	P	B7	B6	B5	B4	B3	B2	B1	B0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B7	B6	B5	B4	B3	B2	B1	B0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B7	B6	B5	B4	B3	B2	B1	B0

**Table 75. LDT\_WAKE\_UP\_3 description and configuration of the bits (default value in bold)**

B7:0	Description	Long duration timer – wake-up value
	00 to FF	Wake-up value (8 least significant bits)
	Reset condition	Power on reset

**13.4 Detail of fail-safe logic register mapping**

**13.4.1 INIT\_FS1B\_TIMING**

**Table 76. INIT\_FS1B\_TIMING register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	0	0	1	p	FS1B_TIME_3	FS1B_TIME_2	FS1B_TIME_1	FS1B_TIME_0	SECURE_3	SECURE_2	SECURE_1	SECURE_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	FS1B_TIME_3	FS1B_TIME_2	FS1B_TIME_1	FS1B_TIME_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	FS1B_TIME_3	FS1B_TIME_2	FS1B_TIME_1	FS1B_TIME_0

**Table 77. INIT\_FS1B\_TIMING. Description and configuration of the bits (Default value in bold)**

FS1B_TIME_3:0 (timing made with fail-safe oscillator)	Description	FS1B timing range factor x1 (FS1B_TIME_RANGE bit = 0)	FS1B timing range factor x8 (FS1B_TIME_RANGE bit = 1)
	0000	0	0
	0001	10 ms	80 ms
	0010	13 ms	104 ms
	0011	17 ms	135 ms
	0100	22 ms	176 ms
	0101	29 ms	228 ms
	<b>0110</b>	<b>37 ms</b>	297 ms
	0111	48 ms	386 ms
	1000	63 ms	502 ms
	1001	82 ms	653 ms
	1010	106 ms	848 ms
	1011	138 ms	1103 ms
	1100	179 ms	1434 ms
	1101	233 ms	1864 ms
	1110	303 ms	2423 ms
	1111	394 ms	3150 ms
Reset condition	Power on reset		
Secure3:0	Description	Secured bits based on write bits	
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6	

**13.4.2 BIST**

**Table 78. BIST register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	0	1	0	P	0	ABIST2_FS1B	ABIST2_VAUX	0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	RES_ERVED	ABIST2_FS1B_OK	ABIST2_VAUX_OK	ABIST1_OK
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	RES_ERVED	ABIST2_FS1B_OK	ABIST2_VAUX_OK	ABIST1_OK

**Table 79. BIST description and configuration of the bits (default value in bold)**

ABIST2_FS1B	Description	Request ABIST execution on FS1B
	<b>0</b>	<b>No action</b>
	1	Launch ABIST on FS1B
	Reset condition	Fail-safe power-on-reset
ABIST2_VAUX	Description	Request ABIST execution on VAUX
	<b>0</b>	<b>No action</b>
	1	Launch ABIST on VAUX
	Reset condition	Fail-safe power-on-reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6
ABIST2_FS1B_OK	Description	Diagnostic of FS1B Analog BIST2 (executed on demand)
	<b>0</b>	<b>FS1B ABIST fail or not executed</b>
	1	FS1B ABIST pass
	Reset condition	Fail-safe power-on-reset
ABIST2_VAUX_OK	Description	Diagnostic of VAUX Analog BIST2 (executed on demand)
	<b>0</b>	<b>VAUX ABIST fail or not executed</b>
	1	VAUX ABIST pass
	Reset condition	Fail-safe power-on-reset
ABIST1_OK	Description	Diagnostic of analog BIST1 (automatically executed)
	0	ABIST1 fail
	<b>1</b>	<b>ABIST1 pass</b>
	Reset condition	Fail-safe power-on-reset

**13.4.3 INIT\_SUPERVISOR**

**Table 80. INIT\_SUPERVISOR register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	0	1	1	P	VCORE_5D	VCCA_5D	VAUX_5D	FS1B_TIME_RANGE	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VCORE_5D	VCCA_5D	VAUX_5D	FS1B_TIME_RANGE
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VCORE_5D	VCCA_5D	VAUX_5D	FS1B_TIME_RANGE

**Table 81. INIT\_SUPERVISOR description and configuration of the bits (default value in bold)**

V <sub>CORE_5D</sub>	Description	Configure the V <sub>CORE</sub> undervoltage in degraded mode. Only valid for 5.0 V
	<b>0</b>	<b>Normal 5.0 V undervoltage detection threshold (V<sub>CORE_FB_UV</sub>)</b>
	1	Degraded mode, lower undervoltage detection threshold applied (V <sub>CORE_FB_UV_D</sub> )
	Reset condition	Power on reset
V <sub>CCA_5D</sub>	Description	Configure the V <sub>CCA</sub> undervoltage in degraded mode. Only valid for 5.0 V
	<b>0</b>	<b>Normal 5.0 V undervoltage detection threshold (V<sub>CCA_UV_5</sub>)</b>
	1	Degraded mode, lower undervoltage detection threshold applied (V <sub>CCA_UV_D</sub> )
	Reset condition	Power on reset
V <sub>AUX_5D</sub>	Description	Configure the V <sub>AUX</sub> undervoltage in degraded mode. Only valid for 5.0 V
	<b>0</b>	<b>Normal 5.0 V undervoltage detection threshold (V<sub>AUX_UV_5</sub>)</b>
	1	Degraded mode; lower undervoltage detection threshold applied (V <sub>AUX_UV_5D</sub> )
	Reset condition	Power on reset
FS1B_TIME_RANGE	Description	Configure the FS1B timing range factor x1 or x8
	<b>0</b>	<b>x1 timing range factor</b>
	1	x8 timing range factor
	Reset condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2= NOT(bit4) Secured_1=bit7 Secured_0=bit6

**13.4.4 INIT\_FAULT**

**Table 82. INIT\_FAULT register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	0	0	P	FLT_ERR_FS	FS1B_CAN_IMPACT	FLT_ERR_IMP_1	FLT_ERR_IMP_0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	FLT_ERR_FS	FS1B_CAN_IMPACT	FLT_ERR_IMP_1	FLT_ERR_IMP_0
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	FLT_ERR_FS	FS1B_CAN_IMPACT	FLT_ERR_IMP_1	FLT_ERR_IMP_0

**Table 83. INIT\_FAULT description and configuration of the bits (default value in bold)**

FLT_ERR_FS	Description	Configure the values of the fault error counter
	<b>0</b>	<b>intermediate = 3; final = 6</b>
	1	intermediate = 1; final = 2
	Reset condition	Power on reset
FS1B_CAN_IMPACT	Description	Configure CAN behavior when FS1B is asserted low
	0	No effect
	<b>1</b>	<b>CAN in RX only or sleep mode when FS1B is asserted (depends on CAN_DIS_CFG bit in INIT_WU2 register)</b>
Reset condition	Power on reset	
FLT_ERR_IMP_1:0	Description	Configure RSTB and FS0B behavior when fault error counter ≥ intermediate value
	00	No effect on RSTB and FS0B
	<b>01</b>	<b>FS0B is asserted low if FLT_ERR_CNT ≥ intermediate value</b>
	10	RSTB is asserted low if FLT_ERR_CNT ≥ intermediate value and WD error counter = WD_CNT_ERR[1:0]
	11	FS0B is asserted low if FLT_ERR_CNT ≥ intermediate value RSTB is asserted low if FLT_ERR_CNT ≥ intermediate value and WD error counter = WD_CNT_ERR[1:0]
	Reset condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

**13.4.5 INIT\_FSSM**

**Table 84. INIT\_FSSM register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	0	1	P	IO_45_FS	RES_ERVED	RES_ERVED	RSTB_DURATION	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	IO_45_FS	RES_ERVED	RES_ERVED	RSTB_DURATION
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	IO_45_FS	RES_ERVED	RES_ERVED	RSTB_DURATION

**Table 85. INIT\_FSSM description and configuration of the bits (default value in bold)**

IO_45_FS	Description	Configure the couple of IO_4:5 as safety inputs for external IC error monitoring
	<b>0</b>	<b>Not safety</b>
	1	Safety critical
	Reset condition	Power on reset
RSTB_DURATION	Description	Configure the RSTB low duration time
	<b>0</b>	<b>10 ms</b>
	1	1.0 ms
	Reset condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

**13.4.6 INIT\_SF\_IMPACT**

**Table 86. INIT\_SF\_IMPACT register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	1	0	P	TDLY_TDUR	DIS_8S	WD_IMPACT_1	WD_IMPACT_0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	TDLY_TDUR	DIS_8S	WD_IMPACT_1	WD_IMPACT_0
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	TDLY_TDUR	DIS_8S	WD_IMPACT_1	WD_IMPACT_0

**Table 87. INIT\_SF\_IMPACT description and configuration of the bits (default value in bold)**

TDLY_TDUR	Description	FS1B delay or FS1B duration mode selection
	<b>0</b>	<b>FS1B t<sub>DELAY</sub> mode</b>
	1	FS1B t <sub>DURATION</sub> mode
	Reset condition	Power on reset
DIS_8S	Description	Disable the 8.0 s timer used to enter deep fail-safe mode
	<b>0</b>	<b>Enabled</b>
	1	Disabled
	Reset condition	Power on reset

**Table 87. INIT\_SF\_IMPACT description and configuration of the bits (default value in bold)...continued**

WD_IMPACT_1:0	Description	Watchdog impact on RSTB and/or FS0B assertion
	00	No effect on RSTB and FS0B if WD error counter = WD_CNT_ERR[1:0]
	<b>01</b>	<b>RSTB only is asserted low if WD error counter = WD_CNT_ERR[1:0]</b>
	10	FS0B only is asserted low if WD error counter = WD_CNT_ERR[1:0]
	11	RSTB and FS0B are asserted low if WD error counter = WD_CNT_ERR[1:0]
	Reset condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

**13.4.7 WD\_WINDOW**

**Table 88. WD\_WINDOW register description**

Write <sup>[1]</sup>																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	1	1	P	WD_WINDOW_3	WD_WINDOW_2	WD_WINDOW_1	WD_WINDOW_0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	WD_WINDOW_3	WD_WINDOW_2	WD_WINDOW_1	WD_WINDOW_0
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	WD_WINDOW_3	WD_WINDOW_2	WD_WINDOW_1	WD_WINDOW_0

[1] Any write command to the WD\_WINDOW register in the normal mode should be followed by a read command to verify the correct change of the WD window duration.

**Table 89. WD\_WINDOW description and configuration of the bits (default value in bold)**

WD_WINDOW_3:0	Description	Configure the watchdog window duration. Duty cycle if set to 50 %
	0000	Disable (in INIT phase only)
	0001	1.0 ms
	0010	2.0 ms
	<b>0011</b>	<b>3.0 ms</b>
	0100	4.0 ms
	0101	6.0 ms
	0110	8.0 ms
	0111	12 ms
	1000	16 ms
	1001	24 ms
	1010	32 ms
	1011	64 ms
	1100	128 ms
	1101	256 ms
	1110	512 ms
	1111	1024 ms
Reset condition	Power on reset	
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

**13.4.8 LFSR**

**Table 90. LFSR register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	0	0	0	P	LFSR_7	LFSR_6	LFSR_5	LFSR_4	LFSR_3	LFSR_2	LFSR_1	LFSR_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	LFSR_7	LFSR_6	LFSR_5	LFSR_4	LFSR_3	LFSR_2	LFSR_1	LFSR_0
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	LFSR_7	LFSR_6	LFSR_5	LFSR_4	LFSR_3	LFSR_2	LFSR_1	LFSR_0



**Table 91. LFSR description and configuration of the bits (default value in bold)**

LFSR_7:0	Description	8 bits LFSR value. Used to write the seed at any time
	0...	bit7:bit0: 10110010 default value at start-up or after a power-on-reset: 0xB2 <sup>[1]</sup> , [2]
	1...	
	Reset condition	Power on reset

[1] Value Bit7:Bit0: 1111 1111 is prohibited.

[2] During a write command, MISO reports the previous register content.

**13.4.9 WD\_ANSWER**

**Table 92. WD\_ANSWER register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	0	0	1	P	WD_ANSWER_7	WD_ANSWER_6	WD_ANSWER_5	WD_ANSWER_4	WD_ANSWER_3	WD_ANSWER_2	WD_ANSWER_1	WD_ANSWER_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	RSTB	FSxB	RESERVED	FSO_G	IO_FS_G	WD_BAD_TIMING	ERR_INT_HW	ERR_INT_SW
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	RSTB	FSxB	RESERVED	FSO_G	IO_FS_G	WD_BAD_TIMING	ERR_INT_HW	ERR_INT_SW

**Table 93. WD\_ANSWER description and configuration of the bits (default value in bold)**

WD_ANSWER_7:0	Description	WD answer from the MCU
	0...	Any value can be written to refresh the watchdog.
	1...	
	Reset condition	Power on reset/RSTB low
RSTB	Description	Report a reset event
	<b>0</b>	<b>No reset</b>
	1	Reset occurred
	Reset condition	Power on reset/read
FSxB	Description	Report a fail-safe event
	0	No fail-safe
	<b>1</b>	<b>Fail-safe event occurred (default state at power up and after LPOFF as FS0B/FS1B are asserted low)</b>
	Reset condition	Power on reset/read
FSO_G <sup>[1]</sup>	Description	Report a fail-safe output failure
	<b>0</b>	<b>No failure</b>
	1	Failure
	Reset condition	Power on reset/read

**Table 93. WD\_ANSWER description and configuration of the bits (default value in bold) ...continued**

IO_FS_G <sup>[2]</sup>	Description	Report an IO monitoring error
	<b>0</b>	<b>No error</b>
	1	Error detected
	Reset condition	Power on reset/read
WD_BAD_TIMING	Description	Report a watchdog timing refresh error
	<b>0</b>	<b>WD timing refresh OK</b>
	1	Wrong WD timing refresh
	Reset condition	Power on reset/read
ERR_INT_HW	Description	Report an error from an internal redundant structure of the fail-safe state machine
	<b>0</b>	<b>No error</b>
	1	Error detected
	Reset condition	Power on reset/read
ERR_INT_SW	Description	Report an error from the EDC of the fail-safe state machine (error detection correction)
	<b>0</b>	<b>No error</b>
	1	Error detected
	Reset condition	Power on reset/read

[1] FSO\_G = RSTB\_short\_high or FS0B\_short\_high or FS0B\_short\_low or FS1B\_short\_high or FS1B\_short\_low

[2] IO\_FS\_G = IO\_45\_fail

Values of the two registers WD\_COUNTER and DIAG\_SF\_ERR are updated at the end of any SPI access to one of the three registers WD\_ANSWER, WD\_COUNTER, and DIAG\_SF\_ERR. To always get up to date values, it is recommended to make two consecutive SPI accesses to WD\_COUNTER and DIAG\_SF\_ERR registers or access (read or write) WD\_ANSWER register first.

Example1: read or write WD\_ANSWER to update the registers, read WD\_COUNTER and DIAG\_SF\_ERR to report the latest information

Example2: read WD\_COUNTER to update the register, read again WD\_COUNTER to report the latest information

**13.4.10 RELEASE\_FSxB**

**Table 94. RELEASE\_FSxB register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	0	1	0	P	RELEASE_FSxB_7	RELEASE_FSxB_6	RELEASE_FSxB_5	RELEASE_FSxB_4	RELEASE_FSxB_3	RELEASE_FSxB_2	RELEASE_FSxB_1	RELEASE_FSxB_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	RES_ERVED	FS1B_SNS	FS0B_SNS	RSTB_SNS
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	RES_ERVED	FS1B_SNS	FS0B_SNS	RSTB_SNS

**Table 95. RELEASE\_FSxB description and configuration of the bits (default value in bold)**

RELEASE_FSxB_7:0	Description	Secured 8 bits word to release the FS0B and FS1B pins
	0...	Depends on LFSR_out value and calculation
	1...	
	Reset condition	Power on reset -> default = 00h
FS1B_SNS	Description	Sense of FS1B pad
	<b>0</b>	<b>FS1B pad sense low</b>
	1	FS1B pad sense high
	Reset condition	Power on reset
FS0B_SNS	Description	Sense of FS0B pad
	<b>0</b>	<b>FS0B pad sense low</b>
	1	FS0B pad sense high
	Reset condition	Power on reset
RSTB_SNS	Description	Sense of RSTB pad
	0	RSTB pad sense low
	<b>1</b>	<b>RSTB pad sense high</b>
	Reset condition	Power on reset

**13.4.11 SF\_OUTPUT\_REQUEST**

**Table 96. SF\_OUTPUT\_REQUEST register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	0	1	1	P	FS1B_REQ	FS1B_DLY_REQ	FS0B_REQ	RSTB_REQ	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	FS1B_DRV	FS1B_DLY_DRV	FS0B_DRV	RSTB_DRV
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	FS1B_DRV	FS1B_DLY_DRV	FS0B_DRV	RSTB_DRV

**Table 97. SF\_OUTPUT\_REQUEST description and configuration of the bits (default value in bold)**

FS1B_REQ	Description	Request FS1B to be asserted low
	<b>0</b>	<b>No request</b>
	1	Request FS1B assertion with immediate assertion, no delay
	Reset condition	Power on reset
FS1B_DLY_REQ	Description	Request activation of FS1B internal pull-up (open/close switch S1)
	0	Close S1
	<b>1</b>	<b>Open S1</b>
	Reset condition	Power on reset

**Table 97. SF\_OUTPUT\_REQUEST description and configuration of the bits (default value in bold)...continued**

FS0B_REQ	Description	Request FS0B to be asserted low
	<b>0</b>	<b>No request</b>
	1	Request FS0B assertion
	Reset condition	Power On reset
RSTB_REQ	Description	Request a RSTB low pulse
	<b>0</b>	<b>No request</b>
	1	Request a RSTB low pulse
	Reset condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6
FS1B_DRV	Description	Sense of FS1B driver command from fail-safe logic (digital)
	<b>0</b>	<b>FS1B digital driver sense low</b>
	1	FS1B digital driver sense high
	Reset condition	Power on reset
FS1B_DLY_DRV	Description	Sense of FS1B driver command from internal pull-up (analog)
	0	FS1B analog driver sense low
	1	FS1B analog driver sense high
	Reset condition	Power on reset
FS0B_DRV	Description	Sense of FS0B driver command from fail-safe logic
	<b>0</b>	<b>FS0B driver sense low</b>
	1	FS0B driver sense high
	Reset condition	Power on reset
RSTB_DRV	Description	Sense of RSTB driver command from fail-safe logic
	0	RSTB driver sense low
	<b>1</b>	<b>RSTB driver sense high</b>
	Reset condition	Power on reset

**13.4.12 INIT\_WD\_CNT**

**Table 98. INIT\_WD\_CNT register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	1	0	0	P	WD_CNT_ERR_1	WD_CNT_ERR_0	WD_CNT_RFR_1	WD_CNT_RFR_0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	WD_CNT_ERR_1	WD_CNT_ERR_0	WD_CNT_RFR_1	WD_CNT_RFR_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	WD_CNT_ERR_1	WD_CNT_ERR_0	WD_CNT_RFR_1	WD_CNT_RFR_0

**Table 99. INIT\_WD\_CNT description and configuration of the bits (default value in bold)**

WD_CNT_ERR_1:0	Description	Configure the maximum value of the WD error counter
	<b>00</b>	<b>6</b>
	01	6
	10	4
	11	2
	Reset condition	Power on reset
WD_CNT_RFR_1:0	Description	Configure the maximum value of the WD refresh counter
	<b>00</b>	<b>6</b>
	01	4
	10	2
	11	1
	Reset condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

**13.4.13 DIAG\_SF\_IOs**

**Table 100. DIAG\_SF\_IOs register description**

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	RSTB_EXT	RSTB_DIAG	FS0B_DIAG_1	FS0B_DIAG_0	FS1B_DIAG_1	FS1B_DIAG_0	RES_ERVED	Io_45_FAIL

**Table 101. DIAG\_SF\_IOs description and configuration of the bits (default value in bold)**

RSTB_EXT	Description	Report an external RSTB
	<b>0</b>	<b>No external RSTB</b>
	1	External RSTB
	Reset condition	Power on reset/read

**Table 101. DIAG\_SF\_IOs description and configuration of the bits (default value in bold)...***continued*

RSTB_DIAG	Description	Report a RSTB short-circuit to high
	<b>0</b>	<b>No Failure</b>
	1	Short-circuit high
	Reset condition	Power on reset/read
FS0B_DIAG_1:0	Description	Report a failure on FS0B
	<b>00</b>	<b>No Failure</b>
	01	Short-circuit low/open load
	1X	Short-circuit high
	Reset condition	Power on reset/read
FS1B_DIAG_1:0	Description	Report a failure on FS1B
	<b>00</b>	<b>No Failure</b>
	01	Short-circuit low/open load
	1X	Short-circuit high
	Reset condition	Power on reset/read
IO_45_FAIL	Description	Report an error in the IO_45 protocol
	<b>0</b>	<b>No error</b>
	1	Error detected
	Reset condition	Power on reset/read

**13.4.14 WD\_COUNTER**

**Table 102. WD\_COUNTER register description**

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	WD_ERR_2	WD_ERR_1	WD_ERR_0	RES_ERVED	WD_RFR_2	WD_RFR_1	WD_RFR_0	RES_ERVED

**Table 103. WD\_COUNTER description and configuration of the bits (default value in bold)**

WD_ERR_2:0	Description	Report the value of the watchdog error counter
	<b>000</b>	From 0 to 5 (6 generate an increase of the FLT_ERR_CNT and this counter is reset to 0)
	to 110	
	Reset condition	Power on reset
WD_RFR_2:0	Description	Report the value of the watchdog refresh counter
	<b>000</b>	From 0 to 6 (7 generate a decrease of the FLT_ERR_CNT and this counter is reset to 0)
	to 111	
	Reset condition	Power on reset

**13.4.15 DIAG\_SF\_ERR**

**Table 104. DIAG\_SF\_ERR register description**

Read	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	FLT_ERR_2	FLT_ERR_1	FLT_ERR_0	RESERVED	V2P5_M_A_OV	V2P5_M_D_OV	FCRBM_OV	FCRBM_UV

**Table 105. DIAG\_SF\_ERR description and configuration of the bits (default value in bold)**

FLT_ERR_2:0	Description	Report the value of the fault error counter
	000	Error counter is set to 1 by default
	001	
	... 110	
	Reset condition	Power on reset
V2P5_M_A_OV	Description	Report an overvoltage on V2P5 main analog regulator
	<b>0</b>	<b>No overvoltage (<math>V_{2P5\_M\_A} &lt; V_{2P5\_M\_A\_OV}</math>)</b>
	1	Overvoltage detected ( $V_{2P5\_M\_A} > V_{2P5\_M\_A\_OV}$ )
	Reset condition	Power on reset/read
V2P5_M_D_OV	Description	Report an overvoltage on V2P5 main digital regulator
	<b>0</b>	<b>No overvoltage (<math>V_{2P5\_M\_D} &lt; V_{2P5\_M\_D\_OV}</math>)</b>
	1	Overvoltage detected ( $V_{2P5\_M\_D} > V_{2P5\_M\_D\_OV}$ )
	Reset condition	Power on reset/read
FCRBM_OV	Description	Report an overvoltage on FCRBM
	<b>0</b>	<b>No overvoltage (<math>FB\_Core - FCRBM &lt; 150\text{ mV}</math>)</b>
	1	Overvoltage detected ( $FB\_Core - FCRBM > 150\text{ mV}$ )
	Reset condition	Power on reset/read
FCRBM_UV	Description	Report an undervoltage on FCRBM
	<b>0</b>	<b>No undervoltage (<math>FB\_Core - FCRBM &gt; -150\text{ mV}</math>)</b>
	1	Undervoltage detected ( $FB\_Core - FCRBM < -150\text{ mV}$ )
	Reset condition	Power on reset/read

**13.4.16 INIT\_VCORE\_OVUV\_IMPACT**

**Table 106. INIT\_VCORE\_OVUV\_IMPACT register description**

Write	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	1	0	0	0	1	P	VCORE_FS_OV_1	VCORE_FS_OV_0	VCORE_FS_UV_1	VCORE_FS_UV_0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VCORE_FS_OV_1	VCORE_FS_OV_0	VCORE_FS_UV_1	VCORE_FS_UV_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VCORE_FS_OV_1	VCORE_FS_OV_0	VCORE_FS_UV_1	VCORE_FS_UV_0

**Table 107. INIT\_VCORE\_OVUV\_IMPACT description and configuration of the bits (default value in bold)**

VCORE_FS_OV_1:0	Description	VCORE_FB overvoltage safety impact
	00	No effect of V <sub>VCORE_FB_OV</sub> on RSTB and FS0B
	01	V <sub>VCORE_FB_OV</sub> does have an impact on RSTB only
	10	V <sub>VCORE_FB_OV</sub> does have an impact on FS0B only
	<b>11</b>	V <sub>VCORE_FB_OV</sub> does have an impact on RSTB and FS0B
	Reset condition	Power on reset
VCORE_FS_UV_1:0	Description	VCORE_FB undervoltage safety impact
	00	No effect of V <sub>VCORE_FB_UV</sub> on RSTB and FS0B
	01	V <sub>VCORE_FB_UV</sub> does have an impact on RSTB only
	<b>10</b>	V <sub>VCORE_FB_UV</sub> does have an impact on FS0B only
	11	V <sub>VCORE_FB_UV</sub> does have an impact on RSTB and FS0B
	Reset condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

**13.4.17 INIT\_VCCA\_OVUV\_IMPACT**

**Table 108. INIT\_VCCA\_OVUV\_IMPACT register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	1	0	0	1	0	P	VCCA_FS_OV_1	VCCA_FS_OV_0	VCCA_FS_UV_1	VCCA_FS_UV_0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VCCA_FS_OV_1	VCCA_FS_OV_0	VCCA_FS_UV_1	VCCA_FS_UV_0
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VCCA_FS_OV_1	VCCA_FS_OV_0	VCCA_FS_UV_1	VCCA_FS_UV_0



**Table 109. INIT\_VCCA\_OVUV\_IMPACT description and configuration of the bits (default value in bold)**

VCCA_FS_OV_1:0	Description	V <sub>C</sub> CA overvoltage safety impact
	00	No effect of V <sub>C</sub> CA_OV on RSTB and FS0B
	01	V <sub>C</sub> CA_OV does have an impact on RSTB only
	10	V <sub>C</sub> CA_OV does have an impact on FS0B only
	<b>11</b>	<b>V<sub>C</sub>CA_OV does have an impact on RSTB and FS0B</b>
	Reset Condition	Power on reset
VCCA_FS_UV_1:0	Description	V <sub>C</sub> CA undervoltage safety impact
	00	No effect of V <sub>C</sub> CA_UV on RSTB and FS0B
	01	V <sub>C</sub> CA_UV does have an impact on RSTB only
	<b>10</b>	<b>V<sub>C</sub>CA_UV does have an impact on FS0B only</b>
	11	V <sub>C</sub> CA_UV does have an impact on RSTB and FS0B
	Reset Condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

**13.4.18 INIT\_VAUX\_OVUV\_IMPACT**

**Table 110. INIT\_VAUX\_OVUV\_IMPACT register description**

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	1	0	0	1	1	P	VAUX_FS_OV_1	VAUX_FS_OV_0	VAUX_FS_UV_1	VAUX_FS_UV_0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VAUX_FS_OV_1	VAUX_FS_OV_0	VAUX_FS_UV_1	VAUX_FS_UV_0
Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VAUX_FS_OV_1	VAUX_FS_OV_0	VAUX_FS_UV_1	VAUX_FS_UV_0

**Table 111. INIT\_VAUX\_OVUV\_IMPACT description and configuration of the bits (default value in bold)**

VAUX_FS_OV_1:0	Description	V <sub>A</sub> UX overvoltage safety impact
	00	No effect of V <sub>A</sub> UX_OV on RSTB and FS0B
	01	V <sub>A</sub> UX_OV does have an impact on RSTB only
	10	V <sub>A</sub> UX_OV does have an impact on FS0B only
	<b>11</b>	<b>V<sub>A</sub>UX_OV does have an impact on RSTB and FS0B</b>
	Reset condition	Power on reset

**Table 111. INIT\_VAUX\_OVUV\_IMPACT description and configuration of the bits (default value in bold)...continued**

VAUX_FS_UV_1:0	Description	V <sub>AUX_UV</sub> undervoltage safety impact
	00	No effect of V <sub>AUX_UV</sub> on RSTB and FS0B
	01	V <sub>AUX_UV</sub> does have an impact on RSTB only
	<b>10</b>	<b>V<sub>AUX_UV</sub> does have an impact on FS0B only</b>
	11	V <sub>AUX_UV</sub> does have an impact on RSTB and FS0B
	Reset condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

**13.4.19 DEVICE\_ID\_FS**

**Table 112. DEVICE\_ID\_FS register description**

Read	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	RES_ERVED	RES_ERVED	RES_ERVED	RES_ERVED	RES_ERVED	RES_ERVED	DFS_HW2	FS1

**Table 113. DEVICE\_ID\_FS description and configuration of the bits (default value in bold)**

DFS_HW2	Description	Report the deep fail-safe hardware configuration (fail-safe logic)
	0	Deep fail-safe disable
	1	Deep fail-safe enable
	Reset condition	Power on reset
FS1	Description	Report the FS1B function availability (depends on part number)
	0	Disabled
	1	Enabled
	Reset condition	Power on reset

**14 List of interruptions and description**

The INTB output pin generates a low pulse when an Interrupt condition occurs. The INTB behavior as well as the pulse duration are set through the SPI during INIT phase. It is possible to mask some Interruption source (see [Section 13.3](#)).

**Table 114. Interruptions list**

Event	Description
V <sub>SNS_UV</sub>	Detection of V <sub>BATTERY</sub> below 8.5 V
V <sub>SUP_UV_7</sub>	Detection of V <sub>SUP</sub> below 7.0 V (after reverse current protection diode)
I <sub>PF</sub>	Input power feed forward. Based on V <sub>SUP</sub> and I <sub>PRE_PEAK</sub>

Table 114. Interruptions list...continued

Event	Description
I <sub>LIM_PRE</sub>	Pre-regulator current limitation
T <sub>WARN_PRE</sub>	Temperature warning on the pass transistor
BoB	Return the running state of V <sub>PRE</sub> converter (buck or boost mode)
V <sub>PRE_STATE</sub> (V <sub>PRE_SMPS_EN</sub> )	Return the activation state of V <sub>PRE</sub> DC-DC converter
V <sub>PRE_OV</sub>	Report a V <sub>PRE</sub> overvoltage detection
V <sub>PRE_UV</sub>	Report a V <sub>PRE</sub> undervoltage detection
T <sub>WARN_CORE</sub>	Temperature warning on the pass transistor
V <sub>CORE_STATE</sub> (V <sub>CORE_SMPS_EN</sub> )	Return the activation state of V <sub>CORE</sub> DC-DC converter
V <sub>CORE_OV</sub>	Report a V <sub>CORE</sub> overvoltage detection
V <sub>CORE_UV</sub>	Report a V <sub>CORE</sub> undervoltage detection
I <sub>LIM_CCA</sub>	V <sub>CCA</sub> current limitation
I <sub>LIM_CCA_OFF</sub>	Current limitation maximum duration expiration. Only used when external PNP connected.
T <sub>WARN_CCA</sub>	Temperature warning on the pass transistor (internal pass transistor only)
TSD <sub>VCCA</sub>	Temperature shutdown of the VCCA
V <sub>CCA_OV</sub>	Report a V <sub>CCA</sub> overvoltage detection
V <sub>CCA_UV</sub>	Report a V <sub>CCA</sub> undervoltage detection
I <sub>LIM_AUX</sub>	V <sub>AUX</sub> current limitation
I <sub>LIM_AUX_OFF</sub>	Current limitation maximum duration expiration. Only used when external PNP connected.
TSD <sub>VAUX</sub>	Temperature shutdown of the VAUX
V <sub>AUX_OV</sub>	Report a V <sub>AUX</sub> overvoltage detection
V <sub>AUX_UV</sub>	Report a V <sub>AUX</sub> undervoltage detection
I <sub>LIM_CAN</sub>	V <sub>CAN</sub> current limitation
V <sub>CAN_OV</sub>	Report a V <sub>CAN</sub> overvoltage detection
TSD <sub>CAN</sub>	Temperature shutdown on the pass transistor. Auto restart when T <sub>J</sub> < (TSD <sub>CAN</sub> – TSD <sub>CAN_HYST</sub> ).
V <sub>CAN_UV</sub>	Report a V <sub>CAN</sub> undervoltage detection
IO_0	Report IO_0 digital state change
IO_2	Report IO_2 digital state change
IO_3	Report IO_3 digital state change
IO_4	Report IO_4 digital state change
IO_5	Report IO_5 digital state change
IO_0_WU	Report IO_0 wake-up event
IO_2_WU	Report IO_2 wake-up event
IO_3_WU	Report IO_3 wake-up event
IO_4_WU	Report IO_4 wake-up event
IO_5_WU	Report IO_5 wake-up event

Table 114. Interruptions list...continued

Event	Description
CAN_WU	Report a CAN wake-up event
CAN_OT	CAN overtemperature detection
RXD_REC	CAN RXD recessive clamping detection (short-circuit to 5.0 V)
TXD_DOM	CAN TXD dominant clamping detection (short-circuit to GND)
CAN_DOM	CAN-bus dominant clamping detection
LIN_WU	Report a LIN wake-up event
LIN_OT	LIN overtemperature detection
RXDL_REC	LIN RXDL recessive clamping detection (short to high)
TXDL_DOM	LIN TXDL dominant clamping detection (short to GND)
LIN_DOM	LIN bus dominant clamping detection
INT_REQ	MCU request for an interrupt pulse
LDT_F1	Long duration timer configured in function 1 and after run value is reach
SPI_ERR	Secured SPI communication check
SPI_CLK	Report a wrong number of CLK pulse different than 16 during the NCS low pulse in main state machine
SPI_REQ	Invalid SPI access (wrong write or read, write to INIT registers in normal mode, wrong address)
SPI_PARITY	Report a parity error in main state machine

15 Typical applications

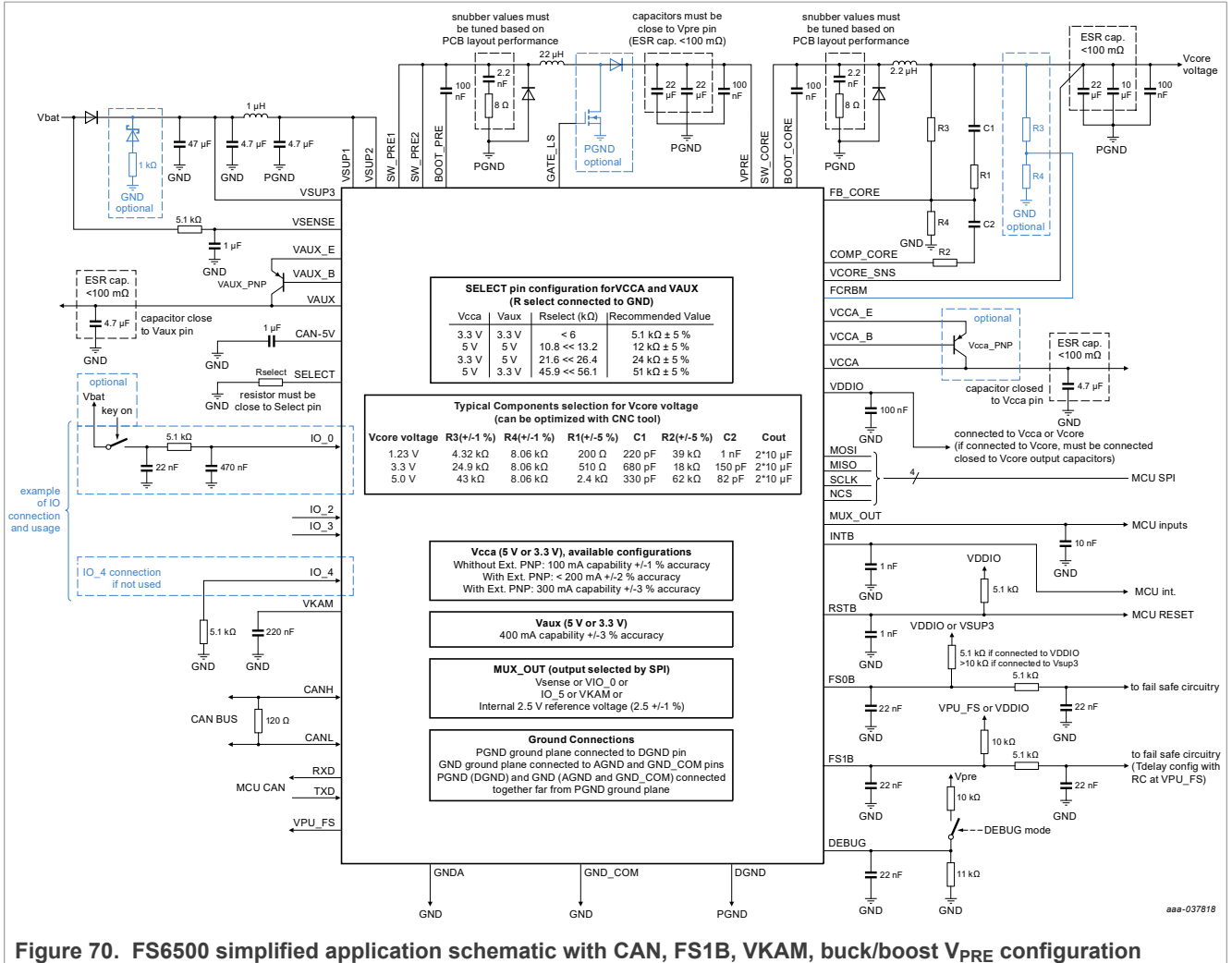


Figure 70. FS6500 simplified application schematic with CAN, FS1B, VKAM, buck/boost VPRE configuration

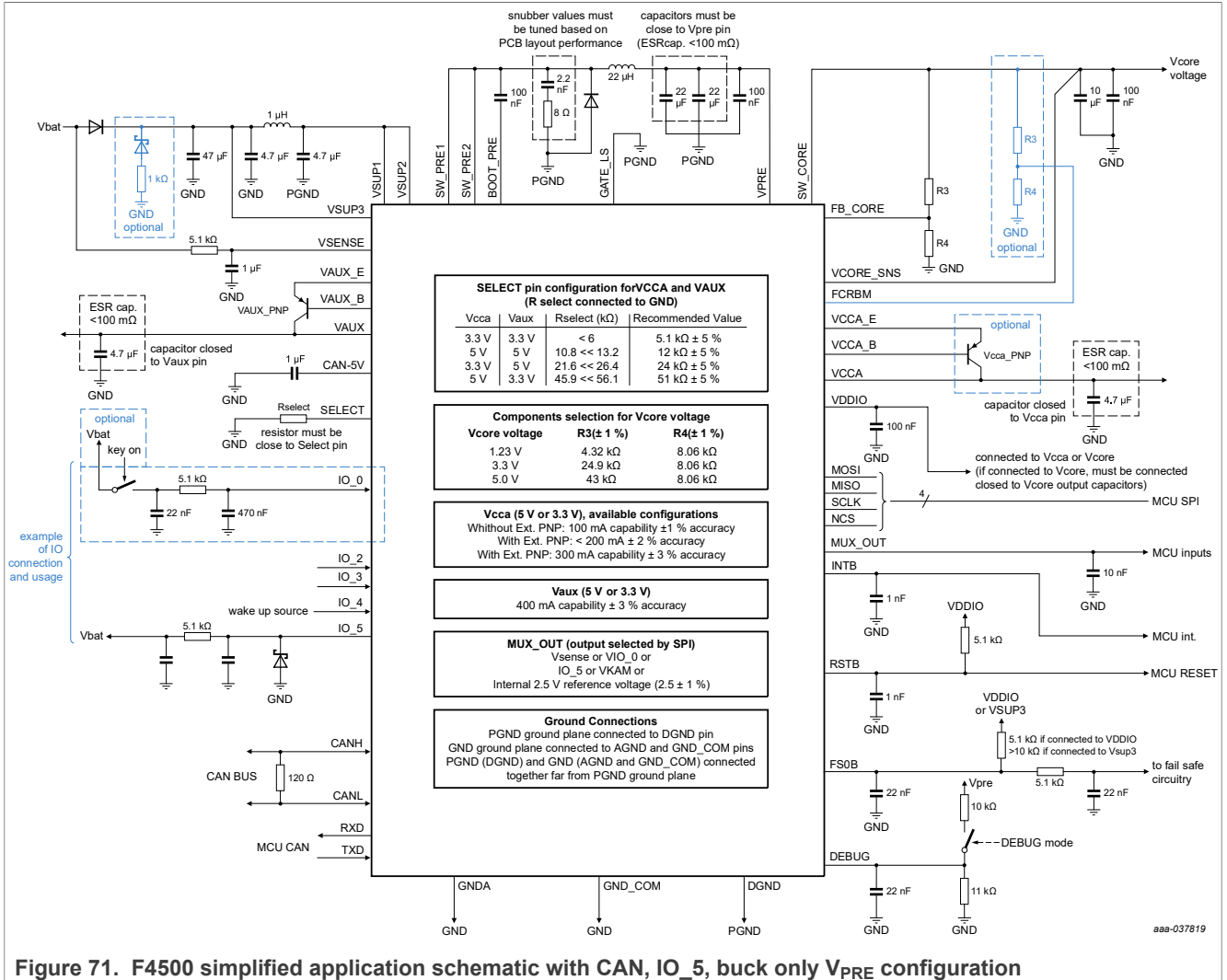


Figure 71. F4500 simplified application schematic with CAN, IO\_5, buck only V<sub>PRE</sub> configuration

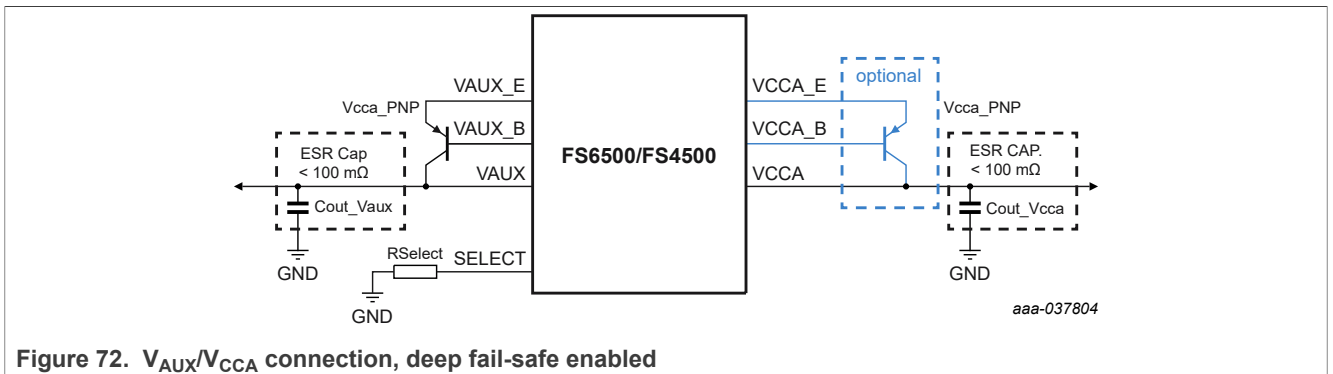


Figure 72. V<sub>AUX</sub>/V<sub>CCA</sub> connection, deep fail-safe enabled

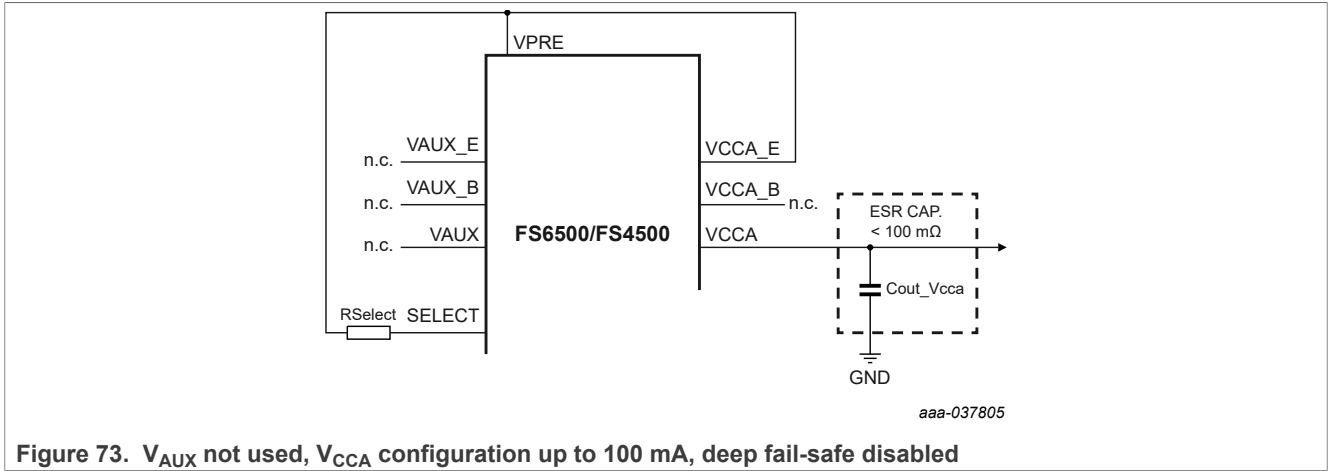


Figure 73.  $V_{AUX}$  not used,  $V_{CCA}$  configuration up to 100 mA, deep fail-safe disabled

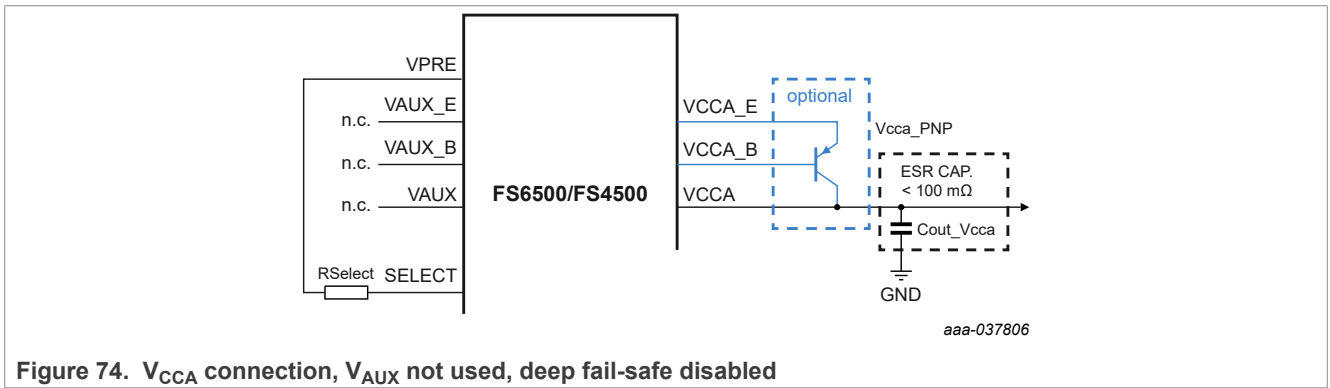


Figure 74.  $V_{CCA}$  connection,  $V_{AUX}$  not used, deep fail-safe disabled

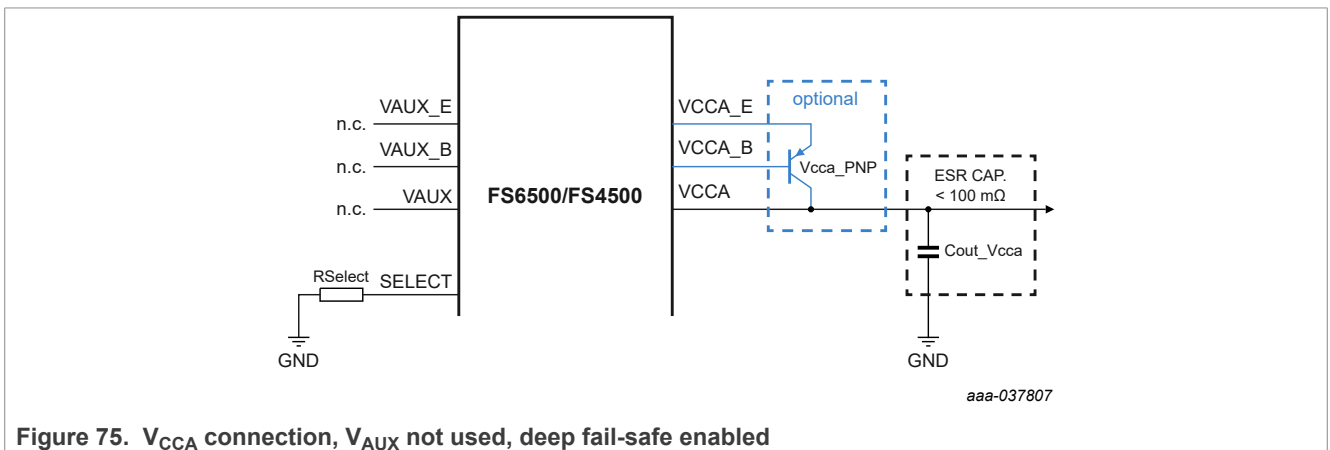


Figure 75.  $V_{CCA}$  connection,  $V_{AUX}$  not used, deep fail-safe enabled

## 16 Packaging

### 16.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to [www.nxp.com](http://www.nxp.com) and perform a keyword search for the drawing's document number.

**Table 115. Package mechanical dimensions**

Package	Suffix	Package outline drawing number
7.0 × 7.0, 48-Pin LQFP exposed pad, with 0.5 mm pitch, and a 4.5 × 4.5 exposed pad	AE	98ASA00173D



16.2 Package outline

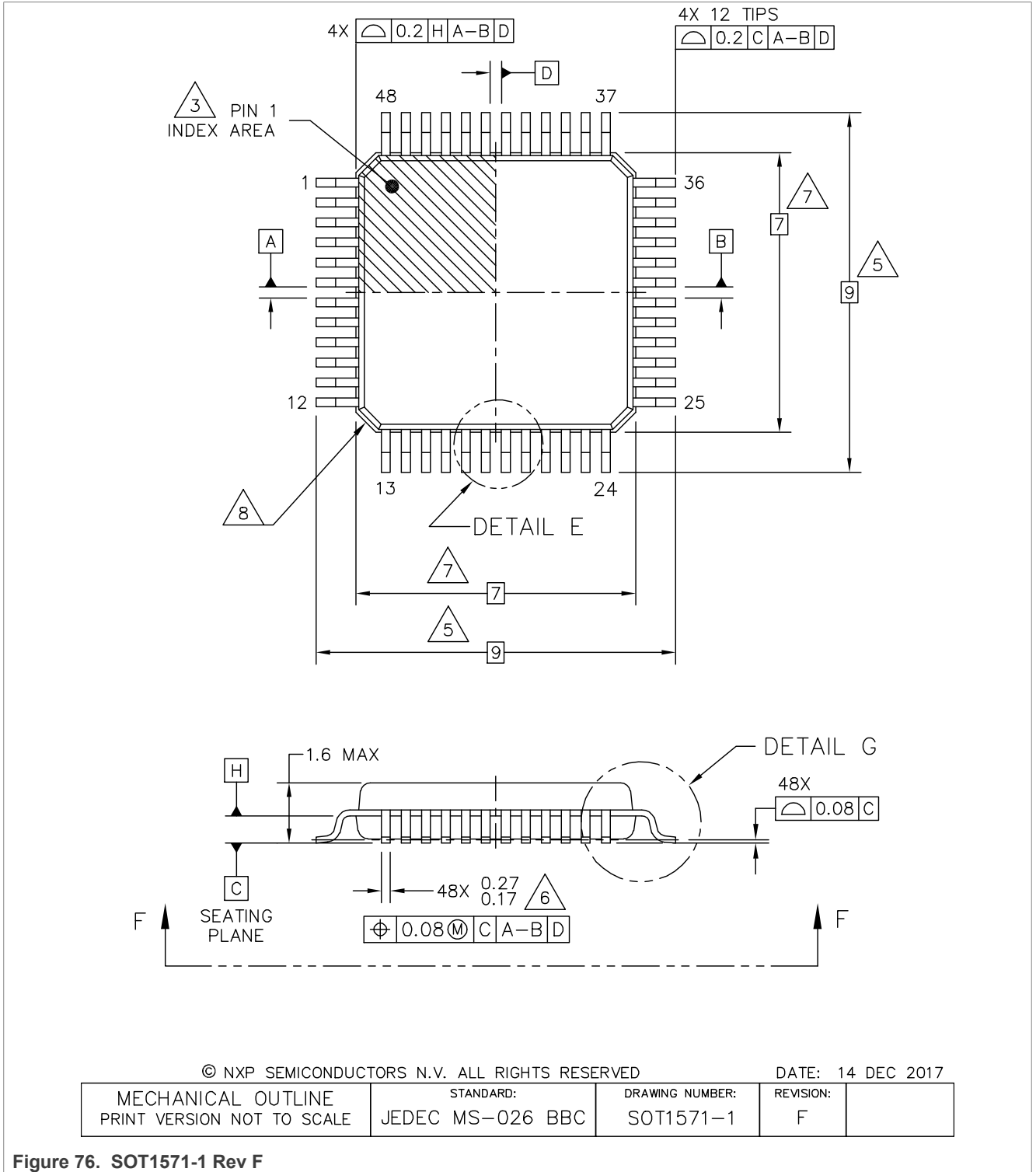


Figure 76. SOT1571-1 Rev F

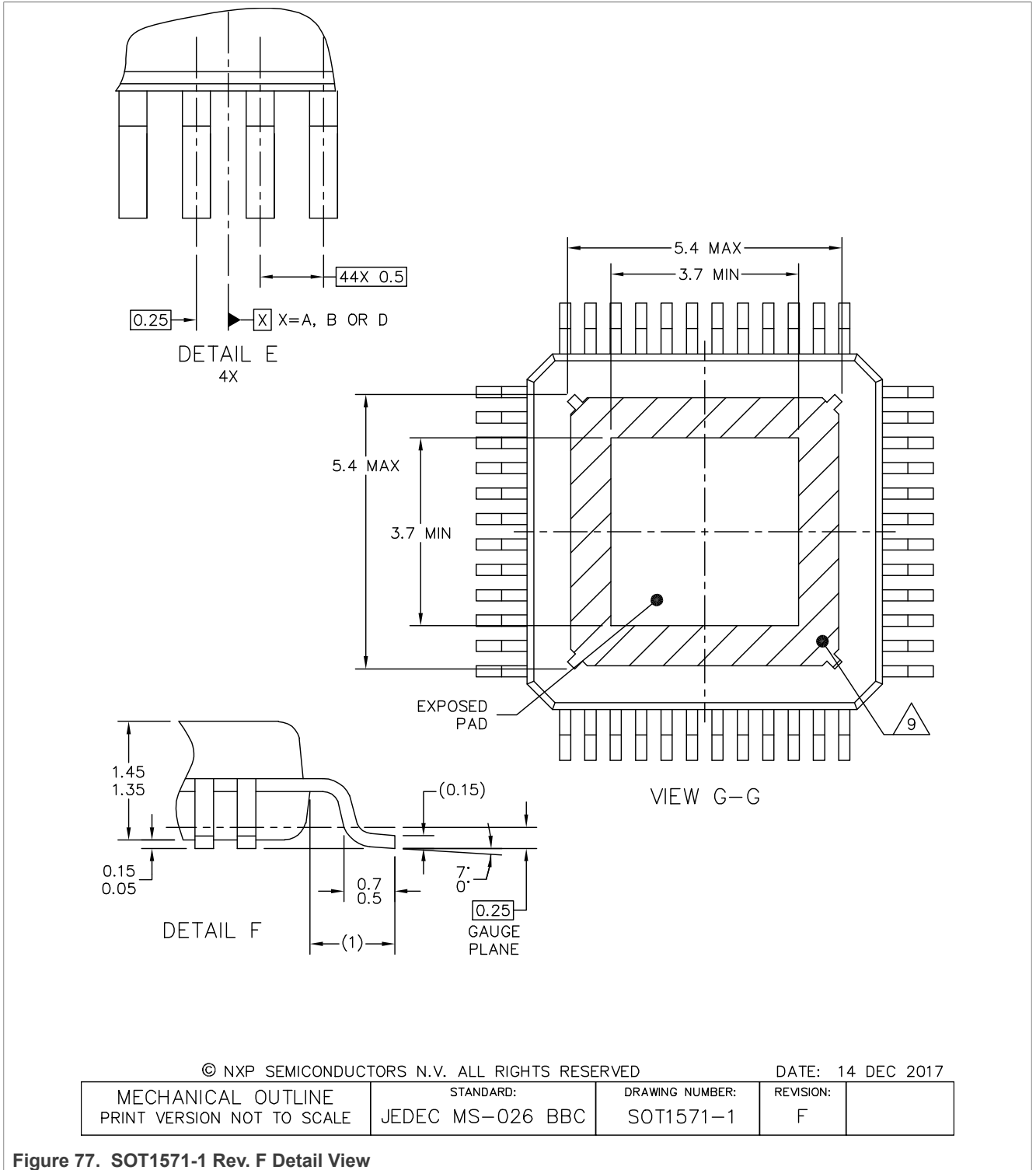


Figure 77. SOT1571-1 Rev. F Detail View

NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
- 4. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
- 5. DIMENSION TO BE DETERMINED AT SEATING PLANE C.
- 6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.
- 7. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
- 8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
- 9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

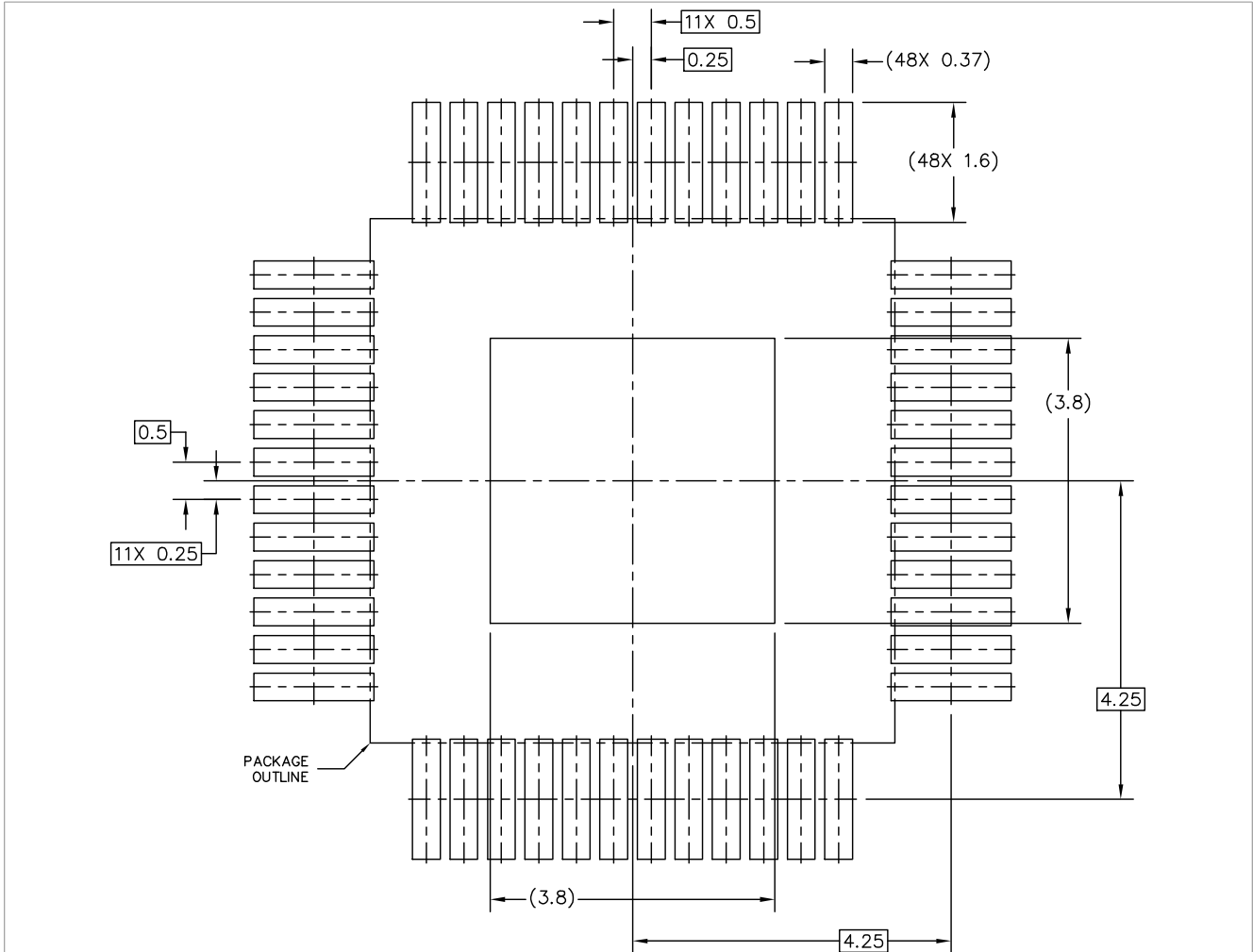
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DATE: 14 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS-026 BBC	DRAWING NUMBER: SOT1571-1	REVISION: F	
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**Figure 78. SOT1571-1 Rev F Notes**

**17 Soldering**



**PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN**

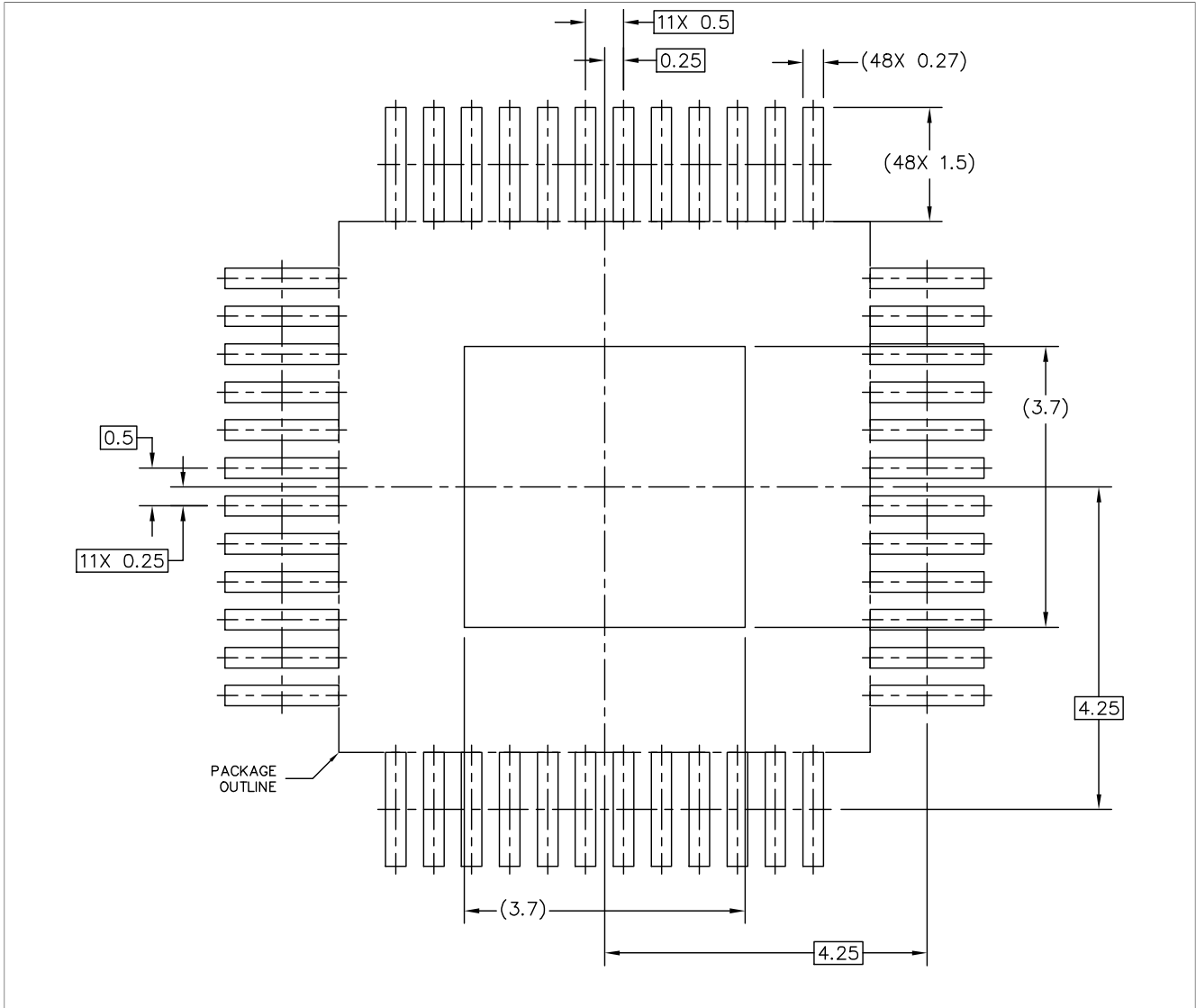
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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS-026 BBC	DRAWING NUMBER: SOT1571-1	REVISION: F	
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**Figure 79. SOT1571-1 Rev. F - PCB design guidelines - solder mask opening pattern**



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

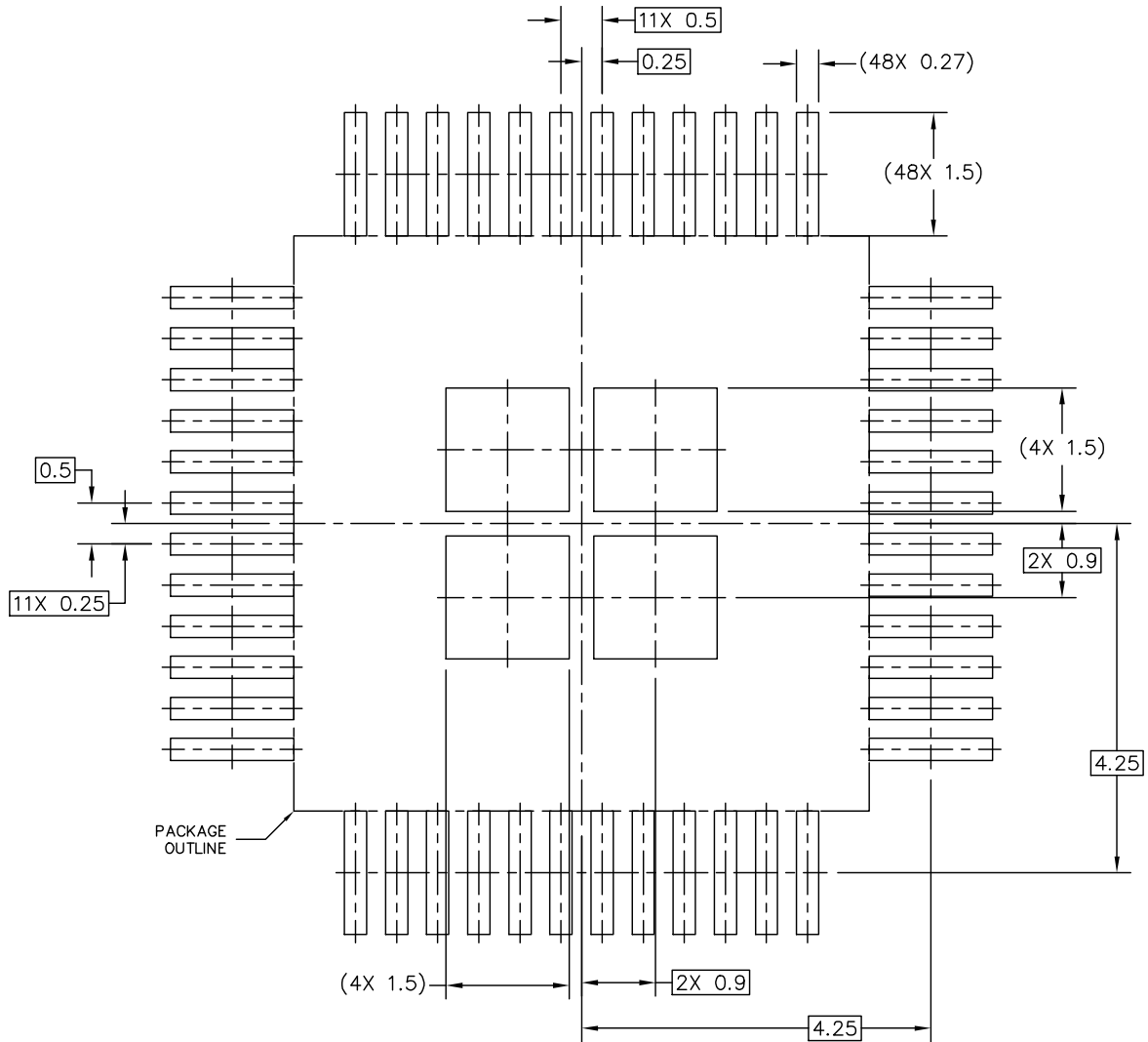
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DATE: 14 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS-026 BBC	DRAWING NUMBER: SOT1571-1	REVISION: F	
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Figure 80. SOT1571-1 Rev. F - PCB design guidelines - I/O pads and solderable area



STENCIL THICKNESS 0.125 OR 0.150

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS-026 BBC	DRAWING NUMBER: SOT1571-1	REVISION: F	
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Figure 81. SOT1571-1 Rev. F - PCB design guidelines - solder paste stencil

## 18 References

Obtain additional information on related NXP products and application solutions through the documents and URLs listed below.

- (1) **AN5238** - FS6500 and FS4500 Safe System Basis Chip Hardware Design and Product Guidelines - Application Note  
<https://www.nxp.com/AN5238-DOWNLOAD>
- (2) **AN4388** - Quad Flat Package (QFP)  
[https://www.nxp.com/files/analog/doc/app\\_note/AN4388.pdf](https://www.nxp.com/files/analog/doc/app_note/AN4388.pdf)
- (3) **FS6500-FS4500PDTCALC** - Power dissipation tool (Excel File)  
[https://www.nxp.com/files/analog/software\\_tools/FS6500-FS4500-power-dissipation-calculator.xlsx](https://www.nxp.com/files/analog/software_tools/FS6500-FS4500-power-dissipation-calculator.xlsx)
- (4) **V<sub>CORE</sub> compensation network simulation tool (CNC)**<sup>[1]</sup>
- (5) **FMEDA** - FS6500/FS4500 ASILB FMEDA<sup>[1]</sup>
- (6) **UM11498** - FS6500/FS4500 ASILB Safety manual – user guide
- (7) **KITFS6507LAEVEM** - FS6507, System Basis Chip, ASIL B, DC-DC 0.8 A Vcore, LDT, CAN, LIN  
<https://www.nxp.com/KITFS6507LAEVEM>
- (8) **KITFS4508CAEEVEM** - FS4508, System Basis Chip, ASIL B, Linear 0.5 A Vcore, FS1b, LDT, CAN  
<https://www.nxp.com/KITFS4508CAEEVEM>
- (9) **FS6500 product summary page** -  
<https://www.nxp.com/FS6500>
- (10) **FS4500 product summary page** -  
<https://www.nxp.com/FS4500>
- (11) **Analog power management homepage** -  
<https://www.nxp.com/products/power-management>
- (12) **ISO 11898-2:2003** - Road vehicles — Controller area network (CAN) — Part 2: High-speed medium access unit  
<https://www.iso.org/standard/33423.html>
- (13) **ISO 11898-5:2007** - Road vehicles — Controller area network (CAN) — Part 5: High-speed medium access unit with low-power mode  
<https://www.iso.org/contents/data/standard/04/12/41284.html>
- (14) **ISO 7637-2:2011** - Road vehicles — Electrical disturbances from conduction and coupling — Part 2: Electrical transient conduction along supply lines only  
<https://www.iso.org/standard/50925.html>
- (15) **ISO 10605:2008** - Road vehicles — Test methods for electrical disturbances from electrostatic discharge  
<https://www.iso.org/standard/41937.html>
- (16) **IEC 61000-4-2:2008** - Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test  
<https://webstore.iec.ch/publication/4189>
- (17) **JESD51-6** - INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - FORCED CONVECTION (MOVING AIR)
- (18) **JESD51-7** - HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES
- (19) **JESD22-A114F** - ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING HUMAN BODY MODEL (HBM)
- (20) **JESD22-C101F** - FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS
- (21) **MIL-STD-883-1, Method 1012.1** - TEST METHOD STANDARD MICROCIRCUITS

- (22) **LIN Specification Package Revision 2.1:2006**  
[https://www.lin-cia.org/fileadmin/microsites/lin-cia.org/resources/documents/LIN-Spec\\_Pac2\\_1.pdf](https://www.lin-cia.org/fileadmin/microsites/lin-cia.org/resources/documents/LIN-Spec_Pac2_1.pdf)
- (23) **LIN Specification Package Revision 2.2A:2010**  
[https://www.lin-cia.org/fileadmin/microsites/lin-cia.org/resources/documents/LIN\\_2.2A.pdf](https://www.lin-cia.org/fileadmin/microsites/lin-cia.org/resources/documents/LIN_2.2A.pdf)
- (24) **SAE J2602-2:201211 - LIN Network for Vehicle Applications Conformance Test**  
[https://www.sae.org/standards/content/j2602/2\\_201211/](https://www.sae.org/standards/content/j2602/2_201211/)

[1] Available upon request.

## 19 Revision history

Table 116. Revision history

Document ID	Release date	Description
FS6500-FS4500-ASILB v. 4	05 August 2024	<ul style="list-style-type: none"> <li>• Product data sheet</li> <li>• CIN 202407025I</li> <li>• Supersedes FS6500-FS4500-ASILB v.3.0</li> <li>• Updated document title from "FS6500, FS4500: ASIL B" to "FS6500-FS4500-ASILB"</li> <li>• Updated status from confidential to public</li> <li>• Updated Revision history to reflect new NXP standard</li> <li>• <a href="#">Section 11.6</a>: changed "(±1.0 % for 5.0 V configuration and ±1.5 % for 3.3 V configuration)," to "(±1.0 % for 5.0 V and 3.3 V configuration)," in the second paragraph.</li> <li>• Changed "master" to "primary" and "slave" to "secondary" throughout, except for LIN topics <a href="#">Section 9</a> and <a href="#">Section 11.12.3</a>, where "master" was changed to "commander" and "slave" to "responder"</li> <li>• Revised <a href="#">Figure 3</a></li> <li>• <a href="#">Section 12.1.7.2</a>: replaced V<sub>PRE_UV_L_4P3</sub> with V<sub>PRE_UV_4P3</sub></li> <li>• Revised <a href="#">Figure 15</a></li> <li>• Revised <a href="#">Figure 16</a></li> <li>• <a href="#">Section 12.5.2</a>: added "regardless of the LFSR register value." to the end of the last paragraph</li> <li>• <a href="#">Section 12.5.2.5</a> changed INIT_WD to INIT_WD_CNT</li> <li>• Revised <a href="#">Figure 18</a> and figure title</li> <li>• Revised <a href="#">Section 12.5.3</a></li> <li>• In <a href="#">Section 12.8.1</a>, removed subhead "Calibration example:" and subsequent text</li> <li>• Added <a href="#">Section 12.8.2</a></li> <li>• In <a href="#">Section 13.1.1</a>, changed "Master Out Slave In" to "primary out, secondary in" and "Master IN slave out" to "primary in, secondary out"</li> <li>• Updated <a href="#">Figure 24</a> title</li> <li>• Revised <a href="#">Figure 61</a></li> <li>• In <a href="#">Section 12.7.4</a>: changed last sentence of first paragraph from "The voltage accuracy is ±1.0 % for 5.0 V configuration and ±1.5 % for 3.3 V configuration ..." to "The voltage accuracy is ±1.0 % for 5.0 V and 3.3 V configuration ..."</li> <li>• In <a href="#">Section 13.1.2</a>: revised all three paragraphs and corrected punctuation</li> <li>• In <a href="#">Section 13.1.4</a>: corrected figure references</li> <li>• <a href="#">Figure 69</a>: corrected the name of the bit 4 field</li> </ul>



Table 116. Revision history...continued

Document ID	Release date	Description
		<ul style="list-style-type: none"> <li>• <a href="#">Table 39</a>: revised the description of the DEV_REV_2:0 bit field</li> <li>• Revised <a href="#">Figure 70</a></li> </ul>
FS6500-FS4500-ASILB v.3.0	09 April 2021	<ul style="list-style-type: none"> <li>• Product data sheet</li> <li>• <a href="#">Section 1</a>: replaced "0.8 A" by "1.5 A"</li> <li>• <a href="#">Section 2</a>: replaced "Family of devices to supply MCU core from 1.0 V to 5.0 V, with SMPS (0.8 A) or LDO (0.5 A)" to "Family of devices to supply MCU core from 1.0 V to 5.0 V, with SMPS (0.8 A, 1.5 A or 2.2 A) or LDO (0.5 A)"</li> <li>• <a href="#">Section 5</a>: updated <a href="#">Table 1</a> and <a href="#">Table 2</a> (added new part numbers)</li> <li>• <a href="#">Section 12.7.8</a>: updated description and <a href="#">Figure 48</a></li> </ul>
FS6500-FS4500-ASILB v.2.0	11 January 2021	<ul style="list-style-type: none"> <li>• Product data sheet</li> <li>• Revised data sheet status from "Preliminary" to "Product".</li> <li>• <a href="#">Section 5.2</a>, revised <a href="#">Table 2</a> changing "PC33..." parts to "MC33..."</li> <li>• <a href="#">Section 7.2</a>, pin number 11, removed "VKAM can be enabled or disabled by default at power up. The differentiation is made by part numbers."</li> <li>• <a href="#">Section 11.1</a>, revised the third bullet adding ", and LIN interface (LIN up to Rev. 2.2<sup>(22)</sup>, (23)/SAEJ2602-2<sup>(24)</sup>), "</li> <li>• <a href="#">Section 13.3.22</a>, <a href="#">Table 64</a> as follows: <ul style="list-style-type: none"> <li>– MOSI bit4: revised "RESERVED" to "LIN_MOD1".</li> <li>– MOSI bit3: revised "RESERVED" to "LIN_MOD0".</li> <li>– MOSI bit2: revised "RESERVED" to "LIN_AUTO_DIS".</li> <li>– MOSI bit0: revised "RESERVED" to "LIN_WU".</li> </ul> </li> </ul>
FS6500-FS4500-ASILB v.1.3	11 June 2020	<ul style="list-style-type: none"> <li>• Preliminary data sheet</li> <li>• Added missing "Security" disclaimer to the legal section.</li> </ul>
FS6500-FS4500-ASILB v.1.2	20 October 2020	<ul style="list-style-type: none"> <li>• Preliminary data sheet</li> <li>• <a href="#">Section 5.2</a>, revised all parts ending with "NAE" or "CAE" to replace "PC33" with "MC33" at the start of the part number.</li> </ul>
FS6500-FS4500-ASILB v.1.1	26 October 2020	<ul style="list-style-type: none"> <li>• Preliminary data sheet</li> <li>• <a href="#">Section 5.2</a>, revised parts list.</li> </ul>
FS6500-FS4500-ASILB v.1.0	15 October 2020	<ul style="list-style-type: none"> <li>• Initial release</li> </ul>

## Legal information

### Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 5 August 2024

Document identifier: FS6500-FS4500-ASILB