MC34063D
DC/DC Converter Control Circuits

DESCRIPTION

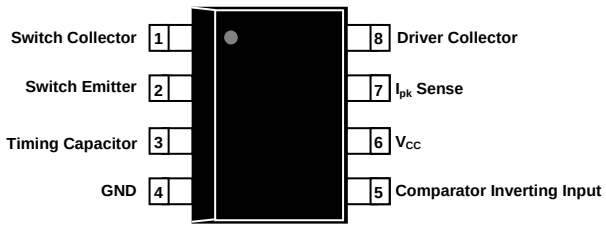
The MC34063D is a monolithic control circuit containing the primary functions required for DC-to-DC converter. This device consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. Employing a minimum number of external components, the MC34063D is designed for Step-Down, Step-Up and Voltage-Inverting applications.

FEATURES

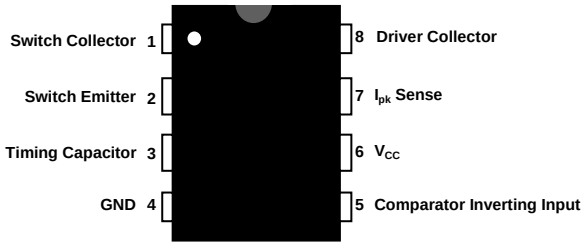
- Operation from 3V to 40V
- Active Current Limiting
- Low Quiescent Current: 3mA
- Output Switch Current in Excess of 1.5A
- Adjustable Output Voltage
- Frequency Operation to 100 kHz
- 2% Reference Accuracy

PIN CONFIGURATION – Top View

8L SOIC



8L PDIP



PACKAGE TOP MARKING:
(For 8L SOIC/PDIP)

MC34063 **FYMXXXS** **GYYWW**

Line 1: Device
Line 2: Lot No. Code
F – Foundry Code (G)
YMXXX – 5 Character Lot No.
S – Split Code
Line 3: Date Code
G – Assembly Vendor Code
YY – Year
WW – Workweek

ORDERING INFORMATION

MC34063D D8 13

Circuit Type:
DC/DC Converter Control Circuits

Package Style:
D8 = SOIC/8L
N8 = PDIP/8L

Packaging Option:
T = Tube
13 = Tape and Reel (13" Reel Dia)

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Supply Voltage		V_{CC}	40	V
Comparator Input Voltage Range		V_{IR}	-0.3 ~ +40	V
Switch Collector Voltage		$V_{C(sw)}$	40	V
Switch Emitter Voltage		V_{SWE}	40	V
Switch Collector to Emitter Voltage		V_{CE}	40	V
Driver Collector Voltage		$V_{C(DR)}$	40	V
Switch Current		I_{SW}	1.5	A
Tamb=25°C	8L PDIP	P_D	1.25	W
Power Dissipation	8L SOIC		0.625	
Operating Ambient Temperature Range		T_{opr}	-40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C
Operating Junction Temperature		T_{opJ}	120	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, Ta = 25°C, unless otherwise specified)

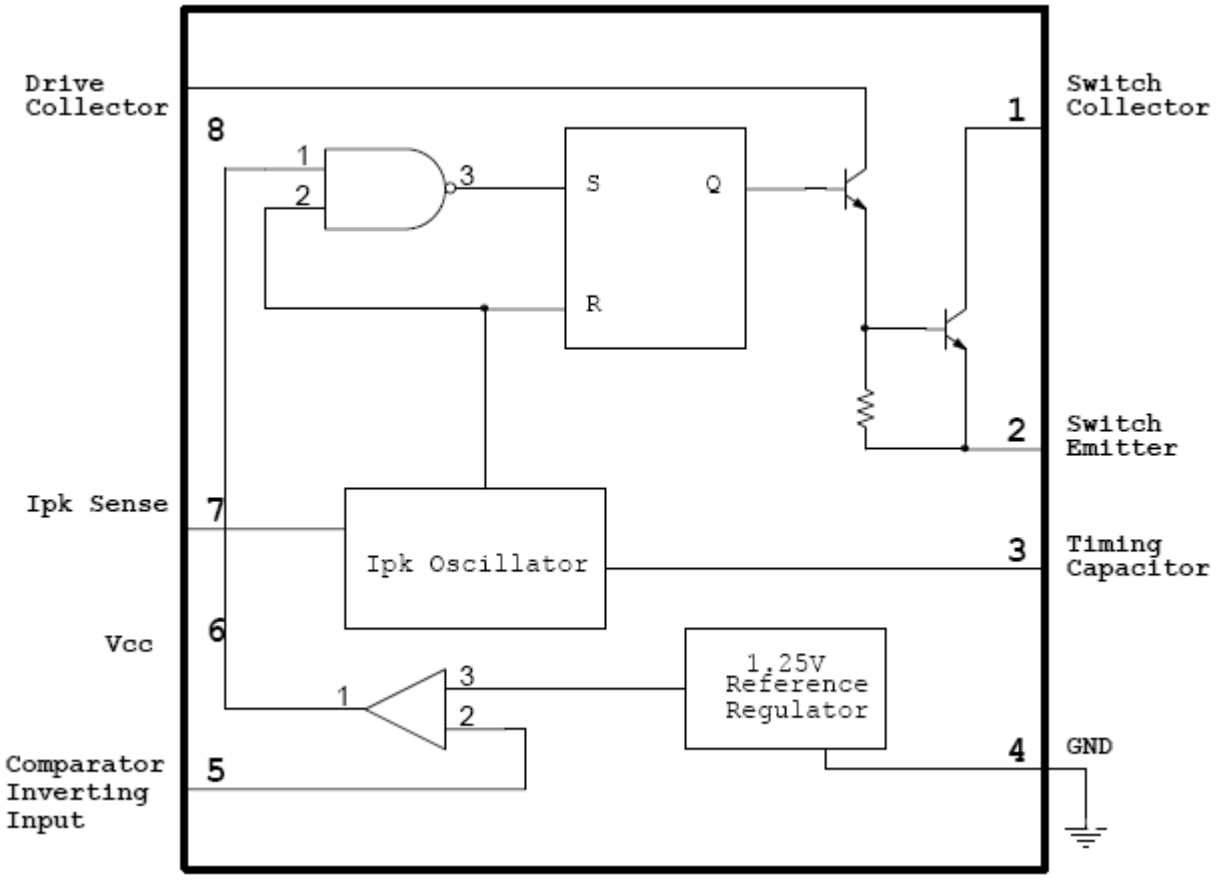
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator						
Charging Current	I_{chg}	Vcc=5~40V, T_A=25°C	24	33	42	µA
Discharge Current	I_{dischg}	Vcc=5~40V, T_A=25°C	140	200	260	µA
Voltage Amplitude	V_{OSC}	T_A=25°C	-	0.6	-	V
Discharge to Charge Current Ratio	K	V_{PIN7}=V_{CC}, T_A=25°C	5.2	6.0	7.5	
Current Limit Sense Voltage	V_{IPK}	I_{dischg}=I_{chg}, T_A=25°C	250	300	350	mV
Output Switch						
Saturation Voltage Darlington Connection	$V_{CE(sat)1}$	I_{SW}=1.0A,$V_{C(SW)}$=$V_{C(DR)}$	-	1.0	1.3	V
Saturation Voltage	$V_{CE(sat)2}$	I_{SW}=1.0A, $I_{C(DR)}$=50mA		0.4	0.7	V
DC Current Gain	h_{FE}	I_{SW}=1.0A, V_{CE}=5.0V	35	150	-	
Collector Off-State Current	$I_{CC(off)}$	V_{CE}=40V, T_A=25°C	-	10	100	nA
Comparator						
Threshold Voltage	V_{FB}		1.227	1.250	1.273	V
Threshold Voltage Line Regulation	ΔV_{FB}	V_{CC}=5~40V	-	1.5	6	mV
Input Bias Current	I_{IB}	V_{IN}=0	-	40	400	nA
Total Device						
Supply Current	I_{CC}	V_{CC}=5~40V,V_{PIN7}=V_{CC} V_{PIN5}>V_{FB}, CT =0.001µF Pin7=Gnd Remaining pins open	-	3	4	mA

APPLICATION INFORMATION

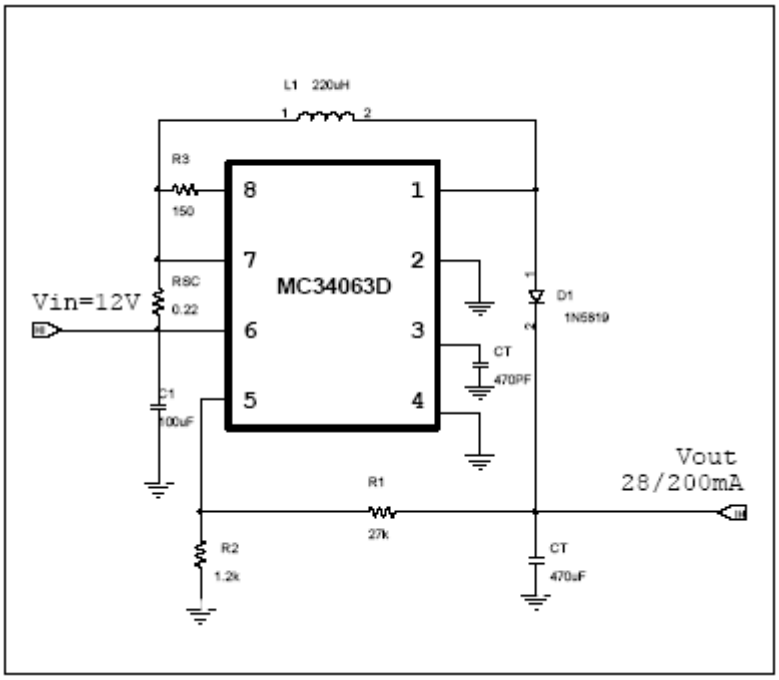
V_{sat} Saturation voltage of the output switch;
t_{on} Output Switch on Time; t_{off} Output Switch off Time;
V_F Forward voltage drop of the output rectifier;
$F_{(min)}$ Minimum desired output switching frequency at the selected values for Vin and Iout.

Calculation	Step-Down	Step-up	Voltage-Inverting
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in(max)} - V_{sat}}$
$(t_{on} + t_{off})max$	$1/F_{min}$	$1/F_{min}$	$1/F_{min}$
C_T	$4 \times 10^{-5}\ t_{on}$	$4 \times 10^{-5}\ t_{on}$	$4 \times 10^{-5}\ t_{on}$
$I_{C(SW)}$	$2 \times I_{out(max)}$	$2 \times I_{out(max)}\ (t_{on} + t_{off})/t_{off}$	$2 \times I_{out(max)}\ (t_{on} + t_{off})/t_{off}$
R_S	$0.3/I_{C(SW)}$	$0.3/I_{C(SW)}$	$0.3/I_{C(SW)}$
$L_{(min)}$	$\frac{V_{in(min)} - V_{sat}}{I_{PK(SW)}} \times t_{on(max)}$	$\frac{V_{in(min)} - V_{sat}}{I_{PK(SW)}} \times t_{on(max)}$	$\frac{V_{in(min)} - V_{sat}}{I_{PK(SW)}} \times t_{on(max)}$
C_O	$\frac{I_{PK(SW)} \times (t_{on} + t_{off})}{8 \times V_{ripple(P-P)}}$	$\frac{I_{out} \times t_{on}}{V_{ripple(P-P)}}$	$\frac{I_{out} \times t_{on}}{V_{ripple(P-P)}}$

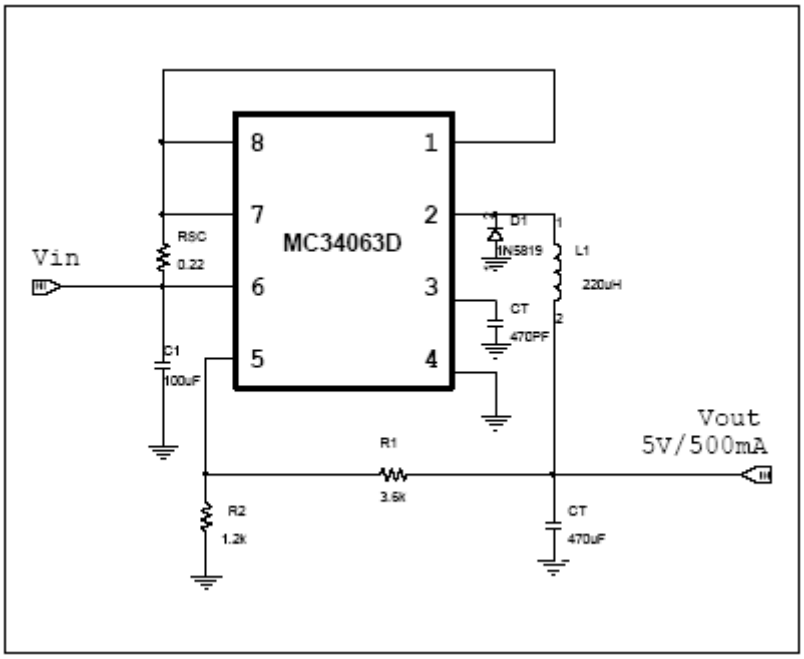
BLOCK DIAGRAM



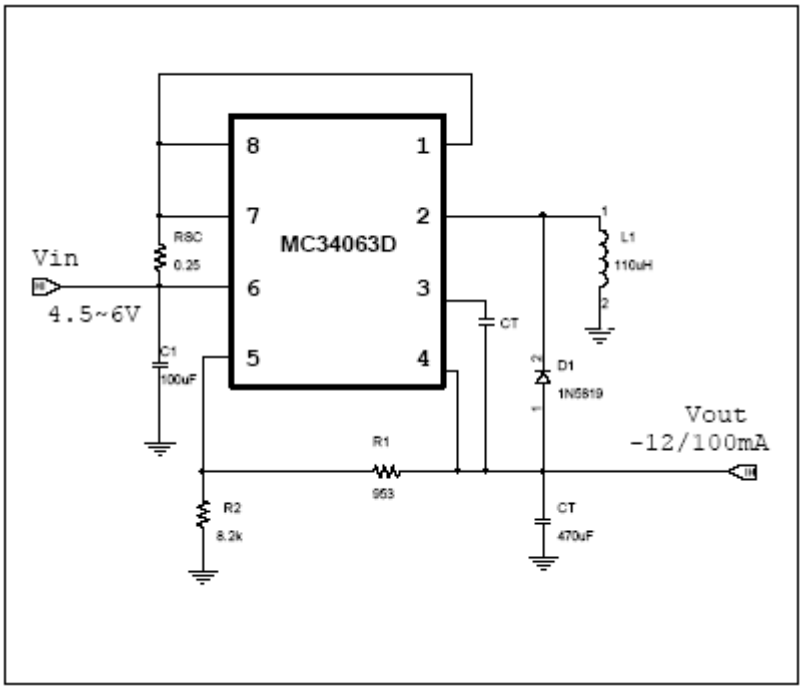
STEP-UP CONVERTER



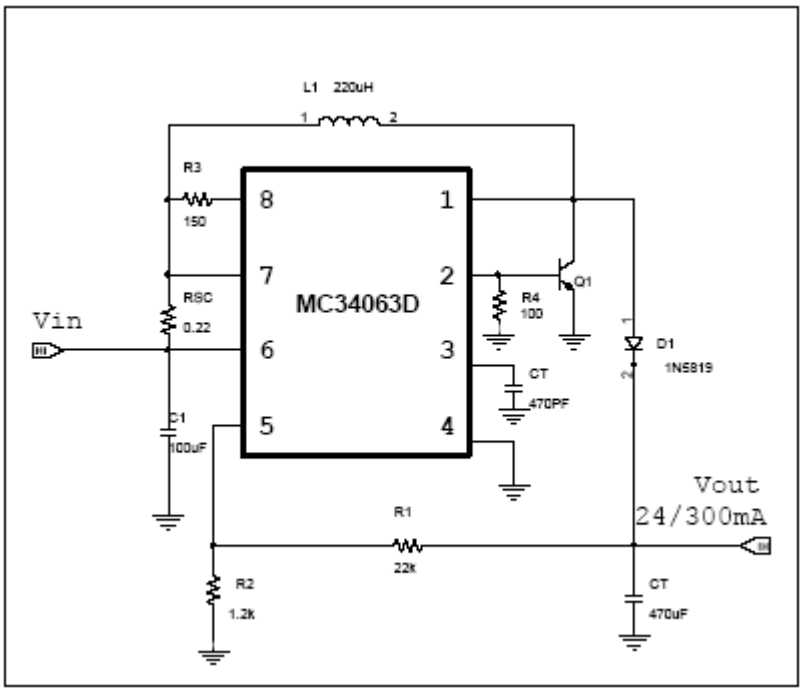
STEP-DOWN CONVERTER



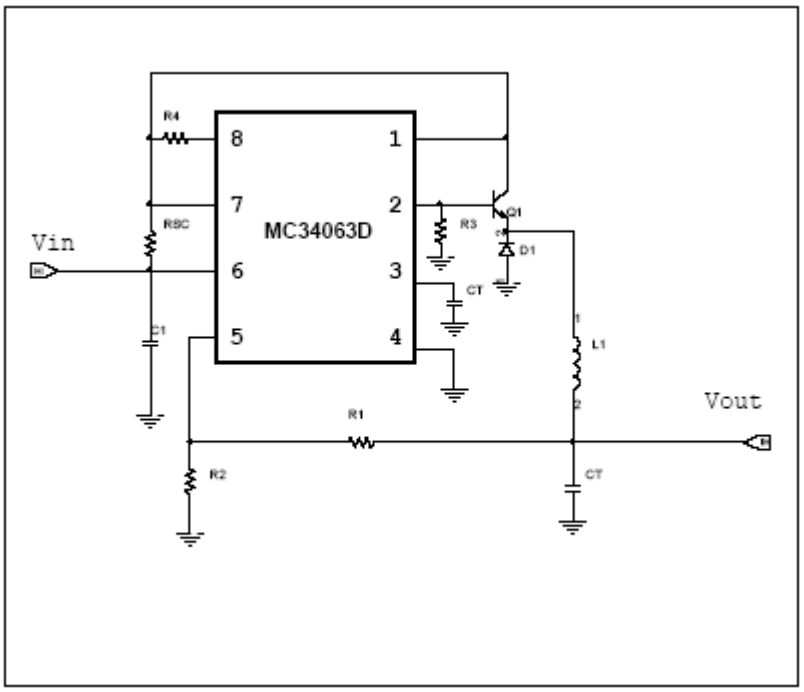
VOLTAGE INVERTING CONVERTER



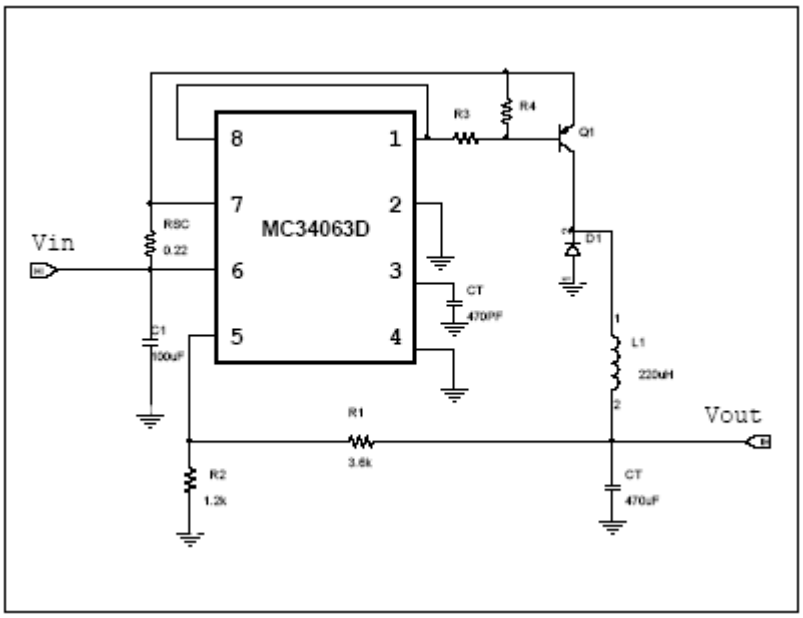
STEP-UP WITH EXTERNAL NPN SWITCH



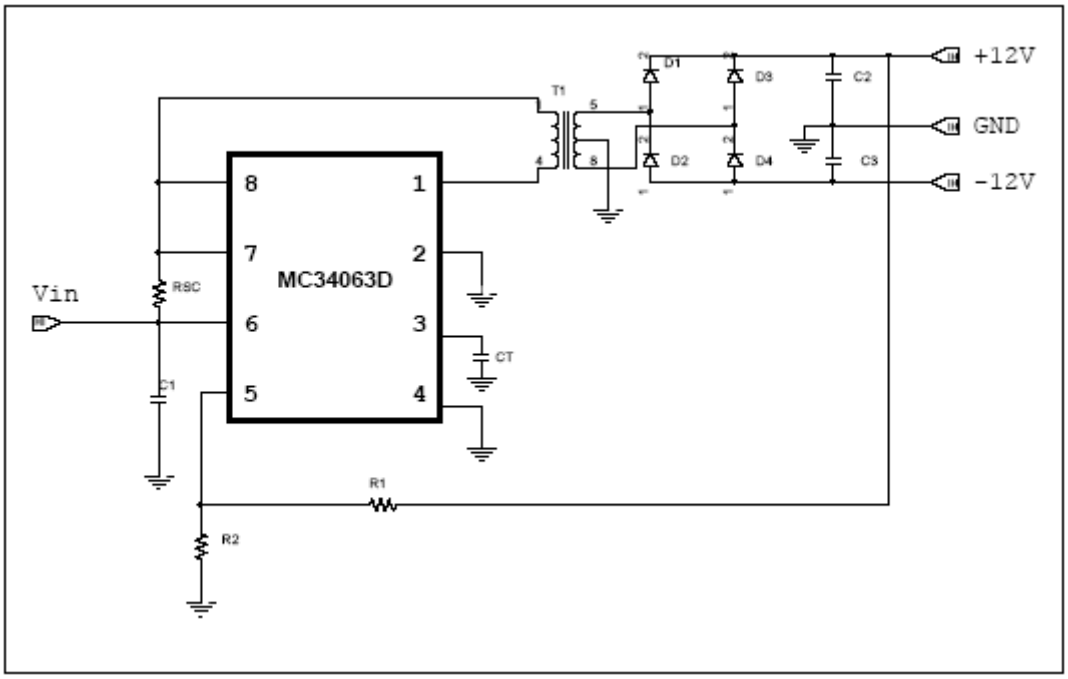
STEP-DOWN WITH EXTERNAL NPN SWITCH



STEP-DOWN WITH EXTERNAL PNP SWITCH

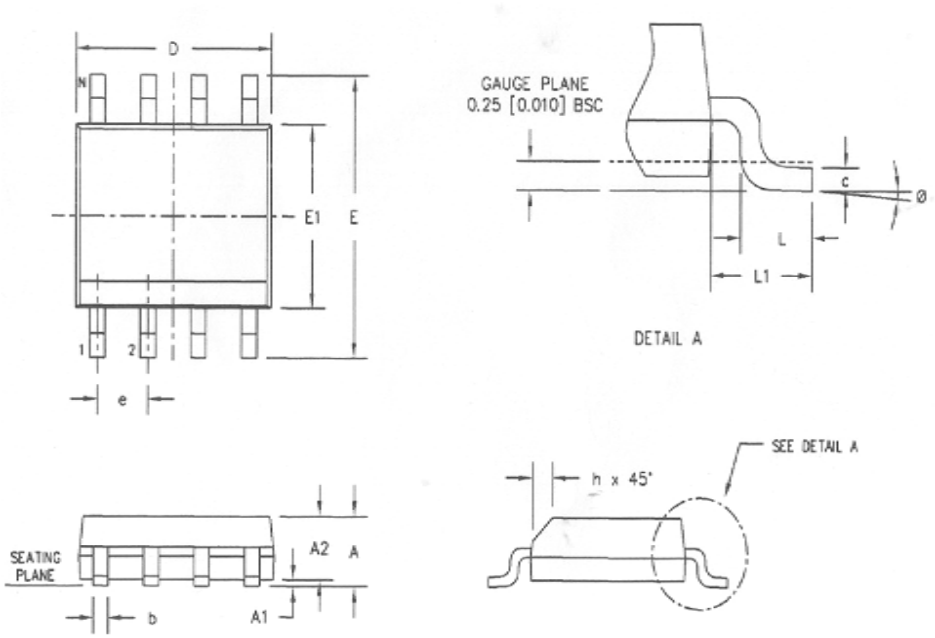


DUAL OUTPUT VOLTAGE



8L-SOIC PACKAGE DIMENSION

8-Lead SOIC Plastic
Surface Mounted Package
SLI Package Code: D8

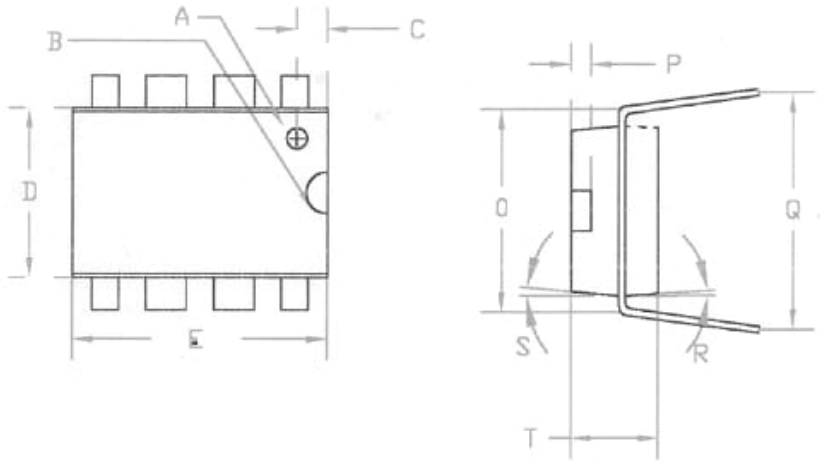


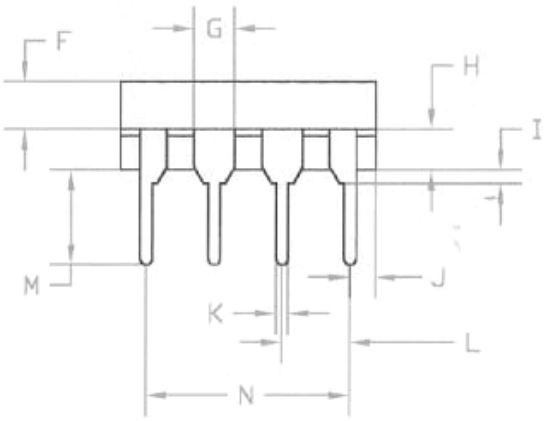
	DIMENSION IN INCHES			DIMENSION IN MM		
SYM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.059	0.062	0.065	1.50	1.57	1.65
A1	0.004	0.008	0.010	0.10	0.20	0.25
A2	0.051	0.054	0.057	1.30	1.37	1.45
b	0.013	0.016	0.020	0.33	0.41	0.51
c	0.007	0.008	0.010	0.18	0.20	0.25
D	0.191	0.193	0.195	4.85	4.90	4.95
E1	0.151	0.153	0.155	3.84	3.89	3.94
E	0.228	0.234	0.240	5.79	5.94	6.10
e	0.050			1.27		
L	0.020	0.024	0.032	0.51	0.61	0.81
L1	0.039	0.041	0.043	0.99	1.04	1.09
Ø	0*	-	B*	0*	-	B*
h	0.011	0.015	0.019	0.28	0.38	0.48

NOTES:
1. **DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.**
2. **COPLANARITY APPLIES TO THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.003" [0.08 mm].**
3. **BASED FROM JEDEC NS-012 VARIATION AA.**

8L-PDIP PACKAGE DIMENSION

8-Lead PDIP Plastic
SLI Package Code: N8

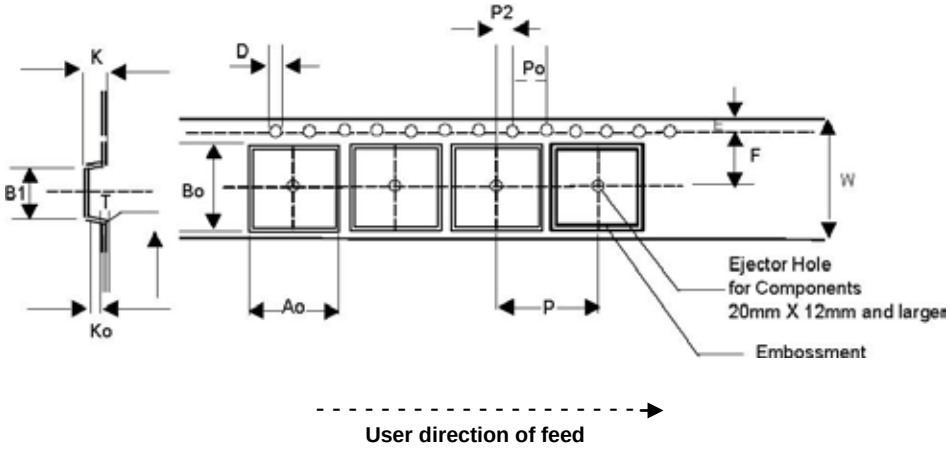




SYMBOL	INCHES			
	MIN	MAX	NOMINAL	TOLERANCE
A			Ø0.031X	0PT0.015
B			r 0.030	
C			0.045	
D			0.250	
E			0.370	±0.005
F			0.060	
G			0.060	
H			0.060	±0.002
I			0.020	
J			0.0375	
K	0.16	0.022	0.019	±0.003
L			0.100	
M	0.145	0.155	0.150	±0.005
N			0.300	
O			0.300	
P			0.030	
Q	0.320	0.380	0.350	±0.03
R			3°	
S			5°	
T			0.130	

PACKAGE MECHANICAL DRAWING

Surface Mountable Tape & Reel Specifications in mm (inch)
(SOIC)



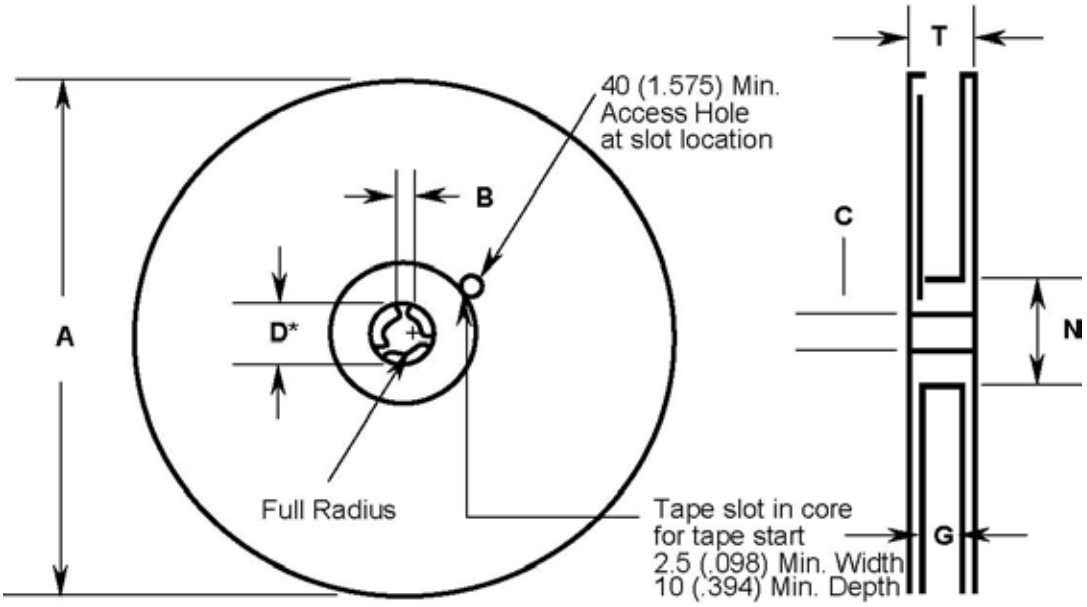
User direction of feed

Tape Size (W)	D	E	P0	T (Max)	A0, B0, K0	T1 (Max)	Constant
8, 12, 16, 24mm	1.55±0.05 (.061±.002)	1.75±0.10 (.069±.004)	4.0±0.10 (.157±.004)	0.400 (.016)	See Note	0.100 (.004)	Dimensions

Tape Size (W)	B1 Max.	D1 Min.	F	K Max.	P2	
8 mm	4.2 (.165)	1.0 (.039)	3.5±0.05 (.138±.002)	2.4 (.094)	2.0±.05	
12 mm	8.2 (.323)	1.5 (.059)	5.5±0.05 (.217±.002)	4.5 (.177)	.079±.002	Variable Dimensions

Per Package Requirement					
Components		Tape Width (W) mm	Cavity Pitch (P) mm	Devices per Reel	
				7” Reel	13” Reel
SOIC	8L	12	8	-	2500

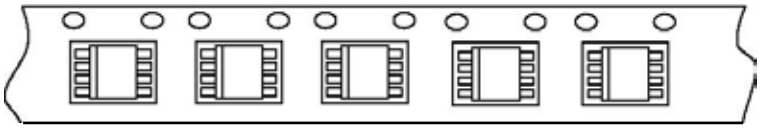
Note: Ao Bo Ko are determined by component size. The clearance between the component and the cavity must be within 0.05 [.002] min. to 0.50 [.020] max. for 8mm tape, 0.05 [.002] min to 0.65 [.026] max for 12mm tape.



REEL DIMENSIONS							
Tape Size	A Max.	B Min.	C	D* Min.	N Min.	G	T Max.
8mm	330 (12.992)	1.5 (.059)	13.0±0.20 (.152±.008)	20.2 (.795)	50 (1.973)	8.4±1.5 0.0 (.331±.059) 0.0	14.4 (.567)
12mm	330 (12.992)	1.5 (.059)	13.0±0.20 (.152±.008)	20.2 (.795)	50 (1.973)	12.4±2.0 0.0 (.488±.078) 0.0	14.4 (.567)

MECHANICAL POLARIZATION

SOIC-8L DEVICE



User direction of feed ->