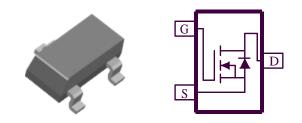
AO3414/MC3414

N-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOT-23 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY				
V _{DS} (V)	$\mathbf{r}_{\mathrm{DS(on)}}\left(\Omega ight)$	I _D (A)		
	$0.047 @ V_{GS} = 4.5V$	4.3		
20	$0.055@V_{GS} = 2.5V$	4.0		
	$0.087@V_{GS} = 1.8V$	3.2		



ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Ratings	Units	
Drain-Source Voltage		V _{DS}	20	V	
Gate-Source Voltage		V _{GS}	±8	V	
Continuous Drain Current ^a	T _A =25°C	In	4.3		
	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	1D	3.6	А	
Pulsed Drain Current ^b		I _{DM}	10		
Continuous Source Current (Diccle Conduction) ^a		Is	1.6	Α	
Power Dissipation ^a	$T_A=25^{\circ}C$	P _n	1.3	w	
	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	I D	0.9		
Operating Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Maximum	Units	
	t <= 5 sec	R _{THJA}	100	°C/W	
Maximum Junction-to-Ambient ^a	Steady-State		166		
Notes					

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a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

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Parameter	Chl	Tost Conditions	Limits			T Insid	
Farameter	Symbol Test Conditions		Min	Тур	Max	Unit	
Static							
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \text{ uA}$	0.4				
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = 8 V$			1	uA	
Zero Gate Voltage Drain Current		$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$			0.1	uA	
	I _{DSS}	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			1	uA	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = 5 V, V_{GS} = 4.5 V$	5			Α	
		$V_{GS} = 4.5 \text{ V}, I_D = 1 \text{ A}$			0.047		
Drain-Source On-Resistance ^A	r _{DS(on)}	$V_{GS} = 2.5 \text{ V}, I_D = 1 \text{ A}$			0.055	Ω	
		$V_{GS} = 1.8 \text{ V}, I_D = 1 \text{ A}$			0.087		
Forward Tranconductance ^A	g_{fs}	$V_{DS} = 5 V, I_{D} = 1 A$		16		S	
Diode Forward Voltage	V _{SD}	$I_{\rm S} = 1 \rm A, V_{\rm GS} = 0 \rm V$		0.6		V	
Dynamic ^b							
Total Gate Charge	Qg	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V},$		6			
Gate-Source Charge	Q_{gs}	$V_{\rm DS} = 10$ V, $V_{\rm GS} = 4.5$ V, $I_{\rm D} = 1$ A		1		nC	
Gate-Drain Charge	Q_{gd}	$I_{\rm D} = 1.71$		2			
Turn-On Delay Time	t _{d(on)}			8			
Rise Time	t _r	$V^{}_{\rm DD}$ = 10 V, $R^{}_{\rm L}$ = 6 $\Omega^{}_{}$, $R^{}_{\rm G}$ = 6 $\Omega^{}_{},$		16		ns	
Turn-Off Delay Time	t _{d(off)}	$v_{\text{GEN}} = 4.5 \text{ v}$		30			
Fall-Time	t _f			14			

Notes

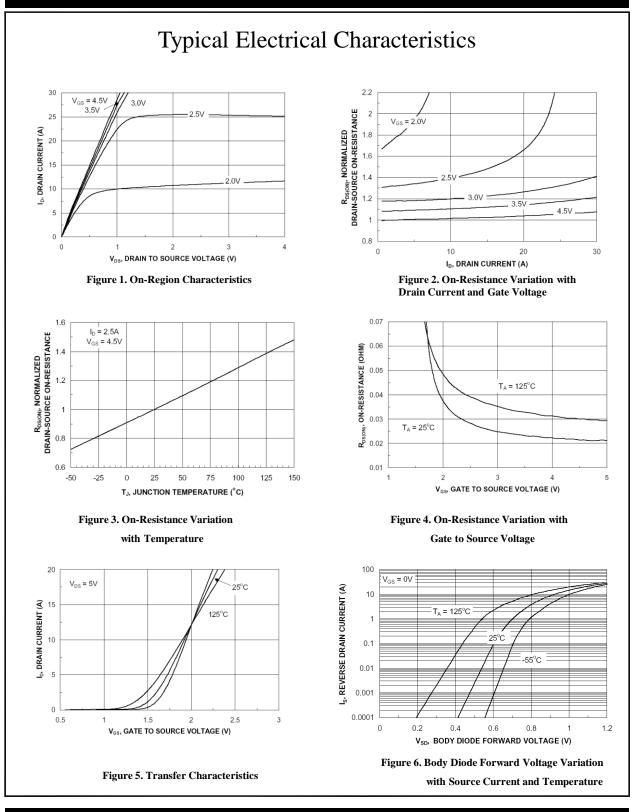
a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.

b. Guaranteed by design, not subject to production testing.

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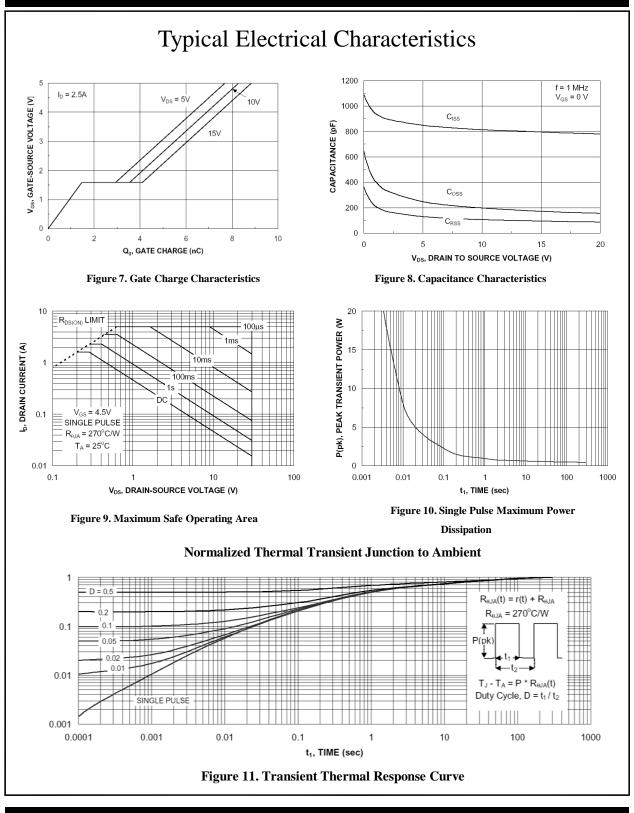
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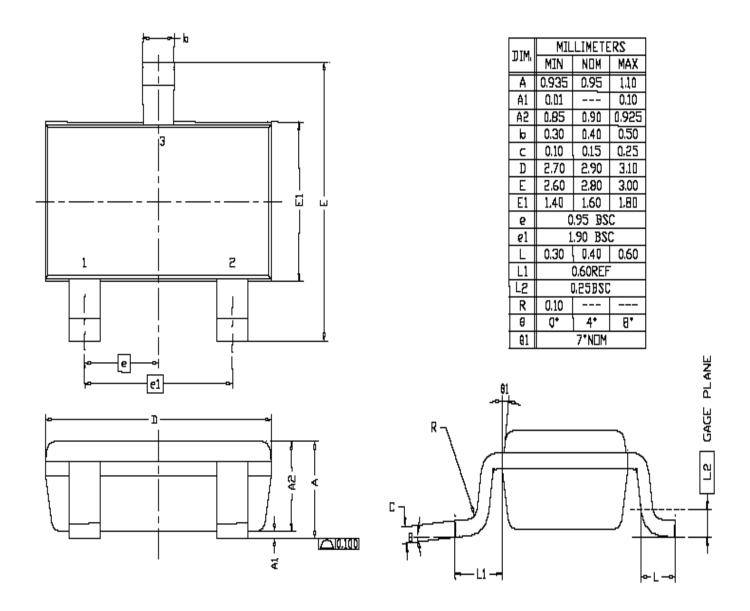
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Package Information



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