MOTOROLA Semiconductors

MC3459

Specifications and Applications Information

QUAD NMOS MEMORY ADDRESS DRIVER

The MC3459 is designed for high-speed driving of the highly capacitive Address select inputs for NMOS Memories. It is also useful in numerous applications requiring a high-current MTTL NAND gate. It is pin-compatible with the popular MC7400 Quad NAND gate.

- Fast Propagation Delay Time – 20 ns Typical with 360 pF Load
- Output Voltages Compatible with NMOS Memories
- Inputs Compatible in MTTL and MDTL Logic Families
- Output Loading Factor – 50

QUAD NMOS ADDRESS LINE DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

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L SUFFIX
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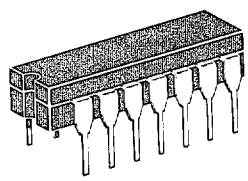
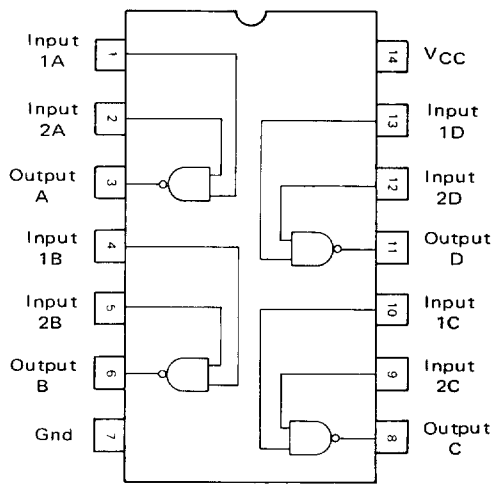
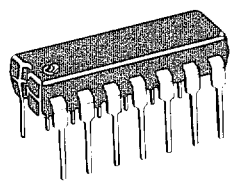
TO-116

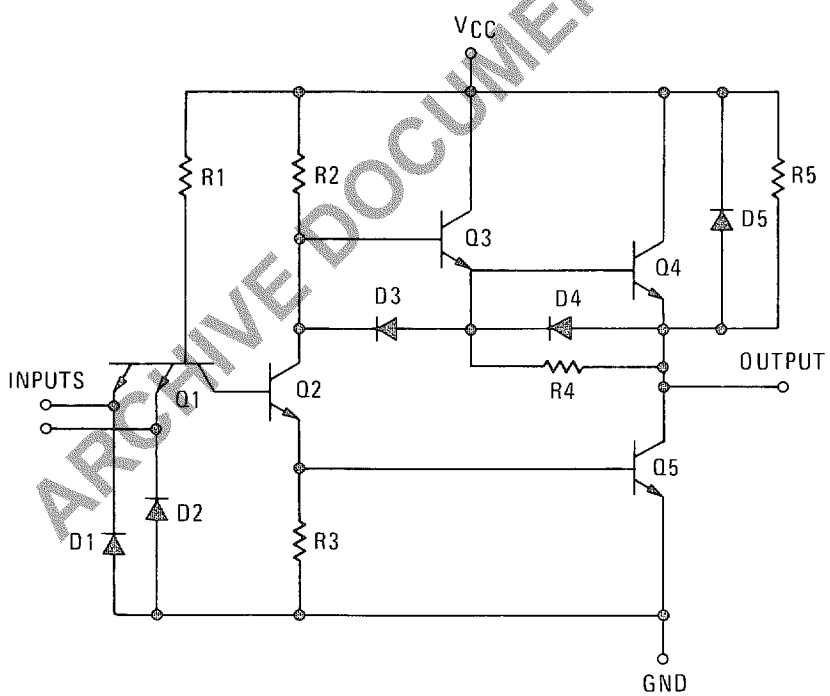




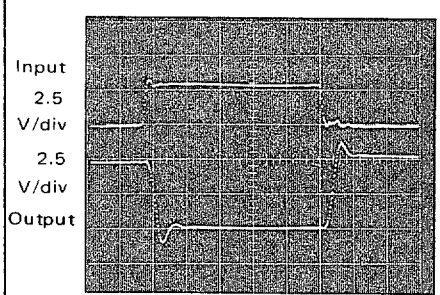


P SUFFIX
PLASTIC PACKAGE
CASE 646

REPRESENTATIVE CIRCUIT SCHEMATIC
(1/4 of Circuit Shown)



TYPICAL OPERATION



V_{CC} = 5.0 V, T_A = 25°C, 50 ns/div, C_L = 360 pF, R_S = 0 Ω

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MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.5	Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation (Package Limitation			
Ceramic Package @ T_A = 25°C	P_D	1000	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Plastic Package @ T_A = 25°C	P_D	830	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Ceramic Package @ T_C = 25°C	P_D	3.0	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	20	mW/°C
Plastic Package @ T_C = 25°C	P_D	1.8	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	14	mW/°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Junction Temperature	T_J		°C
Ceramic Package		175	
Plastic Package		150	
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, 4.75 V ≤ V_{CC} ≤ 5.25 V and 0 ≤ T_A ≤ 70°C)

Characteristic	Symbol	Min	Typ(1)	Max	Unit
Input Voltage – High Logic State	V_{IH}	2.0	–	–	V
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	V
Input Current – High Logic State					
(V_{CC} = 5.25 V, V_{IH} = 2.4 V)	I_{IH1}	–	–	80	μA
(V_{CC} = 5.25 V, V_{IH} = 5.5 V)	I_{IH2}	–	–	2.0	mA
Input Current – Low Logic State (V_{CC} = 5.25 V, V_{IL} = 0.4 V)	I_{IL}	–	–	-3.6	mA
Input Clamp Voltage (I_{IC} = -12 mA)	V_{IC}	–	–	-1.5	V
Output Voltage – High Logic State					V
(V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OH} = -640 μA)	V_{OH1}	3.2	–	–	
(V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OH} = -2.0 mA)	V_{OH2}	2.4	–	–	
Output Clamp Voltage (V_{CC} = 5.25 V, V_{IL} = 0 V, I_{OC} = 5.0 mA)	V_{OC}	–	5.8	6.75	V
Output Voltage – Low Logic State					V
(V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OL} = 640 μA)	V_{OL1}	–	–	0.3	
(V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OL} = 80 mA)	V_{OL2}	–	–	0.7	
Power Supply Current – Outputs High Logic State (V_{CC} = 5.25 V, V_{IL} = 0 V)	I_{CCH}	–	12	18	mA
Power Supply Current – Outputs Low Logic State (V_{CC} = 5.25 V, V_{IH} = 5.0 V)	I_{CCL}	–	85	122	mA

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V, T_A = 25°C, C_L = 360 pF)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time – High to Low Logic State	t_{PHL}	–	21	32	ns
Propagation Delay Time – Low to High Logic State	t_{PLH}	–	16	26	ns

(1) Typical values measured at T_A = 25°C, V_{CC} = 5.0 V.

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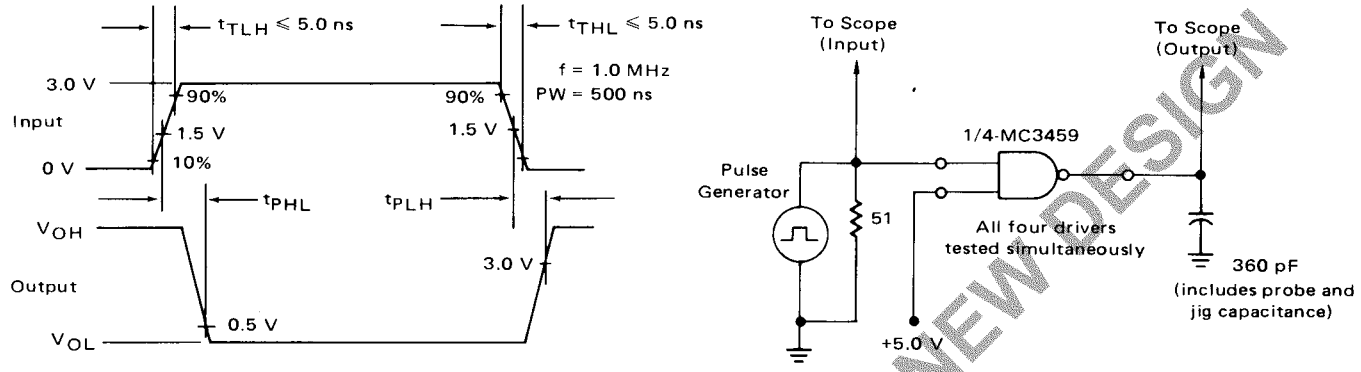
Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES



TYPICAL PREFORMANCE CURVES

FIGURE 2 – POWER CONSUMPTION versus OPERATING FREQUENCY

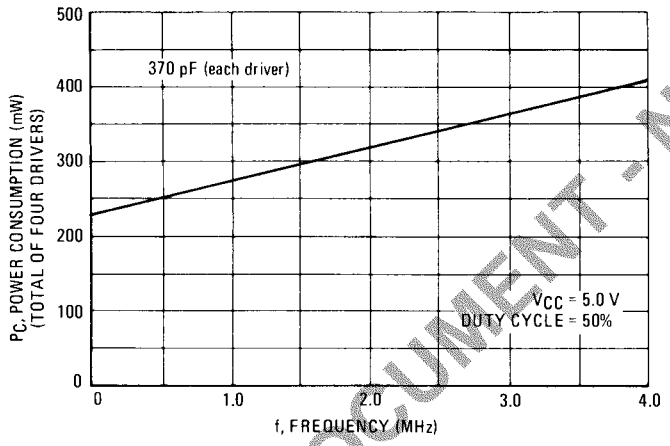


FIGURE 3 – OUTPUT VOLTAGE – HIGH LOGIC STATE versus OUTPUT CURRENT

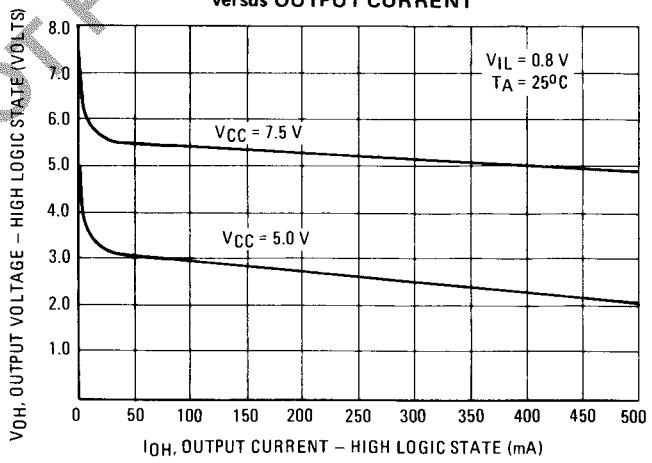


FIGURE 4 – OUTPUT VOLTAGE – HIGH LOGIC STATE versus OUTPUT CURRENT (Expanded Scale)

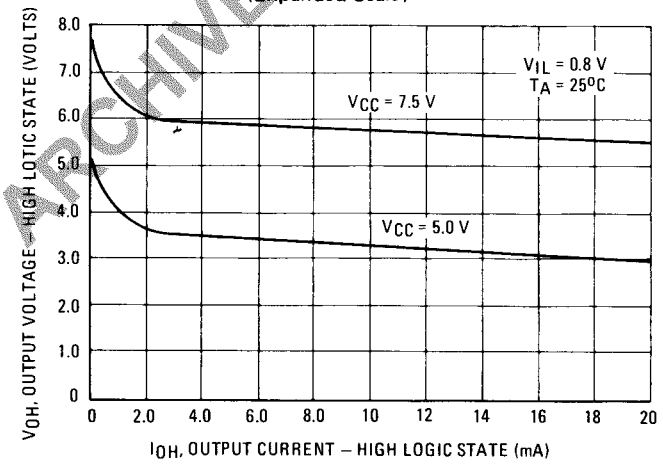
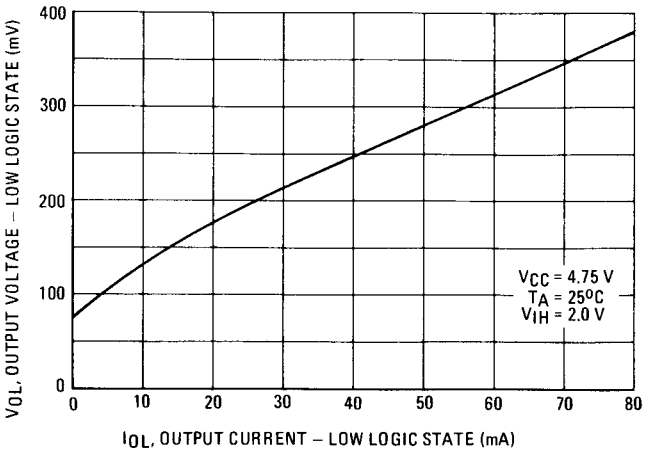


FIGURE 5 – OUTPUT VOLTAGE – LOW LOGIC STATE versus OUTPUT CURRENT



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APPLICATIONS SUGGESTIONS

A majority of the new N-Channel MOS memories have TTL logic compatible inputs that exhibit extremely low input current and capacitance (typically 5 pF to 10 pF). However, in a typical memory system (Figure 6) where some of the inputs such as Address lines have to be common, the total parallel input capacitance can be over 300 pF. Standard TTL logic gates have insufficient current drive capability to rapidly switch a high capacitive load; a high speed buffer, such as the MC3459, is required.

A considerable amount of noise can be generated during switching due to the high speed and high current drive capability of the MC3459. The high capacitive discharge current during the high to low transition, plus current spikes can result in a considerable amount of noise being generated on the ground lead. Current spikes are due to both the upper and lower output drive transistors being on for a short period of time during switching. This causes a very low impedance path between V_{CC} and ground.

In order to minimize the effects of these currents, the following layout rules should be followed:

1. The V_{CC} supply pin of each package should be bypassed with a low inductance 0.01 μF capacitor. The 0.01 μF capacitor will sustain the high surge currents required during switching.
2. There is a large amount of current out of the ground node during switching — the noise seen at this node will be proportional to the ground impedance. The impedance of the ground bus can be reduced by increasing its width. At least a 50 mil ground width is recommended.

Some of the NMOS memories with TTL logic compatible inputs do not actually meet the TTL logic level requirements in the input high state voltage (V_{IH}). There are N-Channel MOS memories with a V_{IH} minimum ranging from 2.4 V to 4.0 V. The MC3459 can directly interface with those N-Channel memories having a V_{IH} minimum of 3.0 V. The higher driver output levels can be accomplished by adding a pull-up resistor to V_{CC} or by increasing the V_{CC} voltage. There are some N-Channel MOS memories, such as the MCM7001, that have a supply requirement of 7.5 V. The high maximum supply voltage rating of the MC3459 can accommodate a 7.5 V V_{CC} supply without affecting its input TTL logic compatibility. Figure 4 gives the typical V_{OH} versus I_{OH} characteristics for both V_{CC} = 5.0 V and V_{CC} = 7.5 V. An expanded output characteristic curve of Figure 4 is illustrated in Figure 5.

The MC3459 can be used in a variety of applications including, high fan-out buffer (drives 50 standard TTL loads) and low impedance transmission line driver.

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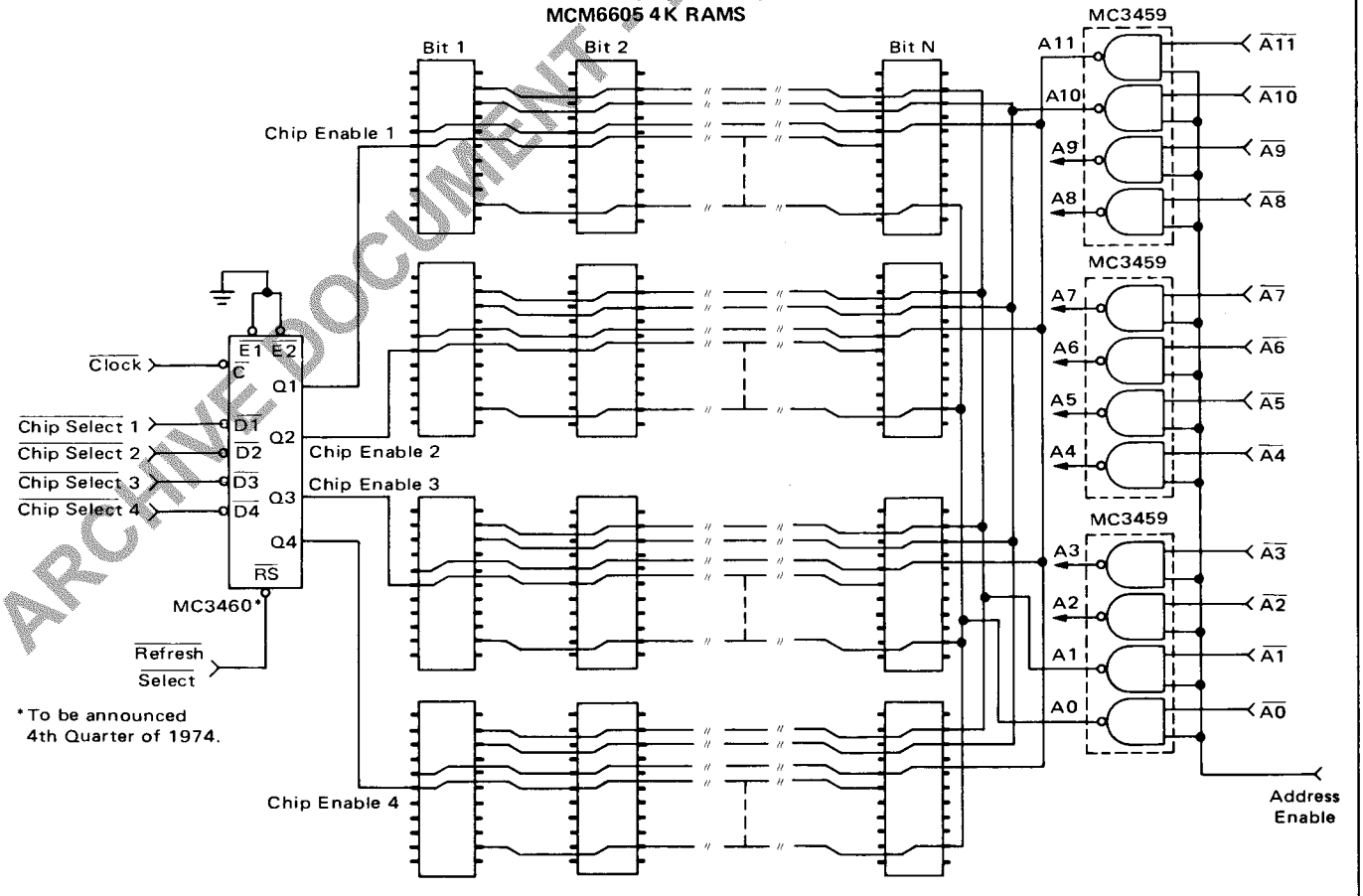
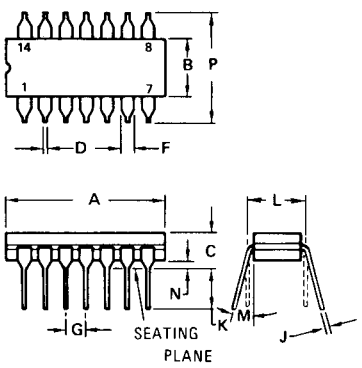
FIGURE 6 – TYPICAL APPLICATION
16 K X N Memory System Employing
MCM6605 4K RAMS



*To be announced 4th Quarter of 1974.

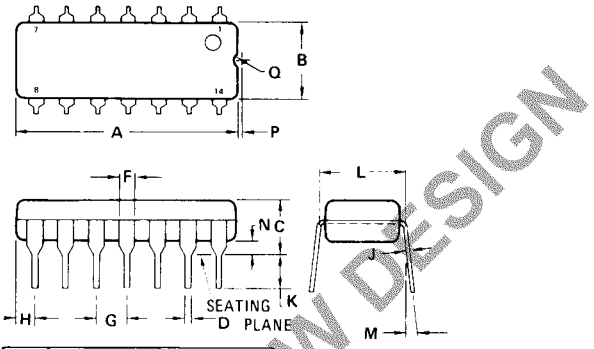
OUTLINE DIMENSIONS



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15^0	–	15^0
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

All JEDEC dimensions and notes apply.

CASE 632
TO-116
L SUFFIX
CERAMIC PACKAGE



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

CASE 646
P SUFFIX
PLASTIC PACKAGE

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