![Texas Instruments logo]

MC3486 Quadruple Differential Line Receiver with 3-State Outputs

1 Features

- Meets or exceeds the requirements of ANSI standards EIA/TIA-422-B and EIA/TIA-423-B and ITU Recommendations V.10 and V.11
- 3-State, TTL-compatible outputs
- Fast transition times
- Operates from single 5-V supply
- Designed to be interchangeable with Motorola™ MC3486

2 Applications

- Motor drives
- Factory automation and control

3 Description

The MC3486 is a monolithic quadruple differential line receiver designed to meet the specifications of ANSI Standards TIA/EIA-422-B and TIA/EIA-423-B and ITU Recommendations V.10 and V.11. The MC3486 offers four independent differential-input line receivers that have TTL-compatible outputs. The outputs utilize 3-state circuitry to provide a high-impedance state at any output when the appropriate output enable is at a low logic level.

The MC3486 is designed for optimum performance when used with the MC3487 quadruple differential line driver. It is supplied in a 16-pin package and operates from a single 5-V supply.
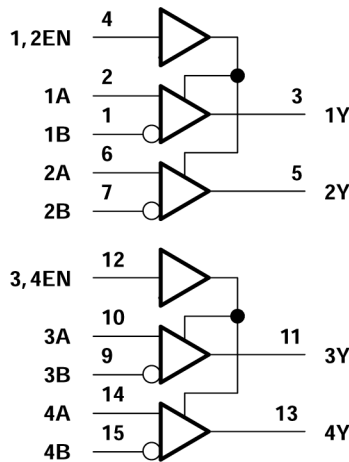
The MC3486 is characterized for operation from 0°C to 70°C.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
MC3486	D (SOIC, 16)	19.3 × 9.4 mm
	N (PDIP, 16)	19.3 × 9.4 mm
	NS (SOP, 16)	10.2 mm × 7.8 mm

(1) For more information, see Section 10.
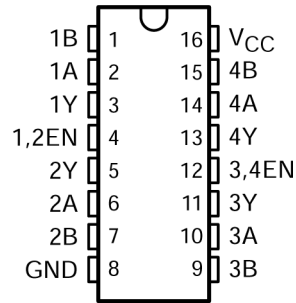(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Logic Diagram (Positive Logic)

Table of Contents

Product Folder Links: *MC3486*

4 Pin Configuration and Functions

```
              ┌───∪───┐
    1B  [ 1        16 ]  V_CC
    1A  [ 2        15 ]  4B
    1Y  [ 3        14 ]  4A
  1,2EN [ 4        13 ]  4Y
    2Y  [ 5        12 ]  3,4EN
    2A  [ 6        11 ]  3Y
    2B  [ 7        10 ]  3A
   GND  [ 8         9 ]  3B
              └───────┘
```

Figure 4-1. D, N, or NS Package
(Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 Differential Receiver Inverting Input
1A	2	I	Channel 1 Differential Receiver Non-Inverting Input
1Y	3	O	Channel 1 Single Ended Output
1,2 EN	4	I	Active High Enable for Channels 1 and 2
2Y	5	O	Channel 2 Single Ended Output
2A	6	I	Channel 2 Differential Receiver Non-Inverting Input
2B	7	I	Channel 2 Differential Receiver Inverting Input
GND	8	GND	Device GND
3B	9	I	Channel 3 Differential Receiver Inverting Input
3A	10	I	Channel 3 Differential Receiver Non-Inverting Input
3Y	11	O	Channel 3 Single Ended Output
3,4 EN	12	I	Active High Enable for Channels 3 and 4
4Y	13	O	Channel 4 Single Ended Output
4A	14	I	Channel 4 Differential Receiver Non-Inverting Input
4B	15	I	Channel 4 Differential Receiver Inverting Input
V_CC	16	PWR	Device VCC (4.75 V to 5.25 V)

(1)   Signal Types: I = Input, O = Output, I/O = Input or Output.

Product Folder Links: *MC3486*

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_I	Input voltage (A or B inputs)		±15	V
V_{ID} (see [2])	Differential input voltage		±25	V
	Enable input voltage		8	V
I_{OL}	Low-level output current		50	mA
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
T_{stg}	Storage temperature range	−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IC}	Common-mode input voltage			±7	V
V_{ID}	Differential input voltage			±6	V
V_{IH}	High-level enable input voltage	2			V
V_{IL}	Low-level enable input voltage			0.8	V
T_A	Operating free-air temperature	0		70	°C

5.3 Thermal Resistance Characteristics

THERMAL METRIC[1]		D (SOIC)	N (PDIP)	NS (SOP)	UNIT
		16-PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	60.6	88.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	48.1	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	40.6	50.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.4	27.5	13.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.8	40.3	50.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IT+}	Differential input high-threshold voltage	V_O = 2.7 V,	I_O = -0.4 mA			0.2	V
V_{IT-}	Differential input low-threshold voltage	V_O = 0.5 V,	I_O = -8 mA		- 0.2[(1)]		V
V_{IK}	Enable-input clamp voltage	I_I = -10 mA				-1.5	V
V_{OH}	High-level output voltage	V_{ID} = 0.4 V, See Note 4 and Figure 6-1	I_O = -0.4 mA,		2.7		V
V_{OL}	Low-level output voltage	V_{ID} = - 0.4 V, See Note 4 and Figure 6-1	I_O = 8 mA,			0.5	V
I_{OZ}	High-impedance-state output current	V_{IL} = 0.8 V,	V_{ID} = -3 V,	V_O = 2.7 V		40	μA
		V_{IL} = 0.8 V,	V_{ID} = 3 V,	V_O = 0.5 V		-40	
I_{IB}	Differential-input bias current	V_{CC} = 0 V or 2.25 V, Other inputs at 0 V	V_I = -10 V			-3.25	mA
			V_I = - 3 V			-1.5	
			V_I = 3 V			1.5	
			V_I = 10 V			3.25	
I_{IH}	High-level enable input current	V_I = 2.25 V				100	μA
		V_I = 2.7 V				20	
I_{IL}	Low-level enable input current	V_I = - 0.5 V				-100	μA
I_{OS}	Short-circuit output current	V_{ID} = 3 v,	V_O = 0,	See Note 5	-15	-100	mA
I_{CC}	Supply current	V_{IL} = 0				85	mA

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.
(2) Refer to ANSI Standards TIA/EIA-422-B and TIA/EIA-423-B for exact conditions.
(3) Only one output should be shorted at a time.

5.5 Switching Characteristics

V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 6-2		28	35	ns
t_{PLH}	Propagation delay time, low- to high-level output			27	30	ns
t_{PZH}	Output enable time to high level	See Figure 6-3		13	30	ns
t_{PZL}	Output enable time to low level			20	30	ns
t_{PHZ}	Output disable time from high level			26	35	ns
t_{PLZ}	Output disable time from low level			27	35	ns

6 Parameter Measurement Information
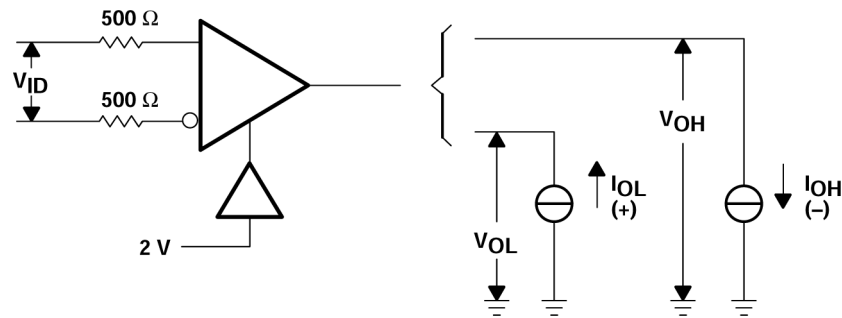
Figure 6-1. V_{OH}, V_{OL}
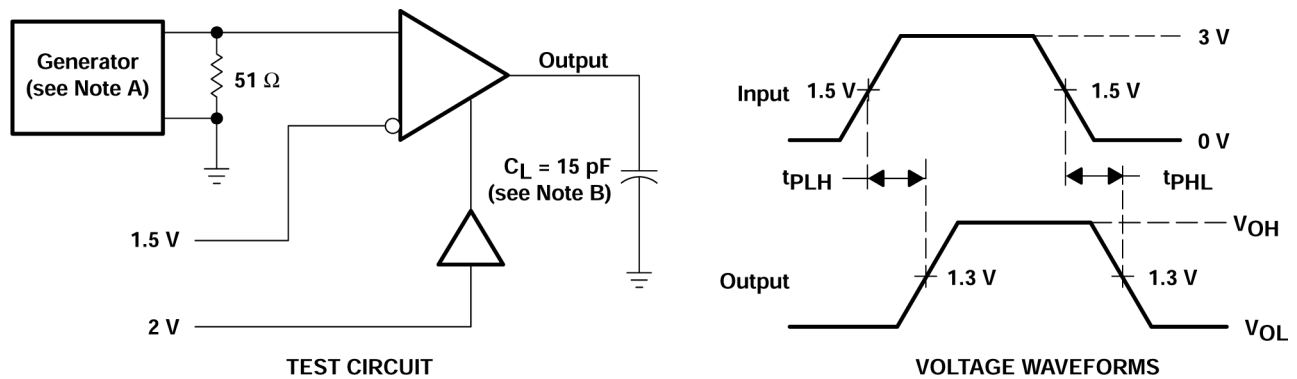
TEST CIRCUIT

VOLTAGE WAVEFORMS

A.   The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.

B. C_L includes probe and stray capacitance.

Figure 6-2. Test Circuit and Voltage Waveforms
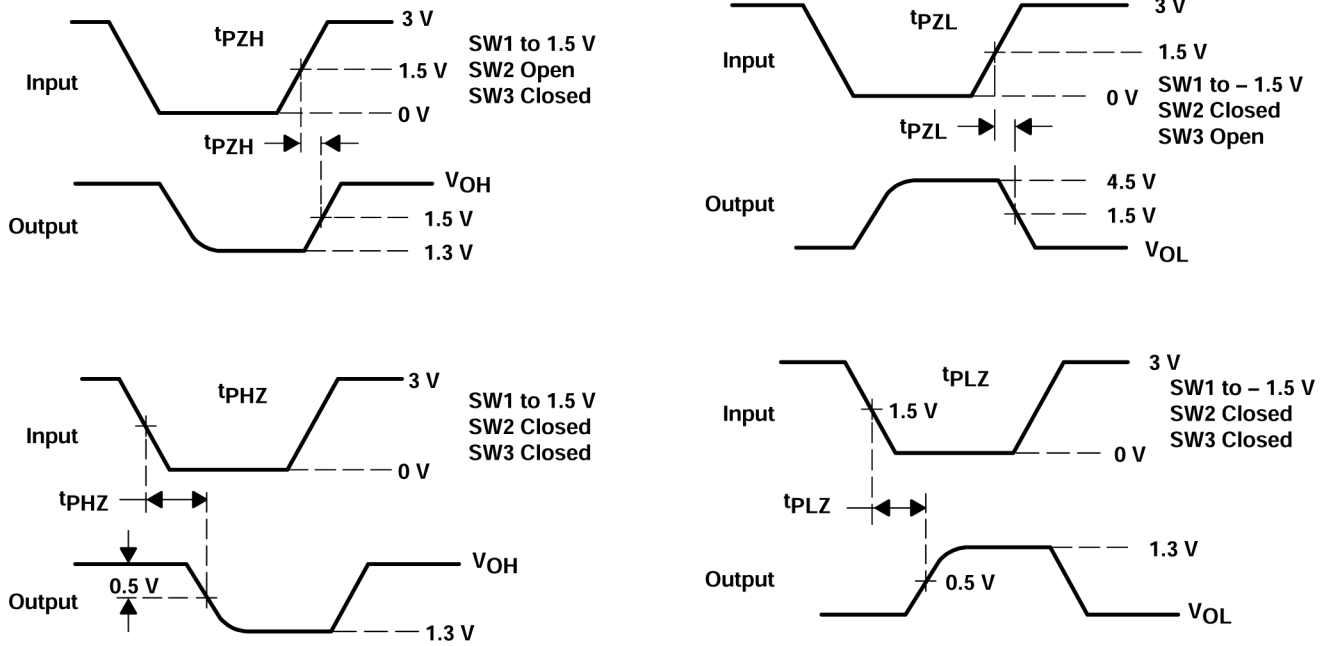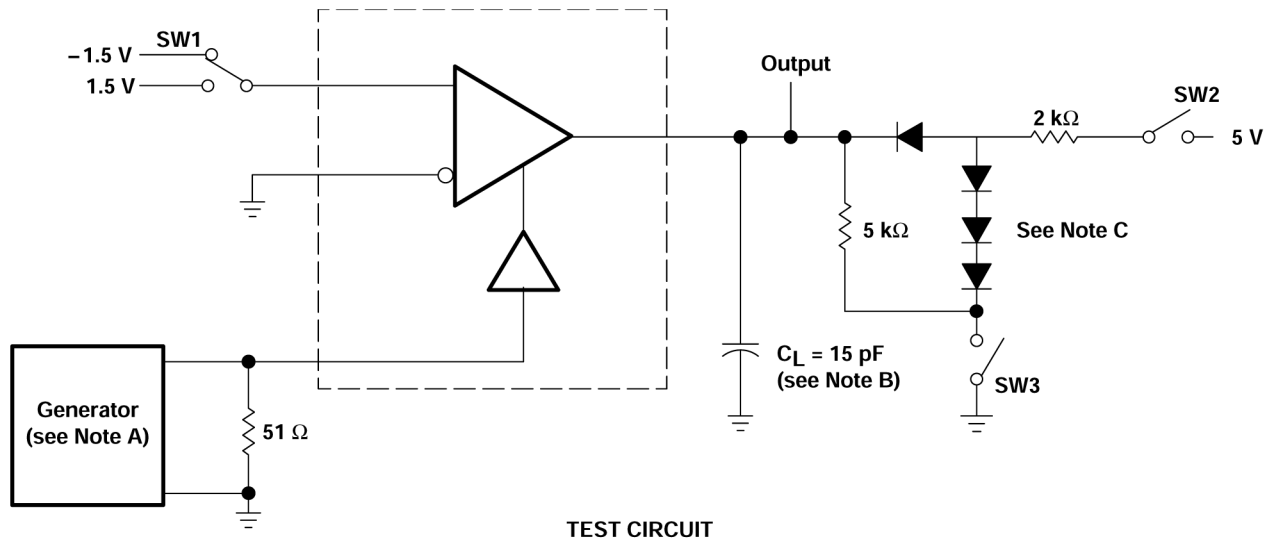
Product Folder Links: *MC3486*

TEST CIRCUIT

Figure 6-3. Test Circuit and Voltage Waveforms

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.

B. C_L includes probe and stray capacitance.

C. All diodes are 1N916 or equivalent.

Product Folder Links: *MC3486*

7 Detailed Description

7.1 Device Functional Modes

Table 7-1. Function Table (Each Receiver)

DIFFERENTIAL INPUTS	ENABLE[1]	OUTPUT
A–B		Y
$V_{ID} \leq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
Irrelevant	L	Z
Open	H	?

(1)   H = high level, L = low level, Z = high impedance (off), ? = indeterminate
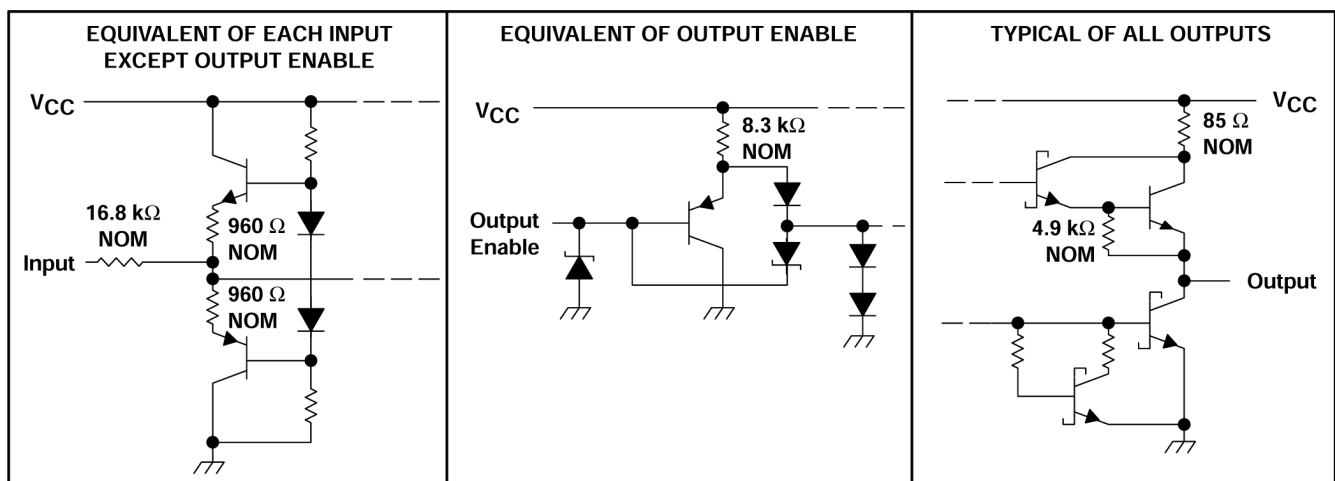
Figure 7-1. Schematics of Inputs and Outputs

Product Folder Links: *MC3486*

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

Motorola™ is a trademark of Motorola.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2002) to Revision D (October 2023) **Page**
• Changed the numbering format for tables, figures, and cross-references throughout the document................ 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MC3486D	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3486	
MC3486DE4	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3486	
MC3486DG4	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3486	
MC3486DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3486	Samples
MC3486DRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3486	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MC3486DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MC3486NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MC3486DR	SOIC	D	16	2500	340.5	336.1	32.0
MC3486NSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
MC3486D	D	SOIC	16	40	507	8	3940	4.32
MC3486DE4	D	SOIC	16	40	507	8	3940	4.32
MC3486DG4	D	SOIC	16	40	507	8	3940	4.32
MC3486N	N	PDIP	16	25	506	13.97	11230	4.32
MC3486N	N	PDIP	16	25	506	13.97	11230	4.32
MC3486NE4	N	PDIP	16	25	506	13.97	11230	4.32
MC3486NE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
△C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) △D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
       △C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0.006 (0,15) each side.
       △D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AC.

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

14x1,27

16x0,55

14x1,27

16x1,50

5,40

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283−4/E 08/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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