ABOV SEMICONDUCTOR
24 SEGMENT X 16 GRID VFD DRIVER WITH KEYSCAN

MC3501

Data Sheet (Ver. 2.3)

Version 2.3

Published by
FAE Team

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REVISION HISTORY

VERSION 2.3(2010. 12. 17) This Book
Modified the Resistor at OSC.
Modified the application circuit.

VERSION 2.1(2010. 07. 15)
Modified the command 4 .

VERSION 2.0 (2010. 04. 23)
Modified the Application Circuit on page 23.

VERSION 1.20 (2009. 01. 06)
Modified the Format of Dout at Transmission (Data Read) on page 20.
Updated the Serial Communication Example on page 21.

VERSION 1.10 (2008. 09. 24)
Updated the frame of a data sheet.

VERSION 1.00 (2008. 08. 14) The first Edition
Modified display mode setting value on page 14
Modified VIL (@Vdd=5.0V) spec . on page 10
Modified fosc spec. on page 11
Modified application circuit on page 23
Modified Package Information on page 24

DESCRIPTION

MC3501 are Vacuum Fluorescent Display (VFD) Controller driven on a 1/8 to 1/16 duty factor housed in 52 plastic LQFP. 24 segment output lines, 16 grid output lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro computer. Serial data is fed to MC3501 via a three-line serial interface.

Device name	Package Type
MC3501	52 LQFP

FEATURES

• CMOS Technology
• Low Power Consumption
• Wide operating voltage V_{DD}=2.7V~5.5V
• Key Scanning (16 x 2 matrix)
• Display Modes : (24 segments, 8digits to 24 segments, 16 digits)
• 8-Step Dimming Circuitry
• Serial Interface for Clock, Data Input, Data Output, Strobe Pins
• No External Resistors needed for driver outputs
• Available in 52-pin LQFP.

Device name	MC3501
Package Type	52 LQFP
Power	VDD : 2EA, VSS : 2EA, VEE : 1EA
Port I/O	I : 6EA , O : 1EA
FIP Output	40 EA

APPLICATION

- Microcomputer Peripheral Devices
- Digital Audio/Video system : CD/MD/VCD/DVD players
- Car Audio
- VCR
- Electric scale meter
- P.O.S.
- Electronic equipment with instructional display

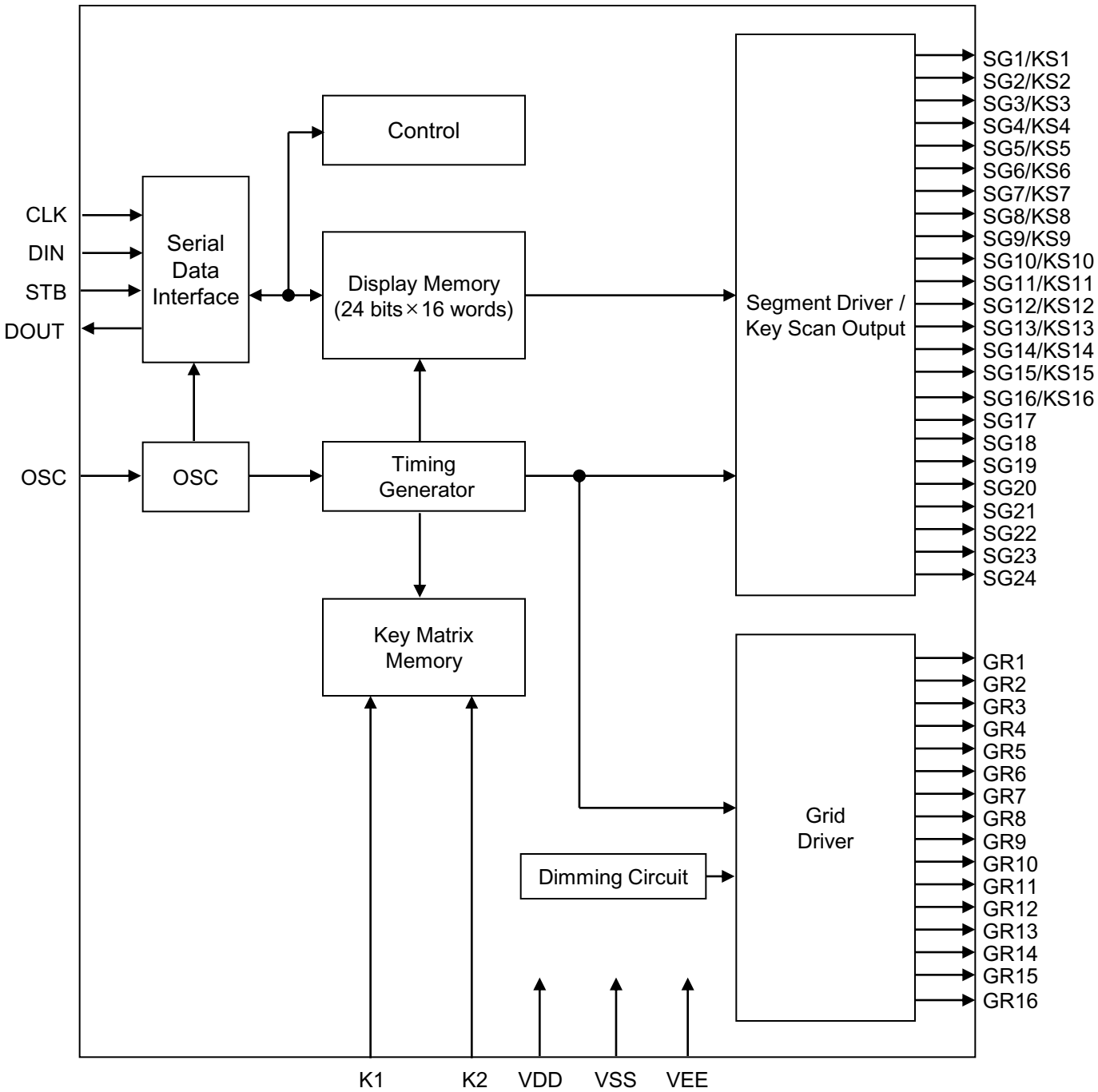
PIN DESCRIPTION

MC3501

PIN NAME	I/O	DESCRIPTION	PIN No.
CLK (Schmitt Trigger)	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge of the shift clock	1
DIN (Schmitt Trigger)	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit)	2
STB (Schmitt Trigger)	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this in is “HIGH”, CLK is ignored.	3
DOUT	O	Data Output Pin (N-Channel, Open-Drain) This pin outputs serial data at the falling edge of the shift clock. (starting from the lower bit) Enable push-pull type output via setting b5,b4 of command 4.	4
K1 to K2	I	Key Data Input Pins The data inputted to these pins is latched at the end of the display cycle.	5,6
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation Frequency.	7
VSS	-	Logic Ground Pin	8,52
VDD	-	Logic Power Pin	9,51
SG1/KS1 to SG16/KS16	O	High-Voltage Segment Output Pins Also acts as the Key Source.	10 to 25
SG17 to SG24	O	High-Voltage Segment Output Pins	26 to 33
GR1 to GR16	O	High-Voltage Grid Output Pins	34 to 49
VEE	-	Pull-Down Level	50

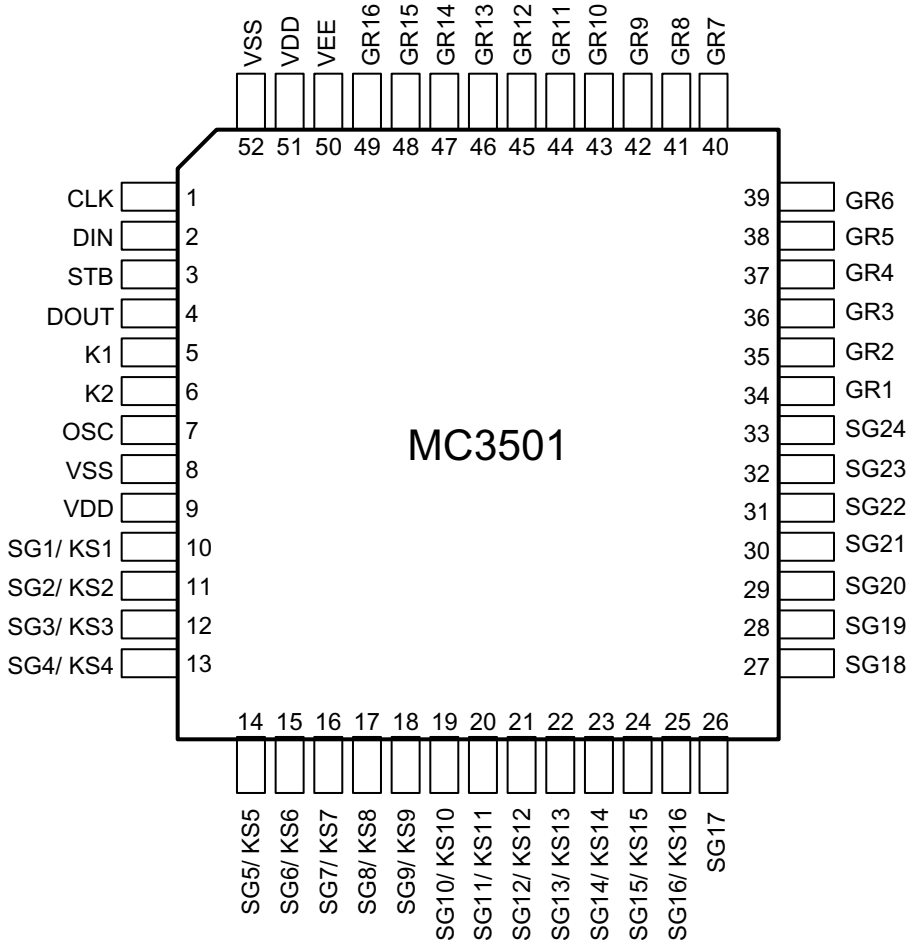
BLOCK DIAGRAM

MC3501



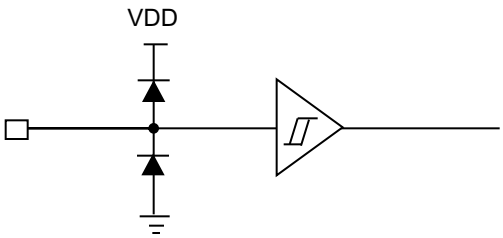
PIN CONFIGURATION

MC3501

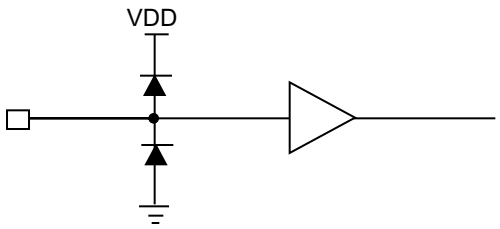


INPUT/OUTPUT PINS SCHEMATIC DIAGRAM

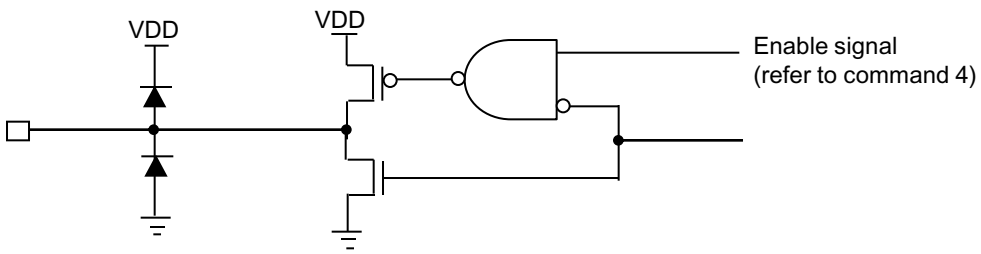
Input pins : CLK,STB, DIN



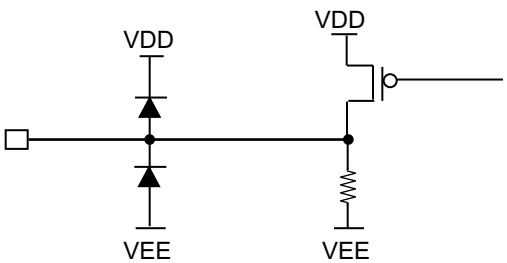
Input pins : K1,K2



Output pin : DOUT



Output pins : SGn, GRn



ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25℃, GND=0V)

Parameter	Symbol	Ratings	Unit
Logic Supply Voltage	VDD	-0.3 to +7	V
Driver Supply Voltage	VEE	VDD+0.3 to VDD-45	V
Logic Input Voltage	VI	-0.3 to VDD+0.3	V
VFD Driver Output Voltage	VO	VEE-0.3 to VDD+0.3	V
VFD Drive Output Current	IOVFD	-40 (Grid) -15 (Segment)	mA
Operating Temperature	Topr	-40 to +85	℃
Storage Temperature	Tstg	-65 to +150	℃

RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Ta= 25℃, GND=0V)

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Logic Supply Voltage	VDD	2.7	5	5.5	V
High-Level Input Voltage (VDD=5V)	VIH	0.75VDD	-	VDD	V
Low-Level Input Voltage (VDD=5V)	VIL	0	-	0.2VDD	V
High-Level Input Voltage (VDD=3.3V)	VIH	0.8VDD	-	VDD	V
Low-Level Input Voltage (VDD=3.3V)	VIL	0	-	0.2VDD	V
Driver Supply Voltage	VEE	VDD-35	-	0	V

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD=5V, GND=0V, VEE=VDD-35V, Ta=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Low-Level Output Voltage	VOLDOUT	IOLDOUT = 4mA DOUT, DIO	-	-	0.4	V
High-Level Output Current	IOHSG	VO = VDD – 2V SG1/KS1 to SG16/KS16, SG17 to SG24	-3	-	-	mA
High-Level Output Current	IOHGR	VO = VDD – 2V GR1 to GR16	-15	-	-	mA
High-Level Input Voltage	VIH	-	0.75VDD	-	VDD	V
Low-Level Input Voltage	VIL	-	0	-	0.2VDD	V
Input Current	II	VI = VDD or VSS	-	-	±1	uA
Dynamic Current Consumption	IDDdyn	Under no load Display Off	-	-	5	mA

(Unless otherwise stated, VDD=3.3V, GND=0V, VEE=VDD-35V, Ta=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Low-Level Output Voltage	VOLDOUT	IOLDOUT = 4mA DOUT, DIO	-	-	0.4	V
High-Level Output Current	IOHSG	VO = VDD – 2V SG1/KS1 to SG16/KS16, SG17 to SG24	-1.5	-	-	mA
High-Level Output Current	IOHGR	VO = VDD – 2V GR1 to GR16	-6	-	-	mA
High-Level Input Voltage	VIH	-	0.8VDD	-	VDD	V
Low-Level Input Voltage	VIL	-	0	-	0.2VDD	V
Input Current	II	VI = VDD or VSS	-	-	±1	uA
Dynamic Current Consumption	IDDdyn	Under no load Display Off	-	-	3	mA

SWITCHING CHARACTERISTICS

(Unless otherwise stated, VDD=5V, GND=0V, VEE=VDD-35V, Ta=25℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Grid rise time	t_{GLH}	CL = 300pF	-	-	0.5	us
Segment rise time	t_{SLH}		-	-	2.0	us
Grid fall time	t_{GHL}		-	-	150	us
Segment fall time	t_{SHL}		-	-	150	us
Oscillation frequency	f_{OSC}	R=82KΩ	250	350	450	KHz

(Unless otherwise stated, VDD=3.3V, GND=0V, VEE=VDD-35V, Ta=25℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Grid rise time	t_{TZH2}	CL = 300pF	-	-	1.2	us
Segment rise time	t_{TZH1}		-	-	4.0	us
Grid fall time	t_{GHL}		-	-	150	us
Segment fall time	t_{SHL}		-	-	150	us
Oscillation frequency	f_{OSC}	R=82KΩ	250	350	450	KHz

TIMING CHARACTERISTICS

(Unless otherwise stated, VDD=5V, GND=0V, VEE=VDD-35V, Ta=25℃)

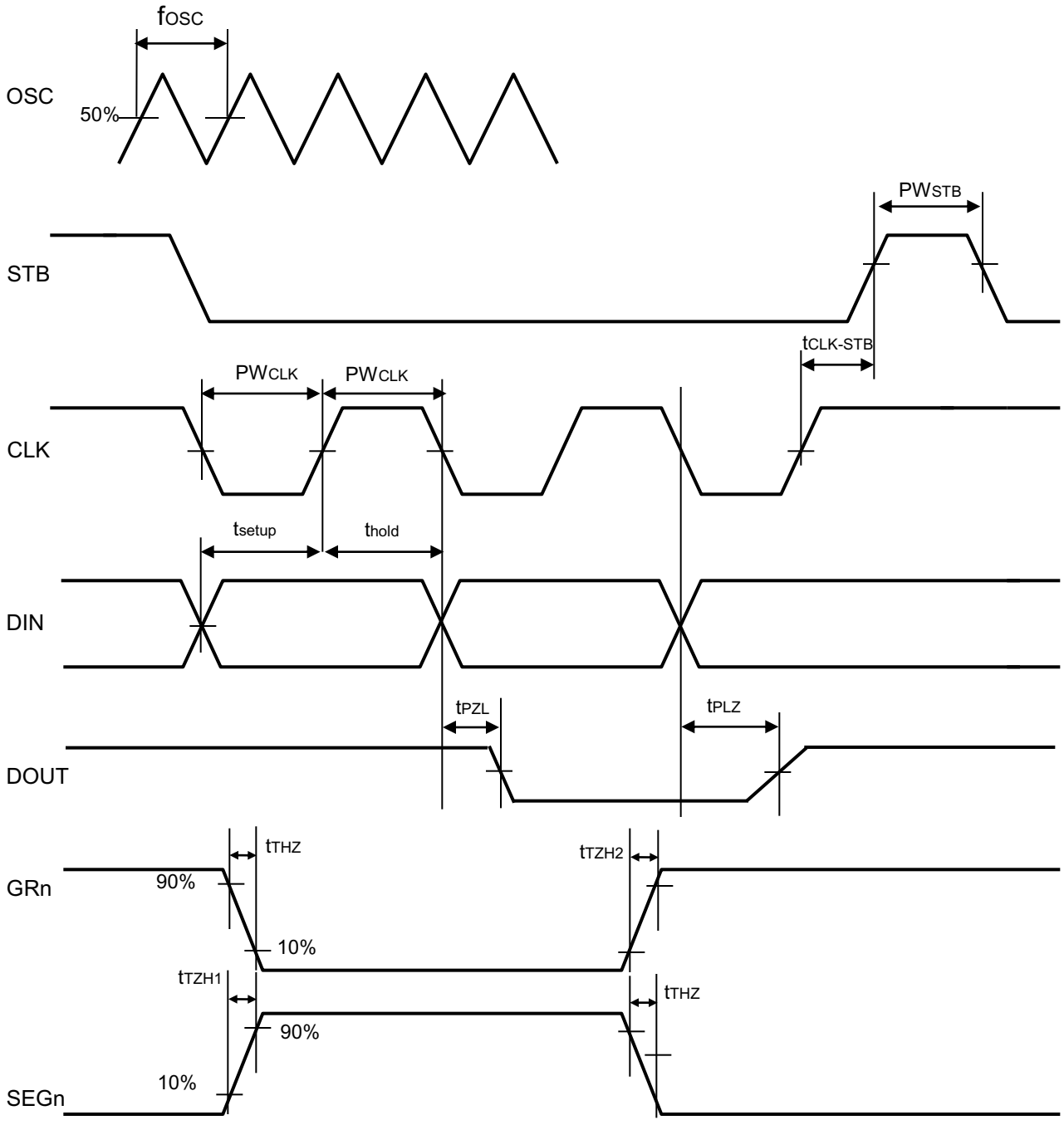
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock pulse width	PW_{CLK}		400			ns
Strobe pulse width	PWSTB		1000			ns
Data setup time	tsetup		100			ns
Data hold time	thold		100			ns
Clock-strobe time	tCLK-STB	CLK ↑ → STB ↑	1000			ns
Propagation delay time	tPZL	R_L=10KΩ, C_L=15pF			100	ns
	tPLZ				400	ns

(Unless otherwise stated, VDD=3.3V, GND=0V, VEE=VDD-35V, Ta=25℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock pulse width	PW_{CLK}		400			ns
Strobe pulse width	PWSTB		1000			ns
Data setup time	tsetup		100			ns
Data hold time	thold		100			ns
Clock-strobe time	tCLK-STB	CLK ↑ → STB ↑	1000			ns
Propagation delay time	tPZL	R_L=10KΩ, C_L=15pF			100	ns
	tPLZ				600	ns

SWITCHING CHARACTERISTIC WAVEFORM

MC3501 Switching Characteristics Waveform is given below.



FUNCTIONAL DESCRIPTION

COMMANDS

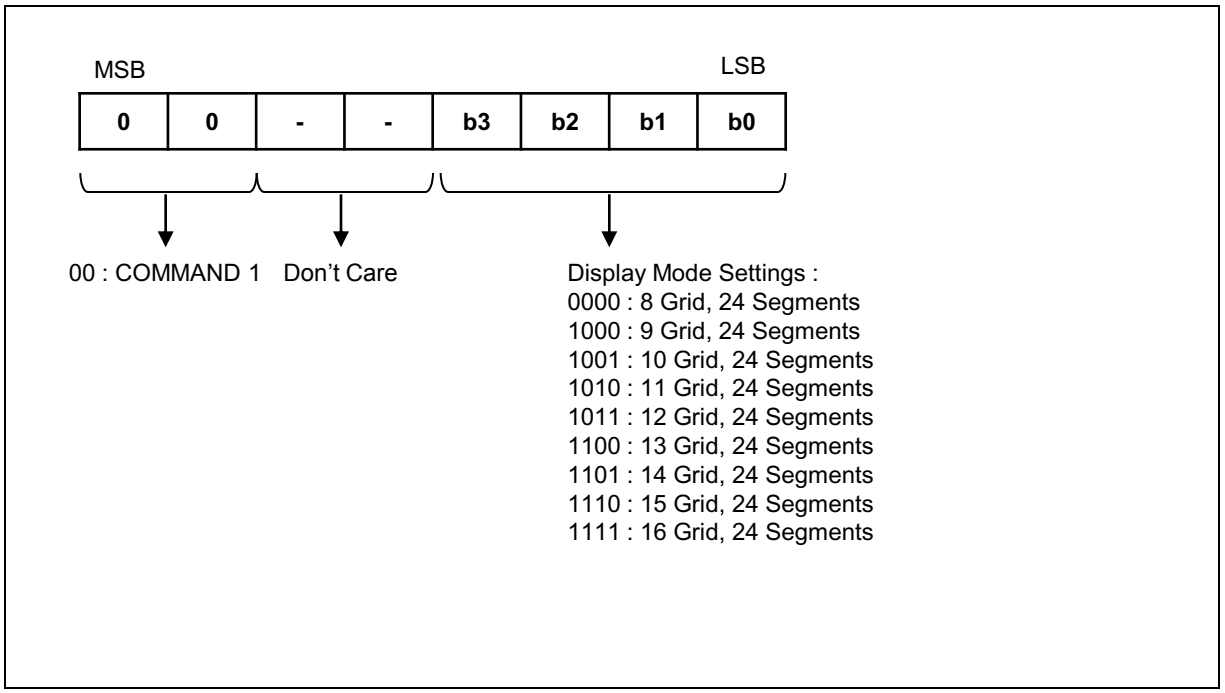
Commands determine the display mode and status of MC3501. A command is the first byte (b0 to b7) inputted to MC3501 via the DIN Pin after STB Pin has changed from “HIGH” to “LOW” State. If for some reason the STB Pin is set to “HIGH” while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMAND 1 : DISPLAY MODE SETTING COMMAND

MC3501 provides 8 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to MC3501 via the DIN Pin when STB is “LOW”. However, for these commands, the bits 5 to 6 (b4 to b5) are ignored, bits 7 & 8 (b6 to b7) are given a value of “0”.

The Display Mode Setting Commands determine the number of segments and grids to be used (1/8 to 1/16 duty, 24 segments). When these commands are executed, the display is forcibly turned off, the key scanning stops. A display command “ON” must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

When Power is turned “ON”, the 16-digit, 24-segment modes is selected.



Display Mode and RAM Address

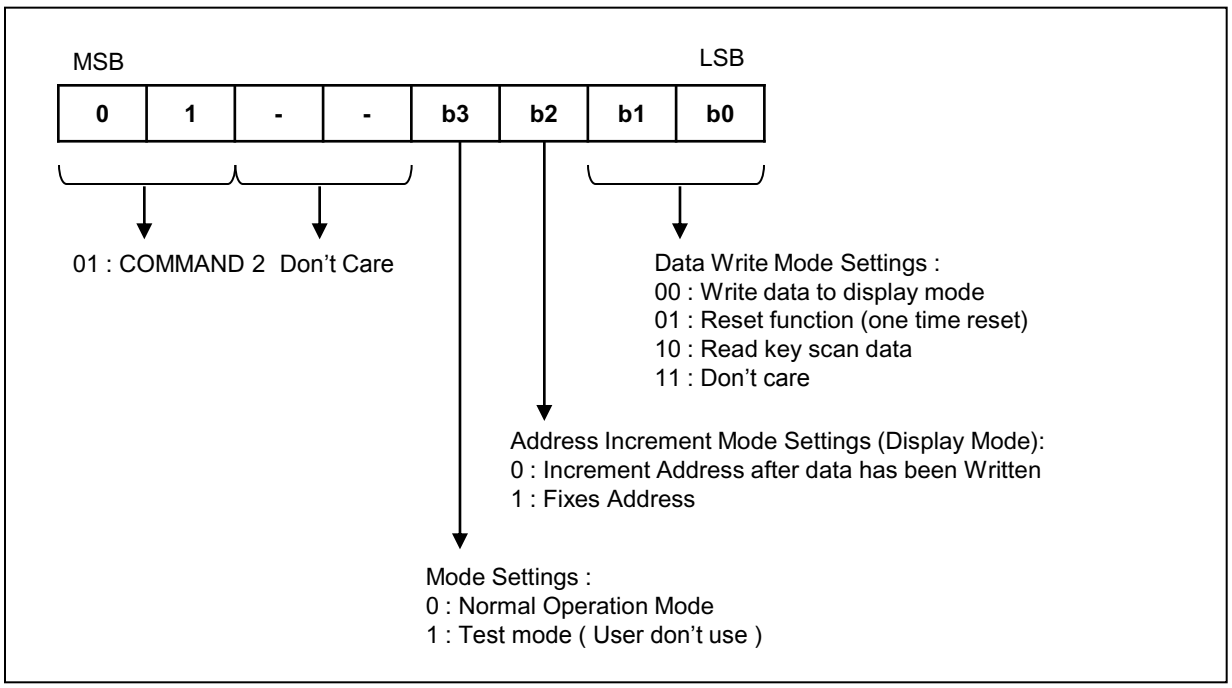
Data transmitted from an external device to MC3501 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of MC3501 are given below in 8bits unit.

SG1 SG4	SG5 SG8	SG9 SG12	SG13 SG16	SG1 7 SG20	SG21 SG24	
$00H_L$	$00H_U$	$01H_L$	$01H_U$	$02H_L$	$02H_U$	DIG1
$03H_L$	$03H_U$	$04H_L$	$04H_U$	$05H_L$	$05H_U$	DIG2
$06H_L$	$06H_U$	$07H_L$	$07H_U$	$08H_L$	$08H_U$	DIG3
$09H_L$	$09H_U$	$0AH_L$	$0AH_U$	$0BH_L$	$0BH_U$	DIG4
$0CH_L$	$0CH_U$	$0DH_L$	$0DH_U$	$0EH_L$	$0EH_U$	DIG5
$0FH_L$	$0FH_U$	$10H_L$	$10H_U$	$11H_L$	$11H_U$	DIG6
$12H_L$	$12H_U$	$13H_L$	$13H_U$	$14H_L$	$14H_U$	DIG7
$15H_L$	$15H_U$	$16H_L$	$16H_U$	$17H_L$	$17H_U$	DIG8
$18H_L$	$18H_U$	$19H_L$	$19H_U$	$1AH_L$	$1AH_U$	DIG9
$1BH_L$	$1BH_U$	$1CH_L$	$1CH_U$	$1DH_L$	$1DH_U$	DIG10
$1EH_L$	$1EH_U$	$1FH_L$	$1FH_U$	$20H_L$	$20H_U$	DIG11
$21H_L$	$21H_U$	$22H_L$	$22H_U$	$23H_L$	$23H_U$	DIG12
$24H_L$	$24H_U$	$25H_L$	$25H_U$	$26H_L$	$26H_U$	DIG13
$27H_L$	$27H_U$	$28H_L$	$28H_U$	$29H_L$	$29H_U$	DIG14
$2AH_L$	$2AH_U$	$2BH_L$	$2BH_U$	$2CH_L$	$2CH_U$	DIG15
$2DH_L$	$2DH_U$	$2EH_L$	$2EH_U$	$2FH_L$	$2FH_U$	DIG16

COMMAND 2 : DATA SETTING COMMAND

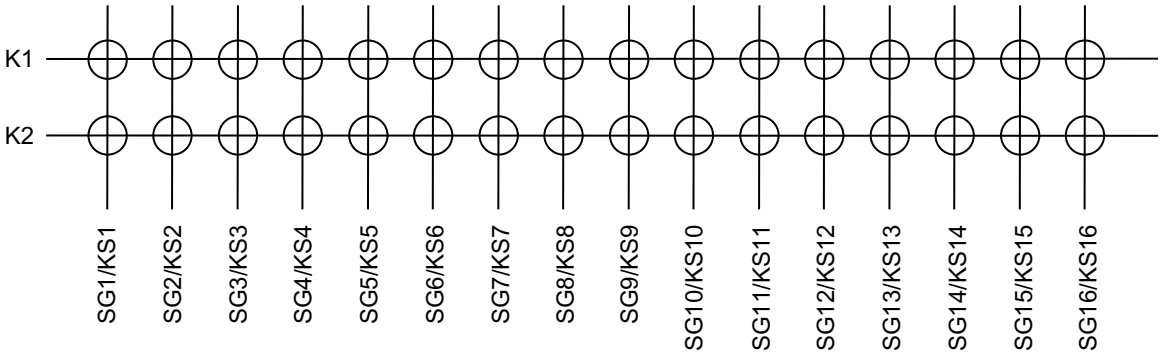
The Data Setting Commands executes the Data Write or Data Read Modes for MC3501. The data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of “1” while bit 8 (b7) is given the value of “0”. Please refer to the diagram below.

When power is turned ON, the bit 4 to bit 1 (b3 to b0) are given the value of “0”.



MC3501Key Matrix & Key Input Data Storage RAM

MC3501 key matrix consists of 16×2 array as shown belows.



Each data inputted by each key are stored as follows. They are read by a READ Command, starting from the last significant bit. When the most significant bit of the data (SG1, b0) has been read, the least significant bit of the next data (SG16, b7) is read.

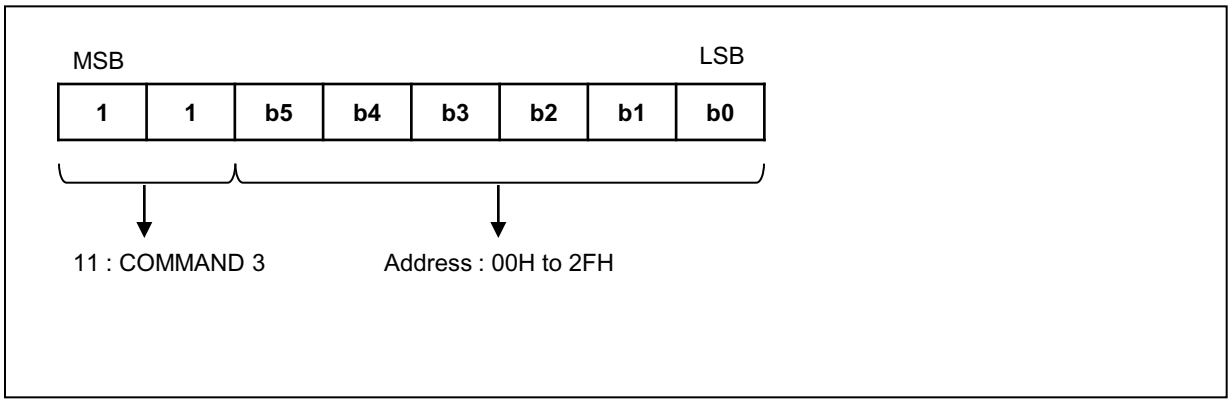
K1 …… K2	K1 …… K2	K1 …… K2	K1 …… K2
SG1/KS1	SG2/KS2	SG3/KS3	SG4/KS4
SG5/KS5	SG6/KS6	SG7/KS7	SG8/KS8
SG9/KS9	SG10/KS10	SG11/KS11	SG12/KS12
SG13/KS13	SG14/KS14	SG15/KS15	SG16/KS16
b0 …… b1	b2 …… b3	b4 …… b5	b6 …… b7

Reading Sequence

COMMAND 3 : ADDRESS SETTING COMMAND

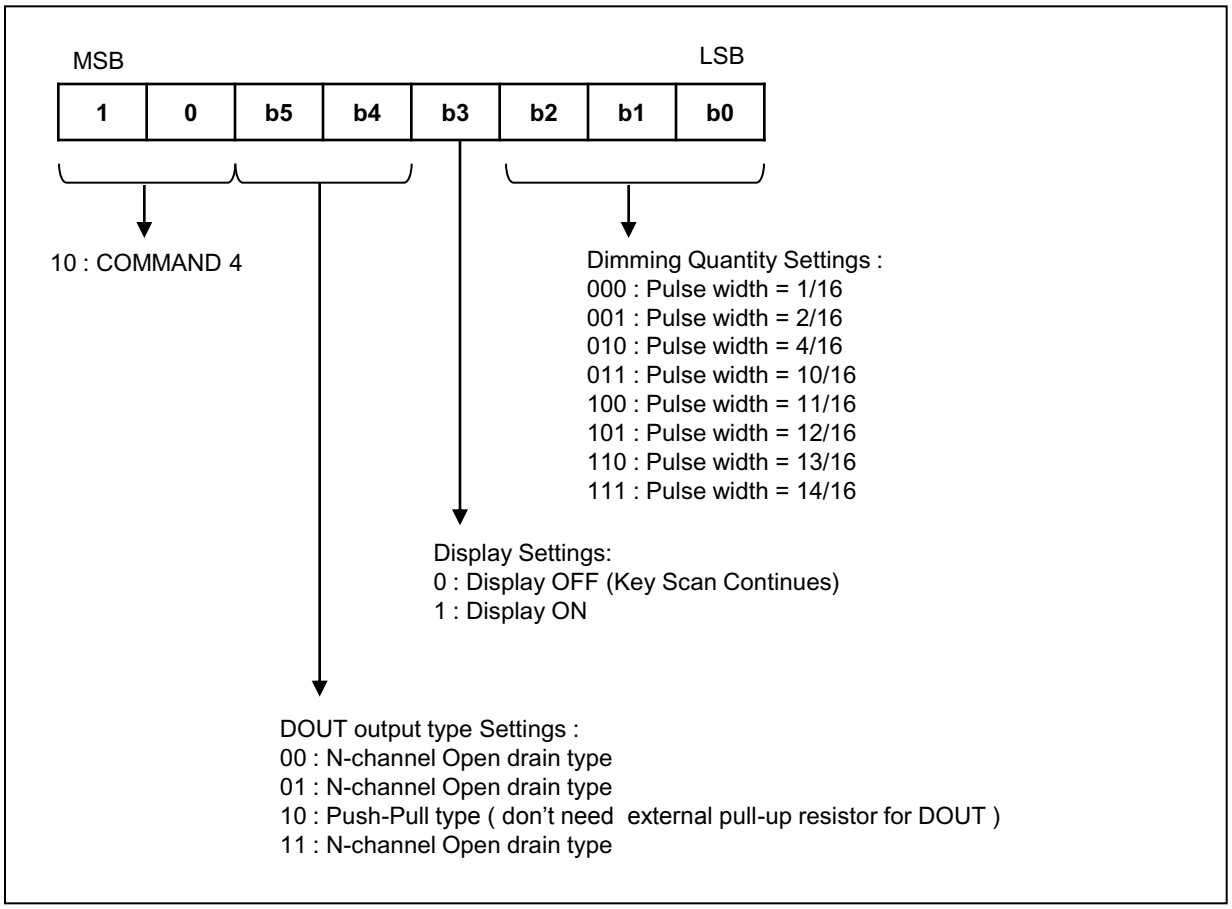
The display memory is addressed by Address Setting Command. The valid address range is “00H” to 2FH”. If the address is set to 30H or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at “00H”.

Please refer to the diagram below.



COMMAND 4 : DISPLAY CONTROL COMMANDS

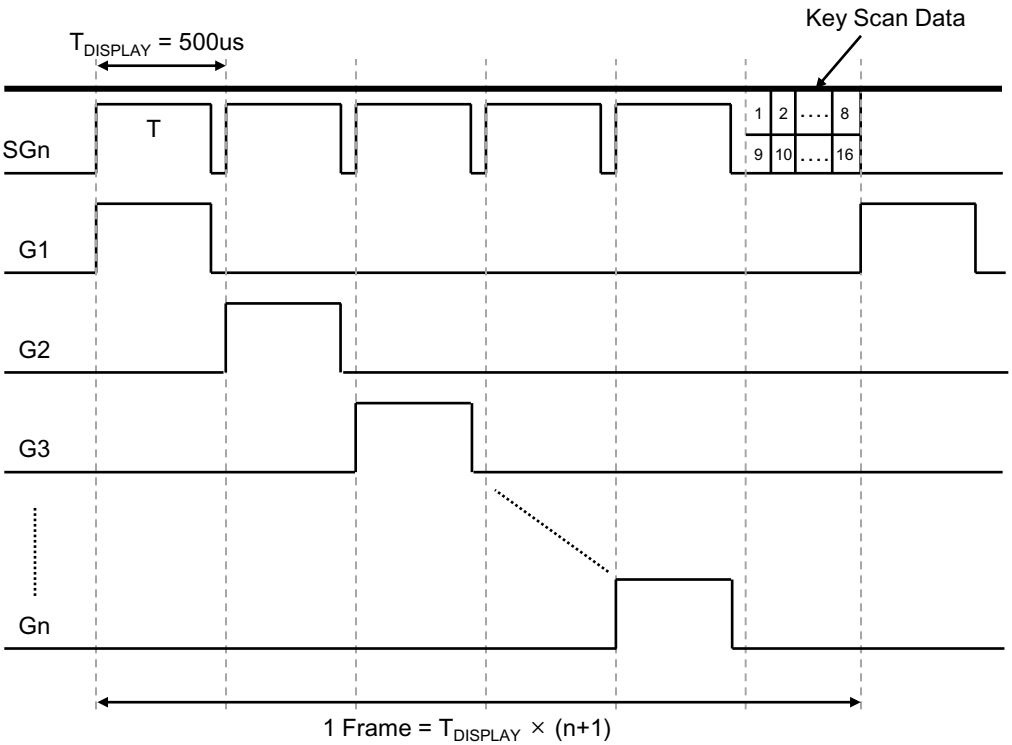
The Display Control Commands are used to turn ON or OFF a display. It is also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the display is turned OFF (the key scanning is stopped) and DOUT is selected N-channel Open drain type.



SCANNING AND DISPLAY TIMING

The Key Scanning and display timing diagram is given below. One cycle of key scanning consists of 2 frames. The data of the 16 x 2 matrix is stored in the RAM.

Operating Frequency (fosc) = 224/T

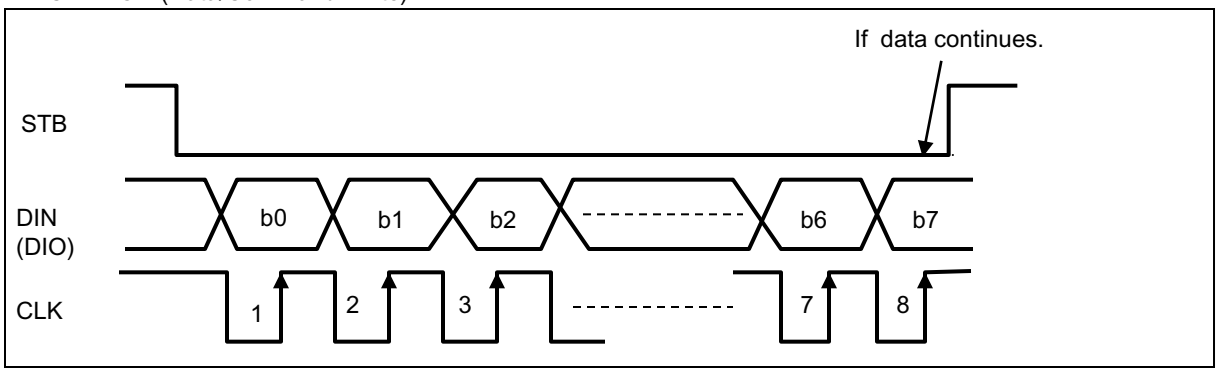


Note : T is the width of segment only

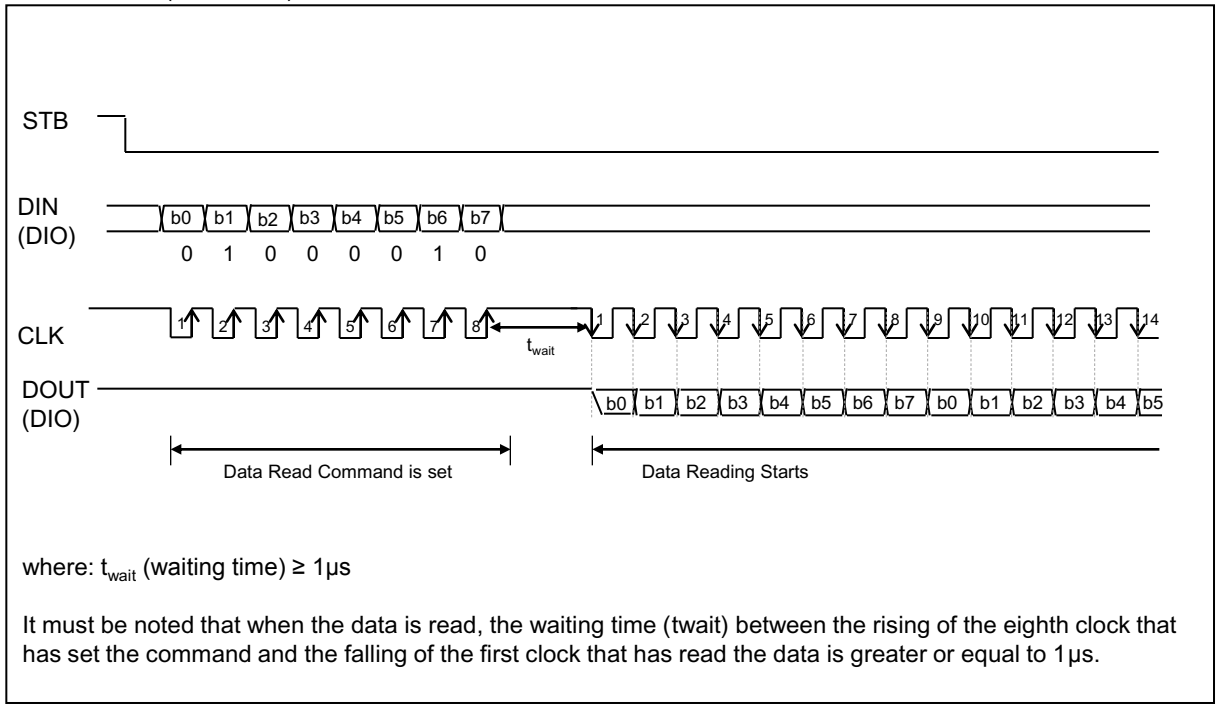
SERIAL COMMUMICATION FORMAT

The following diagram shows the MC3501serial communication format. The DOUT Pin is selected output type (N-channel open-drain type or Push-pull type) via command 4. If DOUT is selected open-drain type output , it is highly recommended that an external pull-up resistor (1KΩ to10KΩ) must be connected to DOUT.

RECEPTION (Data/Command Write)



Transmission (Data Read)

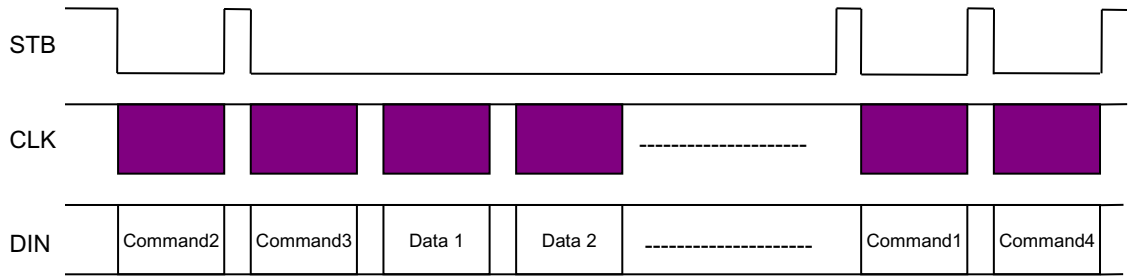


where: t_{wait} (waiting time) ≥ 1μs

It must be noted that when the data is read, the waiting time (twait) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1μs.

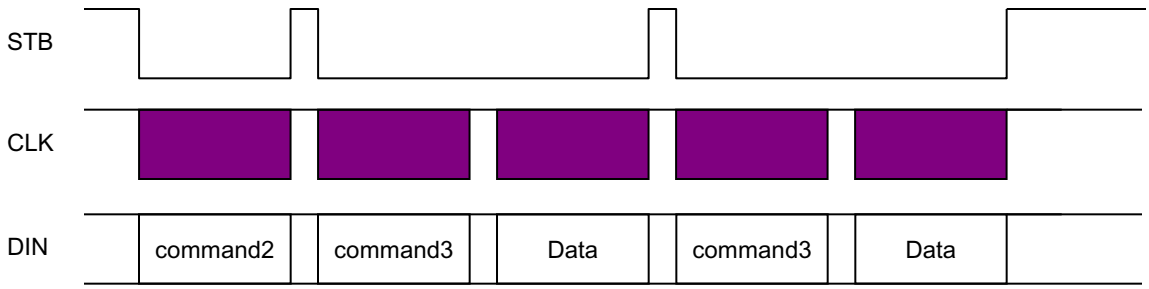
SERIAL COMMUNICATION EXAMPLES

Serial communication timing diagram for initialization setting.



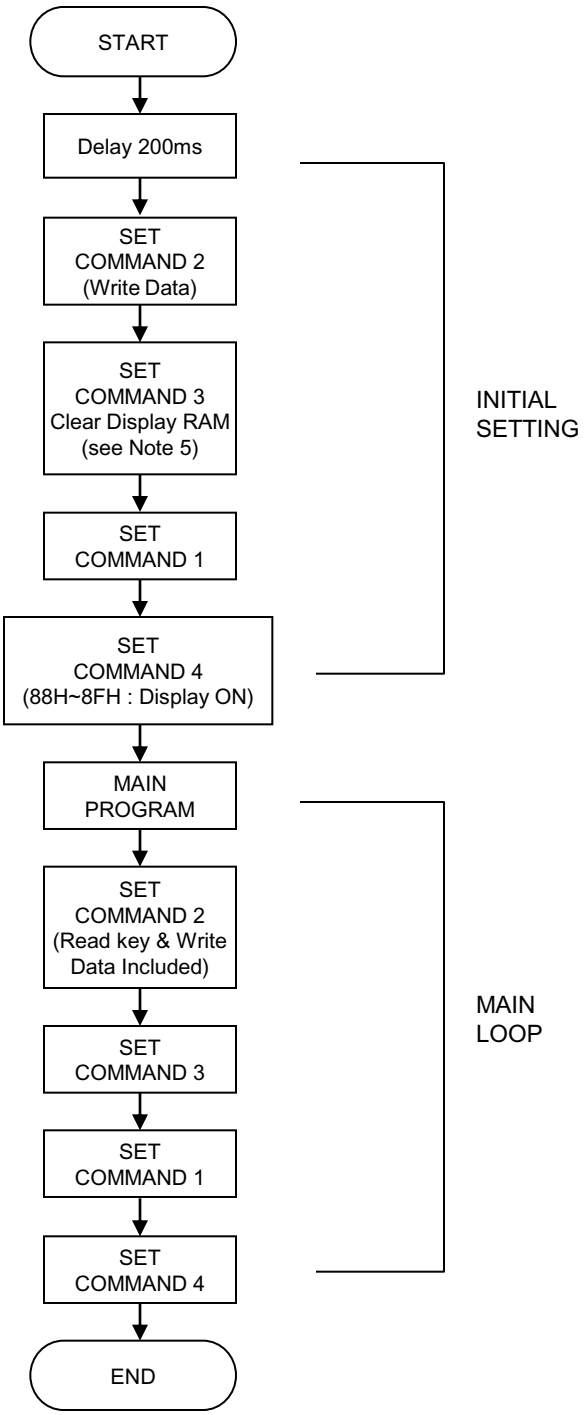
Where : Command 1 : Display Mode Setting
Command 2 : Data Setting Command
Command 3 : Address Setting Command
Data 1 to n : Transfer Display Data (36 Bytes max.)
Command 4 : Display Control Command

Memory updating timing diagram.



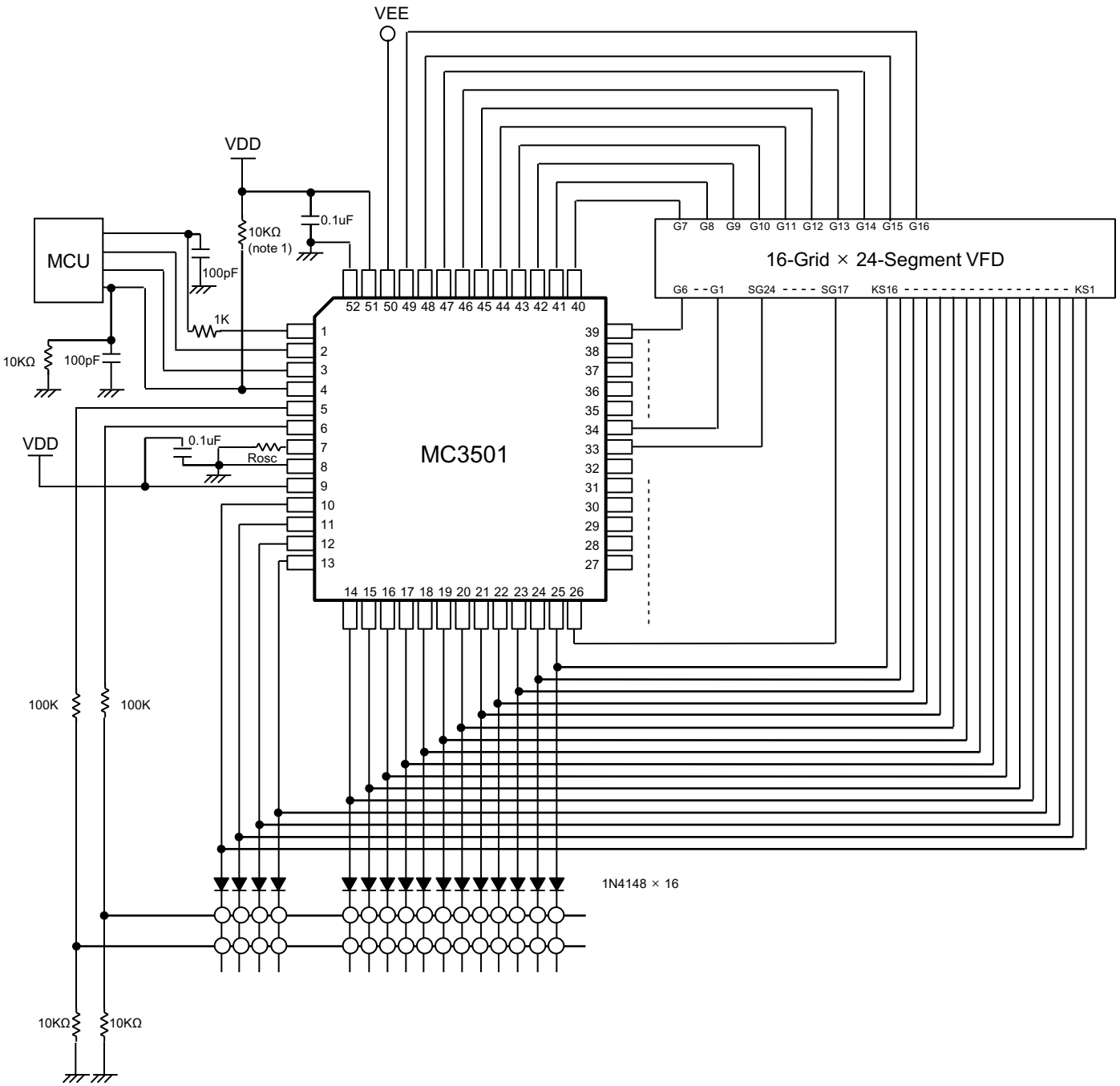
Where : Command 2 -- Data Setting Command
Command 3 -- Address Setting Command
Data -- Display Data

RECOMMENDED SOFTWARE PROGRAMMING FLOW CHART



- Note : 1. Command 1 : Display Mode Setting
  2. Command 2 : Data Setting Commands
  3. Command 3 : Address Setting Commands
  4. Command 4 : Display Control Commands
  5. When IC power is applied for the first time, the contents of the Display RAM are not defined : thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

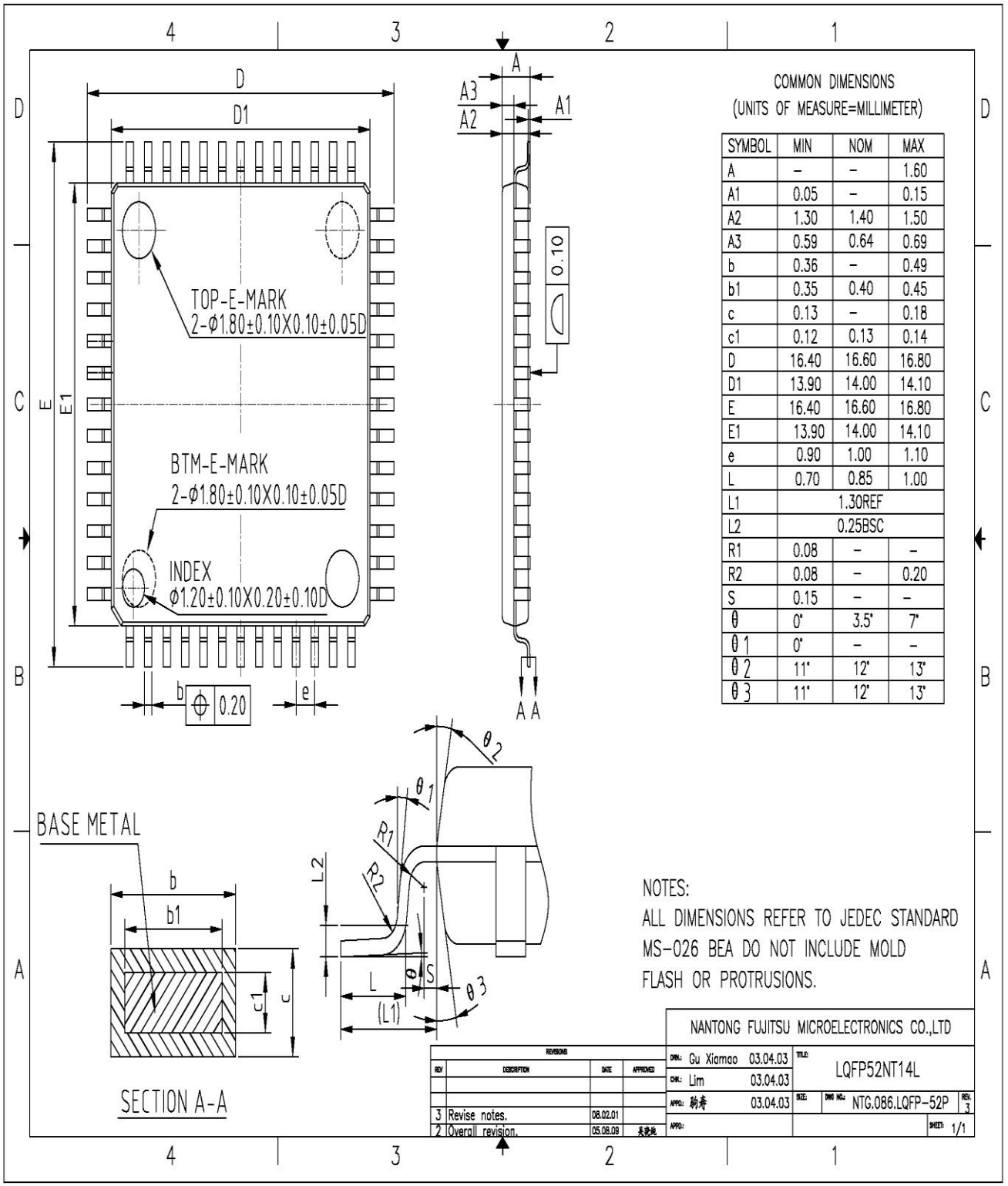
APPLICATION CIRCUIT



(note 1) don't need external pull-up resistor for DOUT (refer to COMMAND 4 on page 20)
- in this case, VDD have to be same level or higher than power of MCU

PACKAGE INFORMATION

52-PIN LQFP



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.36	–	0.49
b1	0.35	0.40	0.45
c	0.13	–	0.18
c1	0.12	0.13	0.14
D	16.40	16.60	16.80
D1	13.90	14.00	14.10
E	16.40	16.60	16.80
E1	13.90	14.00	14.10
e	0.90	1.00	1.10
L	0.70	0.85	1.00
L1	1.30REF		
L2	0.25BSC		
R1	0.08	–	–
R2	0.08	–	0.20
S	0.15	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

REV	DESCRIPTION	DATE	APPROVED
3	Revise notes.	08.02.01	
2	Overall revision.	05.06.09	

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