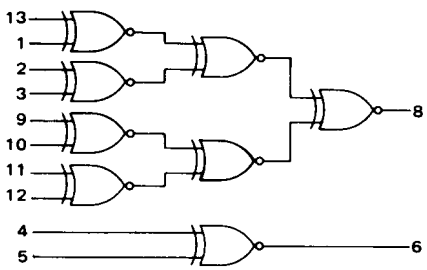
8-BIT PARITY TREE

MC4308
MC4008



V_{CC} = Pin 14
GND = Pin 7

Positive Logic:
8 = 1⊙2⊙3⊙9⊙10⊙11⊙12⊙13
6 = 4⊙5
where X ⊙ Y = ($\overline{X}$ • $\overline{Y}$) + (X • Y)

This device consists of seven Exclusive NOR gates connected to check even parity. The output will be in the logic "1" state as long as the "1" state is present on an even number of inputs. The additional Exclusive NOR gate can be used to connect two 8-bit parity trees to form a 16-bit parity tree, or it can be used to convert the parity tree to check odd parity by connecting one gate input to the output of the parity tree and grounding the other input. This conversion can also be accomplished by connecting a simple inverter to the output of the parity tree.

Input Loading Factor = 2
Output Loading Factor = 10

Total Power Dissipation = 150 mW typ/pkg
Propagation Delay Time = 15-30 ns typ

TYPICAL PROPAGATION DELAY TIMES

FIGURE 1 – THREE-GATE DELAY versus TEMPERATURE

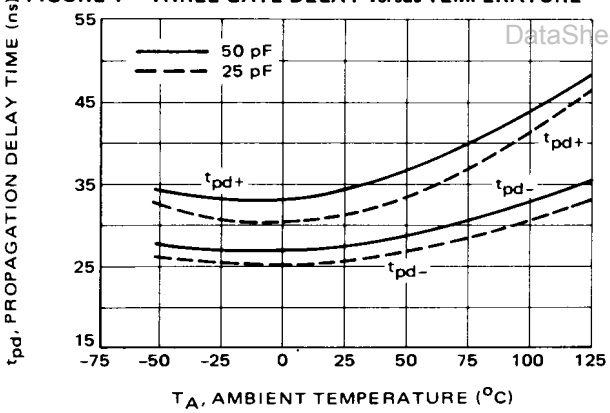


FIGURE 2 – ONE-GATE DELAY versus TEMPERATURE

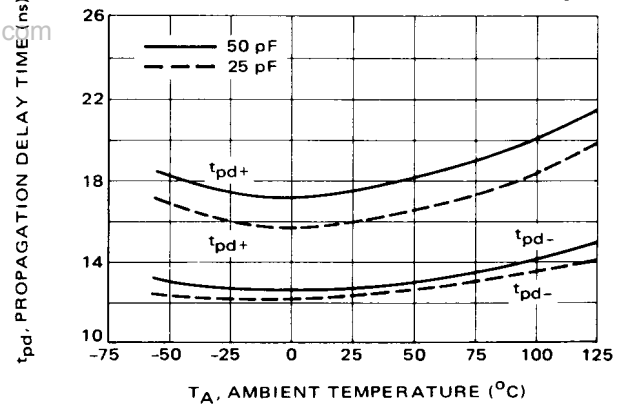


FIGURE 3 – DELAY versus LOAD CAPACITANCE

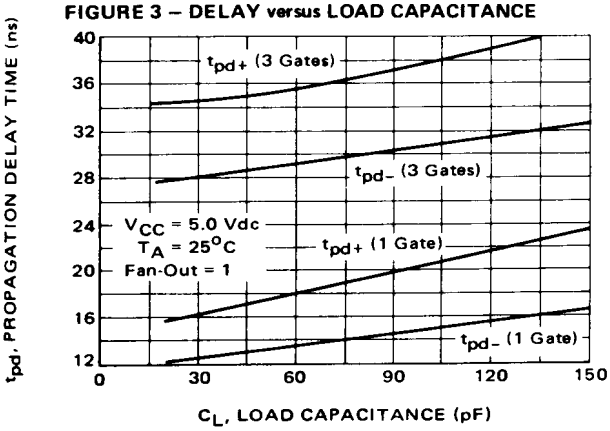


FIGURE 4 – DELAY versus SUPPLY VOLTAGE