

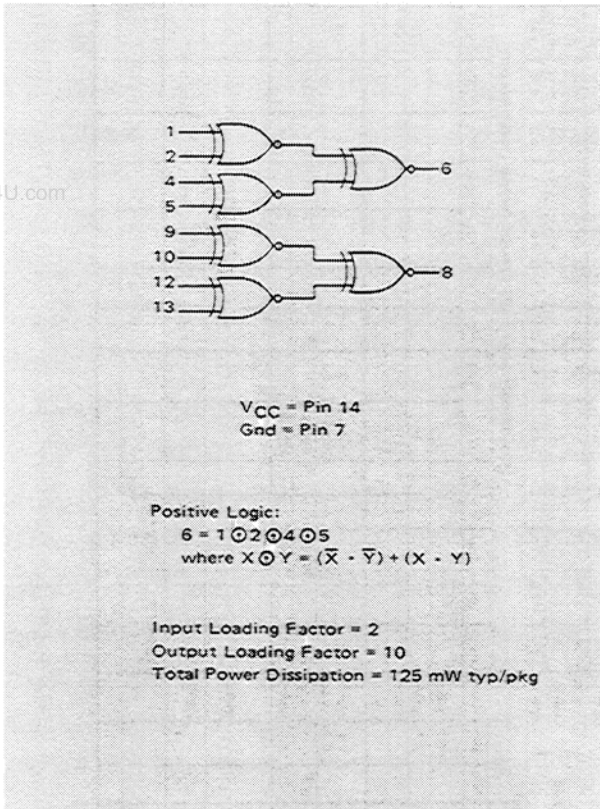


DUAL 4-BIT PARITY TREE

MC4310
MC4010

JULY 1971

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC4010 only.



Three Exclusive NOR gates are connected together to form each of the two 4-bit parity trees in the package. An even number of logic "1" states on the inputs will result in a logic "1" output state. An odd parity checker can be made by connecting an inverter to the output of the device.

TYPICAL PROPAGATION DELAY TIMES

FIGURE 1 - DELAY versus TEMPERATURE

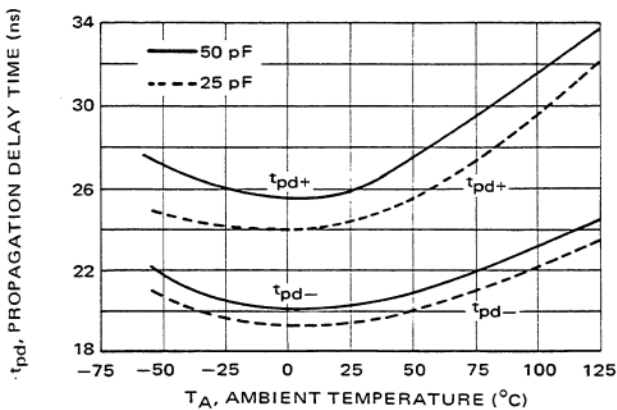


FIGURE 2 - DELAY versus LOAD CAPACITANCE

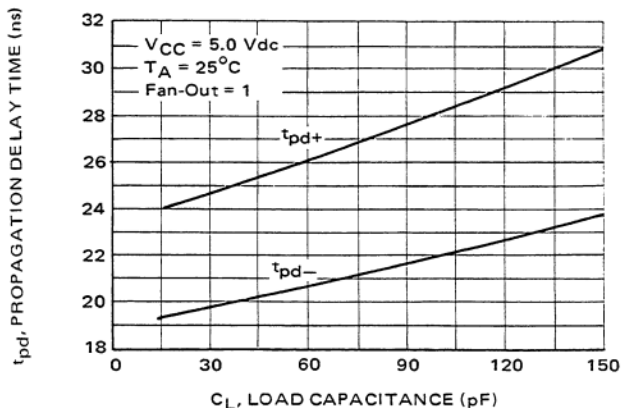
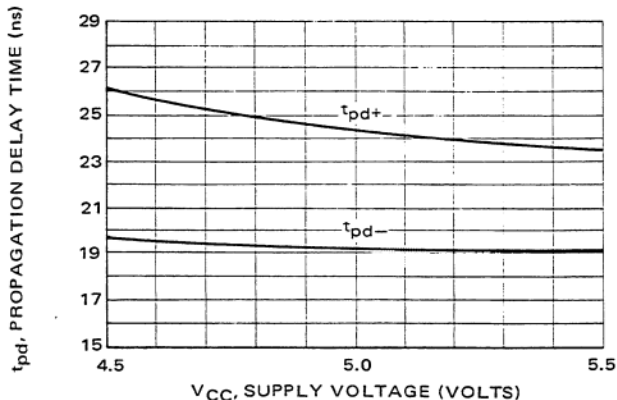
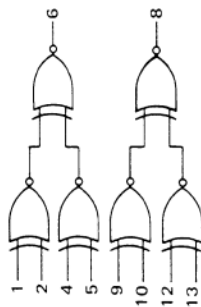


FIGURE 3 - DELAY versus SUPPLY VOLTAGE



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and output in the same manner. To complete testing, test all input-output combinations according to the logic equation.



Characteristic	Symbol	Pin Under Test	TEST CURRENT/VOLTAGE VALUES														
			mA						Volts								
			IOL1	IOL2	IOH	Iin	ID	VIL	VIH	VF	VR	VRH	Vmax	VCC	VCCL	VCCH	VHX
Input																	
Forward Current	IF	1	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2
Leakage Current	IR	1	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80
Breakdown Voltage	BV _{in}	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Clamp Voltage	VD	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Output																	
Output Voltage	VOL	6	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
	VOH	6	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4
Short-Circuit Current	ISC	6	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20
Power Requirements (Total Device)																	
Maximum Power Supply Current	I _{max}	14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Power Supply Drain	IPD	14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Switching Parameters																	
Turn-On Delay	t _{pd-1}	1.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Turn-Off Delay	t _{pd+1}	1.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:																	
MC4010 Test Limits																	
Symbol	Pin	-55°C			+25°C			0°C			+25°C			+75°C			Unit
		Min	Max	Test	Min	Max	Test	Min	Max	Test	Min	Max	Test	Min	Max	Test	
IOL1	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
IOL2	2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
IOH	3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Iin	4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
ID	5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
VIL	6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
VIH	7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
VF	8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
VR	9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
VRH	10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Vmax	11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
VCC	12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
VCCL	13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
VCCH	14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
VHX	15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

INPUT AND OUTPUT LOADING FACTORS
with respect to M TTL and M DTL families

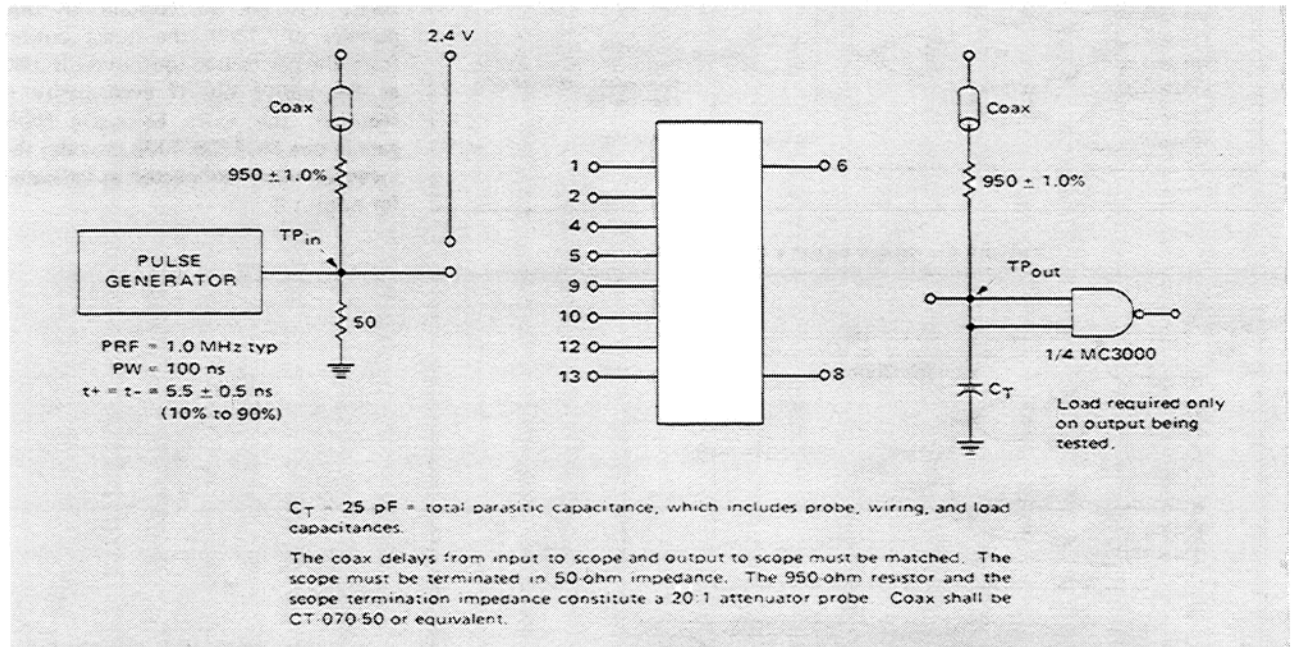
FAMILY	MC4310 INPUT LOADING FACTOR	MC4310 OUTPUT LOADING FACTOR
MC4300	1.0	10
MC500	1.2	12
MC2100	0.8	8
MC3100	0.8	8
MC5400	1.0	10
MC930	1.0*	10

FAMILY	MC4010 INPUT LOADING FACTOR	MC4010 OUTPUT LOADING FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	10
MC830	1.15*	12

* Applies only when input is being driven by M DTL gate with 2.0 kilohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 kilohm pullup resistors reduce drive capability to fan-out of 3.

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SWITCHING TIME TEST CIRCUIT



VOLTAGE WAVEFORMS

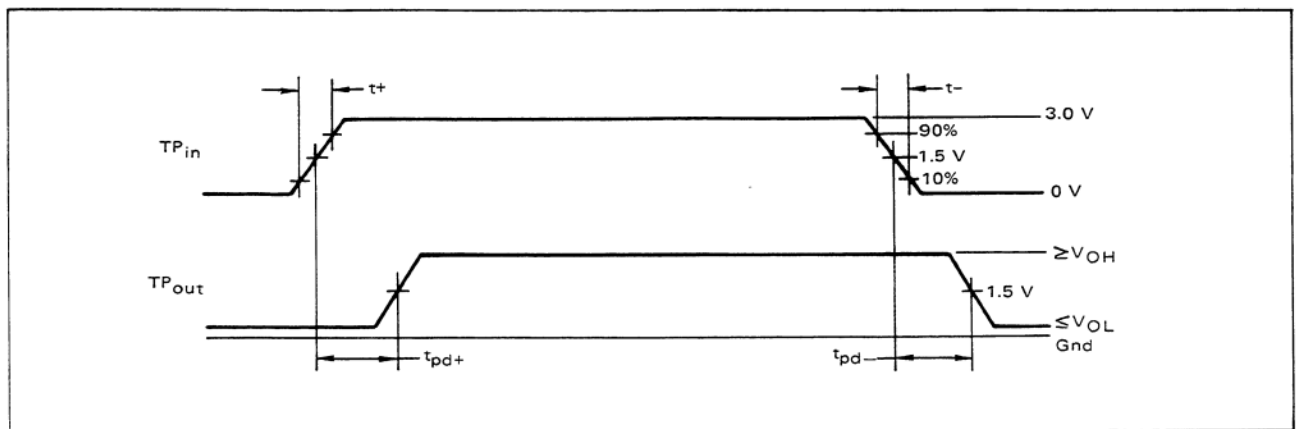
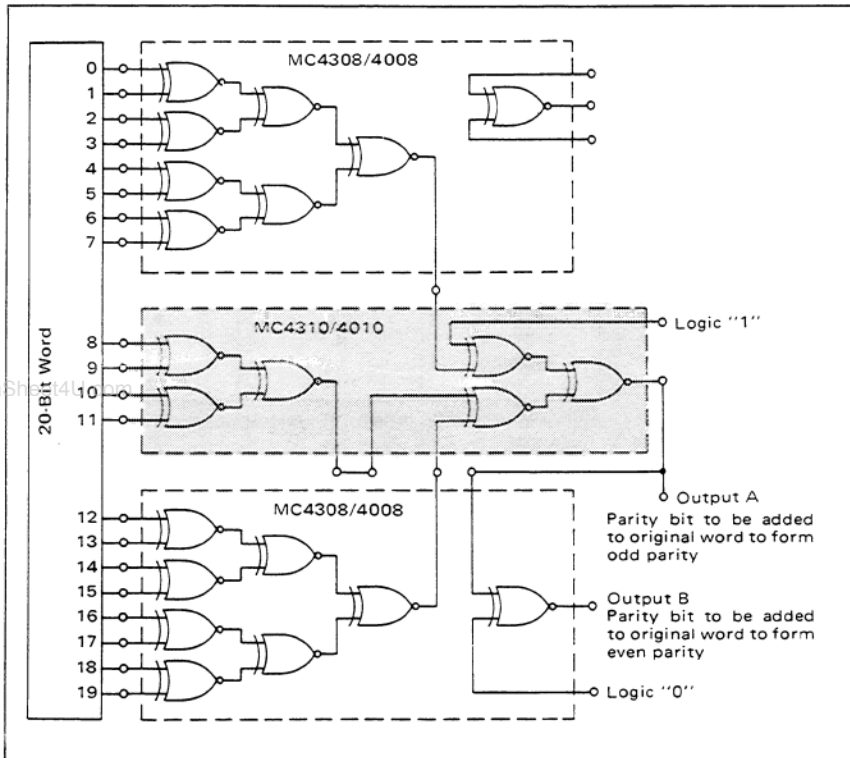


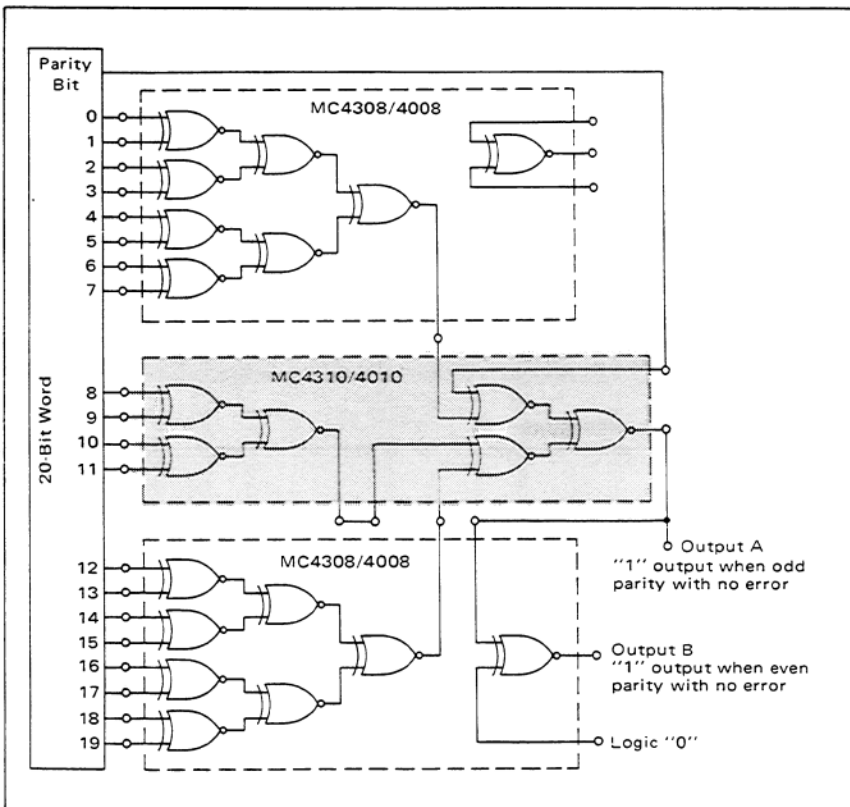
FIGURE 4 – 20-BIT PARITY GENERATOR



APPLICATIONS INFORMATION

A parity generation tree (simple parity) for a 20-bit word is shown in Figure 4. It uses two MC4308/4008 8-bit parity trees and one MC4310/4010 dual 4-bit parity tree. If a parity word containing odd parity is required (i.e., the 20-bit word plus the parity bit are to contain an odd number of "1's"), the direct output from the parity tree (output A) is used as the parity bit. If even parity is required, the extra Exclusive NOR gate in one MC4308/4008 provides the inversion when connected as indicated for output B.

FIGURE 5 – 20-BIT PARITY DETECTOR



A parity detection circuit for a 20-bit word is shown in Figure 5. The 20-bit word is connected to a two-stage parity tree identical to that used for the 20-bit parity generator; however, for the detection circuit the output of the tree must be compared with the input parity bit. The parity bit serves as an input to the second stage of the tree. For odd parity detection, output A will be a logic "1" if no error has occurred. For even parity detection, a logic "1" will appear at output B if no error has been introduced. Longer word lengths can be examined in a similar manner.



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MC4310/D

