COMPLEX FUNCTIONS

MC4300/MC4000 Series

The MTTL complex functions are designed for digital applications in the medium to high-speed range.

These MTTL devices provide significant reduction in package count and increased logic per function over devices in the basic MTTL and MDTL families.

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

All devices shown can be used with all MTTL and MDTL devices; however, the loading factors shown reflect use with other devices in the same MC-number series unless otherwise noted.

Function	Operating Temperature Range		Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Power Dissipation P_D mW typ/pkg
	Type 1 −55 to +125°C	Type 1 0 to +75°C			
Dual 4-Channel Data Selector	MC4300F,L	MC4000F,L,P	10	Control Line = 18 Data Line = 11	150
BCD-to-Binary/Binary-to-BCD Number Converter		MC4001F,L,P	Open Collector I_{OL} = 16 mA	Address Time <45 ns	300
Dual Data Distributor	MC4302F,L	MC4002F,L,P	10	10.5	175
16 Bit Scratch Pad Memory Cell	MC4304F,L	MC4004F,L,P	I_{OL} = 40 mA	Write mode 25 Sense mode 15	250
16 Bit scratch Pad Memory Cell	MC4305F'L	MC4005F,L,P	Open Collector I_{OL} = 20 mA	Write mode 25 Sense mode 15	250
Binary to One-of-Eight Line Decoder	MC4306F,L	MC4006F,L,P	10	14	100
Dual Binary to One-of-Four Line Decoder	MC4307F,L	MC4007F,L,P	10	14	125
8-Bit Parity Tree	MC4308F,L	MC4008F,L,P	10	15 to 30	150
Dual 4 Bit Parity Tree	MC4310F,L	MC4010F,L,P	10	9.5 to 22	125
4-Bit Shift Register	MC4312F,L	MC4012F,L,P	10	22/bit	180
Quad Type D Flip Flop	MC4315F,L	MC4015F,L,P	10	16	190
Programmable Module-N Decade Counter	MC4316F,L	MC4016F,L,P	8	Clock to Q3 = 50 Clock to Bus = 35	250
Programmable Modulo 2, Modulo 5 Counters	MC4317F,L	MC4017F,L,P	8	Clock to Q3 = 50 Clock to Bus = 35	250
Programmable Module-N Hexadecimal Counter	MC4318F,L	MC4018F,L,P	8	Clock to Q3 = 50 Clock to Bus = 35	250
Dual Programmable Modulo 4 Counters	MC4319F,L	MC4019F,L,P	8	Clock to Q3 = 50 Clock to Bus = 35	250

MC4300/4000 Series continued

Function	−55 to +125°C	0 to +75°C	Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Power Dissipation P_D mW typ/pkg
Dual 4-Bit Comparator (Open Collector)	MC4321F,L	MC4021F,L,P	10	20	250
Dual 4-Bit Comparator	MC4322F,L	MC4022F,L,P	10	20	250
4-Bit Universal Counter	MC4323F,L	MC4023F,L,P	10	16/bit	200
Dual Voltage Controlled Multivibrator	MC4324F,L	MC4024F,L,P	7	f_{max} = 30 MHz	150
Full Adder	MC4326F,L	MC4026F,L,P	15/12**	25/13#	90
Full Adder	MC4327F,L	MC4027F,L,P	7/6**	25/13#	90
Adder (Dependent Carry)	MC4328F,L	MC4028F,L,P	15/12**	25/13#	125
Adder (Dependent Carry)	MC4329F,L	MC4029F,L,P	7/6**	25/13#	125
Adder (Independent Carry)	MC4330F,L	MC4030F,L,P	15/12**	25/13#	125
Adder (Independent Carry)	MC4331F,L	MC4031F,L,P	7/6**	25/13#	125
Carry Decoder	MC4332F,L	MC4032F,L,P	—	Δt_{pd} = 4 decoder	20
Quad Latch (Open Collector)	MC4335F,L	MC4035F,L,P	7	25	140
Quad Latch	MC4337F,L	MC4037F,L,P	10	25	150
Inverting/Non-Inverting One-of-Eight Decoder	—	MC4038F,L,P	Open Collector I_{OL} = 20 mA	Address Time <45 ns	240
Seven Segment Character Generator	—	MC4039F,L,P			240
Binary to Two-of-Eight Decoder	—	MC4040F,L,P			200
Single-Error Hamming Code Detector and Generator	—	MC4041F,L,P			240
Quad Predriver	MC4342F,L	MC4042F,L,P	I_{OL} = 50 mA Open Collector	15	120
Dual Line Selector	MC4343F,L	MC4043F,L,P	I_{OL} = 400 mA Pulsed	20	70
Phase-Frequency Detector	MC4344F,L	MC4044F,L,P	10	9.0	85
Non-Inverting One-of-Eight Decoder	—	MC4048F,L,P	Open Collector I_{OL} = 16 mA	Address Time <50 ns)	240
Counter-Latch-Decoder	MC4350F,L	MC4050F.L.P	Open Collector I_{OL} = 40 mA	f_{Tog} = 35 MHz	450
Counter-Latch-Decoder	MC4351F,L	MC4051F,L,P	Open Emitter 40 mA Sourcing Capability @ 10% Duty Cycle	f_{Tog} = 35 MHz	450
Dual Decade Counter	MC4352F,L	MC4052F,L,P	10	f_{Tog} = 40 MHz	350
Dual Hexadecimal Counter	MC4353F,L	MC4053F,L,P	10	f_{Tog} = 40 MHz	350
Dual Decade Up/Down Counter	MC4354F,L	MC4054F,L,P	10	f_{Tog} = 12 MHz	600
Dual Binary Up/Down Counter	MC4355F,L	MC4055F,L,P	10	f_{Tog} = 12 MHz	600
NBCD Adder	MC4356F,L	MC4056F,L,P	10	30	300
Nines Complement/Zero Element	MC4358F,L	MC4058F,L,P	10	30	200
Bus Transfer Switch	MC4360F,L	MC4060F,L,P	10	25	350
Dual Majority Logic Gate	MC4362F,L	MC4062F,L,P	10	Z = 20 Z = 11	75
64-Bit Random Access Memory	—	MC4064F,L,P	Open Collector I_{OL} = 15 mA	Access Time <60 ns	384
Dual MOS-to-TTL Level Translator with Tri-state Output	MC4368F,L	MC4068F,L,P	10	20	150

**MC4300/MC400 Series loading specified for use with MTTLI Devices

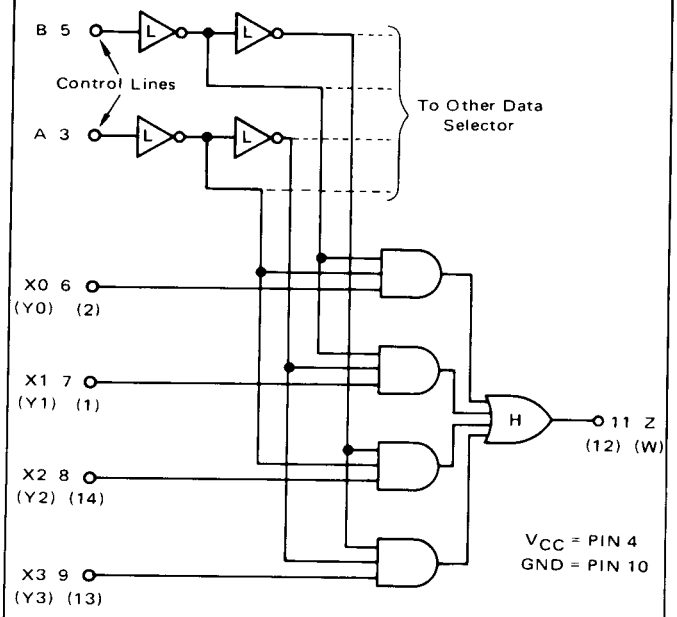
#Add delay, Carry delay

DUAL 4-CHANNEL DATA SELECTOR

MC4300
MC4000

1/2 OF DEVICE SHOWN

(Numbers and symbols in parenthesis are for other half of device.)



$Z = ABX0 + A\bar{B}X1 + \bar{A}BX2 + \bar{A}\bar{B}X3$

$W = ABY0 + A\bar{B}Y1 + \bar{A}BY2 + \bar{A}\bar{B}Y3$

Input Loading Factor = 1

Output Loading Factor = 10

Total Power Dissipation = 150 mW typ/pkg

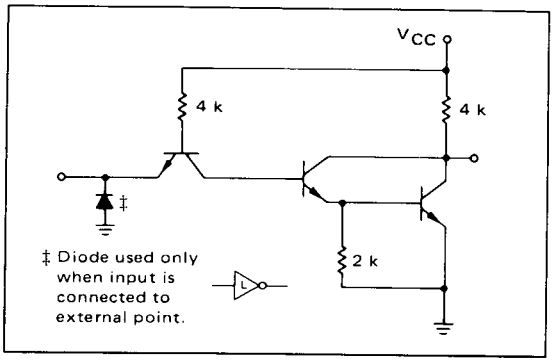
This device consists of two four-channel data selectors with common control lines, constructed from high-level AND-OR gates and low-level inverters. By selecting one of four logic combinations, information on one of the four data inputs will be routed to the output.

Data selectors are useful in applications where digital data is to be routed from one of several registers or locations to another register or location for processing.

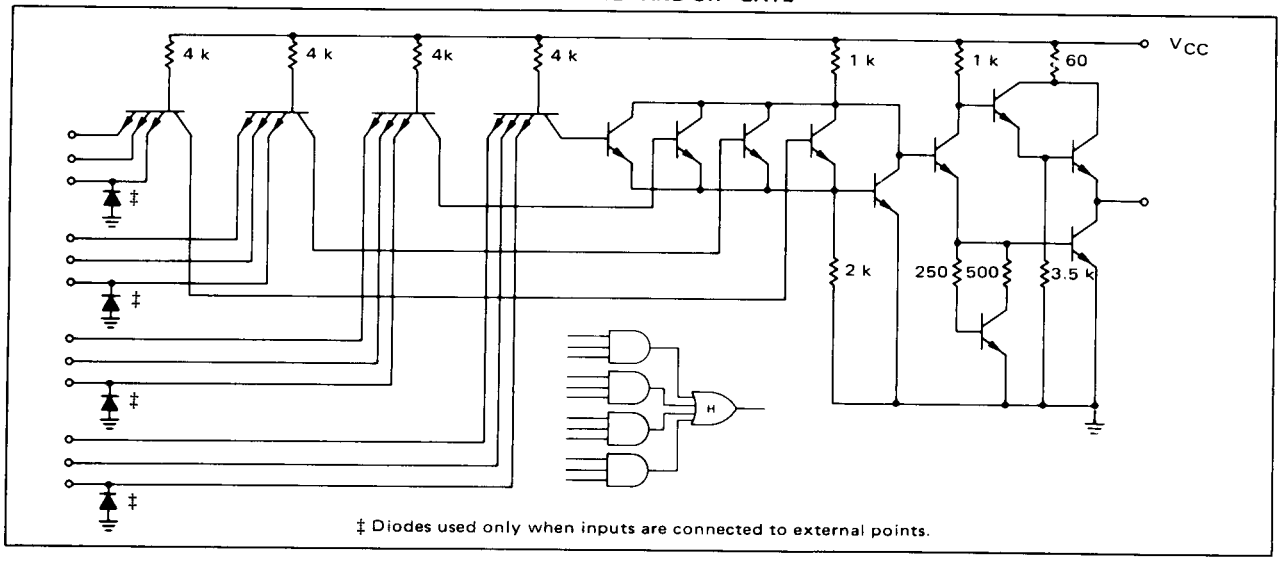
TYPICAL PROPAGATION DELAY TIMES (ns)
$T_A = 25^oC$

INPUT	Z	CONDITIONS
A	18	X0 = X2 = X3 = logic "0", X1 = logic "1". A and B are defined by the logic equations.
B	15	
X1	11	

LOW-LEVEL INVERTER

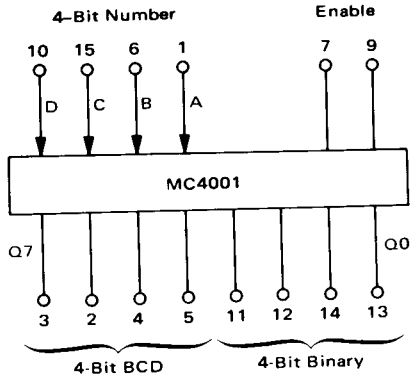


HIGH-LEVEL "AND-OR" GATE



BCD-TO-BINARY/ BINARY-TO-BCD NUMBER CONVERTER

MC4301
MC4001



V_{CC} = Pin 16
GND = Pin 8

TRUTH TABLE (POSITIVE LOGIC)

INPUT				OUTPUT							
				Binary to BCD				BCD to Binary			
D	C	B	A	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0	0	1	0	0
0	1	0	1	1	0	0	0	0	1	0	1
0	1	1	0	1	0	0	1	0	1	1	0
0	1	1	1	1	0	1	0	0	1	1	1
1	0	0	0	1	0	1	1	0	1	0	1
1	0	0	1	1	1	0	0	0	1	1	0
1	0	1	0	1	0	0	0	0	1	1	1
1	0	1	1	1	0	0	1	1	0	0	0
1	1	0	0	1	1	1	0	1	0	0	1
1	1	0	1	1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1	1	0	1	1
1	1	1	1	0	1	0	0	1	1	0	0

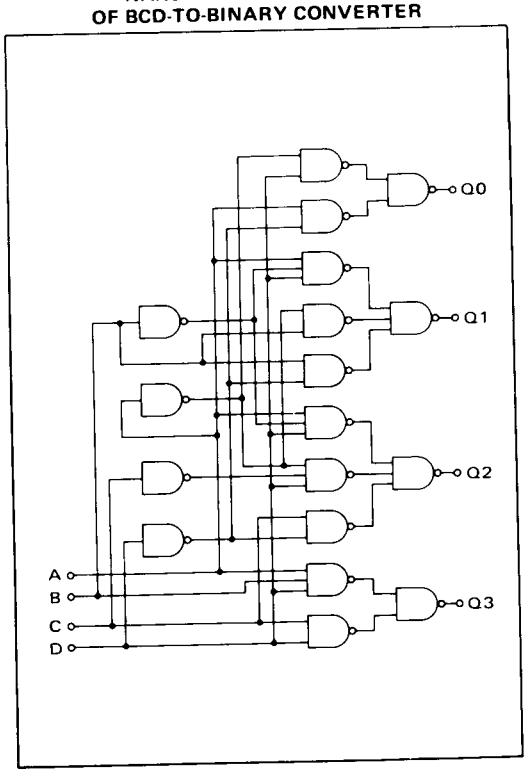
The MC4301/4001 serves as a basic building block in Binary-to-BCD and BCD- to-Binary converters. Conversion of any length binary or BCD word can be accomplished by interconnecting MC4001 packages. The MC4001 also contains a full adder and subtractor.

Features:
- Address times < 45 ns
- Outputs sink 16 mA
- Output capacitance < 7.0 pF @ 1.5 V

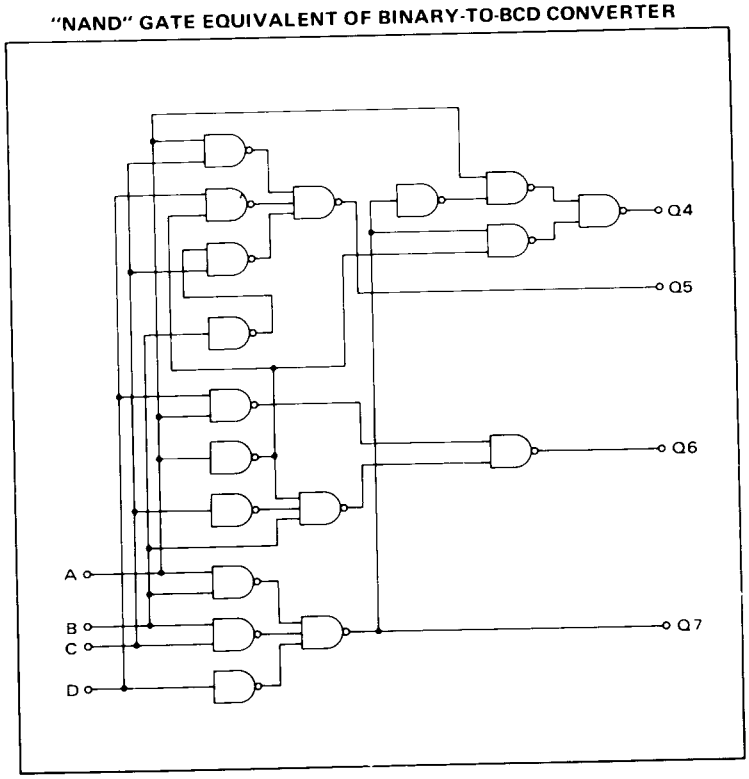
ENABLE INPUT TRUTH TABLE (POSITIVE LOGIC)

E	E	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	FUNCTION ENABLED							

"NAND" GATE EQUIVALENT OF BCD-TO-BINARY CONVERTER

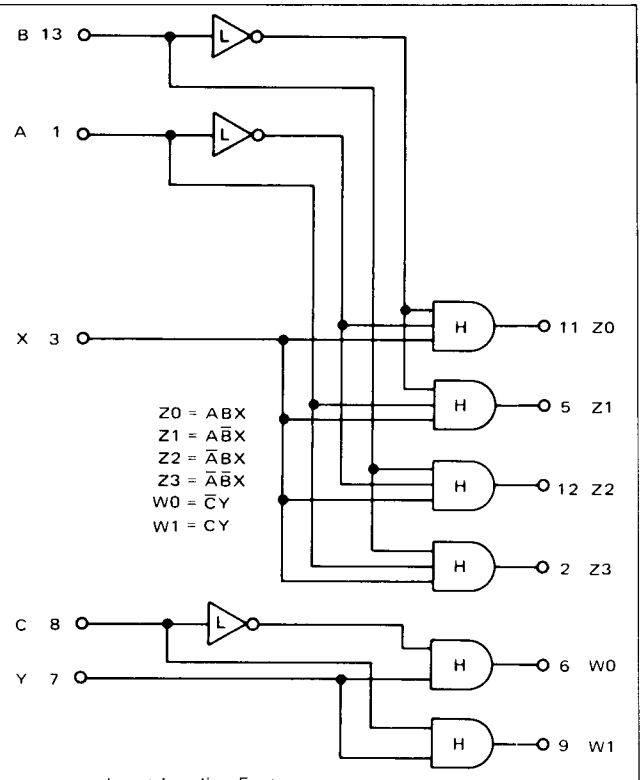


"NAND" GATE EQUIVALENT OF BINARY-TO-BCD CONVERTER



DUAL DATA DISTRIBUTOR

MC4302
MC4002



Input Loading Factor:
A, B = 3
C, Y = 2
X = 4

Output Loading Factor = 10

Total Power Dissipation = 175 mW typ/pkg

V_{CC} = PIN 4
GND = PIN 10

This device consists of two data distributors constructed from high-level AND gates and low-level inverters. One distributes information present at the input line to one of four output lines; the other distributes information present at the input to one of two output lines. The routing path is selected by the logic signals at the control lines A, B or C.

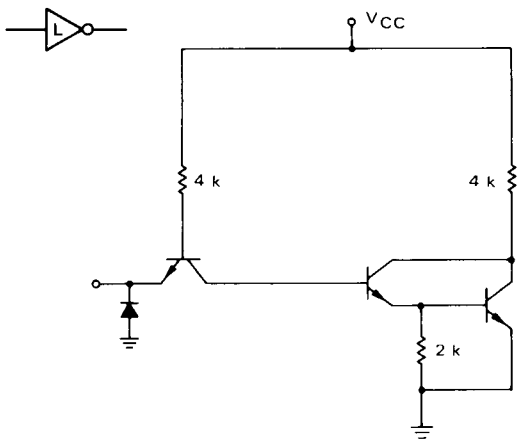
Data distributors are useful in applications where digital data is to be routed from a single register or location to one of several registers or locations for processing.

TYPICAL PROPAGATION DELAY TIMES (ns)
T_A = 25°C

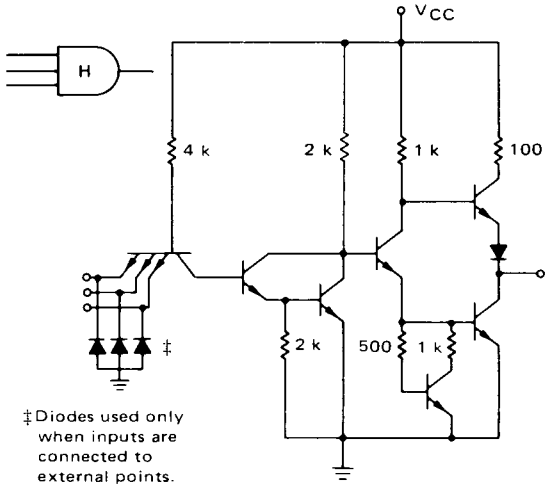
INPUT	Z0	Z1	Z2	Z3
A	14.5	10.5	14.5	10.5
B	14.5	14.5	10.5	10.5
X	10.5	10.5	10.5	10.5

INPUT	W0	W1
C	14.5	10.5
Y	10.5	10.5

LOW-LEVEL INVERTER



HIGH-LEVEL "AND" GATE



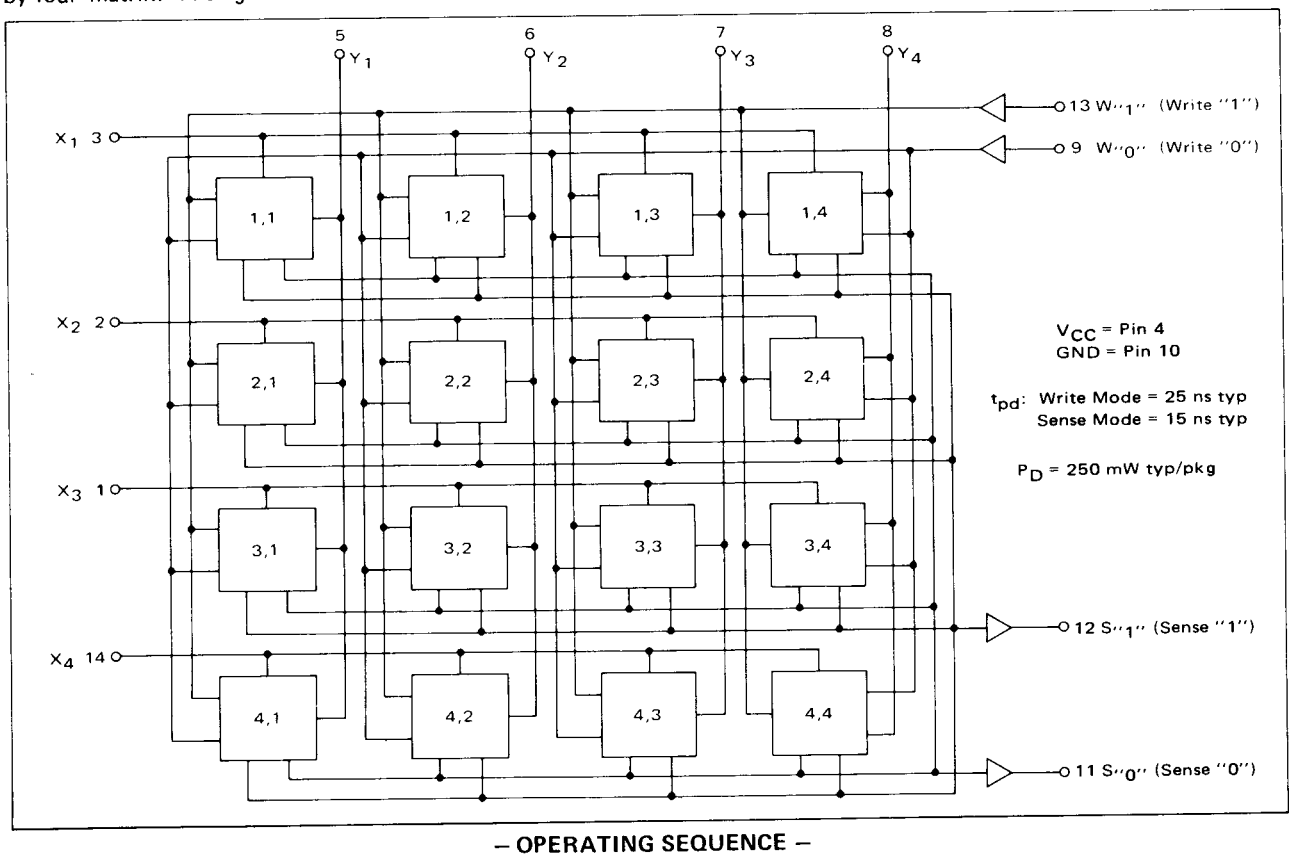
‡Diodes used only when inputs are connected to external points.

16-BIT SCRATCH PAD
MEMORY CELL

MC4304 • MC4305
MC4004 • MC4005

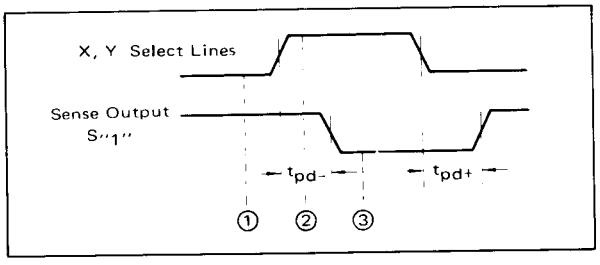
This 16-Bit memory cell serves as the basic building block for scratch pad memory systems having cycle times of less than 100 ns. The basic cell provides 16 words of one-bit memory operating in the non-destructive readout (NDRO) mode.

The memory contains 16 flip-flops arranged in a four-by-four matrix. A single bit of the matrix is selected by driving one of four X select lines and one of four Y select lines above the select threshold. Two sense amplifiers are shared by all 16 bits and provide a double rail output from the selected bit. The sense output of many devices can be "wired ORed" together since the output stage does not have a pullup resistor or network. Two write amplifiers allow a "1" or a "0" to be written into a selected bit.



– OPERATING SEQUENCE –

FIGURE 1 – READ MODE TIMING DIAGRAM

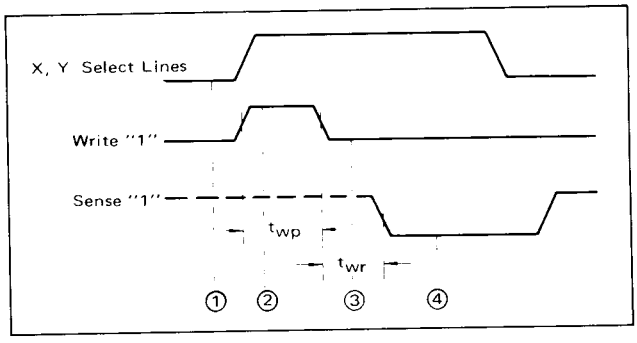


① All X and Y selection lines and both write inputs are low (less than +0.8 V).

② Desired bit selected by driving the appropriate X and Y select lines more positive than +2.1 V.

③ After the turn-on delay time(t_{pd-}), the S"1" output will be low (less than +0.45 V) and the S"0" output will be high (more than +2.5 V), providing that a "1" is stored in the selected bit.

FIGURE 2 – WRITE MODE TIMING DIAGRAM



① All X and Y selection lines and both write inputs are low (less than +0.8 V).

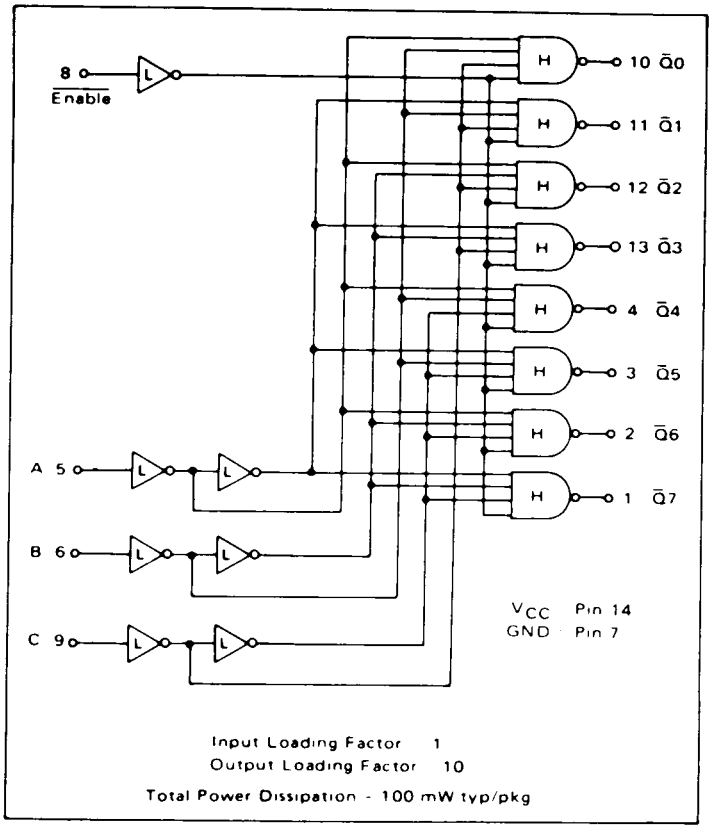
② Bit location selected by driving the appropriate X and Y select lines more positive than +2.1 V. To write a "1", drive the write "1" input more positive than +2.1 V for a minimum time of 25 ns (t_{wp}).

③ Write "1" line returned to low state.

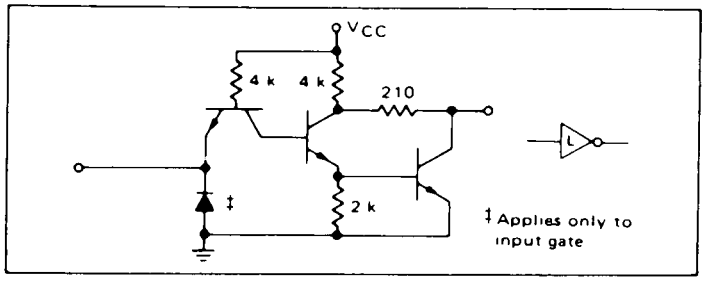
④ The stored bit can be read after the write recovery time (t_{wr}) of 40 ns. (The sense output is in an indeterminate state between steps 2 and 4.)

BINARY TO ONE-OF-EIGHT LINE DECODER

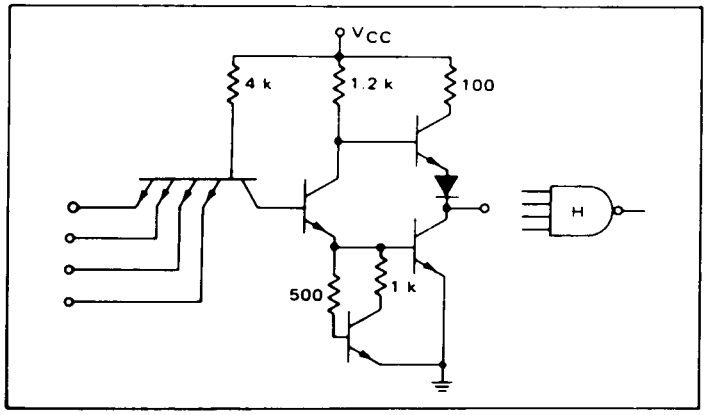
MC4306
MC4006



LOW-LEVEL INVERTER



HIGH-LEVEL GATE



This device converts three lines of input data to a one-of-eight output. The enable line provides an inhibit capability and also allows the decoder to be expanded for larger decoder systems.

The 3-input/8-output decoder consists of high-level and low-level gates internally connected for minimum power consumption and maximum driving capabilities. The enable gate must be in the low state to perform the decode operation shown in the truth table.

The propagation delays shown in the charts are typical and vary according to loading, interconnection wiring length, and the number of logic levels involved.

Ē 0

TRUTH TABLE

C	B	A	Q̄7	Q̄6	Q̄5	Q̄4	Q̄3	Q̄2	Q̄1	Q̄0
0	0	0	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	0	1
0	1	0	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	1	1	0	1	1	1	1
1	0	1	1	1	0	1	1	1	1	1
1	1	0	1	0	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1

1 High State
0 Low State

TYPICAL TURN-ON DELAY TIMES (ns)
T_A 25°C, C_T - 25 pF

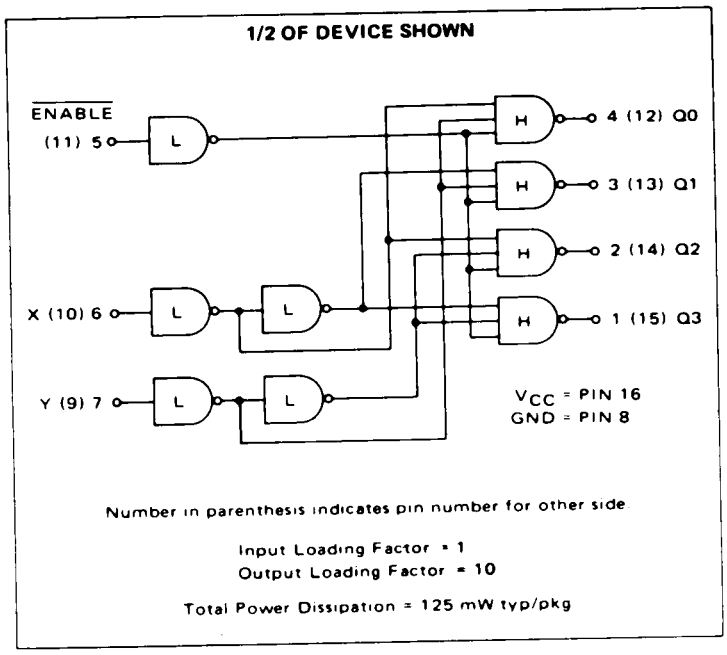
INPUT	Q̄0	Q̄1	Q̄2	Q̄3	Q̄4	Q̄5	Q̄6	Q̄7
A	11.5	16.0	11.5	16.0	11.5	16.0	11.5	16.0
B	11.5	11.5	16.0	16.0	11.5	11.5	16.0	16.0
C	11.5	11.5	11.5	11.5	16.0	16.0	16.0	16.0
Ē	13.5	13.5	13.5	13.5	13.5	13.5	13.5	13.5

TYPICAL TURN-OFF DELAY TIMES (ns)
T_A = 25°C, C_T = 25 pF

INPUT	Q̄0	Q̄1	Q̄2	Q̄3	Q̄4	Q̄5	Q̄6	Q̄7
A	14.0	19.5	14.0	19.5	14.0	19.5	14.0	19.5
B	14.0	14.0	19.5	19.5	14.0	14.0	19.5	19.5
C	14.0	14.0	14.0	14.0	19.5	19.5	19.5	19.5
Ē	14.5	14.5	14.5	14.5	14.5	14.5	14.5	14.5

DUAL BINARY TO ONE-OF-FOUR LINE DECODER

MC4307
MC4007



This device converts two lines of input data to a one-of-four output. The enable line provides an inhibit capability and also allows the decoder to be expanded for larger decoder systems.

The dual 2-input/4-output decoder consists of high-level and low-level gates internally connected for minimum power consumption and maximum driving capabilities. The enable gate must be in the low state to perform the decode operation shown in the truth table.

The propagation delays shown in the charts are typical and vary according to loading, interconnection wiring length, and the number of logic levels involved.

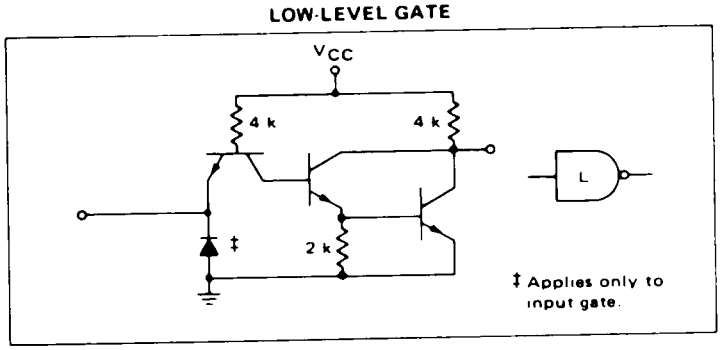
TRUTH TABLE

E = 0

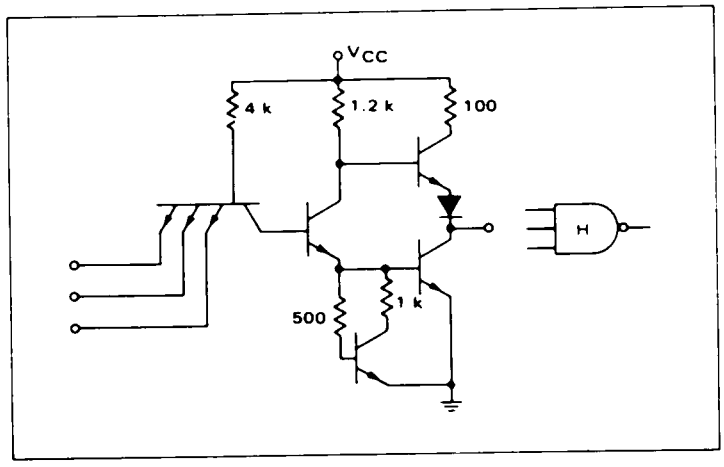
X	Y	Q0	Q1	Q2	Q3
0	0	0	1	1	1
1	0	1	0	1	1
0	1	1	1	0	1
1	1	1	1	1	0

1 = High State
0 = Low State

LOW-LEVEL GATE



HIGH-LEVEL GATE



TYPICAL TURN-ON DELAY TIMES (ns)
$T_A = 25°C$

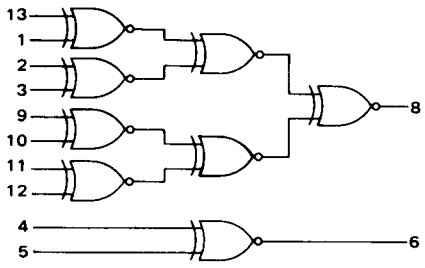
Input	Q0	Q1	Q2	Q3
X	11.5	15.5	11.5	15.5
Y	11.5	11.5	15.5	15.5
$\overline{E}$	13.5	13.5	13.5	13.5

TYPICAL TURN-OFF DELAY TIMES (ns)
$T_A = 25°C$

Input	Q0	Q1	Q2	Q3
X	14.0	19.0	14.0	19.0
Y	14.0	14.0	19.0	19.0
$\overline{E}$	14.5	14.5	14.5	14.5

8-BIT PARITY TREE

MC4308
MC4008



V_{CC} = Pin 14
GND = Pin 7

Positive Logic:
8 = 1⊙2⊙3⊙9⊙10⊙11⊙12⊙13
6 = 4⊙5
where $X \odot Y = (\bar{X} \cdot \bar{Y}) + (X \cdot Y)$

This device consists of seven Exclusive NOR gates connected to check even parity. The output will be in the logic "1" state as long as the "1" state is present on an even number of inputs. The additional Exclusive NOR gate can be used to connect two 8-bit parity trees to form a 16-bit parity tree, or it can be used to convert the parity tree to check odd parity by connecting one gate input to the output of the parity tree and grounding the other input. This conversion can also be accomplished by connecting a simple inverter to the output of the parity tree.

Input Loading Factor = 2
Output Loading Factor = 10

Total Power Dissipation = 150 mW typ/pkg
Propagation Delay Time = 15-30 ns typ

TYPICAL PROPAGATION DELAY TIMES

FIGURE 1 – THREE-GATE DELAY versus TEMPERATURE

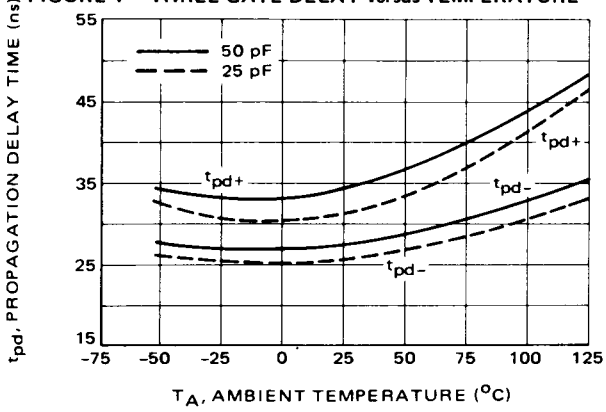


FIGURE 2 – ONE-GATE DELAY versus TEMPERATURE

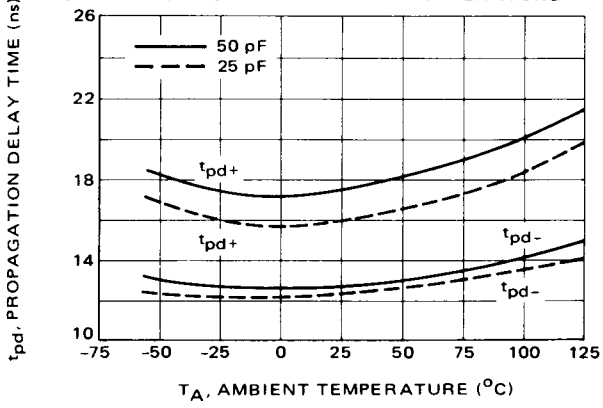


FIGURE 3 – DELAY versus LOAD CAPACITANCE

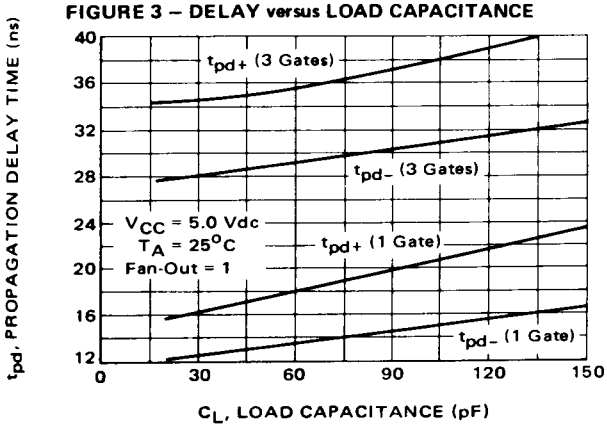
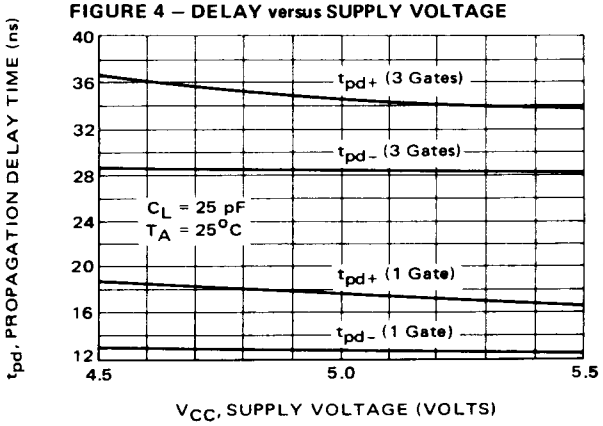
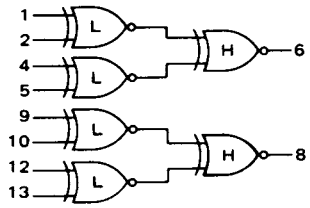


FIGURE 4 – DELAY versus SUPPLY VOLTAGE



DUAL 4-BIT PARITY TREE

MC4310
MC4010



V_{CC} = PIN 14
GND = PIN 7

Positive Logic:
$6 = 1 \odot 2 \odot 4 \odot 5$
where $X \odot Y = \overline{X} \cdot \overline{Y} + X \cdot Y$

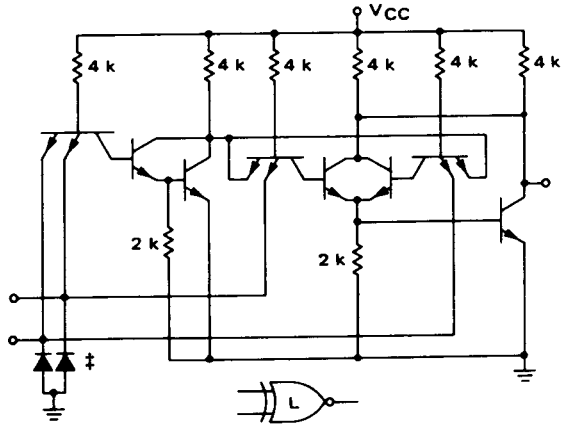
Input Loading Factor = 2
Output Loading Factor = 10

Total Power Dissipation = 125 mW typ/pkg
Propagation Delay Time = 9.5 to 22 ns typ

Three Exclusive NOR gates are connected together to form each of the two 4-bit parity trees in the package. An even number of logic "1" states on the inputs will result in a logic "1" output state. An odd parity checker can be made by connecting an inverter to the output of the device.

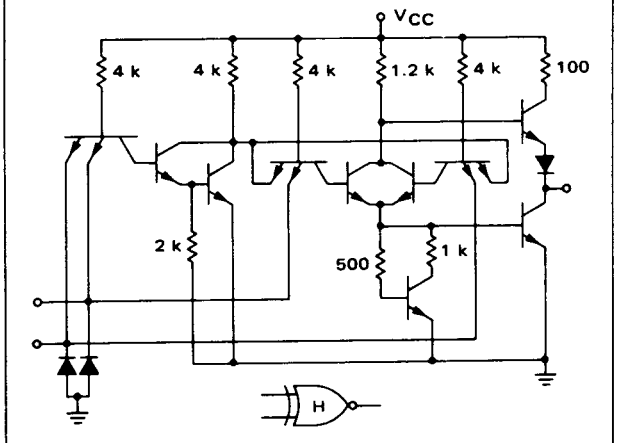
This function is constructed using low and high-level Exclusive NOR gates connected as shown in the logic diagram to maximize output drive capability and minimize power dissipation.

LOW-LEVEL GATE



‡Applies only to input gate.

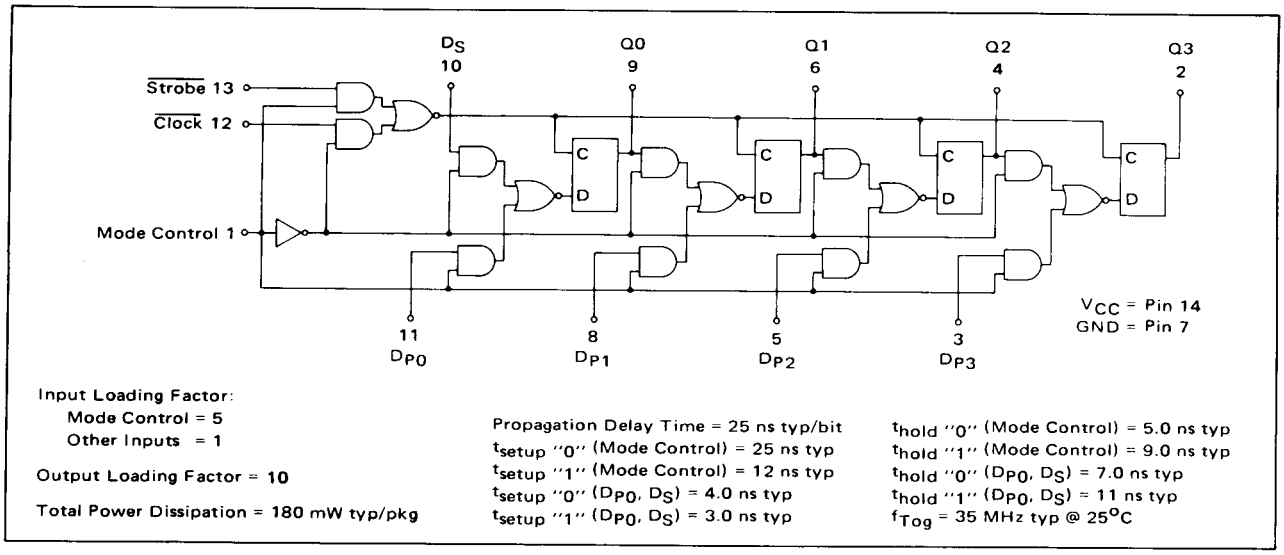
HIGH-LEVEL GATE



4-BIT SHIFT REGISTER

MC4312
MC4012

This 4-bit register provides parallel or serial data entry and retrieval, determined by the logic state of the mode control input. For parallel operation, set the mode control to the logic "1" state and strobe the information at the DP inputs into the register. Serial left-shift operation is achieved in this mode by connecting the Q outputs to the DP inputs of the previous stage. For serial right-shift operation, set the mode control to logic "0" and clock data into the register from D_S.



Input Loading Factor:
Mode Control = 5
Other Inputs = 1

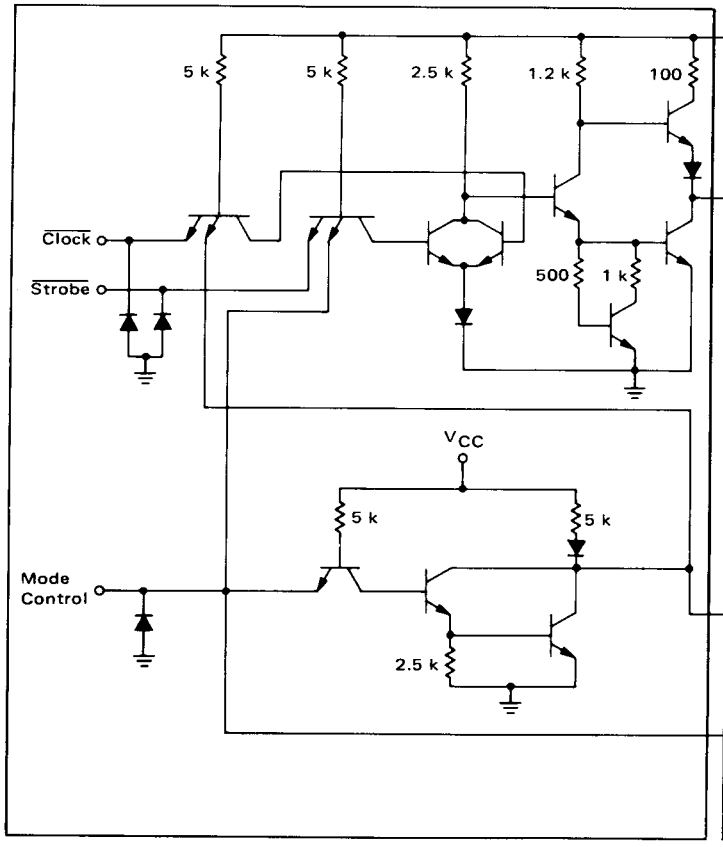
Output Loading Factor = 10

Total Power Dissipation = 180 mW typ/pkg

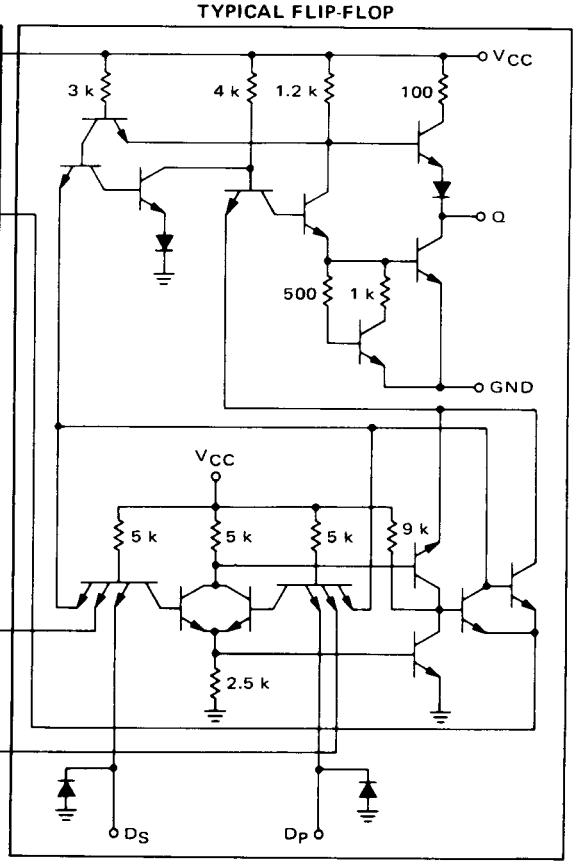
Propagation Delay Time = 25 ns typ/bit
t_{setup} "0" (Mode Control) = 25 ns typ
t_{setup} "1" (Mode Control) = 12 ns typ
t_{setup} "0" (D_{P0}, D_S) = 4.0 ns typ
t_{setup} "1" (D_{P0}, D_S) = 3.0 ns typ

t_{hold} "0" (Mode Control) = 5.0 ns typ
t_{hold} "1" (Mode Control) = 9.0 ns typ
t_{hold} "0" (D_{P0}, D_S) = 7.0 ns typ
t_{hold} "1" (D_{P0}, D_S) = 11 ns typ
f_{Tog} = 35 MHz typ @ 25°C

INPUT GATING



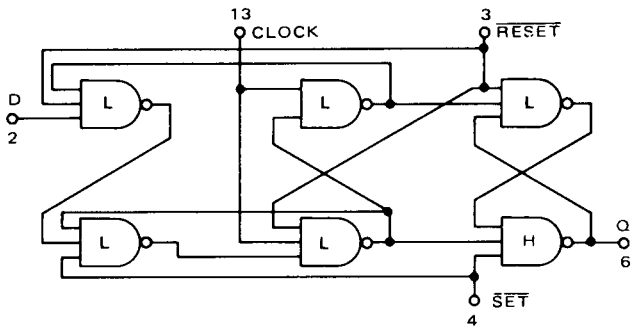
TYPICAL FLIP-FLOP



QUAD TYPE D FLIP-FLOP

MC4315
MC4015

1/4 OF DEVICE SHOWN
(CLOCK AND $\overline{\text{RESET}}$ COMMON TO ALL FOUR FLIP-FLOPS)



Input Loading Factor:
D = 1 CLOCK = 8
$\overline{\text{SET}}$ = 2 $\overline{\text{RESET}}$ = 8

V_{CC} = PIN 16
GND = PIN 8

Output Loading Factor = 10

Total Power Dissipation = 190 mW typ/pkg

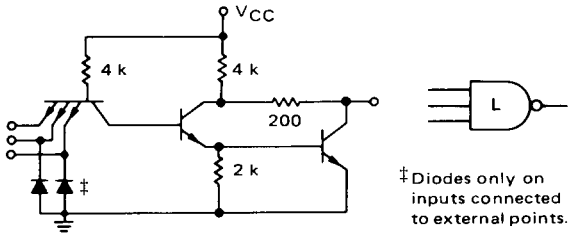
Propagation Delay Time = 16 ns typ

Setup Time = 10 ns max

Hold Time = 10 ns max

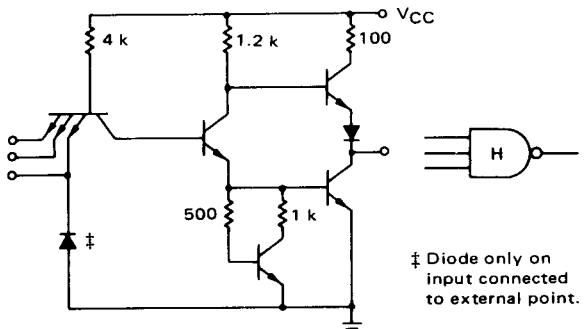
Operating Frequency = 30 MHz typ

LOW-LEVEL GATE



‡Diodes only on inputs connected to external points.

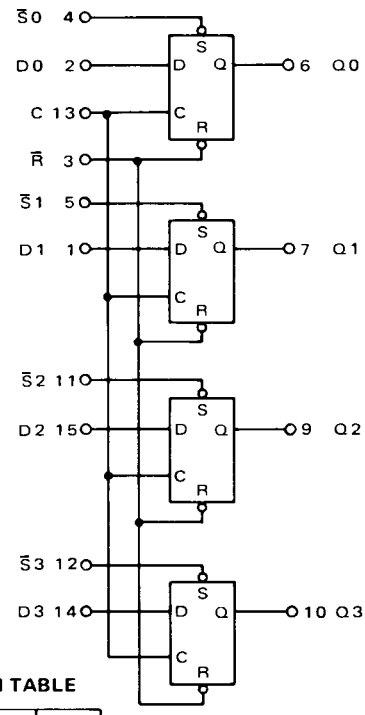
HIGH-LEVEL GATE



‡ Diode only on input connected to external point.

This quad type D flip-flop triggers on the positive edge of the clock input. During the clock transition the state of the D input is transferred to the Q output. The device is useful in shift registers and simple counters.

Power dissipation is minimized and output drive capability is maximized by connecting low and high-level gates as shown by the logic diagram to form each of the four flip-flops.



TRUTH TABLE

D	Q_{n-1}	Q_n
0	0	0
0	1	0
1	0	1
1	1	1

Q_{n-1} = time period prior to clock pulse
Q_n = time period following clock pulse

OPERATING CHARACTERISTICS

Data must be present at the D input 10 ns prior to the rise of the clock, and remain 10 ns after the clock signal rises. Data may be changed any time during the clock cycle except the interval between the setup time (10 ns) and the hold time (10 ns) without affecting the operation of the flip-flop. The data input is inhibited when the clock is high. When the clock is in the low state, the input steering section continually reflects the state of the D input. Information present at the D input during the time interval between the setup and hold times is transferred to the bistable section on the positive edge of the clock, and outputs Q and $\overline{Q}$ respond accordingly.

The flip-flops can be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct $\overline{\text{Set}}$ or $\overline{\text{Reset}}$ inputs.

PROGRAMMABLE MODULO-N COUNTERS

MC4316 MC4016
MC4317 MC4017
MC4318 MC4018
MC4319 MC4019

The monolithic devices are programmable, cascadable, modulo-N-counters. The MC4316/4016 can be programmed to divide by any number (N) from 0 thru 9, the MC4318/4018 from 0 thru 15. The MC4317/4017 consists of a modulo 2 counter which can be programmed to divide by 0 or 1 and a modulo 5 counter which can be programmed to divide by any number from 0 to 4. The MC4319/4019 contains two modulo 4 counters which can be programmed to divide by any number from 0 to 3.

The parallel enable ($\overline{PE}$) input enables the parallel data inputs D0 thru D3. All zeros are entered into the counter by applying a logic "0" level to the master reset ($\overline{MR}$) and $\overline{PE}$ inputs. This causes the counter to stop counting (count = 0). All data inputs are independent of the logic level of the Clock.

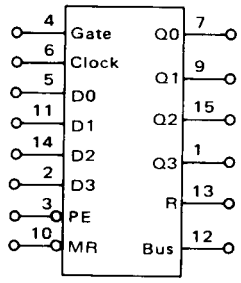
Modulo-N counters are useful in frequency synthesizers, in phase-locked loops, and in other applications where a simple method for frequency division is needed.

All Types:

Input Loading Factor:
Clock, $\overline{PE}$ = 2
D0, D1, D2, D3, Gate = 1
$\overline{MR}$ = 4
Output Loading Factor = 8

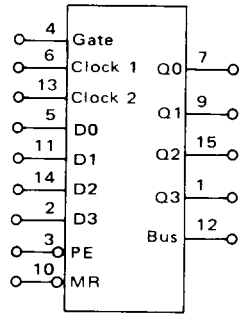
Total Power Dissipation = 250 mW typ/pkg
Propagation Delay Time:
Clock to Q3 = 50 ns typ
Clock to Bus = 35 ns typ

MC4316/4016
MC4318/4018



V_{CC} = Pin 16
Gnd = Pin 8

MC4317/4017
MC4319/4019



V_{CC} = Pin 16
Gnd = Pin 8

MC4316/4016

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC4318/4018

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC4317/4017

COUNT	OUTPUT
	Q0
1	1
0	0

COUNT	OUTPUT		
	Q3	Q2	Q1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

MC4319/4019

COUNT	OUTPUT	
	Q1	Q0
3	1	1
2	1	0
1	0	1
0	0	0

COUNT	OUTPUT	
	Q3	Q2
3	1	1
2	1	0
1	0	1
0	0	0

OPERATING CHARACTERISTICS

Basic operation of the MC4316/4016 and MC4318/4018 is the same. When operated as single stages, the Gate and Clock inputs must be tied together. The internal pullup resistor must be connected to the Buss node (pin 13 to pin 12). The programmable counter is set to count down by a pre-determined number (N) before recycling, according to the binary code present at the parallel preset inputs, P0 thru P3 (see the truth table). The binary information at inputs P0 thru P3 is preset into the counter after applying a logic "0" to the $\overline{PE}$ input. Data may be entered synchronously or asynchronously while $\overline{PE}$ is low, or when outputs Q0, Q1, Q2 and Q3 are in the logic "0" state and the Clock is low.

The counters may be set to divide by 10 (MC4316/4016) or 16 (MC4318/4018) regardless of preset input states by applying a logic "0" to the Buss node. This, in effect, disables the preset inputs and causes a logic "0" to appear at the preset of each flip-flop of the counter. If a binary number greater than nine (1001) is applied to the preset inputs of the MC4316/4016, the counter will ignore the most significant bit and recognize only the three least significant bits.

Cascading of Counters

To cascade counters (Figure 1):

1. Connect Gate inputs of all stages to the Clock of the first stage.
2. Connect all Buss outputs to one common pullup resistor (2.0 kilohms, internal).
3. Connect the Clock input of each stage after the first stage to the Q3 output of the previous stage.
4. Take the divide-by-N pulse from the Buss outputs.

When cascaded, the count mode of the entire string of counters is defined by:

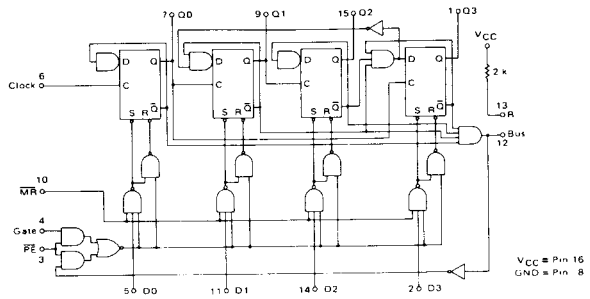
$$N = N_0 + 10\,N_1 + 100\,N_2 + \ldots \text{ (MC4316/4016)}$$

or $$N = N_0 + 16\,N_1 + 256\,N_2 + \ldots \text{ (MC4318/4018)}$$

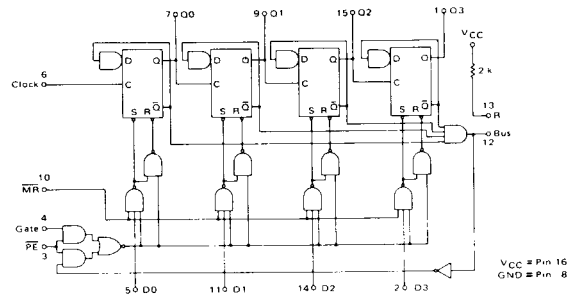
where N_0, N_1, N_2, . . . are the BCD or binary numbers programmed at the zero, first, second, . . . stages.

LOGIC DIAGRAMS

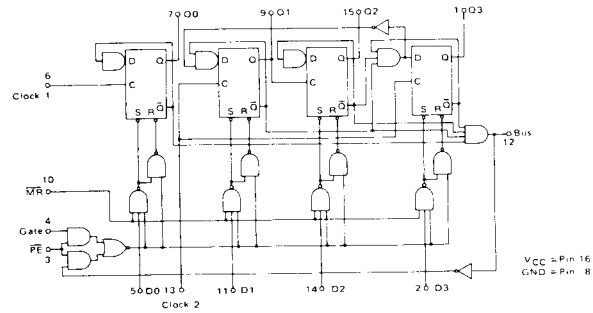
MC4316/4016



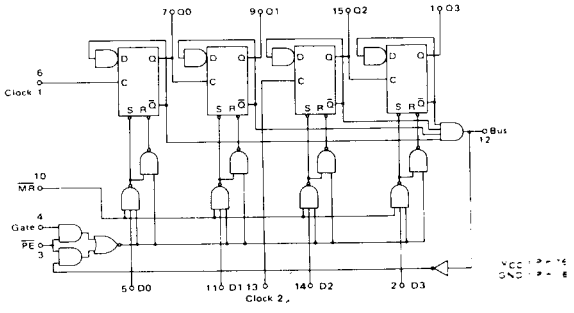
MC4318/4018



MC4317/4017



MC4319/4019



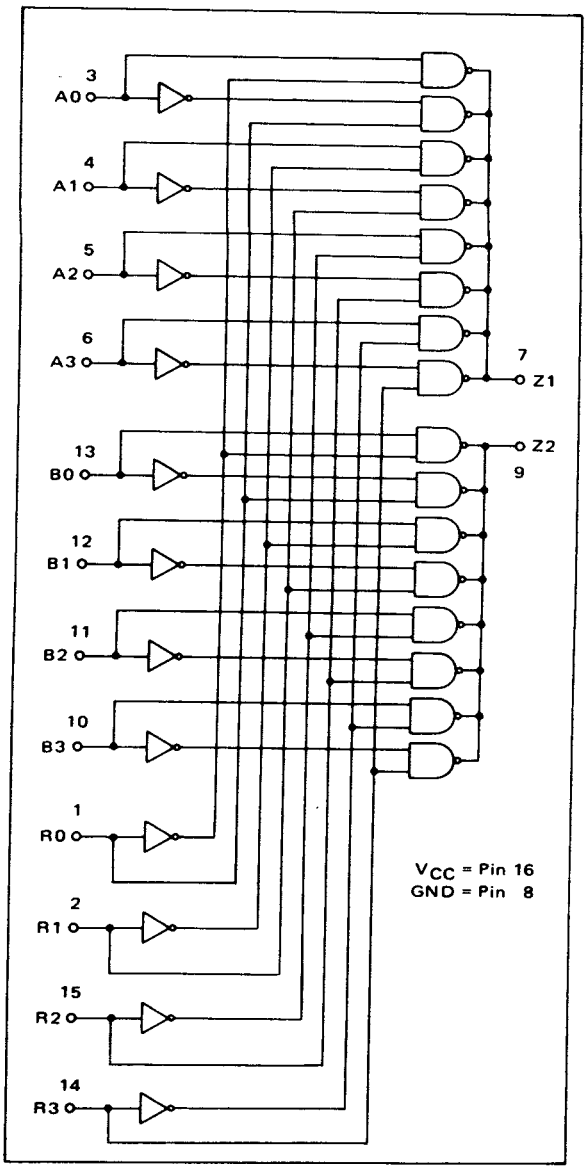
DUAL 4-BIT COMPARATOR

MC4321/4021
MC4322/4022

The 4-bit comparator compares four bits of input information to four bits of reference information. When each bit of the input information is the same as its corresponding reference information, bit for bit, the output of the comparator will be in the high ("1") state. For any other condition, the output of the comparator will be in the low ("0") state.

In this dual 4-bit comparator, the four reference inputs (R) serve both comparators. There is no interrelation between the A and B data inputs of the dual comparator. Output Z1 reflects comparison of the A and R bits, while output Z2 shows conditions at inputs B and R.

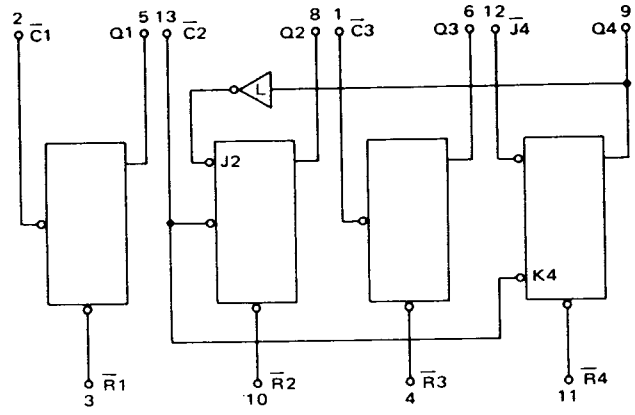
The MC4021 has open-collector outputs; the MC4022 has totem-pole outputs.



A0	A1	A2	A3	B0	B1	B2	B3	R0	R1	R2	R3	Z1	Z2
0	0	0	0	0	0	1	1	0	0	0	0	1	0
0	0	0	0	0	0	1	1	0	0	0	1	0	0
0	0	0	0	0	0	1	1	0	0	1	0	0	0
0	0	0	0	0	0	1	1	0	0	1	1	0	1
0	1	1	0	0	1	0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	1	0	1	0	1	0	1
0	1	1	0	0	1	0	1	0	1	1	0	1	0
0	1	1	0	0	1	0	1	0	1	1	1	0	0
1	0	0	1	1	0	0	0	1	0	0	0	0	1
1	0	0	1	1	0	0	0	1	0	0	1	1	0
1	0	0	1	1	0	0	0	1	0	1	0	0	0
1	0	0	1	1	0	0	0	1	0	1	1	0	0
1	1	1	1	1	1	1	1	1	1	0	0	0	0
1	1	1	1	1	1	1	1	1	1	0	1	0	0
1	1	1	1	1	1	1	1	1	1	1	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Input Loading Factor = 2
Output Loading Factor = 10
Total Power Dissipation = 250 mW typ/pkg
Propagation Delay Time = 20 ns typ

MC4323
MC4023



V_{CC} = Pin 14
GND = Pin 7

Input Loading Factor:
$\bar{J}$ = 1
$\bar{C}1$, $\bar{C}3$ = 2
$\bar{C}2$, $\bar{R}$ = 3

Output Loading Factor = 10

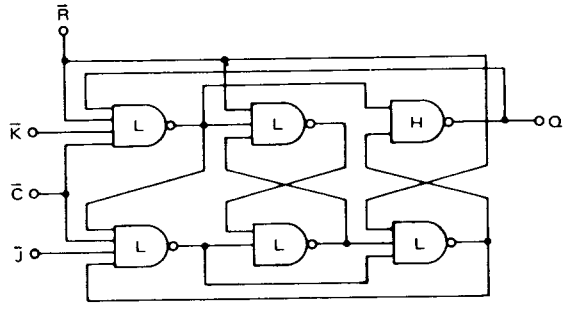
Total Power Dissipation = 200 mW typ/pkg
Propagation Delay Time = 16 ns typ/bit
Operating Frequency = 30 MHz typ

This device is a 4-bit counter with internally connected feedback. Inputs and outputs can be connected to count to any number between two and twelve except seven and eleven. Reset inputs are provided on each flip-flop to allow direct setting of the Q outputs to zero any time during the counting cycle.

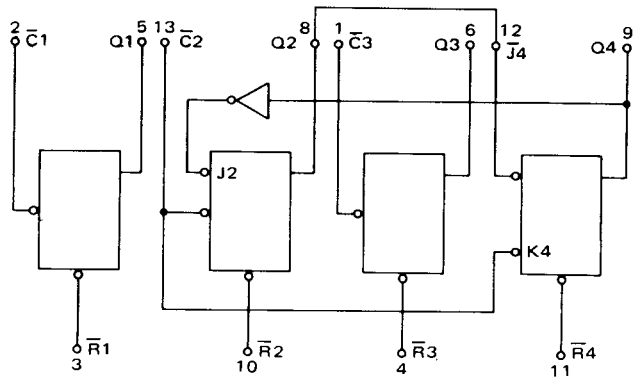
Each flip-flop in the counter is built from high and low-level gates as shown by the logic diagram. The flip-flops and the feedback inverter are connected as shown by the block diagram to provide minimum power dissipation and maximum drive capability.

LOGIC DIAGRAM

One flip flop shown. Only inputs shown on block diagram are present.



COUNTING SEQUENCES



DIVIDE BY 3

C̄2	Q2	Q4
0	0	0
1	1	0
2	0	1

DIVIDE BY 4

C̄1	Q1	Q3
0	0	0
1	1	0
2	0	1
3	1	1

DIVIDE BY 6

C̄1	Q1	Q2	Q4
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1

DIVIDE BY 12

C̄3	Q3	Q1	Q2	Q4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1

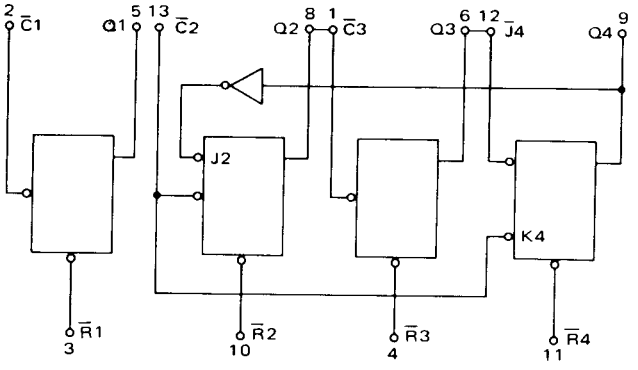
DIVIDE BY 2: Use flip-flop 1 or 3.

DIVIDE BY 3: Use flip-flops 2 and 4, connected as shown. The input signal is applied to C̄2; the output is taken from Q4.

DIVIDE BY 4: Use flip-flops 1 and 3; connect Q1 to C̄3. Apply the input signal to C̄1.

DIVIDE BY 6: In addition to the connection for divide by 3, connect Q1 to C̄2. Apply the input signal to C̄1.

DIVIDE BY 12: In addition to the connections for divide by 6, connect Q3 to C̄1. Apply the input signal to C̄3.



DIVIDE BY 5

C̄2	Q2	Q3	Q4
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1

DIVIDE BY 8

C̄1	Q1	Q2	Q3
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1

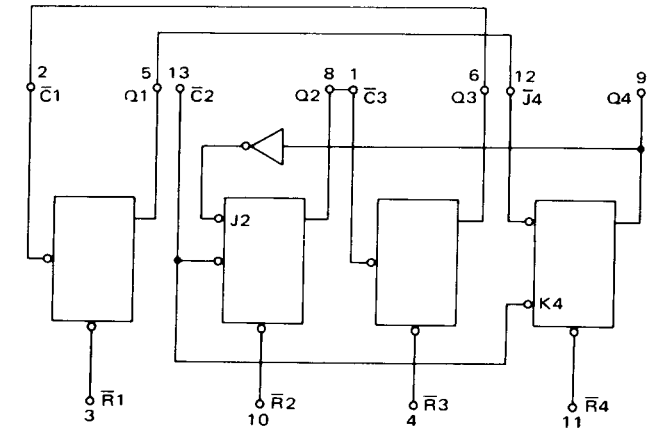
DIVIDE BY 10

C̄1	Q1	Q2	Q3	Q4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

DIVIDE BY 5: Connect flip-flops 2, 3, and 4 as shown. The input signal is applied to C̄2; the output is taken from Q4.

DIVIDE BY 8: Connect flip-flops 2 and 3 as shown for divide by 5, but do not connect Q3 to J̄4. Connect Q1 to C̄2. The input signal is applied to C̄1; the output is taken from Q3.

DIVIDE BY 10: In addition to the connections for divide by 5, connect Q1 to C̄2. Apply the input signal to C̄1.



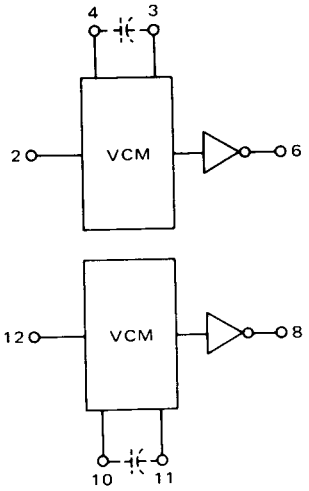
DIVIDE BY 9

C̄2	Q2	Q3	Q1	Q4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1

DIVIDE BY 9: The input signal is applied to C̄2; the output is taken from Q4.

DUAL VOLTAGE-CONTROLLED MULTIVIBRATOR

MC4324
MC4024



The MC4324/4024 voltage-controlled multivibrator provides appropriate level shifting to produce an output compatible with MTTL logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single capacitor. Variation of the output frequency over a 3.5 to 1 range is possible with an input dc control voltage of +1.0 to +5.0 volts.

Voltage-controlled multivibrators are used in phase-locked loops for digital frequency control. They may also be used for some types of A to D converters.

V_{CC}: VCM = 1, 13
Output Buffer = 14

GND: VCM = 5, 9
Output Buffer = 7

External Capacitor for
Frequency Range Determination

Output Loading Factor = 7

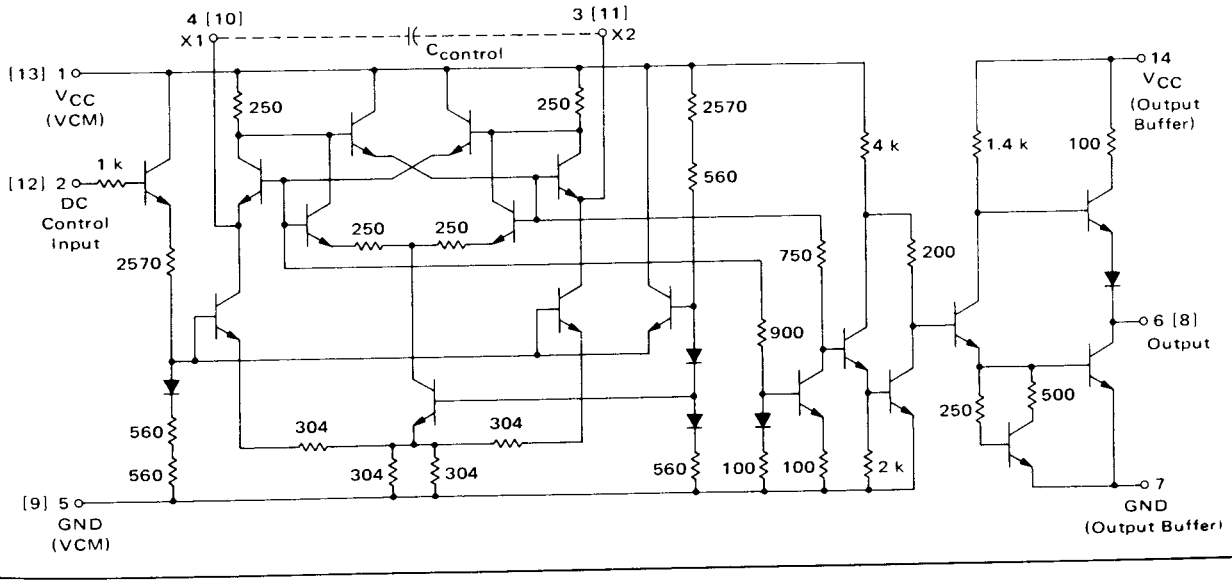
Power Dissipation = 150 mW typ/pkg

Maximum Operating Frequency = 30 MHz typ

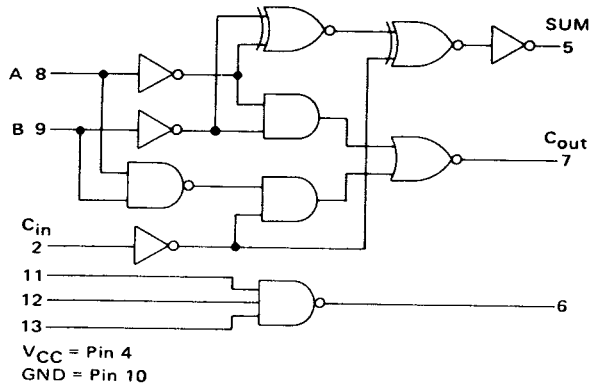
CIRCUIT SCHEMATIC

1/2 OF CIRCUIT SHOWN

(Numbers in brackets are pin numbers for other half.)



MC4326 • MC4327
MC4026 • MC4027



These full adders are designed for serial and ripple-carry parallel adder systems. True Sum and Carry are produced at the output from the input information. A separate 3-input NAND gate is provided on the monolithic chip to provide the inverted Sum or Carry output.

Input Loading Factor:
A, B = 2
C_{in}, Pins 11, 12, 13 = 1

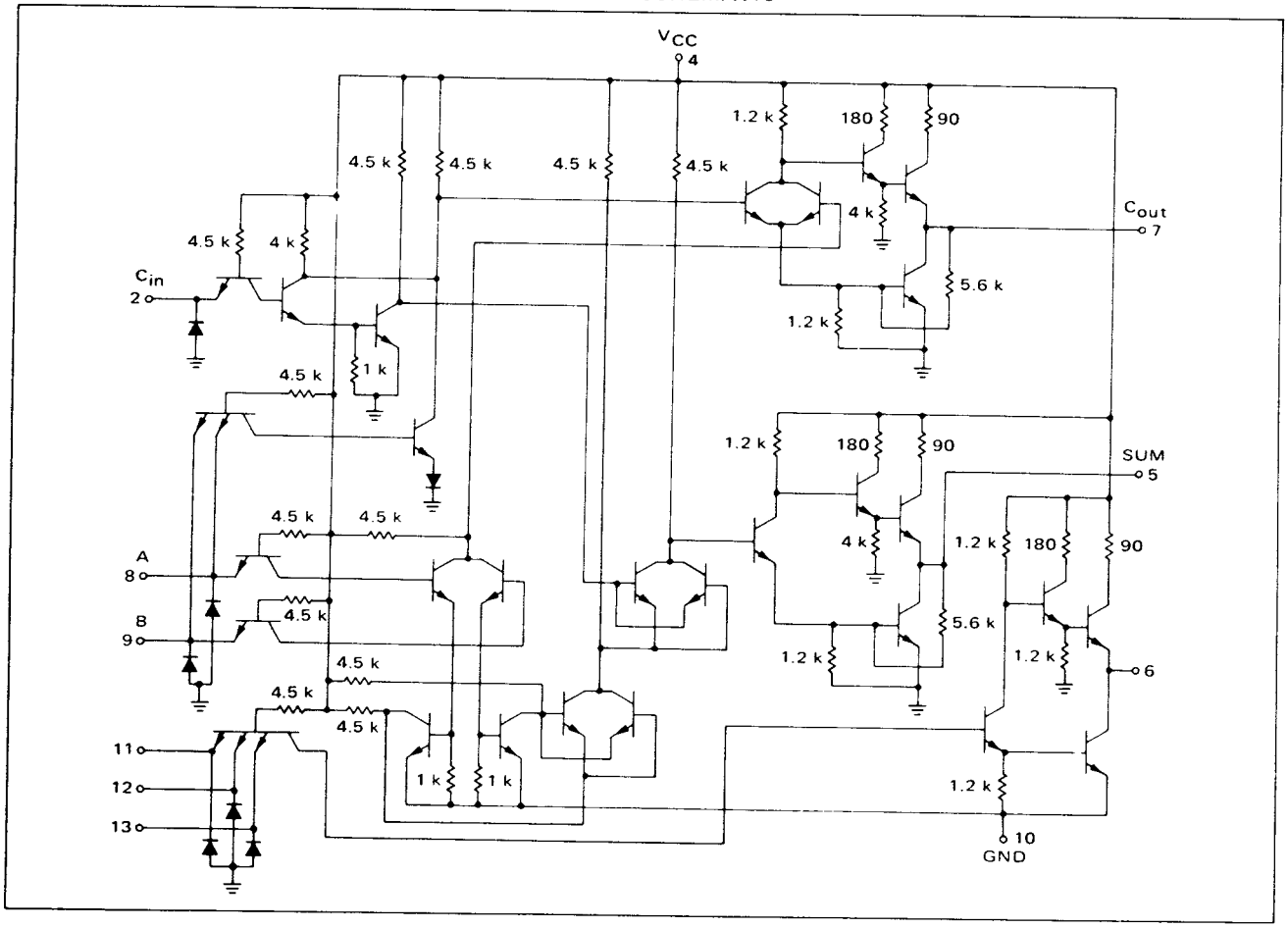
Output Loading Factor:
MC4326 = 15 MTTL I Loads
MC4327 = 7 MTTL I Loads
MC4026 = 12 MTTL I Loads
MC4027 = 6 MTTL I Loads

TRUTH TABLE

Input Pins			Output Pins	
8	9	2	5	7
A	B	C_{in}	SUM	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Total Power Dissipation = 90 mW typ/pkg
Add Delay = 25 ns typ
Carry Delay = 13 ns typ

CIRCUIT SCHEMATIC



MC4328 thru MC4331
MC4028 thru MC4031

This family of fast adders is designed for use in parallel look-ahead carry adder applications where high-speed addition is required. The dependent-carry fast adders have a Carry output that is dependent upon the two input bits for that stage plus the Carry input from all previous stages. The Carry output from the MC4330/31 is independent of the carry from the previous stages.

CONDENSED TRUTH TABLE FOR THE Nth STAGE

Pin Numbers 8	9	11	12,13	13, 14, 1	5	6	7		
A_n	B_n	$C_{in1(n-1)}$	Note 1	Note 2	Sum	$\oplus_{out}$	MC4330/4030 MC4331/4031 C_{out}	MC4328/4028 MC4329/4029 C_{out}	Comment Note 3
0	0	0	0	0	0	0	0	0	–
0	0	0	0	1	1	0	0	0	–
0	0	1	1	0	1	0	0	0	–
0	0	1	1	1	1	0	0	0	ϕ
0	0	1	0	0	1	0	0	0	–
0	0	1	0	1	1	0	0	0	ϕ
0	1	0	0	1	1	0	0	0	ϕ
0	1	0	1	0	1	0	0	0	ϕ
0	1	0	1	1	0	1	0	1	–
0	1	1	0	0	0	1	0	1	–
0	1	1	0	1	0	1	0	1	ϕ
0	1	1	1	0	0	1	0	1	ϕ
0	1	1	1	1	0	1	0	1	ϕ
1	0	0	0	1	1	1	0	1	–
1	0	0	1	0	1	1	0	1	–
1	0	0	1	1	0	1	0	1	ϕ
1	0	1	0	0	0	1	0	1	ϕ
1	0	1	0	1	0	1	0	1	ϕ
1	0	1	1	0	0	1	0	1	ϕ
1	0	1	1	1	0	1	0	1	ϕ
1	1	0	0	0	1	0	1	1	–
1	1	0	0	1	0	0	1	1	–
1	1	0	1	0	0	0	1	1	–
1	1	0	1	1	1	0	1	1	ϕ
1	1	1	0	0	1	0	1	1	–
1	1	1	0	1	1	0	1	1	ϕ
1	1	1	1	0	1	0	1	1	ϕ
1	1	1	1	1	1	0	1	1	ϕ

Note 1 This column represents the AND function whose inputs are pins 13 and 12, and is defined by the expression $(A_{n\,1} \oplus B_{n\,1})(C_{in\,n\,2})$

Note 2 This column represents the AND function whose inputs are pins 13, 14, and 1, and is defined by the expression $(A_{n\,1} \oplus B_{n\,1})(A_{n\,2} \oplus B_{n\,2})(C_{n\,3})$

Note 3. ϕ Don't Care. The "Don't Care" occurs for the MC4330 31/4030 31 only, because the C_n and the $\oplus_n$ from any one previous stage entering a given subsequent stage cannot be simultaneously at logic "1"

Input Loading Factor:
- $\oplus_{in1}$, A, B = 2
- $\oplus_{in2}$, C_{in1}, C_{in2}, C_{in3} = 1

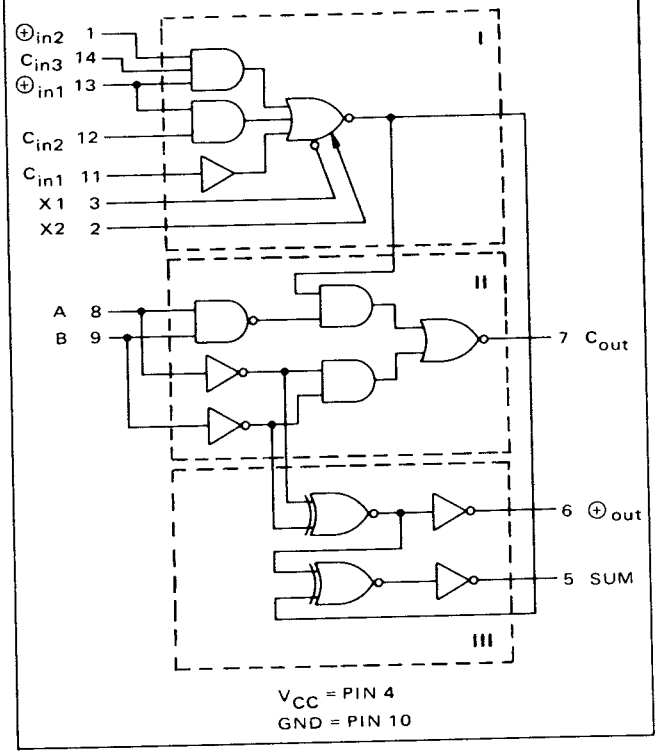
Output Loading Factor:
- MC4328, MC4330 = 15 MTTL I Loads
- MC4329, MC4331 = 7 MTTL I Loads
- MC4028, MC4030 = 12 MTTL I Loads
- MC4029, MC4031 = 6 MTTL I Loads

Total Power Dissipation = 125 mW typ/pkg

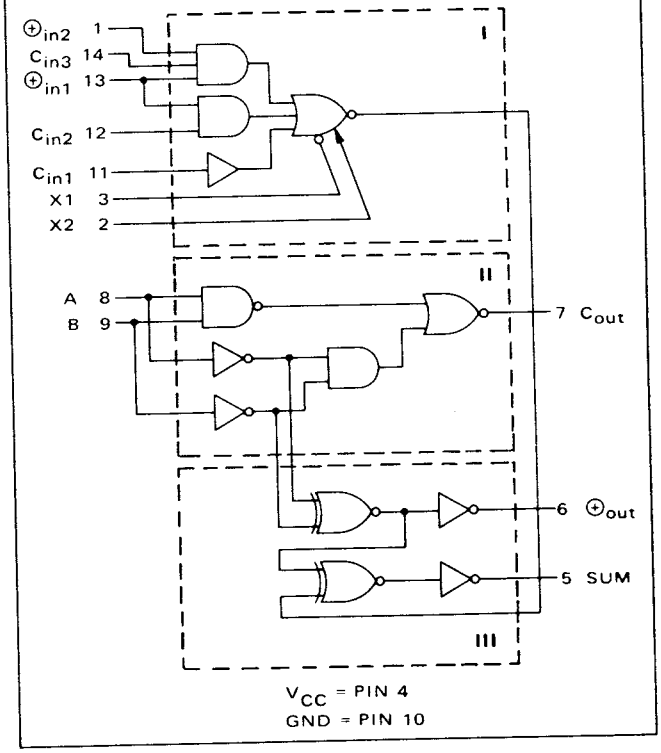
Add Delay = 25 ns typ

Carry Delay = 13 ns typ

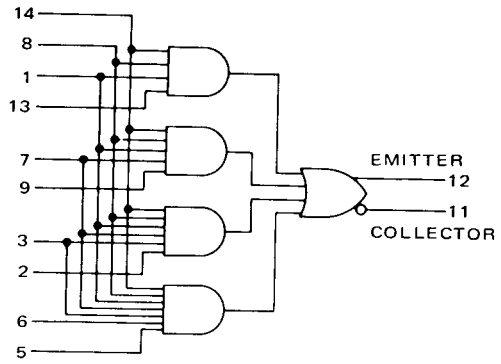
DEPENDENT-CARRY FAST ADDER
MC4328/4028, MC4329/4029



INDEPENDENT-CARRY FAST ADDER
MC4330/4030, MC4331/4031



MC4332
MC4032



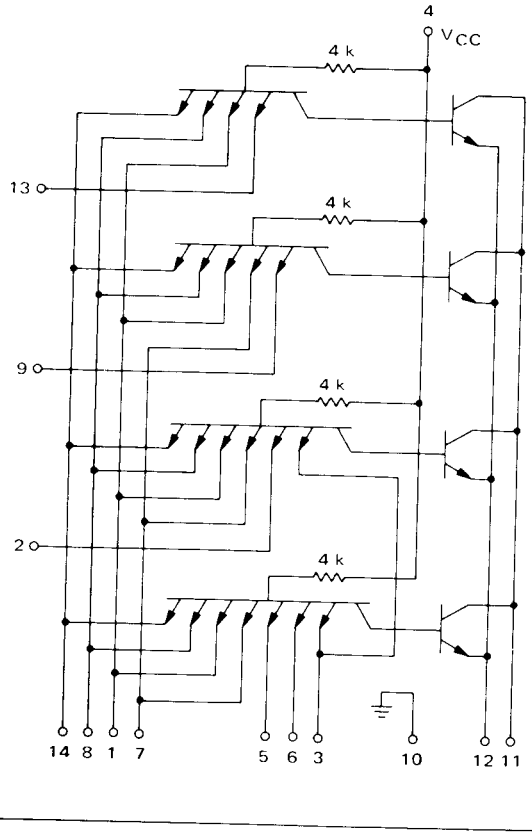
V_{CC} = Pin 4
GND = Pin 10

This 4-wide 4, 5, 6, 7 input AND-OR expander provides the necessary logic for carry decoding between look-ahead carry adder stages using the MC4328/29 and MC4330/31 fast adders.

Input Loading Factor:
- Pins 1, 8, 14 = 4
- Pin 7 = 3
- Pin 3 = 2
- Pins 2, 5, 6, 9, 13 = 1

Total Power Dissipation = 20 mW typ/pkg

Δt_{pd} = 4.0 ns typ/decoder
1.0 ns typ/pF at expander nodes



TYPICAL APPLICATION

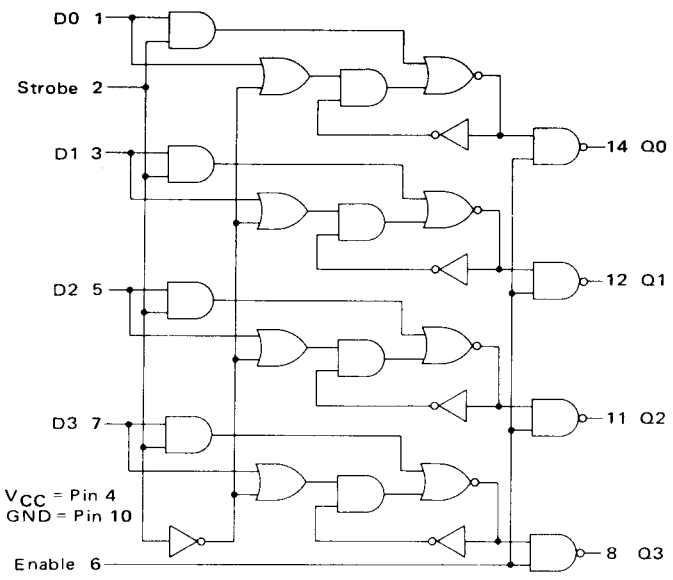
The MC4328/29 and MC4330/31 adders can be used with the MC4332 Carry Decoder to build 8-stage look-ahead carry subsystems. (See the MC4328-31) data sheet for a diagram.) Each stage examines the carry outputs from all previous stages while adding bits A and B for that stage. The carry outputs of the first and eighth stages are dependent upon the carry inputs from previous stages; thus the MC4328/29 adder is used for stages one and eight while the MC4330/31 adder is used for stages two through seven. The MC4332 Carry Decoder is used to expand the look-ahead carry input capability required for stages four through eight.

The add delay of an eight stage adder is equal to the sum of the add delay and the delay from the A and B inputs to the ⊕ output of one stage. Thus the typical add delay for an 8-stage adder is 25 ns +13 ns or 38 ns typical.

When expander inputs are not used they should not be connected to any external point. This minimizes possible problems resulting from noise pick-up.

QUAD LATCH
(Open Collector)

MC4335
MC4035



Two 5.0 k ohm pullup resistors are internally connected to V_{CC} and brought out on pins 9 and 13.

This monolithic device consists of four latch circuits with open collector outputs, common Strobe input, and output enable input. The output of each latch will follow the data input when the Strobe input is in a logical "1" state. When the Strobe is in a logical "0" state, the latch will store the logic state of the data input just prior to the change of the Strobe from a "1" level to a "0" level.

The open collector outputs make this device useful for bussing or wire ORing outputs together. Two 5.0 k ohm resistors are available in the package to provide the passive pullup function in wired-OR or bussed operation. The output enable is useful where it is desirable to gate information out of the latches according to a predetermined timing scheme.

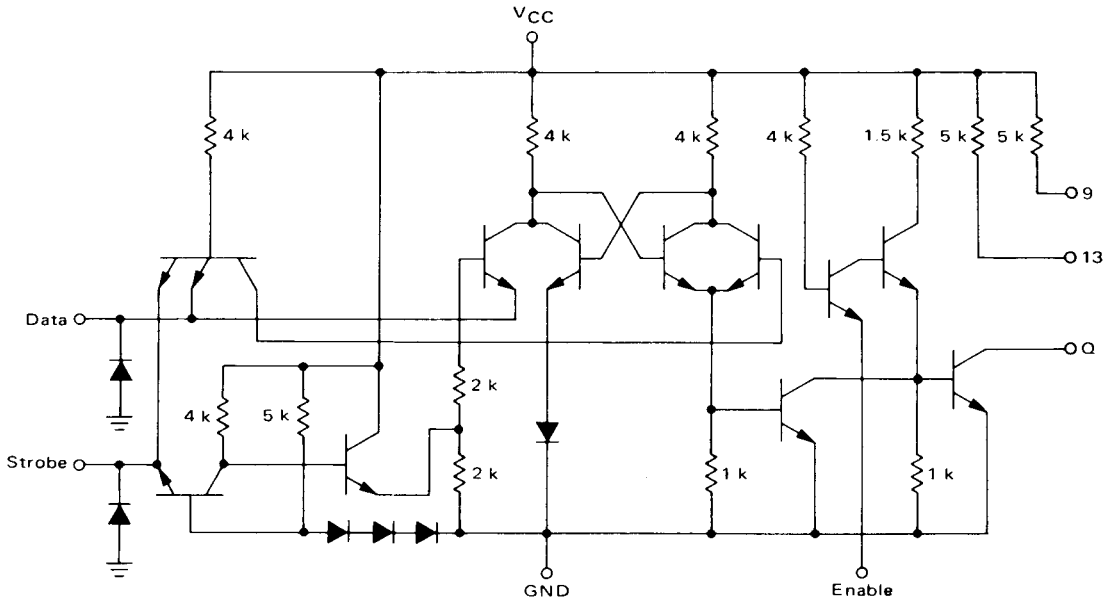
Input Loading Factor (MTTL I Loads):
- Data Input (Strobe High) — MC4335 = 4.2
  MC4035 = 4.0
- Data Input (Strobe Low) — MC4335 = 1.1
  MC4035 = 0.9
- Output Enable — MC4335 = 4.0
  MC4035 = 3.6
- Strobe — MC4335 = 5.2
  MC4035 = 5.2

Output Loading Factor (MTTL I Loads):
- MC4335 = 7 (I_{OL} = 9.3 mAdc)
- MC4035 = 7 (I_{OL} = 11.6 mAdc)

Total Power Dissipation = 140 mW typ/pkg
Propagation Delay Time = 25 ns typ

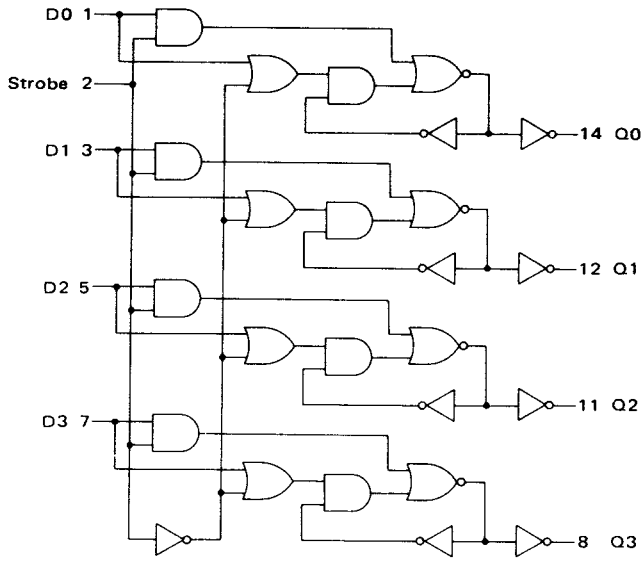
CIRCUIT SCHEMATIC

1/4 OF DEVICE SHOWN



QUAD LATCH

MC4337
MC4037

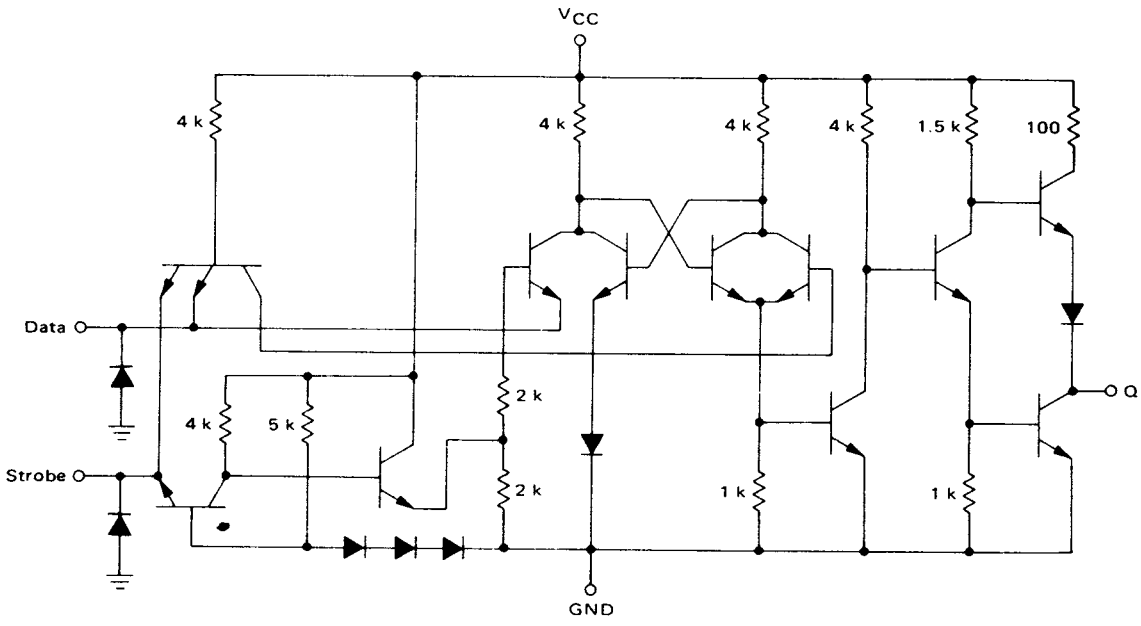


This monolithic device consists of four latch circuits with active pullup networks for high capacitive load drive capability. Separate data inputs and a common Strobe input are provided. Information present on the data inputs prior to the negative edge of the strobe input will be stored in the latch. When the strobe input is high, the Q output will follow the data input.

Input Loading Factor (MTTL I Loads):
Data Input (Strobe High) — MC4337 = 4.2
MC4037 = 4.0
Data Input (Strobe Low) — MC4337 = 1.1
MC4037 = 0.9
Strobe — MC4337 = 5.2
MC4037 = 5.2
Output Loading Factor (MTTL I Loads):
MC4337 = 10 (I_{OL} = 13.3 mAdc)
MC4037 = 10 (I_{OL} = 16.6 mAdc)
Total Power Dissipation = 150 mW typ/pkg
Propagation Delay Time = 25 ns typ

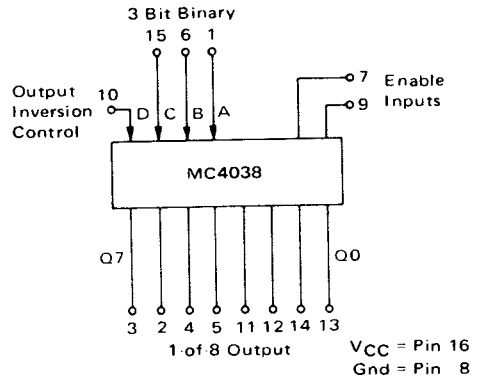
CIRCUIT SCHEMATIC

1/4 OF DEVICE SHOWN



INVERTING/NON-INVERTING ONE-OF-EIGHT DECODER

MC4338
MC4038



TRUTH TABLE (POSITIVE LOGIC)

INPUT				OUTPUT							
D	C	B	A	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

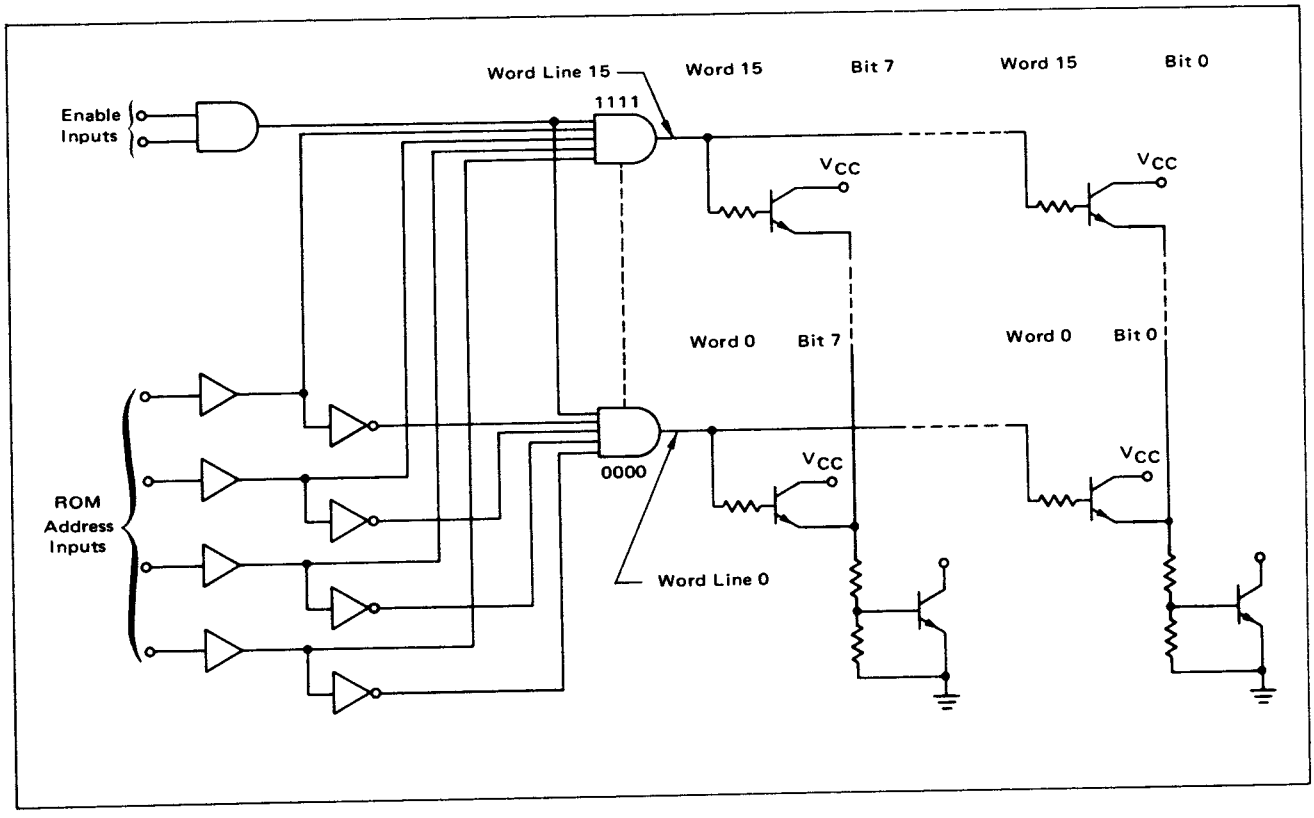
Total Power Dissipation = 240 mW typ/pkg

A 3-bit binary address selects the desired word for the 8-bit output. The inversion control, D, selects half of the memory chip with the bit pattern that defines a 1-of-8 decoder function. When D is a logic "0", the selected output is designated as a logic "0". A logic "1" on D produces a logic "1" on the selected output.

Features:
- Address times < 45 ns
- Outputs sink 20 mA
- Output capacitance < 7.0 pF @ 1.5 V
- Wired OR capability to 64 memories

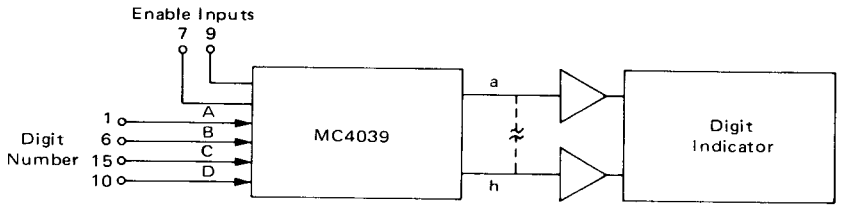
ENABLE INPUT TRUTH TABLE (POSITIVE LOGIC)

E	E	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	FUNCTION ENABLED							



SEVEN-SEGMENT CHARACTER GENERATOR

MC4339
MC4039



Output	a	b	c	d	e	f	g	h
Pin No.	12	11	5	4	13	14	2	3

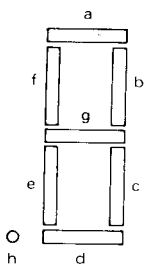
V_{CC} = Pin 16
Gnd = Pin 8

Total Power Dissipation = 240 mW typ/pkg

The MC4339 can directly operate low-voltage lamp indicators. A four digit binary input is translated into combinations of the eight outputs. These combinations correspond to different illuminated segments of the seven-bar digit indicator. The input and output codes with their related numerical digits are shown in the diagram. The enable inputs can be used for automatic blanking.

Features:
- Address times < 45 ns
- Outputs sink 20 mA
- Output capacitance < 7.0 pF @ 1.5 V
- Wired OR capability to 64 memories

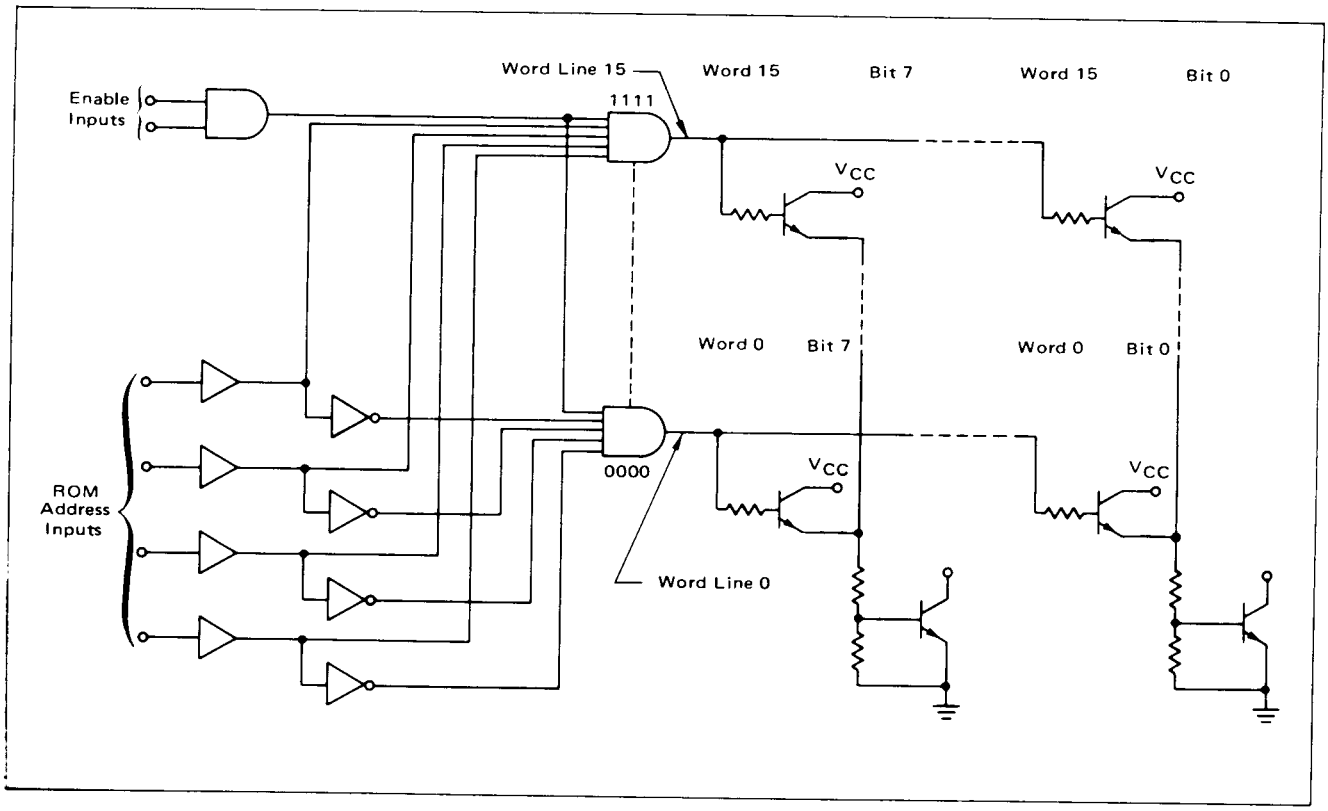
TRUTH TABLE (POSITIVE LOGIC)



DIGIT	SEGMENTS ILLUMINATED	INPUT D	C	B	A	OUTPUT a	b	c	d	e	f	g	h
0	a,b,c,d,e,f	0	0	0	0	0	0	0	0	0	0	1	1
1	b,c	0	0	0	1	1	0	0	1	1	1	1	1
2	a,b,d,e,g	0	0	1	0	0	0	1	0	0	1	0	1
3	a,b,c,d,g	0	0	1	1	0	0	0	0	1	1	0	1
4	b,c,f,g	0	1	0	0	1	0	0	1	1	0	0	1
5	a,c,d,f,g	0	1	0	1	0	1	0	0	1	0	0	1
6	c,d,e,f,g	0	1	1	0	1	1	0	0	0	0	0	1
7	a,b,c	0	1	1	1	0	0	0	1	1	1	1	1
8	a,b,c,d,e,f,g	1	0	0	0	0	0	0	0	0	0	0	1
9	a,b,c,f,g	1	0	0	1	0	0	0	1	1	0	0	1
NONE		1	0	1	0	1	1	1	1	1	1	1	1
•	h (Ext.)	1	0	1	1	1	1	1	1	1	1	1	0
	g	1	1	0	0	1	1	1	1	1	1	0	1
NONE		1	1	0	1	1	1	1	1	1	1	1	1
NONE		1	1	1	0	1	1	1	1	1	1	1	1
NONE		1	1	1	1	1	1	1	1	1	1	1	1

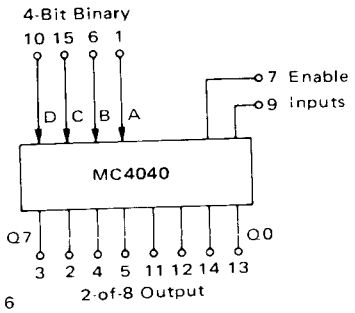
ENABLE INPUT TRUTH TABLE (POSITIVE LOGIC)

E	E	a	b	c	d	e	f	g	h
0	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	FUNCTION ENABLED							



BINARY TO TWO-OF-EIGHT DECODER

MC4340
MC4040



V_{CC} = Pin 16
Gnd = Pin 8

TRUTH TABLE (POSITIVE LOGIC)

INPUT				OUTPUT							
D	C	B	A	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	0	1	1	1	0
0	0	0	1	1	1	1	0	1	1	0	1
0	0	1	0	1	1	1	0	1	0	1	1
0	0	1	1	1	1	1	0	0	1	1	1
0	1	0	0	1	1	0	1	1	1	1	0
0	1	0	1	1	1	0	1	1	1	0	1
0	1	1	0	1	1	0	1	1	0	1	1
0	1	1	1	1	1	0	1	0	1	1	1
1	0	0	0	1	0	1	1	1	1	1	0
1	0	0	1	1	0	1	1	1	1	0	1
1	0	1	0	1	0	1	1	1	0	1	1
1	0	1	1	1	0	1	1	0	1	1	1
1	1	0	0	0	1	1	1	1	1	1	0
1	1	0	1	0	1	1	1	1	1	0	1
1	1	1	0	0	1	1	1	1	0	1	1
1	1	1	1	0	1	1	1	0	1	1	1

Total Power Dissipation = 200 mW typ/pkg

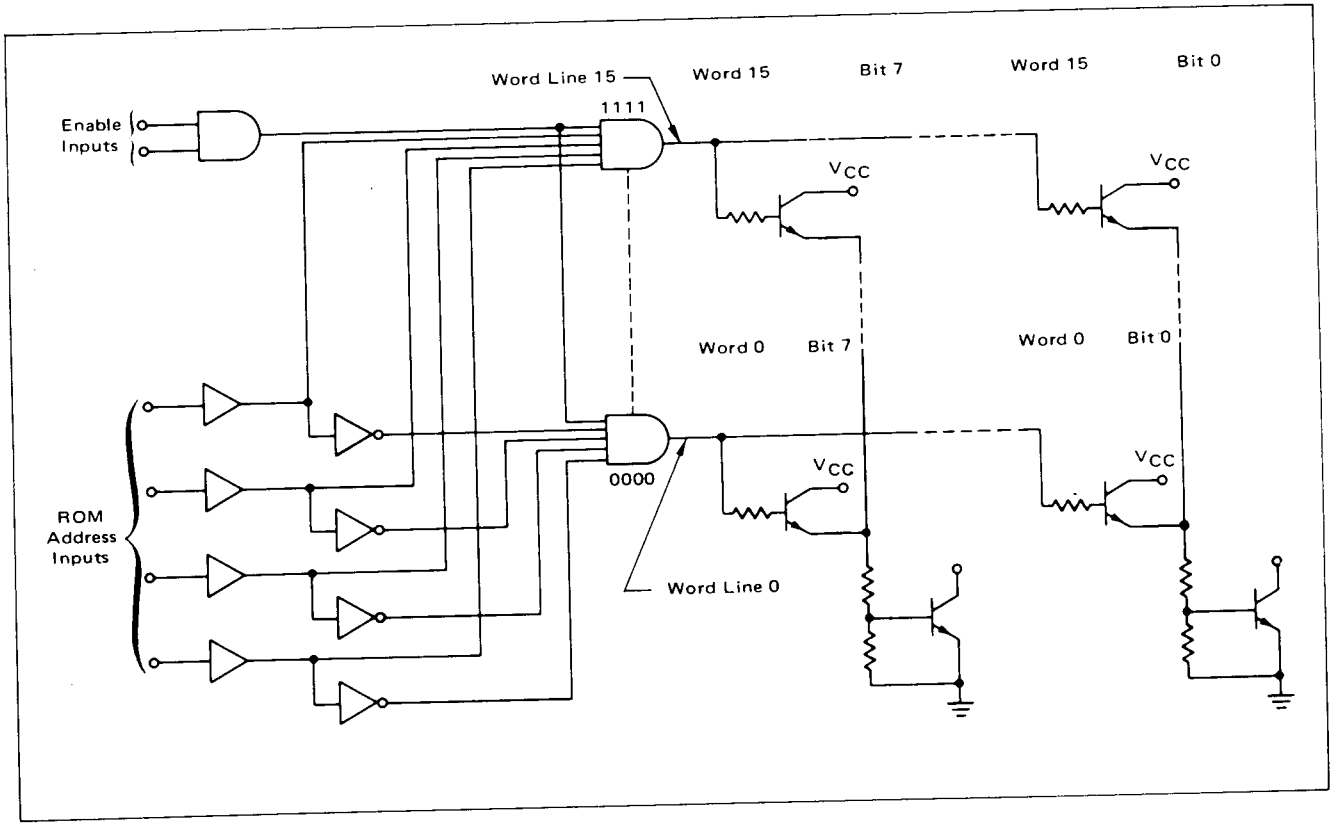
This device, with two enable inputs, transforms any 4-bit binary number to a 2-of-8-bit coded number. The device can also be thought of as a dual binary to 1-of-4 decoder.

Features:

- Address times < 45 ns
- Outputs sink 20 mA
- Output capacitance < 7.0 pF @ 1.5 V
- Wired OR capability to 64 memories

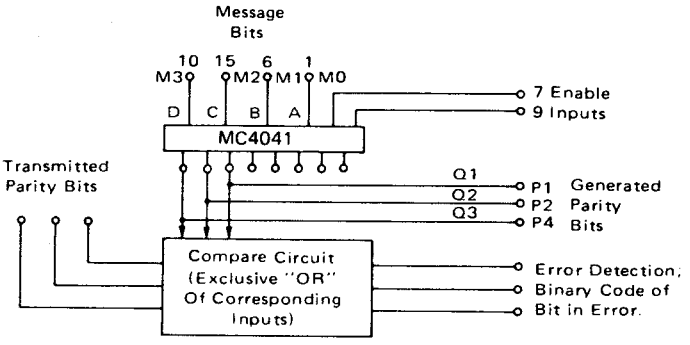
ENABLE INPUT TRUTH TABLE (POSITIVE LOGIC)

E	E	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	FUNCTION ENABLED							



SINGLE-ERROR HAMMING CODE DETECTOR AND GENERATOR

MC4341
MC4041



Output	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Pin No.	13	14	12	11	5	4	2	3

V_{CC} = Pin 16
Gnd = Pin 8

TRUTH TABLE (POSITIVE LOGIC)

INPUT				OUTPUT							
D	C	B	A	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	1	1	1	0
0	0	0	1	0	0	1	1	1	0	0	1
0	0	1	0	0	0	1	0	0	1	0	1
0	0	1	1	1	1	1	0	0	0	1	0
0	1	0	0	0	0	0	1	0	0	1	1
0	1	0	1	1	1	0	1	0	1	0	0
0	1	1	0	1	1	0	0	1	0	0	0
0	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	1	1	0	0	0	1	1	0
1	0	1	0	1	1	0	1	1	0	1	0
1	0	1	1	0	0	0	1	1	1	0	1
1	1	0	0	1	1	1	0	1	1	0	0
1	1	0	1	0	0	1	0	1	0	1	1
1	1	1	0	0	0	1	1	0	1	1	1
1	1	1	1	1	1	1	1	0	0	0	0

Simple Parity: The outputs of bits 0, 6, and 7 provide parity check over the 4 message bits.

Hamming Detection and Correction: Bits 1, 2, and 3 perform the parity calculations necessary for Hamming Code generation or detection on 4 message bits. For greater than 4 bits per message, ROM's may be cascaded. In these cases, bits 4, 5, 6, and 7 perform the necessary parity calculations.

Total Power Dissipation = 240 mW typ/pkg

For more information on this function and its uses, see Application Note AN-446.

The MC4041 is a programmed 128-Bit Read Only Memory suitable for a variety of error detection and correction applications.

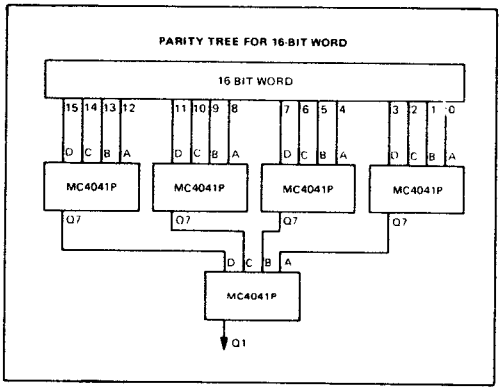
Simple parity trees for error detection can be constructed using the MC4041P as the basic building block. Also, more complex error control schemes, such as Hamming single error detection and correction, can be implemented with this device.

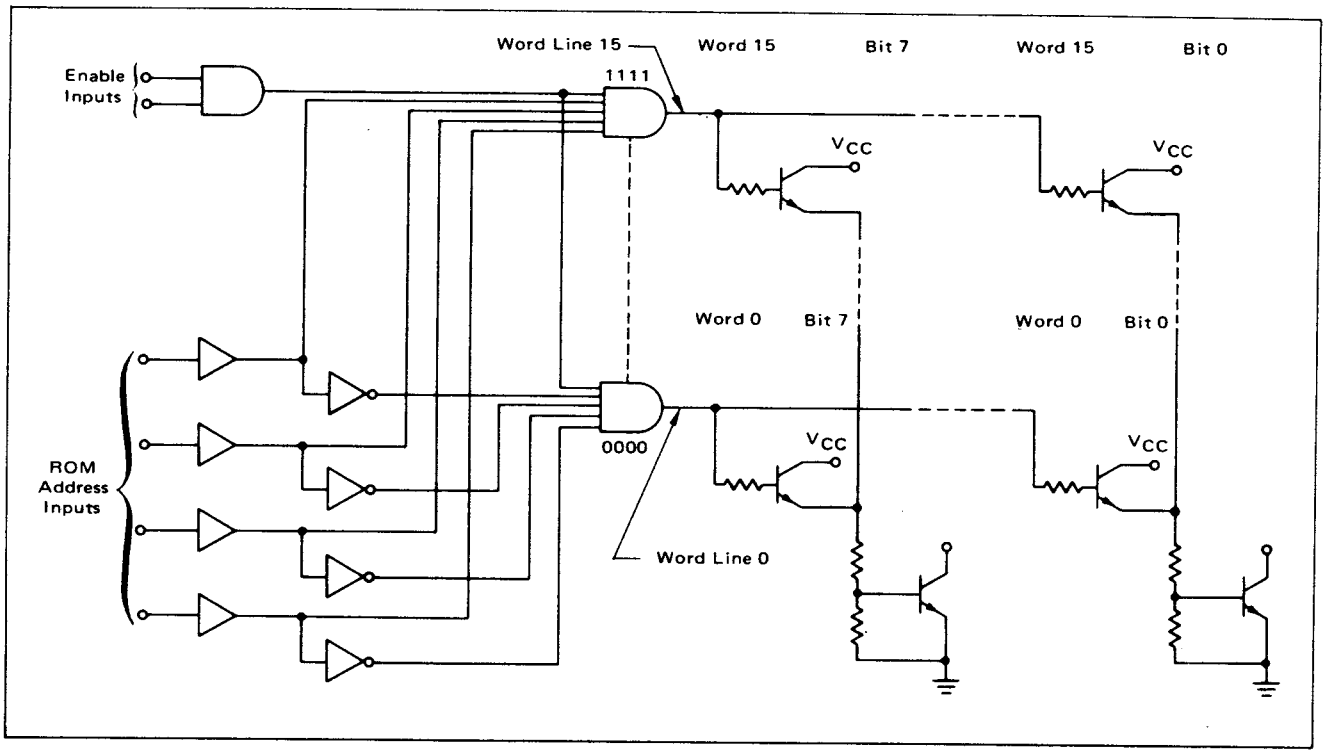
Features:

- Address times < 45 ns
- Outputs sink 20 mA
- Output capacitance < 7.0 pF @ 1.5 V
- Wired OR capability to 64 memories

ENABLE INPUT TRUTH TABLE (POSITIVE LOGIC)

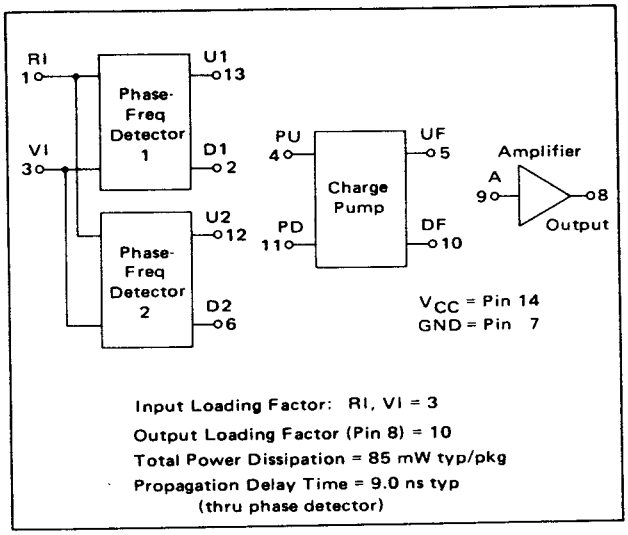
E	E	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	FUNCTION ENABLED							





PHASE-FREQUENCY DETECTOR

MC4344
MC4044



Input Loading Factor: RI, VI = 3

Output Loading Factor (Pin 8) = 10

Total Power Dissipation = 85 mW typ/pkg

Propagation Delay Time = 9.0 ns typ
(thru phase detector)

This device contains two digital phase detectors and a charge pump circuit which converts MTTL inputs to a dc voltage level for use in frequency discrimination and phase-locked-loop applications.

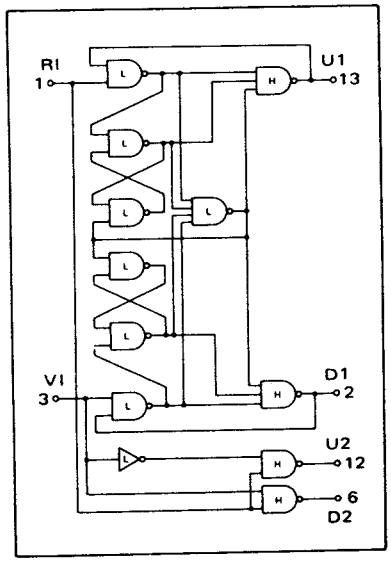
The two phase detectors have common inputs. Phase-frequency detector 1 is locked in (indicated by both outputs high) when the negative transitions of the variable input (VI) and reference input (RI) are equal in frequency and phase. If the variable input is lower in frequency or lags in phase, the U1 (up) output goes low; conversely the D1 (down) output goes low when the variable input is higher in frequency or leads the reference input in phase. It is important to note that the duty cycles of the variable input and the reference input are not important since negative transitions control system operation.

Phase detector 2, on the other hand, is locked in when the variable input phase lags the reference phase by 90° (indicated by the U2 and D2 outputs alternately going low with equal pulse widths). If the variable input phase lags by more than 90°, U2 will remain low longer than D2, and, conversely, if the variable input phase lags the reference phase by less than 90°, D2 remains low longer. In this phase detector the variable input and the reference must have 50% duty cycles.

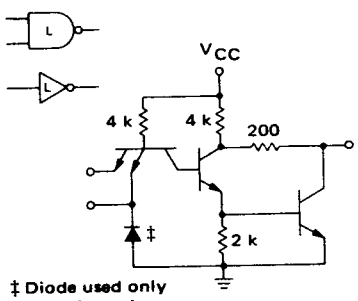
The charge pump accepts the phase detector outputs (U1 or U2 applied to PU, and D1 or D2 applied to PD) and converts them to fixed amplitude positive and negative pulses at the UF and DF outputs respectively. These pulses are applied to a lag-lead active filter, which incorporates external components, as well as the amplifier provided in the MC4344/4044 circuit. The filter provides a dc voltage proportional to the phase error.

PHASE DETECTOR

The phase detector portion of this device is constructed using low and high-level gates interconnected as shown by the logic diagram.

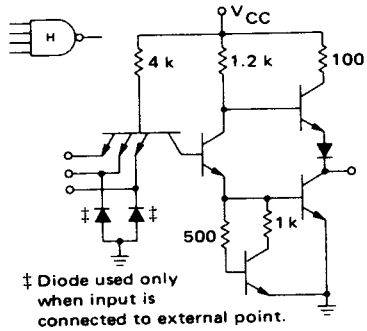


LOW-LEVEL "NAND" GATE



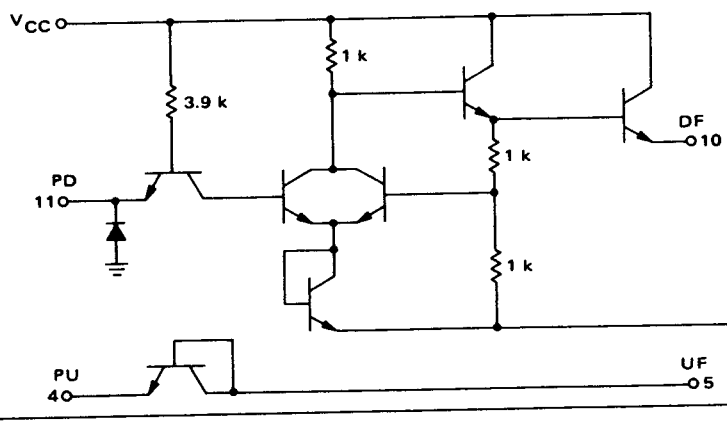
‡ Diode used only when input is connected to external point.

HIGH-LEVEL "NAND" GATE

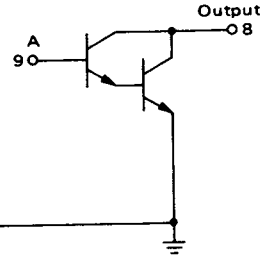


‡ Diode used only when input is connected to external point.

CHARGE PUMP



AMPLIFIER



QUAD PREDRIVER **DUAL LINE SELECTOR**

MC4342 MC4343
MC4042 MC4043

The MC4042 and MC4043 are designed for magnetic memory driver/selector applications.

The MC4042 monolithic quad predriver consists of four high-speed switching transistors, each driven by an MTTL compatible NOR gate. Each NOR gate has an individual address input and a common timing input. The inputs of the MC4042 can be driven directly with standard MTTL decoders such as the MC4006 binary to one-of-eight decoder or the MC4007 dual binary to one-of-four decoder. The open-collector output transistor of the MC4042 will sink 50 mA.

The MC4043 monolithic dual line selector consists of two high-speed 400 mA switches driven by MTTL compatible NOR gates. Each NOR gate has an individual address input and a common timing input. The address and timing inputs of the MC4043 can also be driven directly with standard MTTL decoders such as the MC4006 and MC4007.

The MC4042 and MC4043 input circuits are the same, but the output circuitry is different as shown in the device schematics. The output transistors of both devices have a minimum BV_{CEX} of 15 volts, and are gold doped to increase switching speeds.

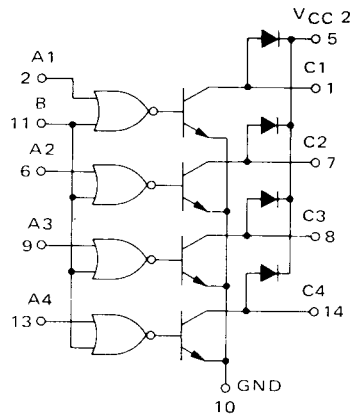
Many memory predriver applications employ transformer coupling between the predriver and driver stages. In such designs, large voltage overshoots occur due to the transformer inductance and high-speed switching currents. The collector of the MC4042 is internally clamped to prevent the collector from exceeding the maximum rated voltage during the switching transitions. The voltage applied to the diode clamp, pin 5, should be the same or greater than the collector voltages at pins 1, 7, 8, and 14, to prevent the diode clamp from being forward biased during nonswitching periods. The output transistor is driven with a conventional totem pole arrangement to provide active pullup and pulldown.

The collectors of the pullup transistors of the MC4043 are available at pins 1 and 7. An external load resistor to V_{CC} must be provided. This reduces power dissipation of the package and provides a means by which the speed of the device can be varied by changing the value of the pullup resistance.

The internal decoding circuitry of the MC4043 is such that both switches can be turned on at one time. However, due to power limitations, care must be taken to ensure that only one switch is turned on at any one time.

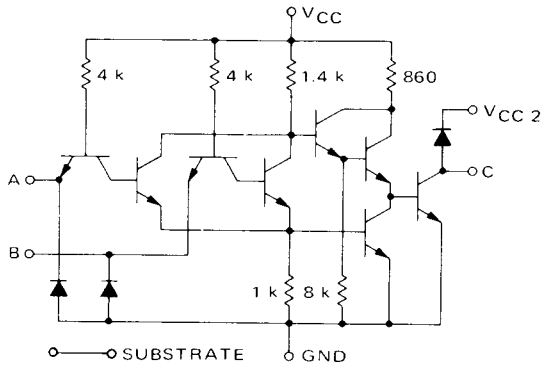
The MC4042 and MC4043 can provide a memory system with an inexpensive, reliable, fast drive system. They are also useful as relay or lamp drivers, high fan-out gates, and MOS drivers.

MC4042



Input Loading Factors:
A = 1, B = 4
Total Power Dissipation = 120 mW typ/pkg
Propagation Delay Time = 15 ns typ

SCHEMATIC (¼ OF DEVICE SHOWN)



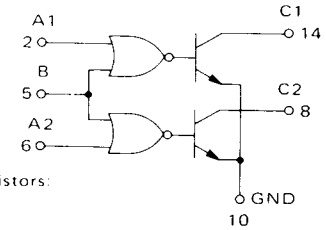
MC4042 AND MC4043

V_{CC} = PIN 4
GND = PIN 10
SUBSTRATE = PIN 3

TRUTH TABLE
(One gate only)

A1	B	C1
0	0	0
0	1	1
1	0	1
1	1	1

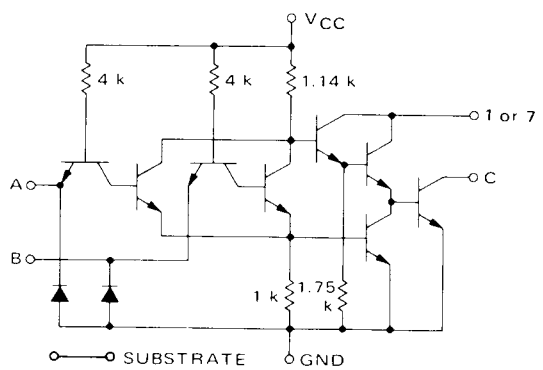
MC4043



Collectors of Output Transistors:
Gate 1 = Pin 1
Gate 2 = Pin 7

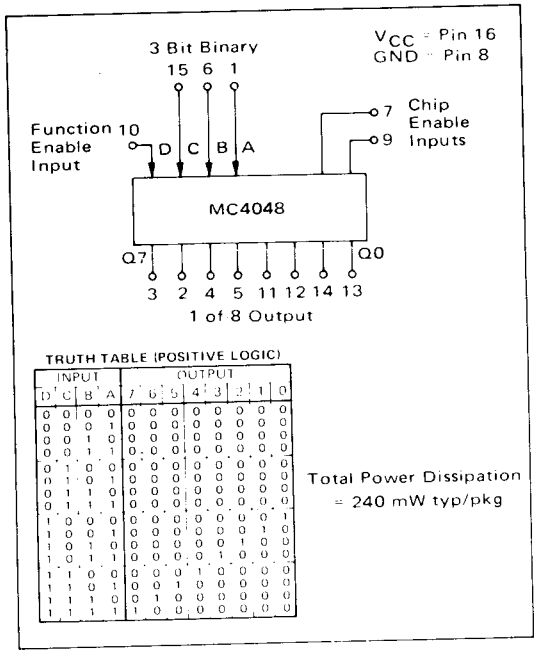
Input Loading Factors: A = 1, B = 2
Total Power Dissipation = 70 mW typ/pkg
Propagation Delay Time = 20 ns typ

SCHEMATIC (½ OF DEVICE SHOWN)



NON-INVERTING
ONE-OF-EIGHT DECODER

MC4348
MC4048



TRUTH TABLE (POSITIVE LOGIC)

INPUT				OUTPUT							
D	C	B	A	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Total Power Dissipation
= 240 mW typ/pkg

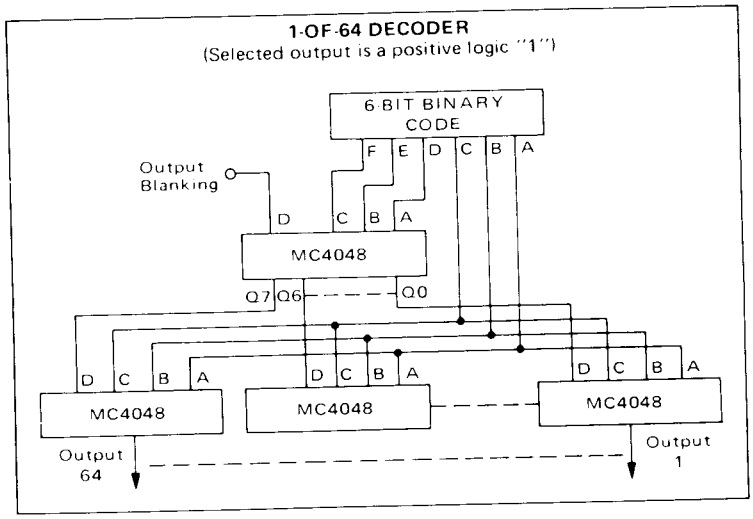
A 3-bit binary address selects the desired word for the 8-bit output, and the selected output goes to a logic "1". The function enable input, D, is useful for expansion of the decoding function. When D is a logic "0" all outputs are logic "0". A logic "1" on D produces a logic "1" on the selected output.

Features:

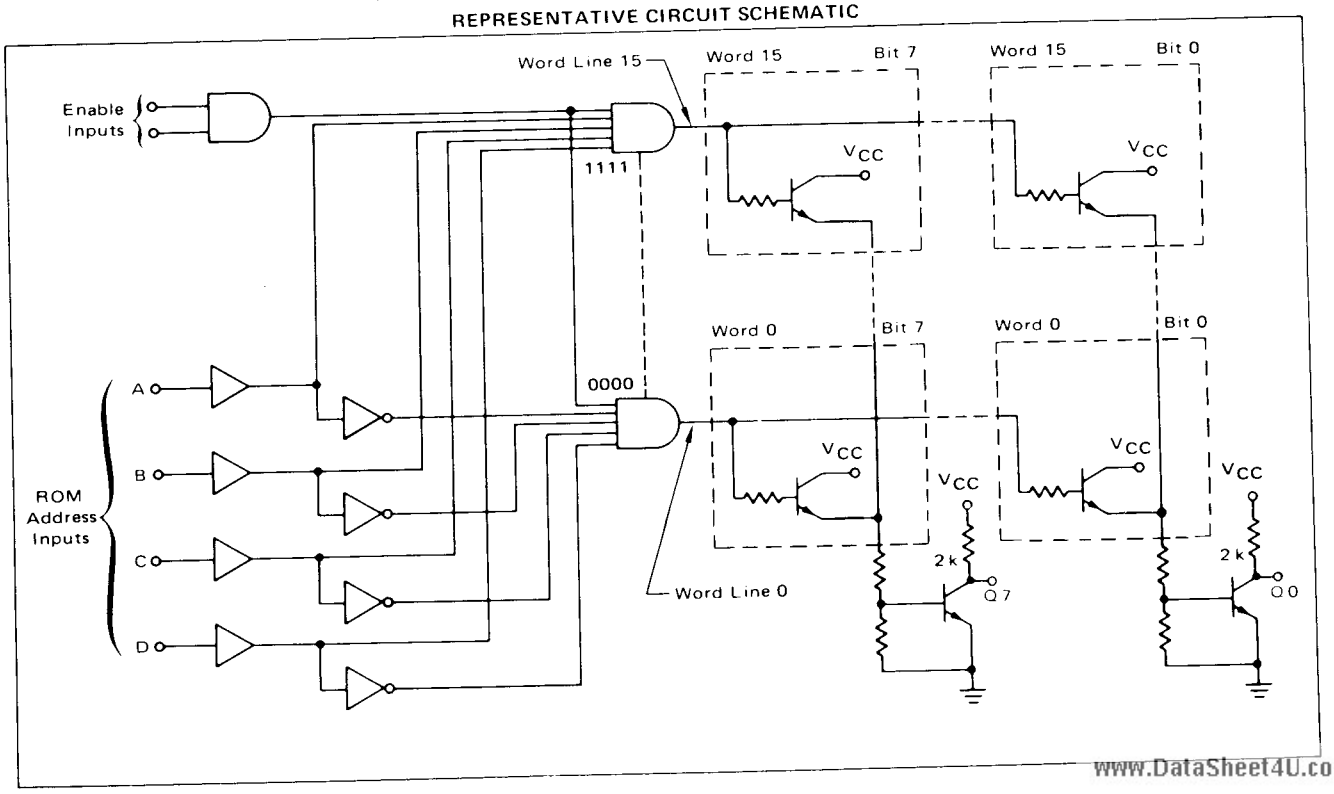
- Address times < 50 ns
- Outputs sink 16 mA
- Output capacitance < 7.0 pF @ 1.5 V

ENABLE INPUT TRUTH TABLE (POSITIVE LOGIC)

E	E	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	FUNCTION ENABLED							



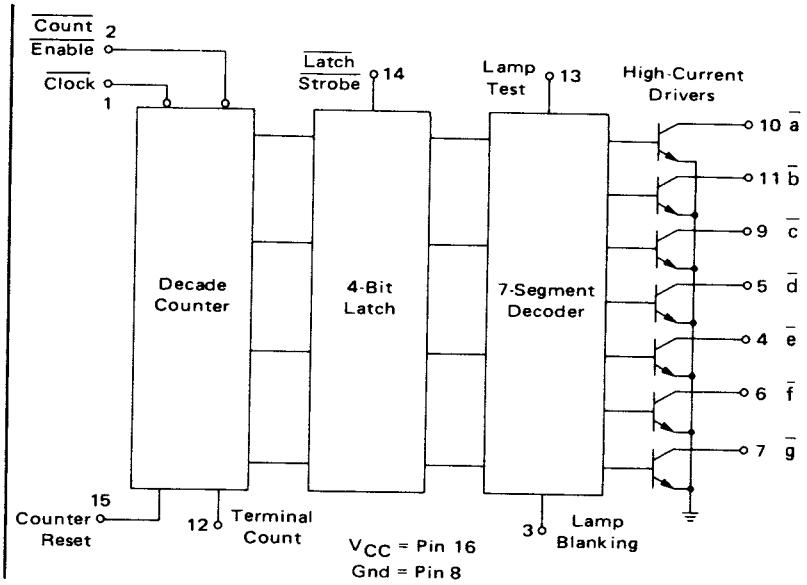
REPRESENTATIVE CIRCUIT SCHEMATIC



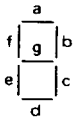
COUNTER-LATCH DECODER

MC4350
MC4050

This monolithic integrated circuit combines the functions of a binary coded decimal counter, a four-bit latch, and a seven-segment decoder/driver. Designed primarily for counting applications such as frequency counters, the circuit contains a leading zero blanking feature activated through the Reset input. For this reason the MC4350/4050 is useful in systems using automatic decimal ranging and/or automatic time base selection. A $\overline{\text{Count}}$ $\overline{\text{Enable}}$ input gates the clock input without restrictions on the clock level and without false-clocking the counter. The Terminal Count is high driving the ninth count, allowing synchronous or asynchronous counter operation when used in conjunction with the $\overline{\text{Count}}$ $\overline{\text{Enable}}$ input and external gating. The Counter Reset places the counter in a non-NBCD state, turning off the output driver transistors when transferred through the latch and decoded. The latch section admits information while the $\overline{\text{Latch}}$ $\overline{\text{Strobe}}$ is high and latches the data on the negative edge of the strobe. The seven-segment decoder/driver provides up to 40 mA drive capability for displays requiring current sinking in the active mode. A lamp blanking input provides intensity modulation. A lamp test feature is also available.



SEGMENT IDENTIFICATION



Total Power Dissipation = 450 mW typ/package
Maximum Toggle Frequency = 40 MHz typ

FUNCTIONAL TRUTH TABLE

FUNCTION		INPUT $\overline{\text{CLOCK}}$	$\overline{\text{CE}}$	CR	$\overline{\text{LST}}$	LT	LB	OUTPUT TC	$\bar{a}$	$\bar{b}$	$\bar{c}$	$\bar{d}$	$\bar{e}$	$\bar{f}$	$\bar{g}$
Lamp Test		X	X	X	X	1	X	–	0	0	0	0	0	0	0
Lamp Blanking		X	X	X	X	0	1	–	1	1	1	1	1	1	1
Reset		X	X	1	1	0	0	0	1	1	1	1	1	1	1
$\overline{\text{Enable}}$		P	1	0	1	0	0	0	1	1	1	1	1	1	1
State Sequence	1	P1	0	0	1	0	0	0	1	0	0	1	1	1	1
	2	P2	0	0	1	0	0	0	0	0	1	0	0	1	0
	3	P3	0	0	1	0	0	0	0	0	0	0	1	1	0
	4	P4	0	0	1	0	0	0	1	0	0	1	1	0	0
	5	P5	0	0	1	0	0	0	0	1	0	0	1	0	0
	6	P6	0	0	1	0	0	0	0	1	0	0	0	0	0
	7	P7	0	0	1	0	0	0	0	0	0	1	1	1	1
	8	P8	0	0	1	0	0	0	0	0	0	0	0	0	0
	9	P9	0	0	1	0	0	1	0	0	0	0	1	0	0
	0	P10	0	0	1	0	0	0	0	0	0	0	0	0	1
	1	P11	0	0	1	0	0	0	1	0	0	1	1	1	1
	Latch	P	0	0	0	0	0	0	1	0	0	1	1	1	1

P = any number of pulses may be applied
P_n = n pulses on the Clock input
X = Don't care

FUNCTION DESCRIPTION

The MC4350/4050 is suited for driving incandescent seven-segment decimal indicators. In addition, only current limiting resistors are needed to allow driving hybrid LED's in the 2.4-volt per segment capability range with common-anode configuration. Use the MC4051 for monolithic LED arrays with common-cathode connection.

Logic "1" allows decoder to be driven directly from counter outputs. Logic "0" stores counter output data as it was immediately prior to "1" to "0" transition.

This input has no effect on the circuit if LT is at logic "1". With LT = logic "0", a logic "1" at this input turns off outputs $\bar{a}$ thru $\bar{g}$; a logic "0" allows $\bar{a}$ thru $\bar{g}$ to display normally.

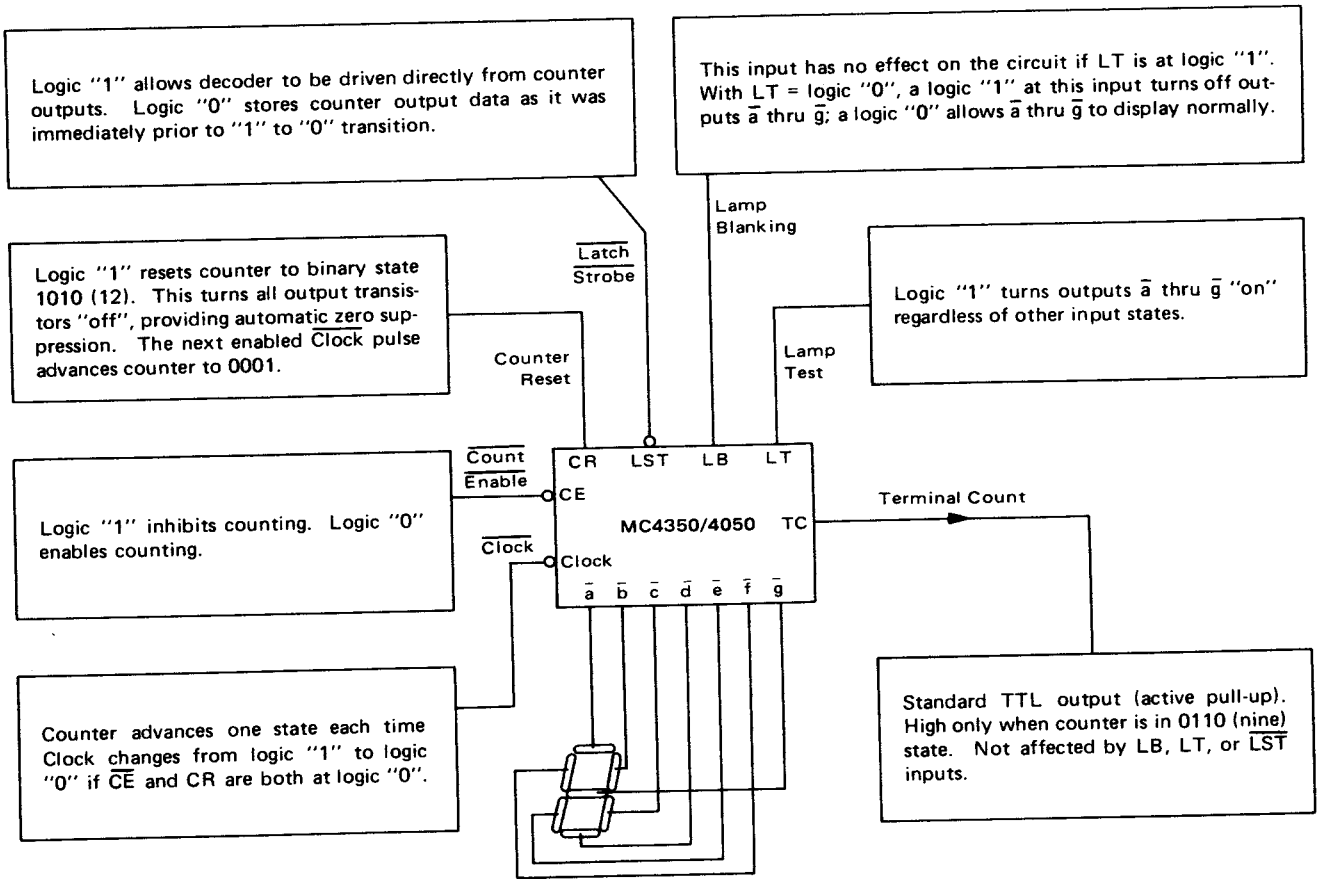
Logic "1" resets counter to binary state 1010 (12). This turns all output transistors "off", providing automatic zero suppression. The next enabled $\overline{\text{Clock}}$ pulse advances counter to 0001.

Logic "1" turns outputs $\bar{a}$ thru $\bar{g}$ "on" regardless of other input states.

Logic "1" inhibits counting. Logic "0" enables counting.

Counter advances one state each time Clock changes from logic "1" to logic "0" if $\overline{\text{CE}}$ and CR are both at logic "0".

Standard TTL output (active pull-up). High only when counter is in 0110 (nine) state. Not affected by LB, LT, or $\overline{\text{LST}}$ inputs.



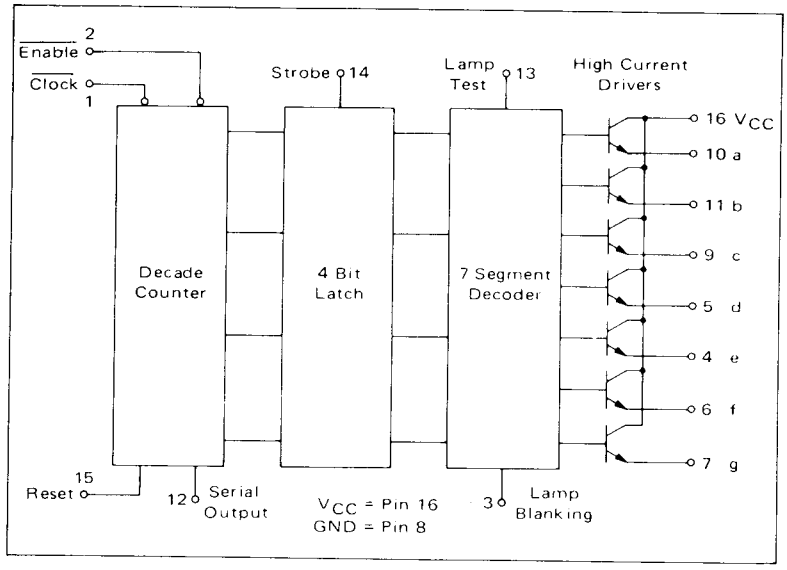
OPERATING DETAILS

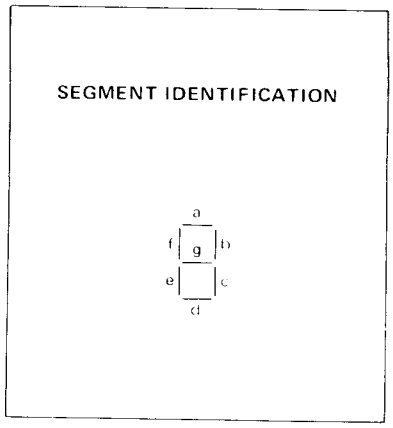
- $\overline{\text{Count Enable}}$ may be changed with $\overline{\text{Clock}}$ either high or low.
- Counter Reset overrides $\overline{\text{Count Enable}}$ and $\overline{\text{Clock}}$. It may be changed regardless of levels present at $\overline{\text{Count Enable}}$ and $\overline{\text{Clock}}$.
- $\overline{\text{Latch Strobe}}$, Lamp Blanking, and Lamp Test may be changed regardless of levels at $\overline{\text{Count Enable}}$, $\overline{\text{Clock}}$, and Counter Reset.
- Refer to Timing Diagram if a logic "1" to "0" transition on $\overline{\text{Clock}}$ can occur while levels are changing on $\overline{\text{Count Enable}}$ or $\overline{\text{Latch Strobe}}$, or if a logic "0" to "1" transition of Counter Reset can occur simultaneously with a "0" to "1" transition of $\overline{\text{Latch Strobe}}$.
- Tie all unused inputs to ground except for $\overline{\text{Latch Strobe}}$, which must be returned to a logic "1" level if not used.
- Outputs $\bar{a}$ thru $\bar{g}$ are open-collector transistors capable of sinking 40 mAdc with outputs low, and sustaining 8.0 Vdc minimum (15 Vdc typical) with outputs high.

MC4351
MC4051

This device is a monolithic MSI integrated circuit combining the functions of an NBCD counter, four-bit latch, and a seven-segment decoder/driver. The counter advances on the negative edge of the $\overline{\text{Clock}}$, subject to control by the $\overline{\text{Enable}}$ input. The Serial Output is high driving the ninth count, allowing synchronous or asynchronous counter operation when used in conjunction with the $\overline{\text{Enable}}$ input and some external gating. The counter Reset places the counter in a non-NBCD state, turning off the output driver transistors when transferred through the latch and decoded. This feature gives automatic suppression of leading zeros in the display. The latch section admits information while the Strobe is high and latches the data on the negative edge of the strobe. The seven-segment decoder/driver is active high and will source up to 40 mA at a 10% duty cycle or 15 mA at a 100% duty cycle. A lamp blanking input is provided for intensity modulation. A lamp test feature is also available.

The output structure of this device is an open emitter-follower configuration whose equivalent circuit is a voltage source with a relatively small series resistance. Although this resistance increases when the output is grounded, the situation is potentially destructive to the device. When the outputs are in the high ("1") state, they should not be connected to ground through an impedance of less than 100 ohms.





Total Power Dissipation = 450 mW typ/package
Maximum Toggle Frequency = 35 MHz typ

FUNCTIONAL TRUTH TABLE

FUNCTION		INPUT $\overline{C}$	$\overline{E}$	R	S	LT	LB	OUTPUT S_{out}	a	b	c	d	e	f	g
Lamp Test		X	X	X	X	1	X		1	1	1	1	1	1	1
Lamp Blanking		X	X	X	X	0	1		0	0	0	0	0	0	0
$\overline{\text{Reset}}$		X	X	1	1	0	0	0	0	0	0	0	0	0	0
$\overline{\text{Enable}}$		P	1	0	1	0	0	0	0	0	0	0	0	0	0
State Sequence	1	P1	0	0	1	0	0	0	0	1	1	0	0	0	0
	2	P2	0	0	1	0	0	0	1	1	0	1	1	0	1
	3	P3	0	0	1	0	0	0	1	1	1	1	0	0	1
	4	P4	0	0	1	0	0	0	0	1	1	0	0	1	1
	5	P5	0	0	1	0	0	0	1	0	1	1	0	1	1
	6	P6	0	0	1	0	0	0	1	0	1	1	1	1	1
	7	P7	0	0	1	0	0	0	1	1	1	0	0	0	0
	8	P8	0	0	1	0	0	1	1	1	1	1	1	1	1
	9	P9	0	0	1	0	0	0	1	1	1	1	0	1	1
	0	P10	0	0	1	0	0	0	1	1	1	1	1	1	0
	1	P11	0	0	1	0	0	0	0	1	1	0	0	0	0
	Latch	P	0	0	0	0	0	0	0	1	1	0	0	0	0

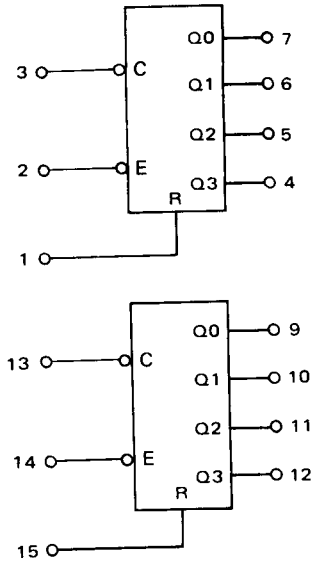
P = any number of pulses may be applied
P_n = n pulses on the Clock input
X = Don't care

DUAL DECADE COUNTER

MC4352
MC4052

DUAL HEXADECIMAL COUNTER

MC4353
MC4053



V_{CC} = Pin 16
Gnd = Pin 8

The MC4352/4052 and MC4353/4053 consist of two independent up counters. The counters advance on the negative edge of the $\overline{\text{clock}}$ when the $\overline{\text{enable}}$ input is low. The count is held when the $\overline{\text{enable}}$ input is high. The $\overline{\text{enable}}$ input should not be taken to the high level while the $\overline{\text{clock}}$ is high, as erroneous triggering can result. A high level on the reset input places the counter in the 0000 state, overriding the $\overline{\text{clock}}$ and $\overline{\text{enable}}$ inputs. As charge control steering is utilized in this design, capacitive loading on the outputs should be kept at a minimum.

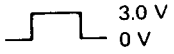
Total Power Dissipation = 350 mW typ/pkg
Maximum Toggle Frequency = 40 MHz typ

FUNCTIONAL TRUTH TABLE

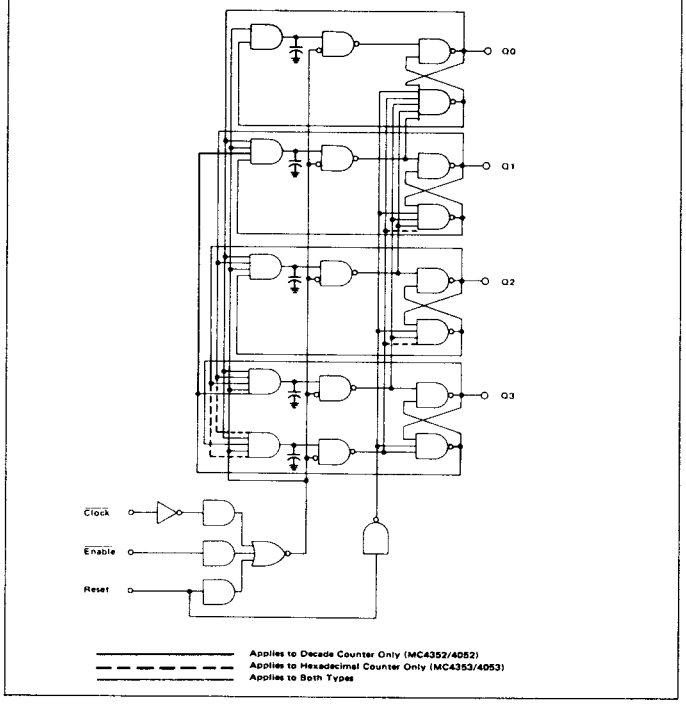
INPUT			MC4352/4052 OUTPUT				MC4353/4053 OUTPUT			
R	$\overline{E}$	$\overline{C}$	Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0
1	X	X	0	0	0	0	0	0	0	0
0	1	P	0	0	0	0	0	0	0	0
0	0	P1	0	0	0	1	0	0	0	1
0	0	P2	0	0	1	0	0	0	1	0
0	0	P3	0	0	1	1	0	0	1	1
0	0	P4	0	1	0	0	0	1	0	0
0	0	P5	0	1	0	1	0	1	0	1
0	0	P6	0	1	1	0	0	1	1	0
0	0	P7	0	1	1	1	0	1	1	1
0	0	P8	1	0	0	0	1	0	0	0
0	0	P9	1	0	0	1	1	0	0	1
0	0	P10	0	0	0	0	1	0	1	0
0	0	P11	0	0	0	1	1	0	1	1
0	0	P12	Above Sequence Repeats				1	1	0	0
0	0	P13					1	1	0	1
0	0	P14					1	1	1	0
0	0	P15					1	1	1	1
0	0	P16					0	0	0	0
0	0	P17					0	0	0	1

Reset
Enable

P = any number of pulses may be applied
P_n = n pulses on the Clock input
X = Don't Care

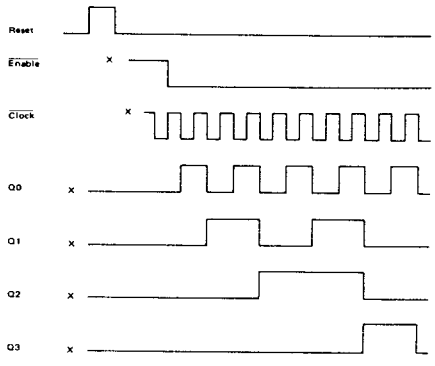


LOGIC DIAGRAM
(1/2 of Device Shown)

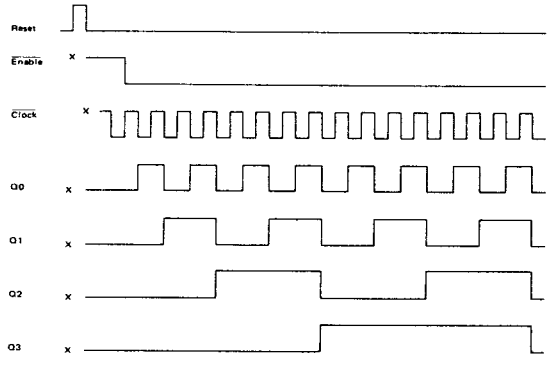


FUNCTIONAL DIAGRAMS

MC4352/4052 DECADE COUNTER



MC4353/4053 HEXADECIMAL COUNTER



X = Don't care

DUAL DECADE UP/DOWN COUNTER

MC4354
MC4054

DUAL BINARY UP/DOWN COUNTER

MC4355
MC4055

These devices are presettable, synchronous (clocked) up/down coutners. The MC4354/4054 is a decade counter consisting of two separate but cascaded counters. One counter counts the least significant decade, and the other the most significant decade. The counter counts to 1001 1001, or 99, before resetting to 0000 0000. The MC4355/4055 is a binary counter consisting of two separate hexadecimal counters which are cascaded. This counter is essentially an 8-bit binary counter which counts to 1111 1111, or 255, before resetting to 0000 0000.

Both counters in a package are preset by means of a high level on the Preset (P) input. (The Preset input overrides all synchronous inputs: Clock, $\overline{SEI}$, and $\overline{UE}$.) Information is then loaded into the least significant counter thru inputs D0, D1, D2 and D3, and into the most significant counter thru inputs D0', D1', D2', and D3'.

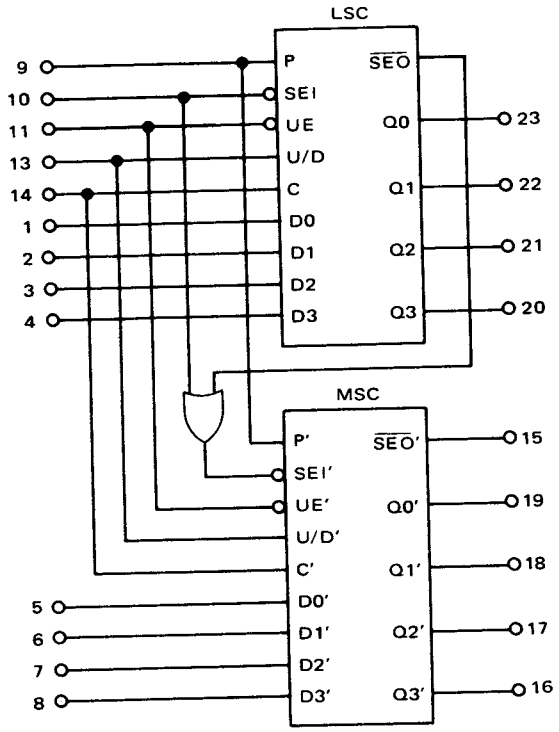
The Up/$\overline{Down}$ input determines the mode of counting: up when high, down when low.

Two Enable inputs are part of these circuits. The Unit Enable ($\overline{UE}$) affects only the counters within a specific package. The Serial Enable ($\overline{SEI}$) not only affects a particular package, but also furnishes a signal at the Serial Enable Output ($\overline{SEO}$) for control of succeeding packages in a counter chain. A high input to $\overline{SEI}$ forces $\overline{SEO}$ high. When $\overline{SEI}$ is low, $\overline{SEO}$ decodes the terminal state of the counter, independently from the $\overline{UE}$ control, when the counters are in the terminal state. (Terminal state is defined as 0000 0000 when counting down, and as 1111 1111 (256) for the binary counter and 1001 1001 (99) for the decade counter when counting up.)

Both the Serial Enable ($\overline{SEI}$) and the Unit Enable ($\overline{UE}$) must be low for the counter to be clocked. Logic levels on both of these lines must be settled prior to the trailing edge of the Clock, and must remain stable while the Clock is low.

The count state may change only on the leading edge of a Clock pulse. Any changes on the control inputs (Up/$\overline{Down}$, $\overline{SEI}$, and $\overline{UE}$) must be made while the Clock is high.

Counting data is read out on Q0 thru Q3 for the least significant counter, and Q0' thru Q3' for the most significant counter.



Input Loading Factors:
$\overline{SEI}$ = 3
$\overline{UE}$, Clock = 2
All Others = 1
Output Loading Factor = 10
Total Power Dissipation = 600 mW typ/pkg
Maximum Operating Frequency = 12 MHz typ

V_{CC} = Pin 24
Gnd = Pin 12

MC4354/4054

COUNT	INPUTS													OUTPUTS								
						TENS				UNITS				TENS				UNITS				
	C	$\overline{UE}$	$\overline{SEI}$	U/$\overline{D}$	P	D3′	D2′	D1′	D0′	D3	D2	D1	D0	Q3′	Q2′	Q1′	Q0′	Q3	Q2	Q1	Q0	$\overline{SEO}$
0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	0	1	0	1	0	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	1
2	A	1	0	1	0									0	0	0	0	0	0	0	1	1
3	A	1	0	1	0									0	0	0	0	0	0	1	0	1
4	A	1	0	1	0									0	0	0	0	0	0	1	1	1
5	A	1	0	1	0									0	0	0	0	0	1	0	0	1
6	A	1	0	1	0									0	0	0	0	0	1	0	1	1
7	A	1	0	1	0									0	0	0	0	0	1	1	0	1
8	A	1	0	1	0									0	0	0	0	0	1	1	1	1
9	A	1	0	1	0									0	0	0	0	1	0	0	0	1
10	A	1	0	1	0									0	0	0	0	1	0	0	1	1
11	A	1	0	1	0									0	0	0	0	1	0	0	0	1
12	A	1	0	1	0									0	0	0	0	0	1	1	1	1
⋮	84A	0	0	1	0									0	0	0	0	0	0	1	0	1
97	A	0	0	1	0									*								1
98	A	0	0	1	0									1	0	0	1	0	1	1	1	1
99	A	0	0	1	0									1	0	0	0	1	0	0	0	1
00	1	0	0	1	0									1	0	0	0	1	0	0	1	0
00	1	0	0	0	0									1	0	0	0	0	0	0	0	1
00	0	0	0	0	0									0	0	0	0	0	0	0	0	0
99	A	0	0	0	0									0	0	0	0	0	0	0	1	0
98	A	0	0	0	0									0	0	0	0	0	0	0	0	1
97	A	0	0	0	0									0	0	0	0	0	0	0	1	1
⋮	94A	0	0	0	0									1	0	0	1	1	0	0	0	1
02	A	0	0	0	0									1	0	0	0	0	0	0	1	1
01	A	0	0	0	0									0	0	0	0	0	0	0	0	1
00	1	0	0	0	0									0	0	0	0	0	0	0	1	0
00	1	0	0	1	0									0	0	0	0	0	0	0	0	1
00	1	0	0	0	0									0	0	0	0	0	0	0	0	0
97	0	0	0	0	1	1	0	0	1	0	1	1	1	0	0	0	1	0	0	0	1	1
97	0	0	0	0	0	1	0	0	1	0	1	1	1	0	0	0	1	1	1	1	1	0
96	A	0	0	0	0	X	X	X	X	X	X	X	X	0	0	0	0	1	1	1	0	1
95	A	0	0	0	0	X	X	X	X	X	X	X	X	0	0	0	0	1	1	0	1	1
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

X = Don't Care

*Outputs count from 12 to 96 during these 84 clock pulses.

**Outputs count from 97 to 13 during these 94 clock pulses.

MC4355/4055

The MC4355/4055 works in the same manner as the MC4354/4054 except the least significant counter counts to 1111 before clocking the most significant counter, and both counters count to 1111 1111 or 255 before resetting to 0.

NBCD ADDER

MC4356
MC4056

Input Loading Factor: C_{in} = 5
A,B = 2
Output Loading Factor = 10
Total Power Dissipation = 300 mW typ/pkg
Propagation Delay Time = 30 ns typ

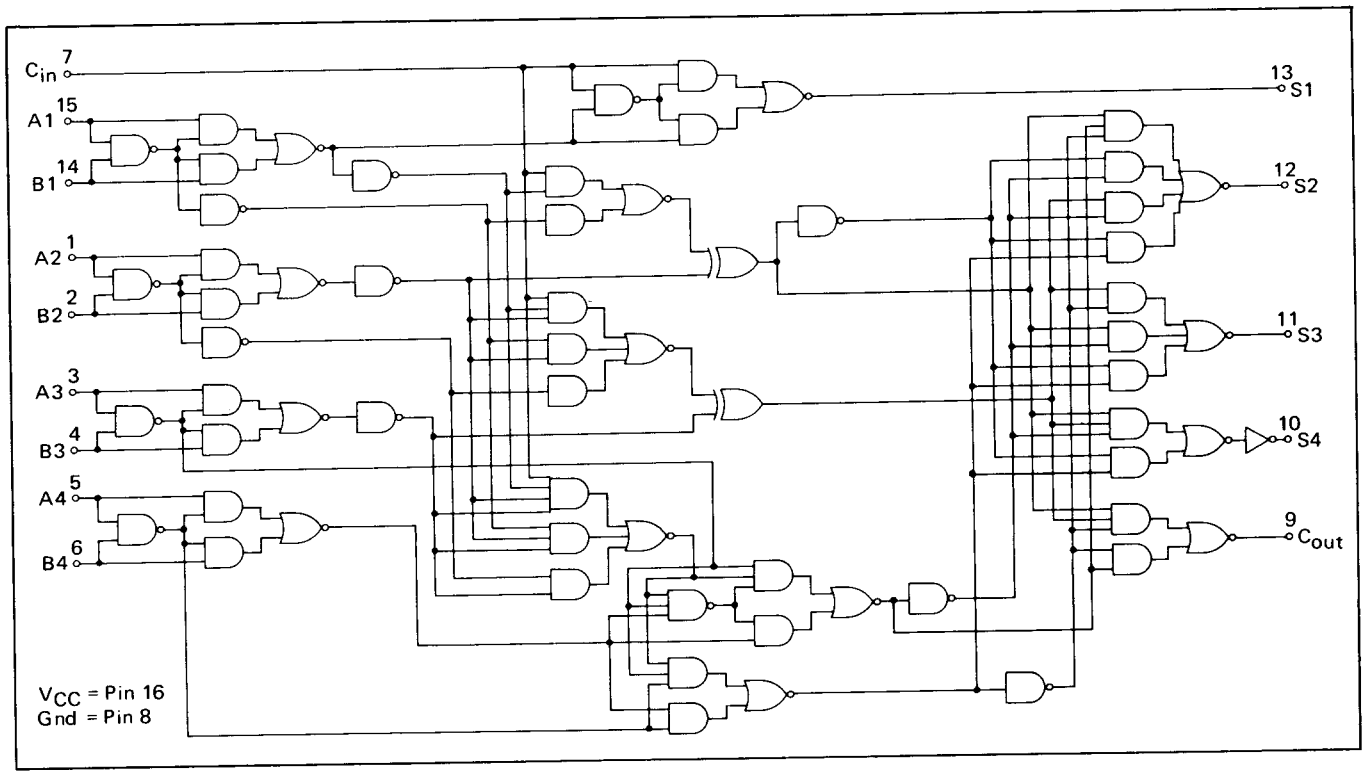
The MC4356/4056 adds two 4-bit numbers in NBCD (Natural Binary Coded Decimal) format. Sum and Carry outputs are generated, also in NBCD code.

NBCD adders are used in such applications as machine controls (to avoid conversion of NBCD data to binary numbers), and in phase-locked loops together with programmable counters. This adder can also subtract, when coupled to a 9's complement logic function.

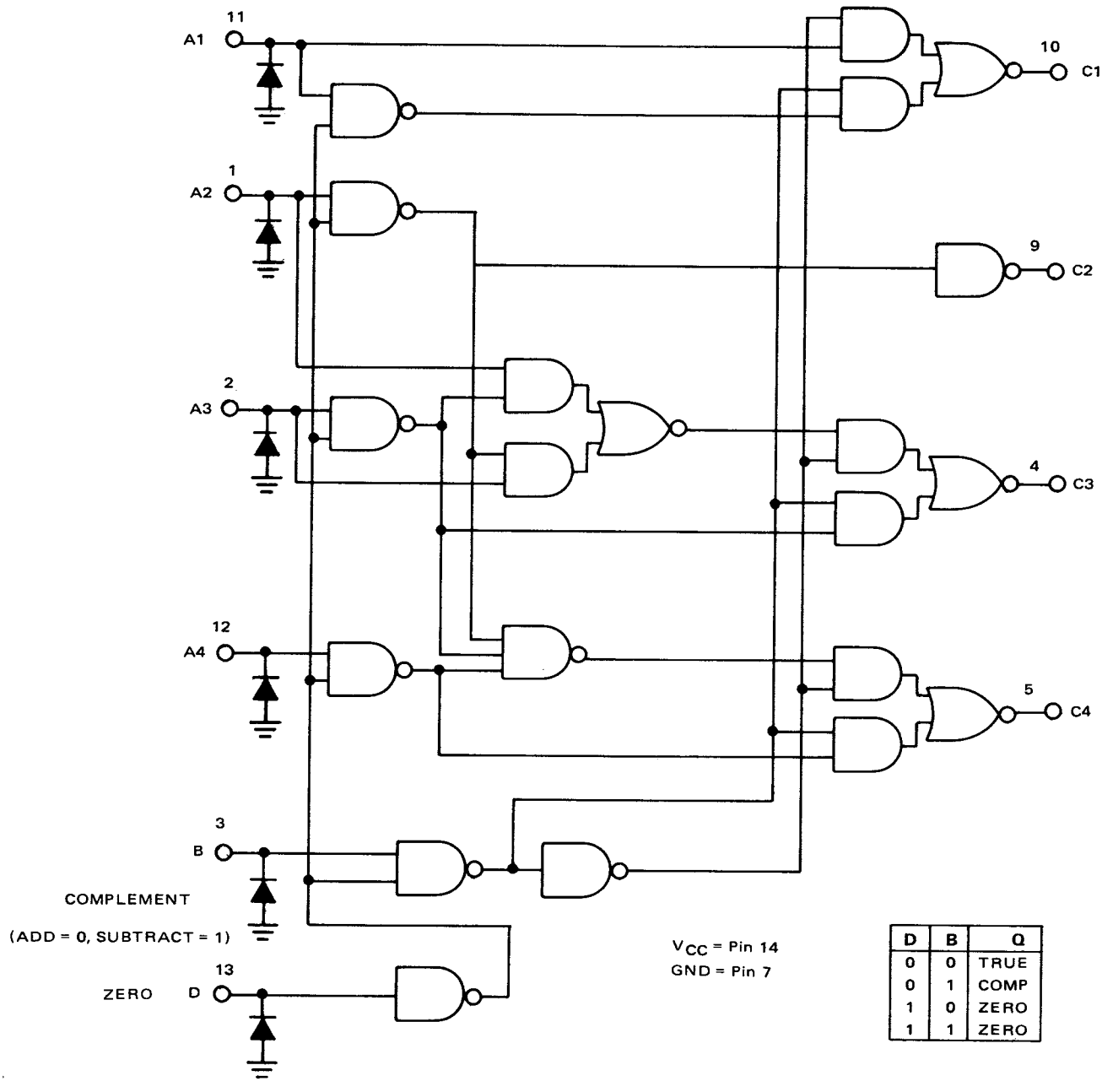
TRUTH TABLE*

INPUT									OUTPUT				
A4	A3	A2	A1	B4	B3	B2	B1	C_{in}	C_{out}	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	1	0	0	0	1	0	0	0	0	1	0	0	0
0	1	0	0	0	1	0	0	1	0	1	0	0	1
0	1	1	1	0	1	0	0	0	1	0	0	0	1
0	1	1	1	0	1	0	0	1	1	0	0	1	0
1	0	0	1	1	0	0	1	1	1	1	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	0	0
1	0	0	1	0	0	0	1	0	1	0	0	0	0

*This is only a partial truth table and is provided to illustrate the logic function of this device.



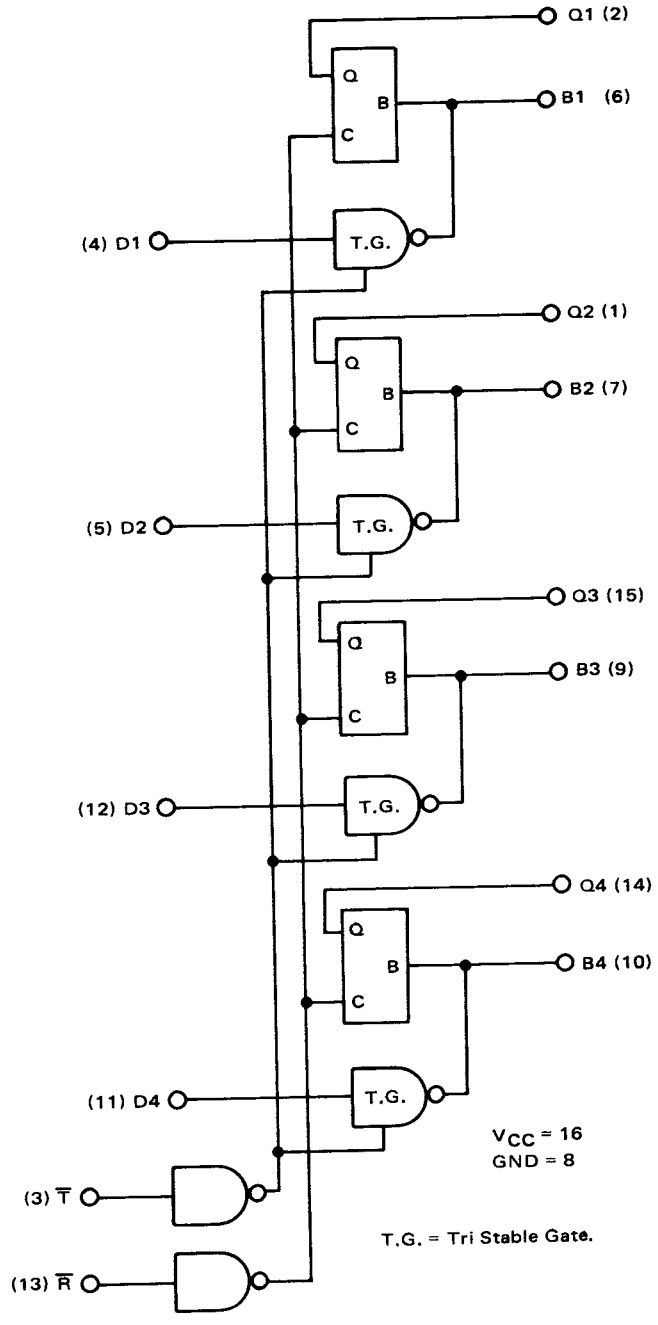
MC4358
MC4058



D	B	Q
0	0	TRUE
0	1	COMP
1	0	ZERO
1	1	ZERO

NBCD COMPLEMENTOR/ZERO ELEMENT

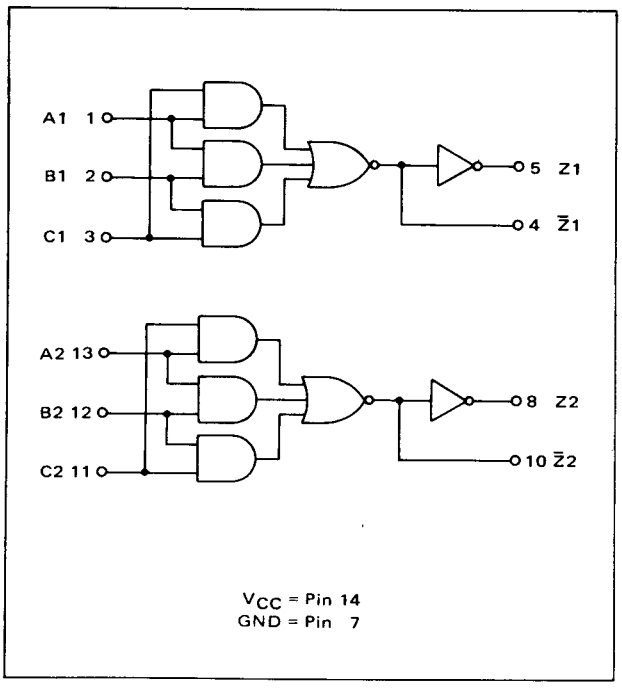
MC4360
MC4060



LOGIC DIAGRAM

DUAL
MAJORITY LOGIC GATE

MC4362
MC4062

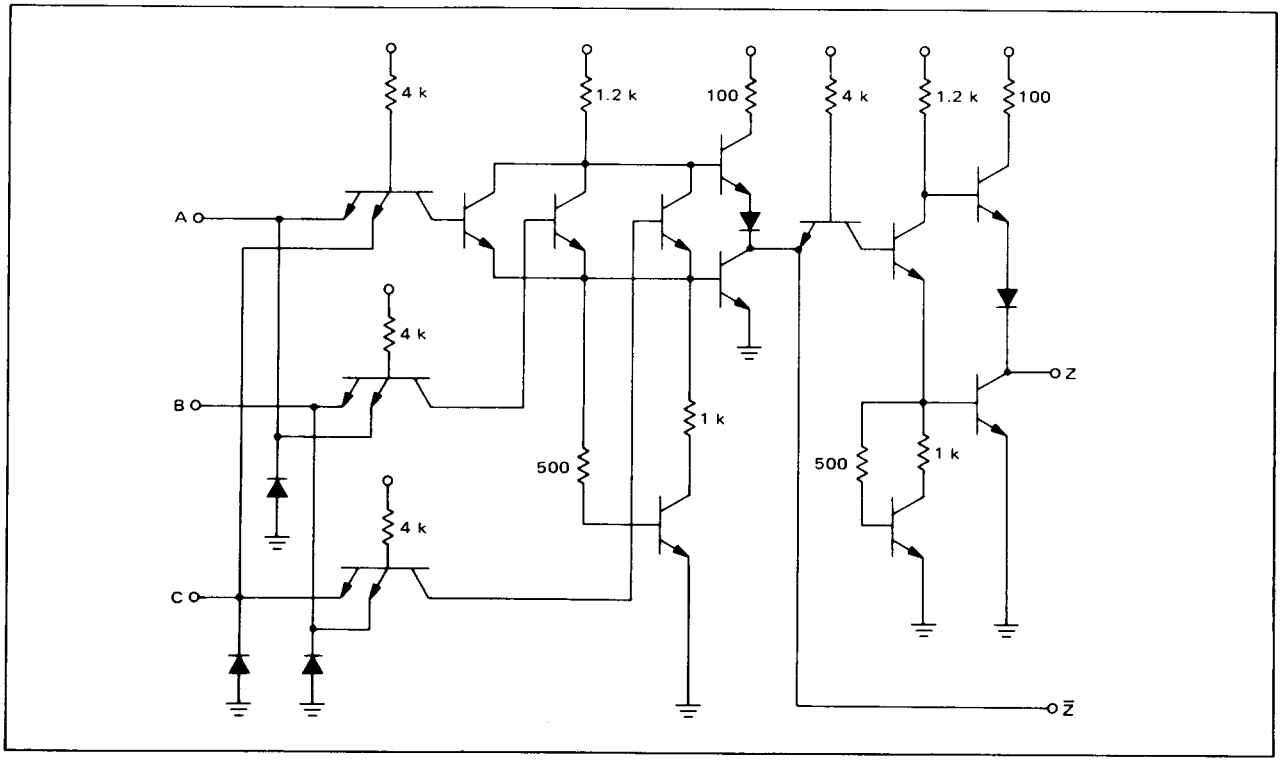


This integrated circuit offers the designer additional versatility in logic design. When any two or all three of the inputs are raised to the "1" level, the output goes to the "1" level. The output, Z, and its complement, $\overline{Z}$, are both available.

INPUT			OUTPUT	
A	B	C	Z	$\overline{Z}$
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0

Total Power Dissipation = 75 mW typ/pkg
Propagation Delay Time = 20 ns typ (Z Output)
11 ns typ ($\overline{Z}$ Output)

CIRCUIT SCHEMATIC
(1/2 OF DEVICE SHOWN)



64-BIT RANDOM ACCESS MEMORY

MC4364
MC4064

64-BIT RANDOM ACCESS MEMORY

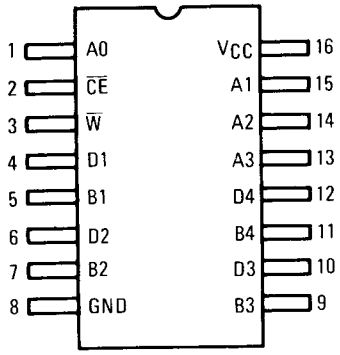
The **MC4364/4064** is a 64-Bit random access memory organized as a 16-word by 4-bit array. Schottky-diode-clamped transistors are utilized to obtain fast switching speeds, and Schottky clamp diodes are used on all inputs to provide minimum line reflection. The high speed of this memory makes it ideal in scratch pad operation.

Address decoding is incorporated in the circuit providing 1-of-16 decoding from the four address lines. Separate Data In and Data Out lines, together with a Chip Enable provide for easy expansion of memory capacity. A Write is provided to enable data presented at the Data In lines to be entered at the addressed storage cells. When writing, Data Out is the complement of the Data In.

The open-collector output transistors are also Schottky barrier devices and combine greater current sinking capability with lower leakage currents, thereby increasing the wire-OR capability of these devices.

- Both Minimum and Maximum Access Times Specified
- Binary Addressing
- Chip Enable for Memory Expansion
- Outputs May Be "Wire ORed"
- Logic Levels Compatible with MDTL and All MTTL Families
- Low-Voltage Input Clamp Diodes
- Access Time < 60 ns
- Power Dissipation Typically 6 mW/bit
- Outputs Sink 15 mA

PIN ASSIGNMENT



TRUTH TABLE

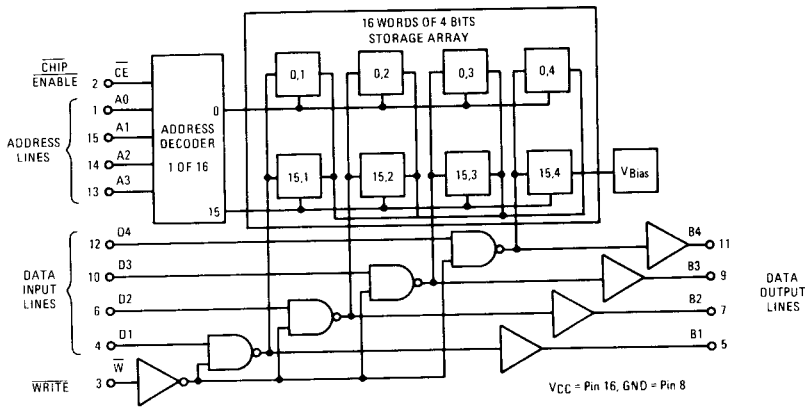
W	D	CE	DATA OUT
0	0	X	1
0	1	X	0
1	X	0	Read
1	X	1	1

X = Don't Care

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage – All Inputs	V_{in}	5.5	Vdc
Output Voltage – All Outputs	V_D	5.5	Vdc
Output Current	I_D	100	mAdc
Operating Temperature Range – MCM4364L – MCM4064L	T_A	-55 to +125 0 to +85	°C
Thermal Resistance, Junction to Ambient (Typical)	θ_{JA}	110	°C/W
Thermal Resistance, Junction to Case (Typical)	θ_{JC}	60	°C/W
Storage Temperature Range	T_{stg}	-65 to +160	°C

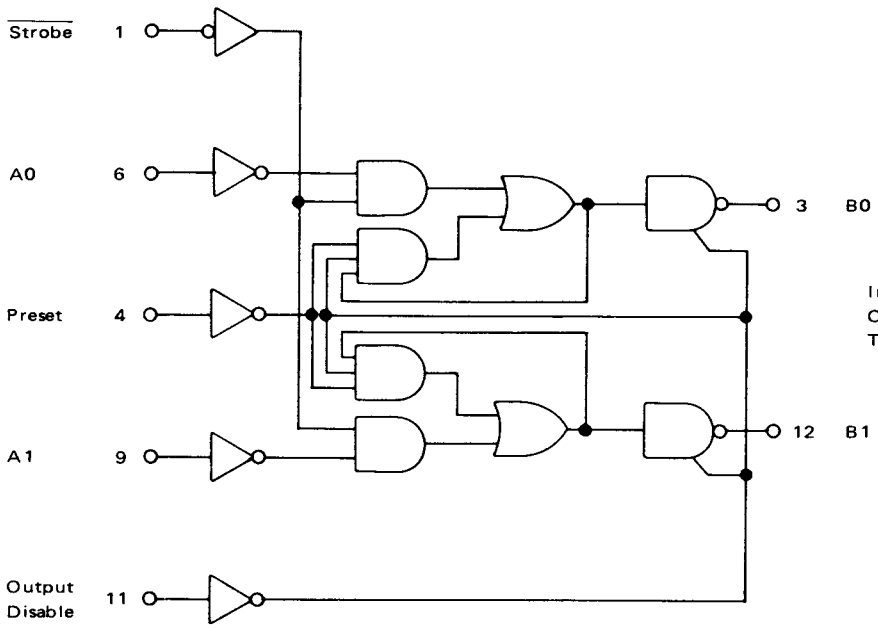
BLOCK DIAGRAM



DUAL MOS-TO-TTL LEVEL TRANSLATOR WITH THREE-STATE OUTPUT

MC4368
MC4068

The MC4368/4068 is a dual MOS-to-TTL translator designed to sense the open-drain output current of MOS memories such as the 1103 type. The device has several features that greatly enhance system performance and reduce package count: (1) no external components are required for interfacing, (2) current rather than voltage is sensed, (3) latch capabilities are available, (4) the device has bus driver capabilities, (5) the three-state output feature allows a number of outputs to be tied together on a common data bus without sacrificing the speed of the totem pole output, and (6) only the standard TTL 5-volt power supply is required.



Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 150 mW typ/pkg

A0 and A1 are current sensing inputs.

For maximum noise suppression, also connect pins 5, 8 and 10 to ground (they are internally connected to substrate).

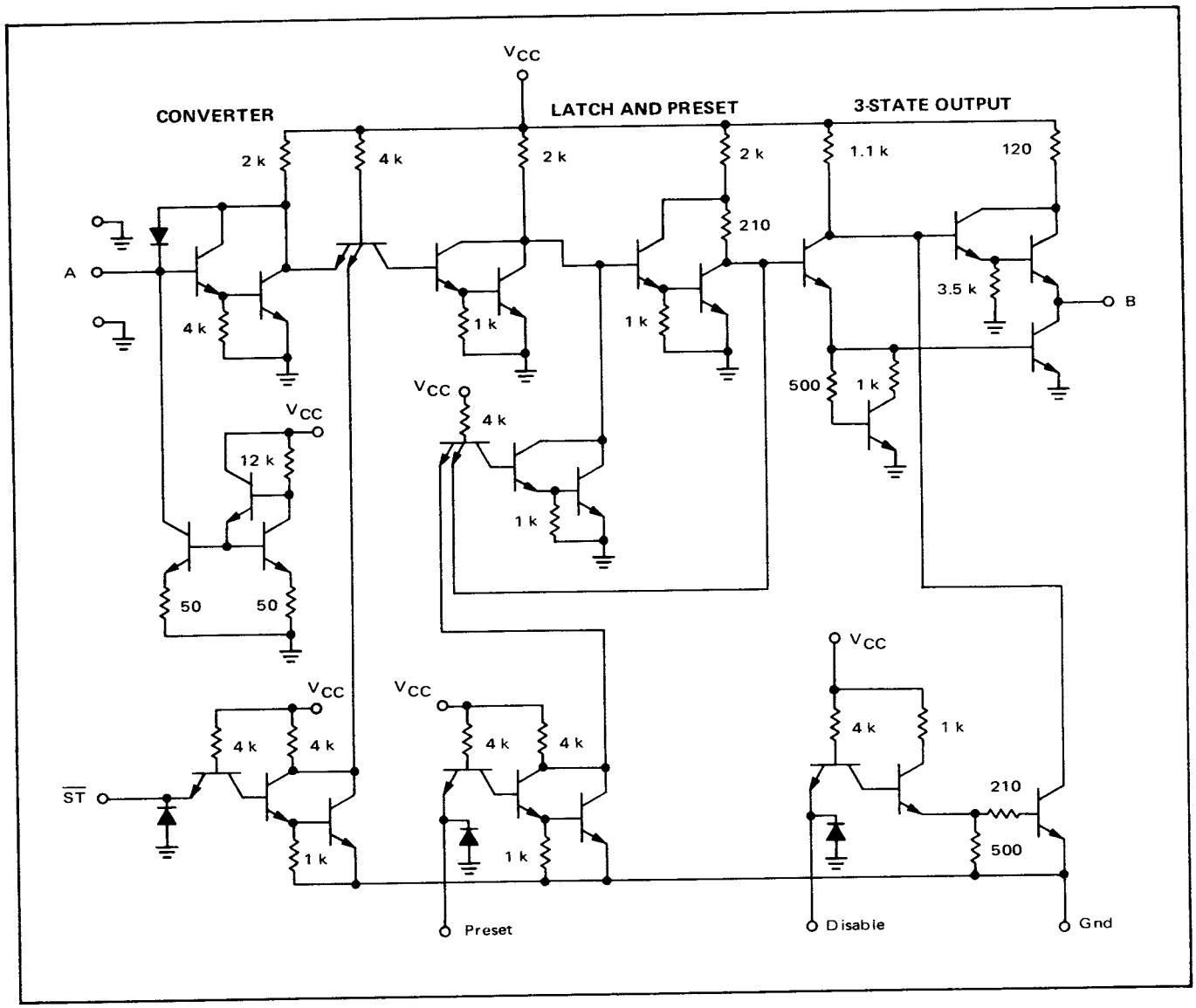
V_{CC} = Pin 14
Gnd = Pin 7

TRUTH TABLE

DIS	$\overline{ST}$	P	A0	A1	B0	B1
V_{ILT}	V_{IHT}	V_{ILT}	I_{S2}	I_{S2}	V_{OL}	V_{OL}
V_{ILT}	V_{IHT}	V_{IHT}	I_{S2}	I_{S2}	V_{OH}	V_{OH}
V_{ILT}	V_{IHT}	V_{ILT}	I_{S2}	I_{S2}	V_{OH}	V_{OH}
V_{ILT}	V_{IHT}	V_{ILT}	I_{S1}	I_{S1}	V_{OH}	V_{OH}
V_{ILT}	V_{ILT}	V_{ILT}	I_{S1}	I_{S1}	V_{OL}	V_{OL}
V_{ILT}	V_{IHT}	V_{ILT}	I_{S1}	I_{S1}	V_{OL}	V_{OL}
V_{ILT}	V_{IHT}	V_{ILT}	I_{S2}	I_{S2}	V_{OL}	V_{OL}
V_{IHT}	V_{ILT}	V_{ILT}	I_{S1}	I_{S1}	H*	H*
V_{IHT}	V_{IHT}	V_{IHT}	I_{S1}	I_{S1}	L**	L**

Ground pins 5, 7, 8, and 10.
*Outputs connected to V_{CC} thru 470 ohm resistor, H = 4.88 V min.
**Outputs connected to ground thru 220 ohm resistor, L = 55 mV max.

CIRCUIT SCHEMATIC
(1/2 of Device and Common Inputs Shown)



OPERATING CHARACTERISTICS

The MC4368/4068 is divided into three basic functions: (1) conversion of the MOS cell current to TTL voltage levels, (2) latching, and (3) coupling to the data bus.

The converter uses a darlington with negative feedback which provides a low input impedance and a fast recovery of the cell data line from noise. A fixed current logic threshold is provided by a sense amplifier arrangement. This threshold is nominally equal to one half of the minimum cell output current and is relatively unaffected by changes in temperature and power supply voltage. Ground pins are provided on each side of the current inputs. These effectively isolate the sensitive inputs from transients.

The latch contains two darlington NANDs which are ORed into another darlington. One NAND is used to strobe the converted MOS cell output into the latch and the other provides feedback for the latch and the preset function.

The latch is then coupled to the output data bus via a three-state output, which allows a number of these outputs to be tied together on a common data bus without sacrificing the speed of the totem pole output.