1.3 W Stereo Class AB Audio Power Amplifier

General Description

The MC4066 is a 1.3W bridge-connected dual audio power amplifier , when supplied with 5V voltage,the MC4066 can deliver 1.3W to a 8Ω load with the THD+N rate lower than 1.0%.

The dual audio power amplifier design of MC4066 provides high quality dual-channel output while requiring few external components and consumingvery little PCB space.

The MC4066's power-saving feature is another plus tailored for handheld device. When the power-saving mechanism is activated, only 0.04μA current is running on the MC4066. Other features such as thermal shutdown protection and "click and pops" reduction during power-up ensure the safety and reliability in real applications.

The MC4066 is available in a 3mm*3mm*0.75mm 16-pin QFN package

Features

- Po at 1% THD+N, VDD = 5V
  RL = 8 Ω 1.3W (typ)
- 2.7-5.5V operation
- 0.04μA ultra low current shutdown mode
- Suppress pop & click circuitry
- PSRR @ 217Hz:70dB(TYP)
- Thermal shutdown protection
- RoHS compliant and 100% lead(Pb)-free

Applications

- PAD,GPS
- Mobile Phones
- Notebook,EPC
- Portable Electronis devices

Function Block Diagram

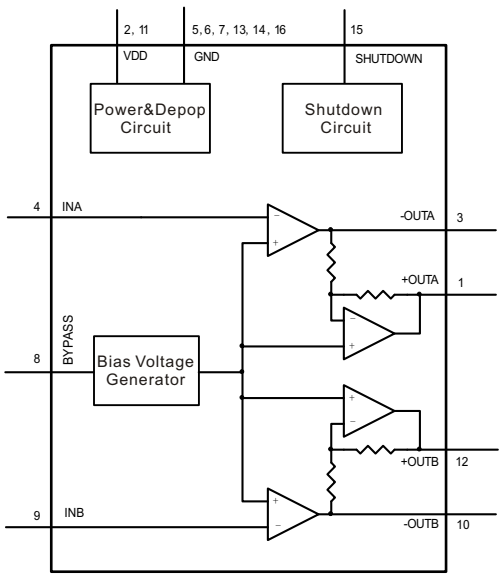


Figure1.

1.3 W Stereo Class AB Audio Power Amplifier

Pin Configuration

QFN 3X3_16L

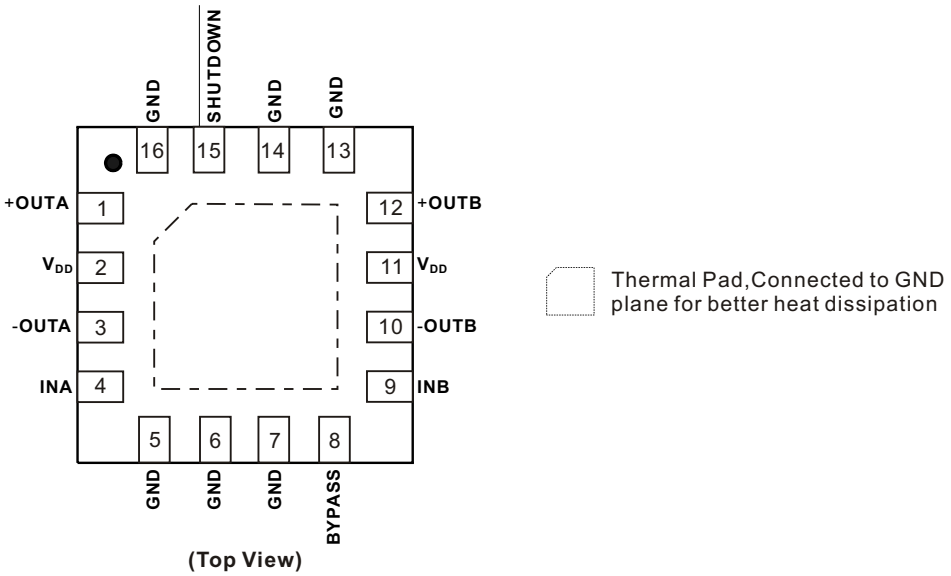


Figure 2

Pin Descriptions

Pin	Symbol	Description
1	+OUTA	Left channel +output
2,11	VDD	Supply Voltage
3	-OUTA	Left channel -output
4	INA	Left Channel Input
8	Bypass	Capacitor which provides the common mode voltage
9	INB	Right Channel Input
10	-OUTB	Right channel -output
12	+OUTB	Right channel +output
15	$\overline{\text{Shutdown}}$	Shut down control, hold low for shutdown mode
5 , 6 , 7 , 13 , 14 , 16	GND	GND

1.3 W Stereo Class AB Audio Power Amplifier

Typical Application

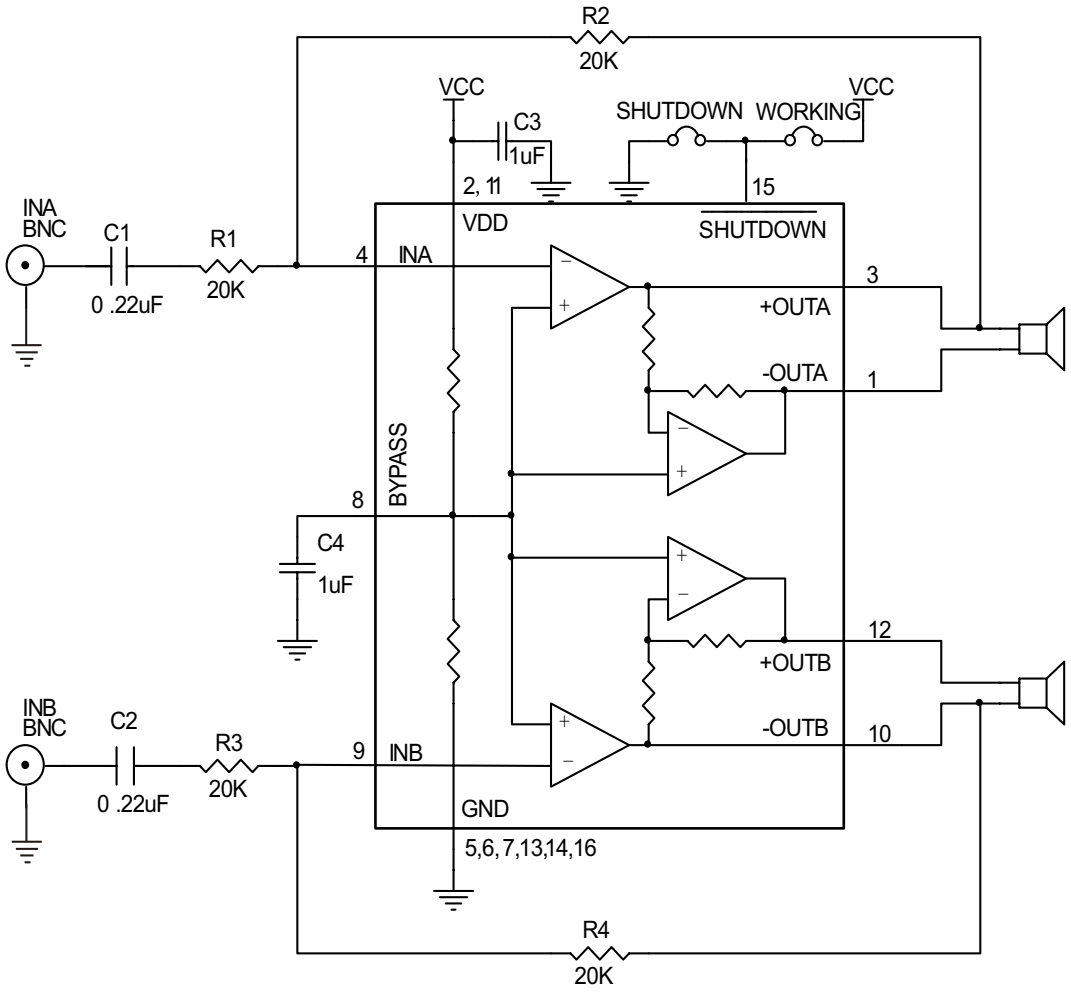


Figure 3.

1.3 W Stereo Class AB Audio Power Amplifier

Absolute Maximum Ratings[1]

Symbol	Description	Value	Unit
V_{DD}	Supply Voltage at no Input Signal	6	V
V_I	Input Voltage	-0.3 to VDD+0.3	V
T_J	Junction Temperature	150	°C
T_{SDR}	Maximum Lead Soldering Temperature , 10 Seconds	260	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C

Recommended Operating Conditions

Symbol	Description	Value	Unit
V_{DD}	Supply Voltage	2. 7~5.5	V
T_A	Ambient Temperature Range	-40~85	°C
T_J	Junction Temperature Range	-40~125	°C

Thermal Information[2]

Symbol	Description	Value	Unit
θ_{JA}	Thermal Resistance-Junction to Ambient	42	°C/W
θ_{JC}	Thermal Resistance-Junction to Case	3	°C/W

Ordering and Marking Information

Device	Package Type	Device Marking	Reel Size	Tape Width	Quantity
MC4066	QFN 3X3_16L	XXXXX MC4066	13''	12mm	5000 units

ESD Susceptibility

ESD Susceptibility-HBM ---------- 2kV
ESD Susceptibility-MM ---------- 200V

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device.Functional operation at conditions other than the operating conditions specified is not implied.Only one Absolute Maximum Rating should be applied at one time.
2. The ThermalPad on the bottom of the IC should soldered directly to the PCB's ThermalPad area that with several thermal vias connect to the ground plan,and the PCB is a 2-layer,5-inch square area with 2oz copper thickness.

1.3 W Stereo Class AB Audio Power Amplifier

Electrical Characteristics(5V)

（V_{DD}= 5V, T_A = 25°C unless otherwise noted）

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_{DD}	Quiescent power supply current V_{IN}=0V, Io=0A			6.0	10	mA
I_{SD}	Shutdown current GND applied to the shutdown pin			0.04	1.0	uA
V_{IH}	Shutdown input voltage high			1.2	1.5	V
V_{IL}	Shutdown input voltage low		0.7	1		V
T_{WU}	Turn on time 1uF bypass cap(C4)			100		ms
Vos	Output offset voltage V_{IN}=0V			5		mV
Po	Output power	THD+N=1% , f=1 kHz R_L=8Ω	1.1	1.3		W
		THD+N=10% , f=1k Hz R_L=8Ω		1.6		W
THD+N	Total harmonic Distortion+noise 1K Hz, Avd=2 R_L=8Ω , Po= 0. 7W			0.06		%
PSRR	Power Supply Rejection ratio	Input unterminated 217Hz, R_L=8Ω Vripple= 200mV p-p C4= 1uF,		70		dB
		Input unterminated 1KHz, R_L=8Ω Vripple= 200mV p-p C4 =1uF,		60		dB
		Input grounded 217Hz, R_L=8Ω Vripple= 200mV p-p C4 =1uF,		70		dB
		Input grounded 1KHz, R_L=8Ω Vripple= 200mV p-p C4 =1uF,		65		dB
Xtalk	Channel separation f=1K Hz, C4 = 1uF			80		dB

1.3 W Stereo Class AB Audio Power Amplifier

Electrical Characteristics(3V)

(V_{DD}= 3V, T_A = 25°C unless otherwise noted)

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_{DD}	Quiescent power supply current V_{IN}=0V, Io=0A			3	6	mA
I_{SD}	Shutdown current GND applied to the shutdown pin			0.02	0.5	uA
V_{IH}	Shutdown input voltage high			1.1	1.3	V
V_{IL}	Shutdown input voltage low		0.5	0.8		V
T_{WU}	Turn on time 1uF bypass cap(C4)			95		ms
Vos	Output offset voltage V_{IN}=0V			2.5		mV
Po	Output power	THD+N=1% , f=1 kHz R_L=8Ω	0.35	0.45		W
		THD+N=10% , f=1k Hz R_L=8Ω		0.54		W
THD+N	Total harmonic Distortion+noise 1K Hz, Avd=2 R_L=8Ω , Po= 0.25W			0.08		%
PSRR	Power Supply Rejection ratio	Input unterminated 217Hz, R_L=8Ω Vripple= 200mV p-p C4= 1uF,		74		dB
		Input unterminated 1KHz, R_L=8Ω Vripple= 200mV p-p C4 =1uF,		64		dB
		Input grounded 217Hz, R_L=8Ω Vripple= 200mV p-p C4 =1uF,		70		dB
		Input grounded 1KHz, R_L=8Ω Vripple= 200mV p-p C4 =1uF,		65		dB
Xtalk	Channel separation f=1K Hz, C4 = 1uF			80		dB

1.3 W Stereo Class AB Audio Power Amplifier

Typical Operating Characteristics

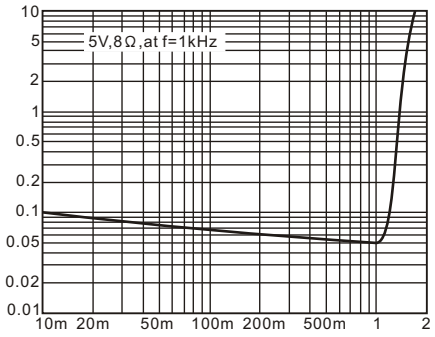


Figure4.THD+N vs. Output Power

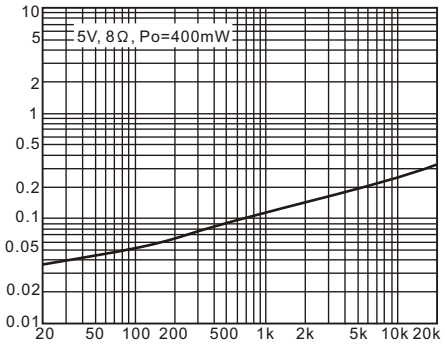


Figure5.THD+N vs. Frequency

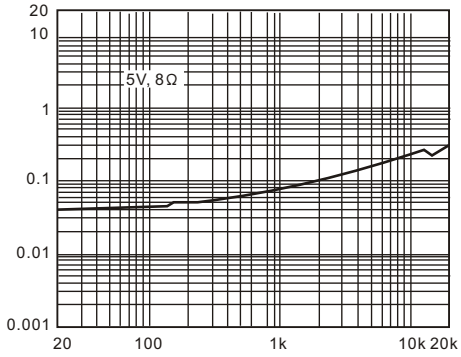


Figure6.THD+N vs. Frequency

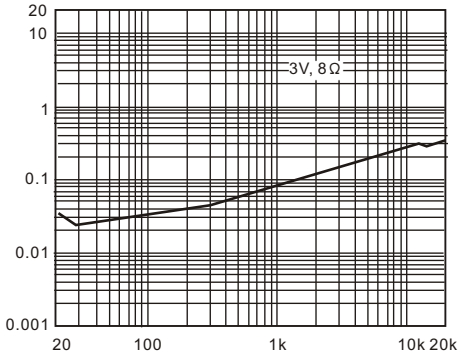


Figure7.THD+N vs. Frequency

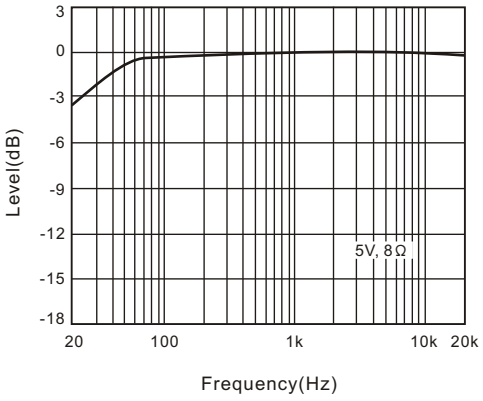


Figure8.Frequency Response

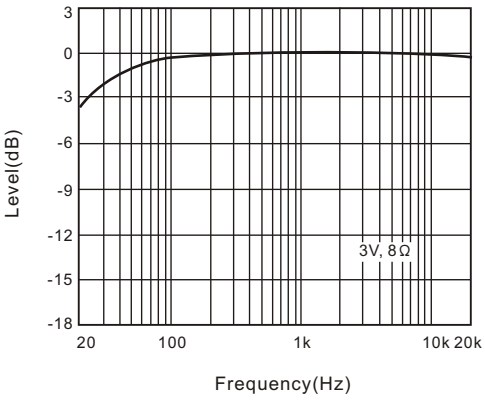


Figure9.Frequency Response

1.3 W Stereo Class AB Audio Power Amplifier

Typical Operating Characteristics (Continued)

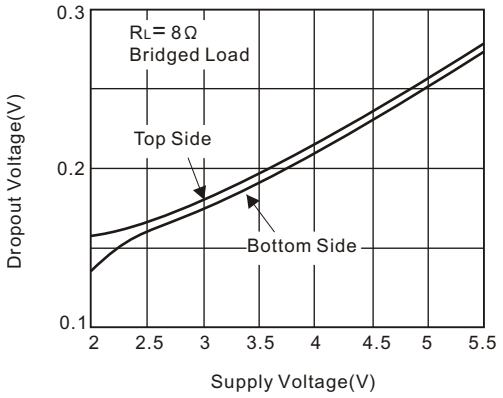


Figure 10,Dropout Voltage vs Supply Voltage

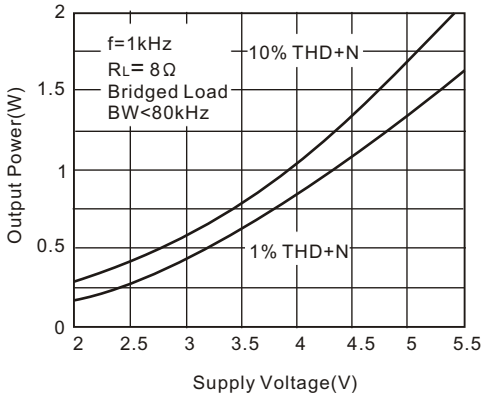


Figure 11,Output Power vs Supply Voltage

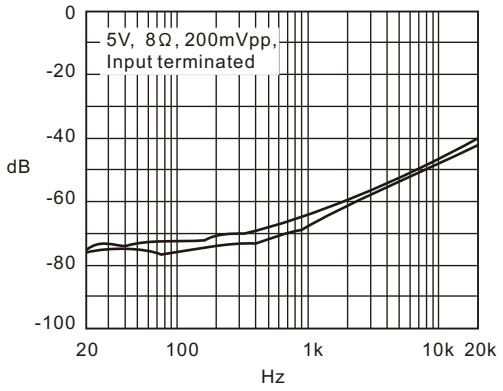


Figure12.PSRR vs. Freq.

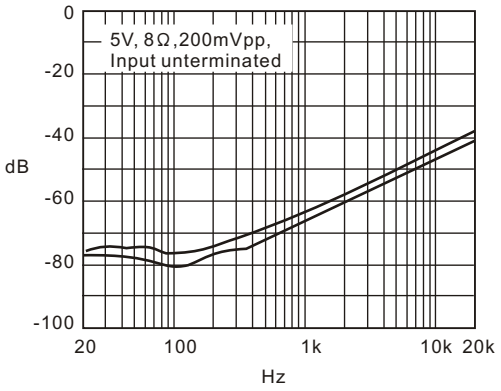


Figure13.PSRR vs. Freq.

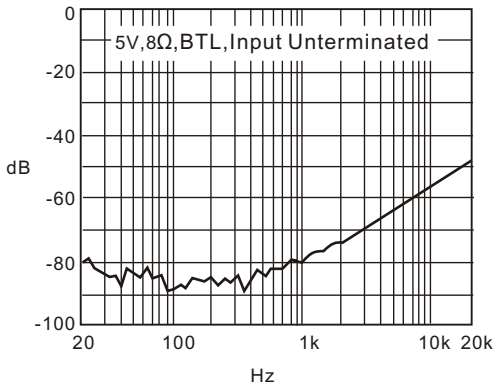


Figure 14,PSRR vs. Freq.

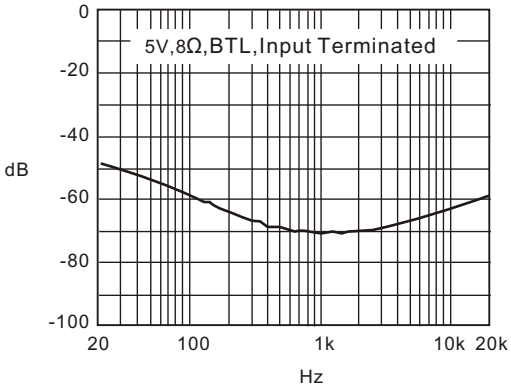


Figure 15,PSRR vs. Freq.

1.3 W Stereo Class AB Audio Power Amplifier

Typical Operating Characteristics (Continued)

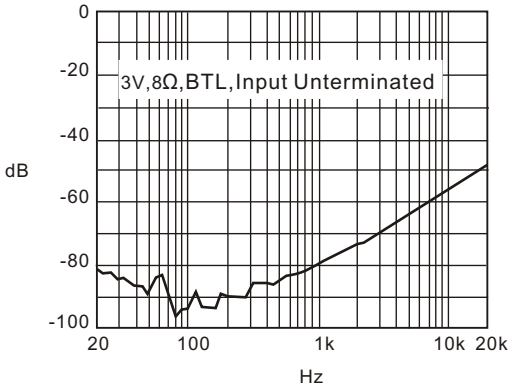


Figure 16,PSRR vs. Freq.

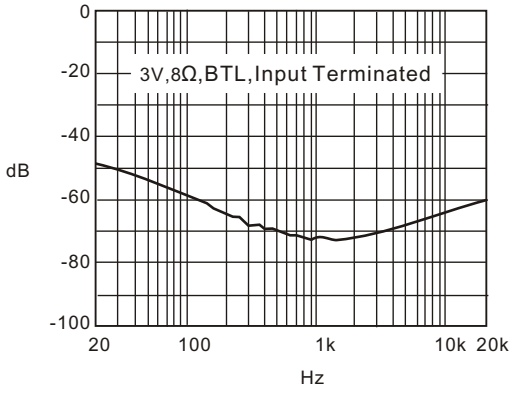


Figure 17,PSRR vs. Freq.

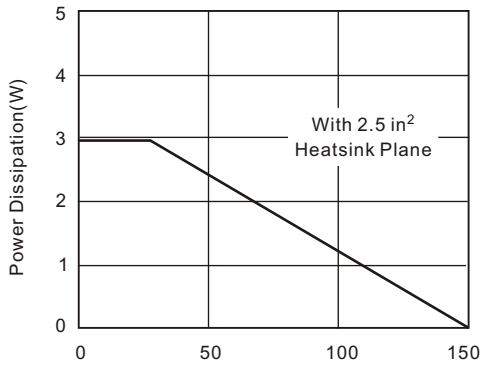


Figure 18,Power Derating Curve

1.3 W Stereo Class AB Audio Power Amplifier

Applications Information

Bridged Amplifier

The MC4066 consists of two pairs of amplifiers which form a Dual-channel stereo amplifier. External feedback resistors R2, R4 and input resistors R1 and R3 set the closed-loop gain of Amp A (-out) and Amp B (-out) while two internal 20kΩ resistors set Amp A's (+out) and Amp B's (+out) gain at 1. The amplifiers' (-OUT) outputs also serve as (+OUT)'s inputs and produce (+OUT) outputs identical in magnitude but opposite in phase with the(-OUT) signal.Hence the load between the(+OUT) and (-OUT) is driven differentially,or in another word,in bridge mode.
The differential gain result:

$$A_{VD} = 2 * (Rf/Ri) \qquad (1)$$

Bridge mode amplifier provides four times the output power of that from single-ended amplifier under the same condition.However,the power increase calculation assumes that amplifier is not current limited or that the output signal is not clipped.Therefore,to ensure minimum output signal clipping,care must be taken when choosing an amplifier's closed-loop gain.

Power Dissipation

Power dissipation is critical for either single-ended or bridged amplifier board design. Equation(2) indicates the maximum power dissipation for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L) \qquad (2)$$
(Single-Ended)

The MC4066 where two operational amplifiers per channel are adopted,the internal power dissipation per channel is four times that of a single-ended amplifier,as indicated in Equation (3).Given a 5V input power and a 8Ω output load, the maximum total power dissipation is 0.63W for single channel or 1.23W for stereo output.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \qquad (3)$$
(Bridge-mode)

For MC4066 single channel power dissipation must not exceed the P_{DMAX}' value in equation(4). The MC4066's T_{MAX} is 150°C; θ_{JA} is 20°C/W given that the package is soldered to a DAP pad that expands to a copper area of 5 square inches on PCB.Equation(5) is a variation of Equation (4) for calculating the maximum ambient temperature at maximum stereo power dissipation when junction temperature limitation is not exceeded.

$$P_{DMAX}' = (T_{JMAX} - T_A)/\theta_{JA} \qquad (4)$$

$$T_A = T_{JMAX} - 2*P_{DMAX}\theta_{JA} \qquad (5)$$

The examples above assume that a device is a surface mount part operating around the maximum power dissipation point.Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases,If P_{DMAX} in Equation(2) or (3) exceeds P_{DMAX}' in Equation (4),measures should be taken by either decreasing the supply voltage,increasing load impedance,reducing the ambient temperature or adding external heat sink.When heat sink is applied to system design,the θ_{JA} equals(θ_{JC}+θ_{JA} +θ_{SA}).(θ_{JC}:junction-to-case thermal impedance; θ_{CS}:case-to-sink thermal impedance;θ_{SA}:sink-to-ambient thermal impedance;)

Power Supply Bypassing

Proper power supply bypassing is critical for low noise performance and high power supply rejection in a power amplifier.Applications employing 5V regulator typically use a 10uF in parallel with a 0.1uF filter capacitor to stabilize the regulator's output ,reduce noise on the supply line,and impove the supply's transient response.However,their presence does not eliminate the need for a 1.0uF tantalum bypass capacitor connected between the MC4066's power supply pins and the ground.Do not substitute a ceramic capacitor for the tantalum, or it would cause oscillation.Optimizing the length of leads and traces between the MC4066 and ground also help to improve the power supply bypassing.

1.3 W Stereo Class AB Audio Power Amplifier

Components

Proper external components are essential for building up an MC4066 system.Although the MC4066 can function well with various external component combinations,most optimized performance and cost are achieved only with careful selection.

The MC4066 is unity-gain stable which provides wide design feasibility for designers.The gain is set to meet individual application requirements but no higher in order to get minimum THD+N and maximum Signal-Noise Ratio(SNR). However,lower gain demands input signals with greater voltage swings to achieve maximum output power.Fortunately,many signal sources such as CODECs have outputs of 1V_{RMS} (2.83V_{P-P}).

Input Capacitor

High value input coupling capacitors(C1,C2) are required to amplifying the low inputting audio signal as illustrated in Figure 1.However,high value capacitor can be expensive in cost and big in size which may become a fatal issue for handheld devices.Besides,the speakers in handheld and portable devices,either internal or external,seldom reproduce signals below 150Hz.Therefore,big input capacitor has very little influence in output signal quality in applications using limited frequency response speakers.

Besides the cost and size,C1 and C2 also influence the click and pop performance.When the supply voltage is fed in,a transient(pop) is generated as the charge on the input capacitor changes from 0 to a quiescent state.The magnitude of the pop is proportional to the input capacitance.The higher the capacitance is,the more time it requires to reach quiescent DC voltage(usually 0.5V_{DD}) when charged with a fixed current.The amplifier output charges the input capacitor through the feedback resistirs (R2,R4).Therefore,pops can be minimized with input capacitance no higher than necessary to provide -3dB frequency.

R1 and R3 are input resistors.C1 and C2 produce -3dB high pass filter cutoff frequency as stated in Equation(6).

$$f_{-3dB}=1/(2\pi R_{IN}C_{IN})=1/(2\pi R1C1) \quad (6)$$

Bypass Capacitor

Bypass capacitor determines the time needed for setting MC4066 to quiescent operation and plays an important role in minimizing turn-on pops.The slower the output ramp to quiescent DC voltage(0.5V_{DD} nominal),the smaller the turn-on pop is.The relationship between the capacitance and turn-on time is listed in the table below.In Figure 1,C4 is a 1.0uF bypass capacitor which,altogether with C1,minimizes the pops and clicks.

C4	T_{ON}
0.01uF	38ms
0.1uF	40ms
0.22uF	50ms
0.47uF	70ms
1.0uF	100ms

Micro-Power Shutdown

The MC4066's power saving scheme is realized through the SHUTDOWN pin and the voltage applied on it.The micro-power shutdown is performed to turn off the amplifier's bias circuitry as long as the SHUTDOWN pin is grounded. Typically,current as low as 0.04uA can be achieved by applying a votage close to GND to the SHUTDOWN pin.

The Micro-Power shutdown can be initiated and controlled by either a single-pole,single-throw switch,or a microprocessor,or a microcontroller. A switch is employed in the reference design illustrated in Figure 1.Connect an external 100k resistor between the SHUTDOWN pin and the ground;connect the switch between the SHUTDOWN pin and V_{DD}. Closing the switch sets the amplifier in normal function,while opening the switch sets the SHUTDOWN pin to ground through the 100k resistor and consequently actives the shutdown. The switch and resistor design guarantees that the SHUTDOWN pin is not float to prevent unwanted state changes.In digital systems, where mircoprocessoes or microcontrollers are deployed,digital output can be applied to control the SHUTDOWN input voltage.

Optimizing Click and Pop Reduction Performance

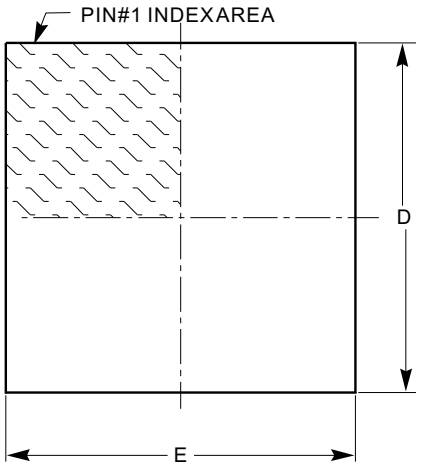
The MC4066 contains circuitry that minimizes turn-on and shutdown transients or “clicks and pop”. For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. When the part is turned on, an internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 VDD. As soon as the voltage on the bypass pin is stable, the device becomes fully operational. Although the BYPASS pin current cannot be modified, changing the size of C4 alters the device’s turn-on time and the magnitude of “clicks and pops”. Increasing the value of C4 reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C4 increases, the turn-on time increases. There is a linear relationship between the size of C4 and the turn-on time.

In order eliminate “clicks and pops”,all capacitors must be discharged before turn-on. Rapidly switching V_{DD} on and off may not allow the capacitors to fully discharge,which may cause”clicks and pops”.

1.3 W Stereo Class AB Audio Power Amplifier

Package Information

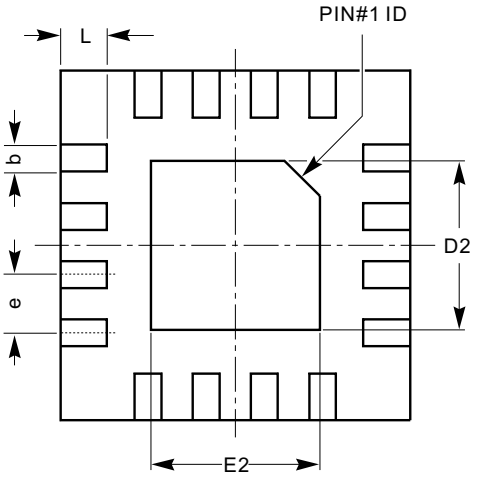
QFN 3X3_16L



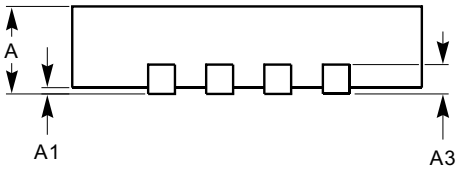
TOP VIEW

Unit: mm

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D	2.90	3.00	3.10
D2	1.40	-	1.80
E	2.90	3.00	3.10
E2	1.40	-	1.80
e		0.50 BSC	
L	0.30	0.40	0.50



BOTTOM VIEW



FRONT VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Package body sizes exclude mold flash and gate burrs.
(3) Complies with JEDEC standard MO-220.

ED: DOC.QFN 3X3_16L-090720