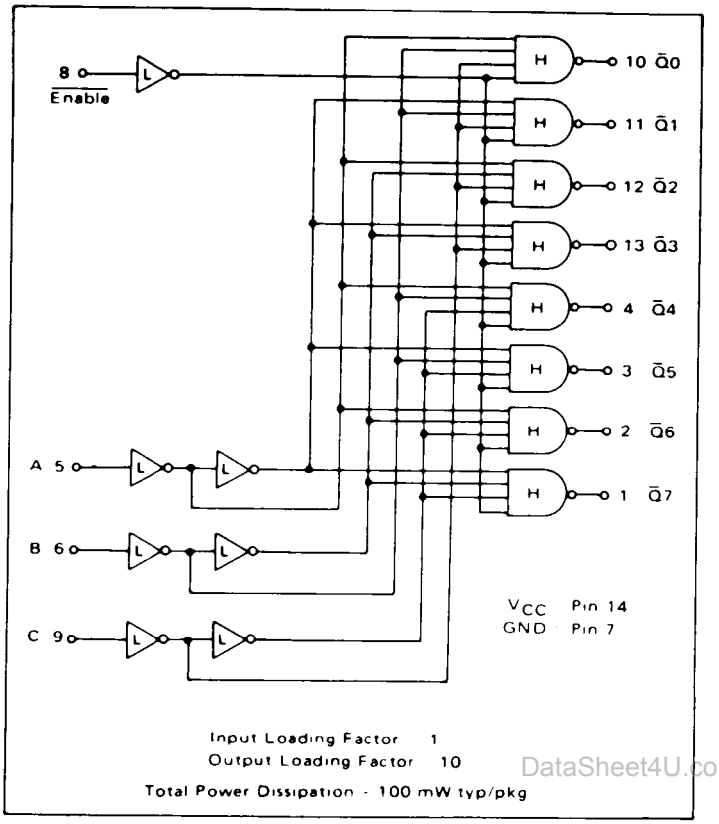
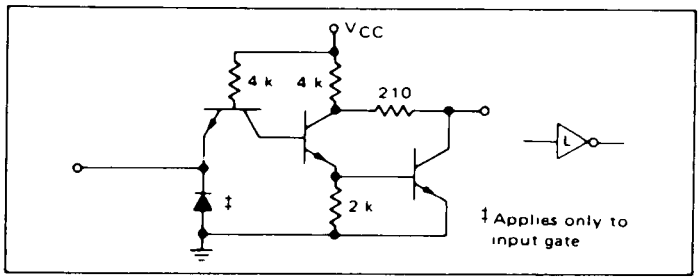
BINARY TO ONE-OF-EIGHT LINE DECODER

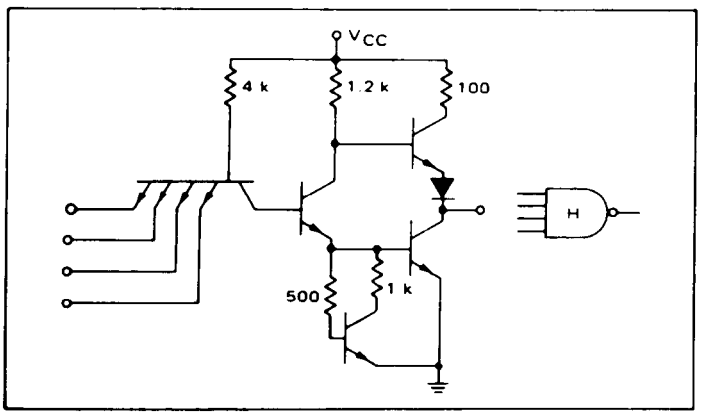
MC4306
MC4006



LOW-LEVEL INVERTER



HIGH-LEVEL GATE



This device converts three lines of input data to a one-of-eight output. The enable line provides an inhibit capability and also allows the decoder to be expanded for larger decoder systems.

The 3-input/8-output decoder consists of high-level and low-level gates internally connected for minimum power consumption and maximum driving capabilities. The enable gate must be in the low state to perform the decode operation shown in the truth table.

The propagation delays shown in the charts are typical and vary according to loading, interconnection wiring length, and the number of logic levels involved.

$\bar{E}$ 0

TRUTH TABLE

C	B	A	Q̄7	Q̄6	Q̄5	Q̄4	Q̄3	Q̄2	Q̄1	Q̄0
0	0	0	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	0	1
0	1	0	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	1	1	0	1	1	1	1
1	0	1	1	1	0	1	1	1	1	1
1	1	0	1	0	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1

1 High State
0 Low State

TYPICAL TURN-ON DELAY TIMES (ns)
T_A 25°C, C_T - 25 pF

INPUT	Q̄0	Q̄1	Q̄2	Q̄3	Q̄4	Q̄5	Q̄6	Q̄7
A	11.5	16.0	11.5	16.0	11.5	16.0	11.5	16.0
B	11.5	11.5	16.0	16.0	11.5	11.5	16.0	16.0
C	11.5	11.5	11.5	11.5	16.0	16.0	16.0	16.0
$\bar{E}$	13.5	13.5	13.5	13.5	13.5	13.5	13.5	13.5

TYPICAL TURN-OFF DELAY TIMES (ns)
T_A = 25°C, C_T = 25 pF

INPUT	Q̄0	Q̄1	Q̄2	Q̄3	Q̄4	Q̄5	Q̄6	Q̄7
A	14.0	19.5	14.0	19.5	14.0	19.5	14.0	19.5
B	14.0	14.0	19.5	19.5	14.0	14.0	19.5	19.5
C	14.0	14.0	14.0	14.0	19.5	19.5	19.5	19.5
$\bar{E}$	14.5	14.5	14.5	14.5	14.5	14.5	14.5	14.5