QUAD TYPE D FLIP-FLOP

MC4315
MC4015

1/4 OF DEVICE SHOWN
(CLOCK AND RESET COMMON TO ALL FOUR FLIP-FLOPS)

13 CLOCK   3 RESET

D
2

L

L   L   L

L   L   H   Q
6

SET
4

Input Loading Factor:
    D = 1   CLOCK = 8
    SET = 2   RESET = 8

V_{CC} = PIN 16
GND = PIN 8

Output Loading Factor = 10

Total Power Dissipation = 190 mW typ/pkg

Propagation Delay Time = 16 ns typ

Setup Time = 10 ns max

Hold Time = 10 ns max

Operating Frequency = 30 MHz typ
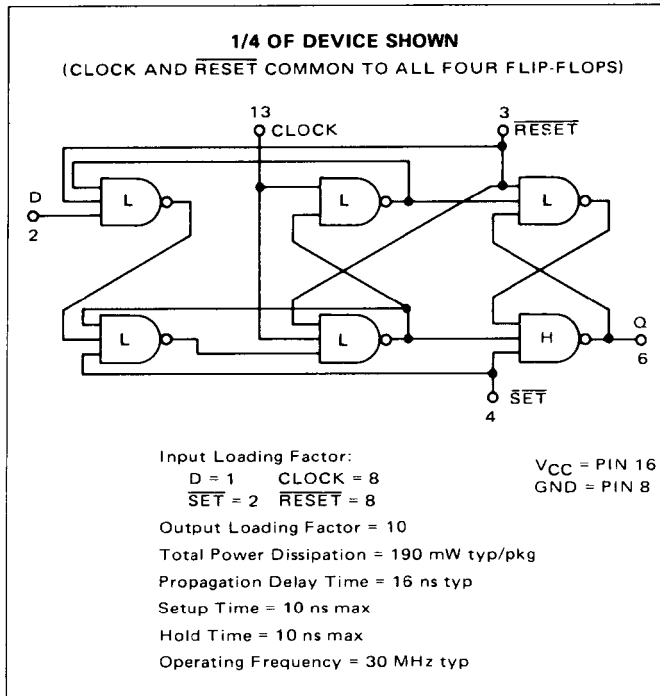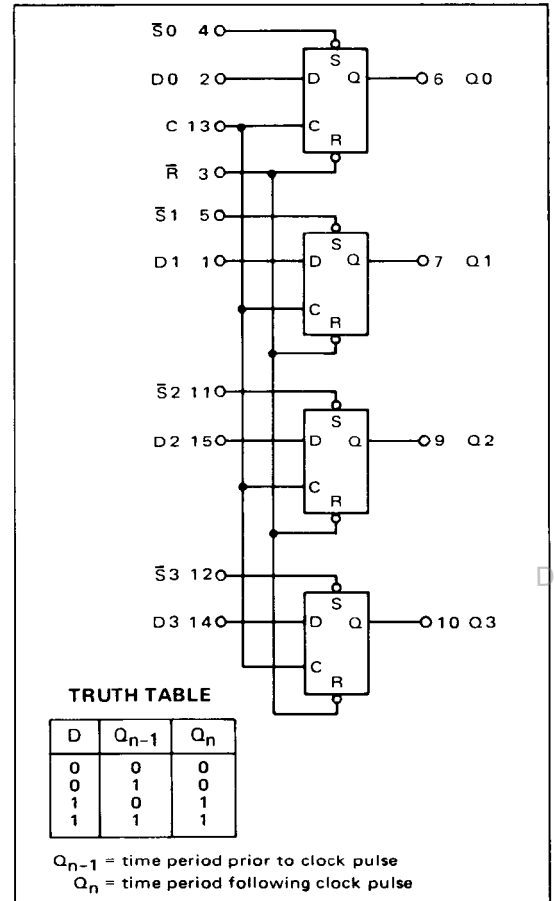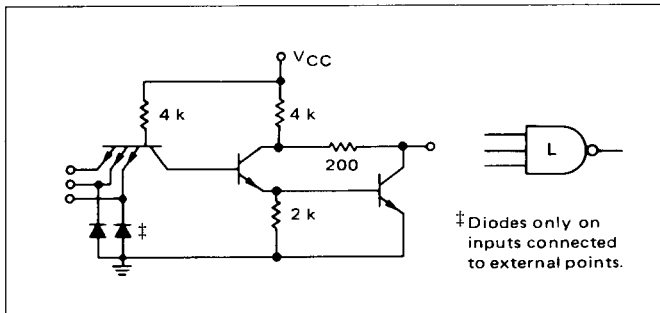
This quad type D flip-flop triggers on the positive edge of the clock input. During the clock transition the state of the D input is transferred to the Q output. The device is useful in shift registers and simple counters.

Power dissipation is minimized and output drive capability is maximized by connecting low and high-level gates as shown by the logic diagram to form each of the four flip-flops.
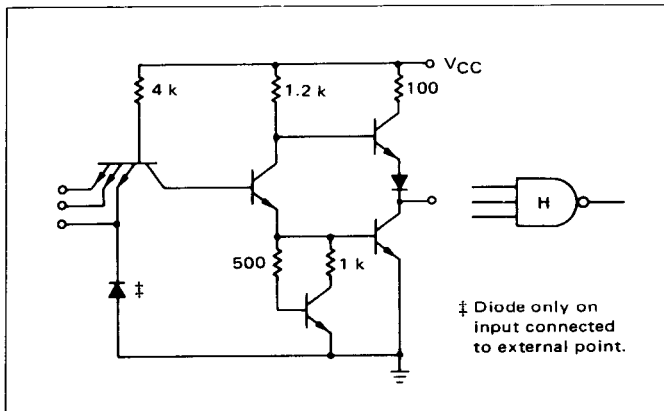
S0 4
D0 2   S D Q   6   Q0
C 13   C
R 3   R

S1 5
D1 1   S D Q   7   Q1
             C
             R

S2 11
D2 15   S D Q   9   Q2
             C
             R

S3 12
D3 14   S D Q   10 Q3
             C
             R

TRUTH TABLE

D	Q_{n-1}	Q_n
0	0	0
0	1	0
1	0	1
1	1	1

Q_{n-1} = time period prior to clock pulse
Q_n = time period following clock pulse

LOW-LEVEL GATE

V_{CC}

4 k   4 k

200

2 k

‡ Diodes only on inputs connected to external points.

L

HIGH-LEVEL GATE

V_{CC}

4 k   1.2 k   100

500   1 k

‡ Diode only on input connected to external point.

H

OPERATING CHARACTERISTICS

Data must be present at the D input 10 ns prior to the rise of the clock, and remain 10 ns after the clock signal rises. Data may be changed any time during the clock cycle except the interval between the setup time (10 ns) and the hold time (10 ns) without affecting the operation of the flip-flop. The data input is inhibited when the clock is high. When the clock is in the low state, the input steering section continually reflects the state of the D input. Information present at the D input during the time interval between the setup and hold times is transferred to the bistable section on the positive edge of the clock, and outputs Q and $\overline{Q}$ respond accordingly.

The flip-flops can be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct Set or Reset inputs.